

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT PACKARD ENTERPRISE COMPANY,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

IPR2022-00115
Patent 7,464,240 B2

Before KEN B. BARRETT, NABEEL U. KHAN, and
STEPHEN E. BELISLE, *Administrative Patent Judges*.

BELISLE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Case Posture

Hewlett Packard Enterprise Co. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1, 3, 7, and 8 (“Challenged Claims”) of U.S. Patent No. 7,464,240 B2 (Ex. 1001, “the ’240 patent”). Petitioner identifies itself as a real party in interest. Pet. vii. Intellectual Ventures II LLC (“Patent Owner”) identifies itself as a real party in interest (Paper 5, 1), and timely filed a Preliminary Response to the Petition (Paper 8, “Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b) (2018); 37 C.F.R. § 42.4(a) (2021). We may not institute an *inter partes* review “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Applying those standards, and upon consideration of the information presented in the Petition and Preliminary Response, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to any of challenged claims 1, 3, 7, and 8 of the ’240 patent. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Accordingly, constrained by the record before us, we deny institution of an *inter partes* review of the ’240 patent.

B. Related Matters

The parties indicate that the ’240 patent is involved in one U.S. district court action, namely, *Intellectual Ventures I LLC et al. v. Hewlett Packard Enterprise Co.*, No. 6:21-cv-00596 (W.D. Tex.). Pet. vii; Paper 5, 1.

Patent Owner also indicates that U.S. Patent Application Nos. 12/113,606, filed May 1, 2008, now U.S. Patent No. 7,882,320; 12/123,303, filed May 19, 2008, now U.S. Patent No. 7,930,468; and 12/123,324, filed May 19, 2008, now U.S. Patent No. 7,949,820, claim the benefit of the '240 patent. Paper 5, 1.

Petitioner indicates that it also has filed a Petition in IPR2022-00116 requesting an *inter partes* review of claims 1–3 and 5–8 of U.S. Patent No. 7,882,320, another patent owned by Patent Owner. Pet. vii.

C. The '240 Patent

The '240 patent is titled “Hybrid Solid State Disk Drive With Controller,” and issued on December 9, 2008, from U.S. Patent Application No. 11/439,619, filed May 23, 2006. Ex. 1001, codes (10), (21), (22), (45), (54).

The '240 patent generally relates to a “hybrid solid-state storage device,” as shown, for example, in Figure 1, reproduced below. Ex. 1001, 3:36–37.

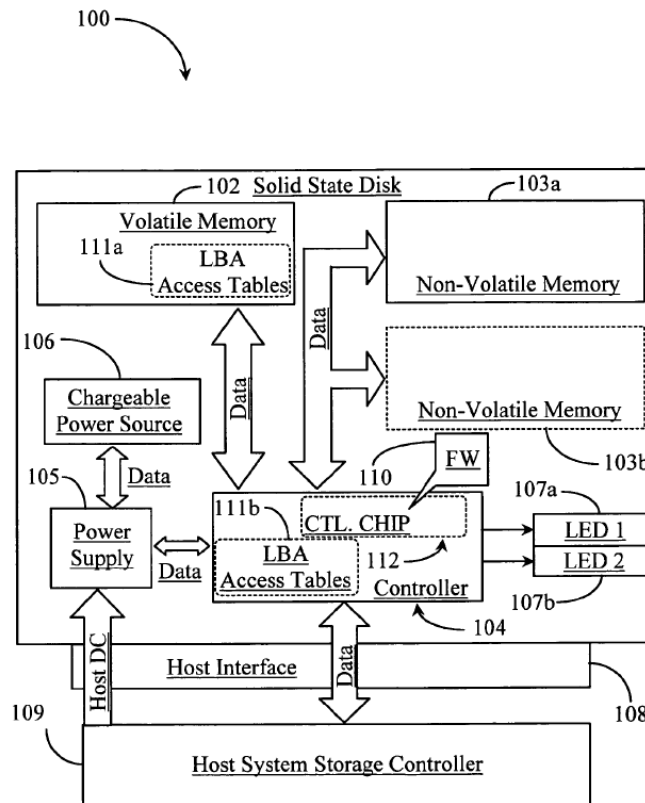


Fig. 1

Figure 1 depicts a block diagram of a high-speed solid-state non-volatile disk.

Ex. 1001, 3:4–6, Fig. 1. As shown in Figure 1 above, hybrid solid-state storage device 100 includes, in part, volatile memory 102, non-volatile memory 103a (or alternative also 103b), and onboard controller 104. *Id.* at 3:36–5:20. Controller 104 “is adapted primarily to manage data writes and reads incoming from a host to both volatile memory 102 and to non-volatile memory 103a.” *Id.* at 5:12–14.

According to the ’240 patent, “it is desired to provide a pure solid-state disk drive that may be implemented as a normal hard drive package that is recognized and read by a host system as a single non-volatile storage disk.” Ex. 1001, 1:46–53. Also according to the ’240 patent, the solid-state

disk drive employs “unique data management methods that consider available volatile and non-volatile memory on [a] disk [] as a hybrid of RAM and Flash for smart data caching and data access from cache or Flash and for permanent data storage to non-volatile memory at appropriate but, optimally, infrequent times.” *Id.* at 6:10–17.

D. Illustrative Claim

The '240 patent includes eight claims, of which claims 1, 3, 7, and 8 are challenged. Claim 1 is the only independent claim, and is reproduced below.

1. A solid-state drive comprising[:]
a volatile memory;
a non-volatile memory; and
a controller for managing read and write requests to the volatile and non-volatile memories;
wherein upon receiving a write request including an address and data, the controller determines if the address is referenced at a first location in the volatile memory, and if so, overwrites any data at the first location, and if not referenced in a first location, writes the data to a second location marked as available for writing in the volatile memory, associating the second location with the address, and wherein upon receiving a read request including an address, the controller determines if the address is referenced in at any location in the volatile portion, and if so, reading data from that location, and if not, reading data from the address in the non-volatile memory, and wherein the controller periodically compares valid data volume in the volatile memory with a preset threshold, and upon exceeding the threshold, selects and moves data that has been longest in the volatile memory without alteration from the volatile to the non-volatile memory, and marks the locations from which the data is moved as available for writing in the volatile portion.

Ex. 1001, 17:7–18:3.

E. Applied References

Petitioner relies upon the following references:

Harari et al., U.S. Patent No. 6,523,132 B1 (Ex. 1004, “Harari”), filed September 8, 2000, issued February 18, 2003.

Tobita et al., U.S. Patent No. 5,862,083 (Ex. 1005, “Tobita”), filed April 30, 1996, issued January 19, 1999.

Y. Hu, T. Nightingale, and Q. Yang, “RAPID-Cache—A Reliable and Inexpensive Write Cache for High Performance Storage Systems,” IEEE Transactions on Parallel and Distributed Systems, vol. 13, no. 3, 290–307 (March 2002) (Ex. 1006, “Hu”).

Pet. 2, 17–25.

F. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1, 3, 7, and 8 of the ’240 patent based on the following grounds.

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 3, 7	102 ¹	Harari
1, 3, 7	103	Harari
1, 3, 7, 8	103	Harari, Hu
1, 3, 7	102	Tobita
1, 3, 7	103	Tobita
1, 3, 7, 8	103	Tobita, Hu

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103. Because the ’240 patent was filed before March 16, 2013, the effective date of the relevant amendment, the pre-AIA versions of §§ 102 and 103 apply.

Pet. 2. For each of the above grounds based on § 103, Petitioner’s challenge to the listed claims is based on the listed reference(s) “in view of . . . the knowledge of a POSITA,” where “POSITA” means a person of ordinary skill in the art. Pet. 2. Petitioner also relies upon the Declaration of Dr. Vivek Subramanian (Ex. 1003).

II. ANALYSIS

A. Applicable Law

Petitioner challenges the patentability of claims 1, 3, 7, and 8 of the ’240 patent on grounds that the claims would have been anticipated under 35 U.S.C. § 102 or obvious under 35 U.S.C. § 103 in light of various references including: Harari, Tobita, and Hu. “In an [*inter partes* review], the petitioner has the burden from the onset to show *with particularity* why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)) (emphasis added). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review).

To serve as an anticipatory reference under 35 U.S.C. § 102, “the reference must disclose each and every element of the claimed invention, whether it does so explicitly or inherently.” *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009). “The identical invention must be shown in as complete detail *as is contained in the . . . claim.*” *Richardson v. Suzuki*

Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989) (emphasis added).

The elements must be arranged as required by the claim, “but this is not an ‘*ipsissimis verbis*’ test,” i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990) (citing *Akzo N.V. v. United States Int’l Trade Comm’n*, 808 F.2d 1471, 1479 & n.11 (Fed. Cir. 1986)).

A claim is unpatentable under 35 U.S.C. § 103 if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when of record, objective evidence of obviousness or non-obviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Secondary considerations may include the following: “commercial success, long felt but unsolved needs, failure of others, etc.”² *Id.* The totality of the evidence submitted may show that the challenged claims would not have been obvious to one of ordinary skill in the art. *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984). When evaluating a combination of teachings, we must also “determine whether there was an apparent reason to combine the known elements in the

² At this stage of the proceeding, Patent Owner has not presented objective evidence of non-obviousness.

fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

We analyze the challenges presented in the Petition in accordance with the above-stated principles.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art, at the time of the invention of the ’240 patent:

would have had at least a bachelor’s degree in electrical engineering or an equivalent, plus three years of experience in the field of memory device design. Additional education in the field of electrical engineering such as a masters or doctorate degree may serve as a substitute for experience in the field. A person with less education but more relevant practical experience may also meet this standard.

Pet. 16 (citing Ex. 1003 ¶ 28). Patent Owner does not present an alternative definition at this stage of the proceeding. *See generally* Prelim. Resp.

We regard Petitioner’s proposed definition as reasonable, and consistent with the prior art before us. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (determining that the Board of Patent Appeals and Interferences did not err in concluding that the level of ordinary skill in the art was best determined by the references of record). Accordingly, we apply the level of skill set forth above, which also is consistent with the testimony of Dr. Subramanian (Ex. 1003 ¶ 28).

C. Claim Construction

Neither Petitioner nor Patent Owner proposes any claim terms for construction. Pet. 17 (“Petitioner interprets the claims ‘in accordance with the ordinary and customary meaning . . . as understood by one of ordinary

skill in the art.”); Prelim. Resp. 7 (“Patent Owner submits that all claim terms should be given their ordinary and customary meaning in light of the claims, specification, and file history of the ’240 patent as would have been read by a skilled artisan.”). We do not find that the express construction of any term is necessary for this decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

D. Anticipation and Obviousness of Claims 1, 3, and 7 over Harari

Petitioner contends claims 1, 3, and 7 are unpatentable under 35 U.S.C. § 102 as anticipated by Harari (Ex. 1004) or under 35 U.S.C. § 103 as obvious over Harari “alone or in view of the knowledge of a POSITA.” Pet. 25–38. Patent Owner opposes Petitioner’s contentions. Prelim. Resp. 13–32. Based on our review of the Petition and Preliminary Response, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that any of claims 1, 3, and 7 is unpatentable as anticipated by or obvious over Harari, as discussed below. We begin with an overview of Harari.

1. Overview of Harari

Harari relates generally “to semiconductor electrically erasable programmable read only memories (EEPROM), and specifically to a system of integrated circuit Flash EEPROM chips,” as shown, for example, in Figure 1A, reproduced below. Ex. 1004, 1:15–18, Fig. 1A.

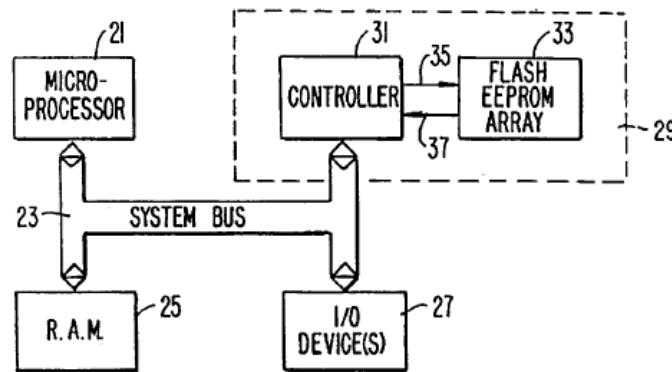


FIG. 1A

Figure 1A depicts a general microprocessor system including a Flash EEprom memory system.

Id. at 2:66–67, Fig. 1A.

Harari's computer system architecture depicted in Figure 1A above includes microprocessor 21 connected to system bus 23; random access, main system memory 25; at least one or more input-output devices 27, such as a keyboard, monitor, or modem; and "a large amount of long-term, non-volatile memory 29." Ex. 1004, 3:29–37. According to Harari, "[t]ypically, such a memory [29] is a disk drive with a capacity of tens of megabytes of data storage," and "[t]his data is retrieved into the system volatile memory 25 for use in current processing, and can be easily supplemented, changed or altered." *Id.* at 3:38–41. According to Harari:

One aspect of the present invention is the substitution of a specific type of semiconductor memory system for the disk drive but without having to sacrifice non-volatility, ease of erasing and rewriting data into the memory, speed of access, low cost and reliability. This is accomplished by employing an array of electrically erasable programmable read only memories (EEprom's) integrated circuit chips.

Id. at 3:42–48. In Harari, bulk storage memory 29 includes memory controller 31 connected to computer system bus 23, and array 33 of EEPROM integrated circuit chips, where data and instructions are communicated from controller 31 to EEPROM array 33 primarily over serial data line 35, and data and status signals are communicated from EEPROM 33 to controller 31 over serial data lines 37. *Id.* at 3:53–61.

Harari discloses that “a cache memory is used in a novel way to insulate the Flash EEPROM memory device from enduring too many program/erase cycles.” Ex. 1004, 12:61–63. According to Harari, “[t]he primary function of the cache is *to act on writes* to the Flash EEPROM memory and *not on reads* of the Flash EEPROM memory, unlike the case with traditional caches.” *Id.* at 12:63–66 (emphases added). Instead, “[d]uring *read* of a new sector in the Flash EEPROM memory 33, the data file is read out and *sent directly to the host through the controller*. This file is not used to fill the cache memory 705 as is done in the traditional cache systems.” *Id.* at 13:45–48 (emphases added).

We further discuss below the disclosure of Harari in connection with the parties’ arguments.

2. *Independent Claim 1: “wherein upon receiving a read request including an address, the controller determines if the address is referenced in at any location in the volatile portion, and if so, reading data from that location, and if not, reading data from the address in the non-volatile memory”*

Independent claim 1 requires, in relevant part, “wherein upon receiving a read request including an address, the controller determines if the address is referenced in at any location in the volatile portion, and if so,

reading data from that location, and if not, reading data from the address in the non-volatile memory.” Ex. 1001, 17:19–24. The parties dispute, *inter alia*, whether Petitioner’s cited evidence adequately supports Petitioner’s contention that Harari discloses or teaches this “read” limitation. *See, e.g.*, Prelim. Resp. 26–32; Pet. 32–33.

Petitioner contends “Harari discloses *for all embodiments* that the controller *can* handle a data read request from a host by either [a] ‘reading addressed user data first from the cache memory, if stored therein;’ or [b] ‘reading addressed user data [. . .] from the array, if not stored in the cache memory,’ where the ‘array’ refers to ‘an array of non-volatile memory cells.’” Pet. 32–33 (citing Ex. 1004, Cl. 18 (17:50–18:23), Cl. 9 (16:62–17:21), Fig. 6, 8:60–9:26; Ex. 1003 ¶ 117) (emphases added). Petitioner also contends:

[I]n Harari, “[d]uring read of a new sector in the Flash EEprom memory 33, the data file is read out and sent directly to the host through the controller. This file is not used to fill the cache memory 705 as is done in the traditional cache systems.” Ex[1004], 13:45-49.

As described in Harari, and known to a POSITA, a read request from a host includes an address. Ex[1004], FIG. 6; Ex[1003], ¶118. The address is used to read data from flash memory (Ex[1004], 9:18-19 (“the memory device reads the address sent it and begins sending serial data from the addressed sector”)), or from cache memory ((Ex[1004], 13:57-58 (storing file identifier information in tag memory))).

Pet. 33. Petitioner’s declarant makes these same statements verbatim, without more, and with no additional citations to evidence. *See* Ex. 1003 ¶¶ 117–119. We find Petitioner’s arguments unpersuasive.

Before turning to Patent Owner’s preliminary response, we are mindful that although one of ordinary skill in the art may understand that two references or embodiments within a reference *could be* combined, this does not itself imply a reason or motivation to combine the references or embodiments. *Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987 993–94 (Fed. Cir. 2017); *see also Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”).

Patent Owner argues Petitioner relies (improperly) on a combination of elements from different embodiments in Harari to allegedly disclose or teach the subject “read” limitation along with the other limitations of claim 1, without explaining sufficiently, let alone with particularity, how or why the skilled artisan *would* have combined such embodiments or had an expectation of success in doing so. *See* Prelim. Resp. 13–19, 26–32. In particular, Patent Owner argues “Petitioner relies on the ‘first’ and ‘second’ embodiments of the specification’s write cache” for purposes of the “write” limitation³ in claim 1. *Id.* at 32; *see* Pet. 29–32. Patent Owner argues that Petitioner then, for purposes of this “read” limitation, leaps to relying on the

³ The “write” limitation of independent claim 1 recites “wherein upon receiving a write request including an address and data, the controller determines if the address is referenced at a first location in the volatile memory, and if so, overwrites any data at the first location, and if not referenced in a first location, writes the data to a second location marked as available for writing in the volatile memory, associating the second location with the address.” Ex. 1001, 17:12–19.

disclosure of “reading addressed user data first from the cache memory” found only in Harari’s embodiments recited in claims 9 and 18, but not otherwise disclosed in Harari’s specification. *See* Prelim. Resp. 31 (“Because claims 9 and 18 fundamentally contradict the specification’s write cache only embodiment, these claims at best disclose a *different* embodiment than the write cache only embodiment. These embodiments are not interchangeable.” (citations omitted)); *see also id.* at 27–32.

Patent Owner argues “Petitioner alleges without explanation or citation that the read cache disclosure of claims 9 and 18 is ‘for all embodiments,’” and that “[t]his assertion is conclusory and not supported by Harari.” Prelim. Resp. 32 (citations omitted). Patent Owner argues “Harari expressly contradicts this assertion by disclosing that the specification’s write cache system ‘act[s] on writes to the Flash EEPROM memory *and not on reads of the Flash EEPROM memory.*’” *Id.* (citing Ex. 1004, 12:63–65); *see* Ex. 1004, 13:45–48 (“During *read* of a new sector in the Flash EEPROM memory 33, the data file is read out and *sent directly to the host through the controller.* This file is *not used to fill the cache memory 705* as is done in the traditional cache systems.” (emphases added)).

Patent Owner concludes, and we agree for the reasons discussed above, that Petitioner does not explain sufficiently, let alone with particularity, how or why the skilled artisan *would* have combined such distinct embodiments or had an expectation of success in doing so. *See* Prelim. Resp. 31–32; *In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (obviousness allegations based on combining multiple embodiments from a single reference require evidence that a skilled artisan would have had a rational reason to combine such embodiments and a reasonable

expectation that such combinations would be successful); *ABiomed, Inc. v. Maquet Cardiovascular, LLC*, IPR2017-01204, Paper 9 at 11 (PTAB Oct. 23, 2017) (denying institution where Petitioner failed to provide a sufficient rationale to combine the teachings of the reference’s different embodiments); *Google LLC v. AGIS Software Development, LLC*, IPR2018-01086, Paper 10 at 19 (PTAB Dec. 4, 2018) (same); *see also KSR*, 550 U.S. at 418 (“A patent composed of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art.”).

In addition, Patent Owner argues Petitioner’s combination of select features from Harari’s different embodiments to arrive at the invention of claim 1 is fraught with hindsight bias. Prelim. Resp. 32 (“Petitioner’s reliance on claims 9 and 18 for this [read] element is thus yet another example of Petitioner cherry picking disparate disclosures from disparate embodiments in order to cobble together a system that allegedly arrives at the claimed invention.”), 2 (“Petitioner’s analysis throughout is fundamentally based on improper hindsight.”). We agree with Patent Owner that, but for hindsight, neither Petitioner nor its expert explains sufficiently, let alone with particularity, why the skilled artisan would have considered combining such distinct embodiments as claimed or had an expectation of success in doing so. *See InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (“It appears that [the expert] relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”); *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570 (Fed. Cir. 1996) (citing *W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 1553 (Fed. Cir. 1983)) (“To draw on hindsight knowledge of

the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction—an illogical and inappropriate process by which to determine patentability.”). Although “[a] person of ordinary skill is also a person of ordinary creativity, not an automaton” (*KSR*, 550 U.S. at 421), the Federal Circuit has observed that “‘the prejudice of hindsight bias’ often overlooks that the ‘genius of invention is often a combination of known elements which in hindsight seems preordained.’” *Polaris Industries, Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068 (Fed. Cir. 2018).

Similarly, we also find neither Petitioner nor its expert explains sufficiently, let alone with particularity, how or why the proposed combination of select features from different embodiments in Harari represents an identical showing of every element *arranged as in claim 1*. See *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990) (“For a prior art reference to anticipate . . . , every element of the claimed invention must be identically shown in a single reference,” and “[t]hese elements must be arranged as in the claim under review.”).

For the foregoing reasons, and constrained by the Petition, we are not persuaded that the cited evidence adequately supports Petitioner’s contention that Harari discloses or teaches the subject “read” limitation, as recited in independent claim 1 (i.e., in the context of the limitations of claim 1 as a whole).

3. Summary

For the foregoing reasons, we determine that Petitioner has not demonstrated a reasonable likelihood of success in establishing the unpatentability of claim 1, or claims 3 and 7 which depend therefrom, as

anticipated by Harari or obvious over Harari “alone or in view of the knowledge of a POSITA.”

E. Anticipation and Obviousness of Claims 1, 3, and 7 over Tobita

Petitioner contends claims 1, 3, and 7 are unpatentable under 35 U.S.C. § 102 as anticipated by Tobita (Ex. 1005) or under 35 U.S.C. § 103 as obvious over Tobita “alone or in view of the knowledge of a POSITA.” Pet. 45–62. Patent Owner opposes Petitioner’s contentions. Prelim. Resp. 33–44. Based on our review of the Petition and Preliminary Response, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing that any of claims 1, 3, and 7 is unpatentable as anticipated by or obvious over Tobita, as discussed below. We begin with an overview of Tobita.

1. Overview of Tobita

Tobita relates generally to “a control method and system when a flash memory is used as a semiconductor disk or a main memory in an information processing system.” Ex. 1005, 1:9–11.

Figure 82 of Tobita is reproduced below.

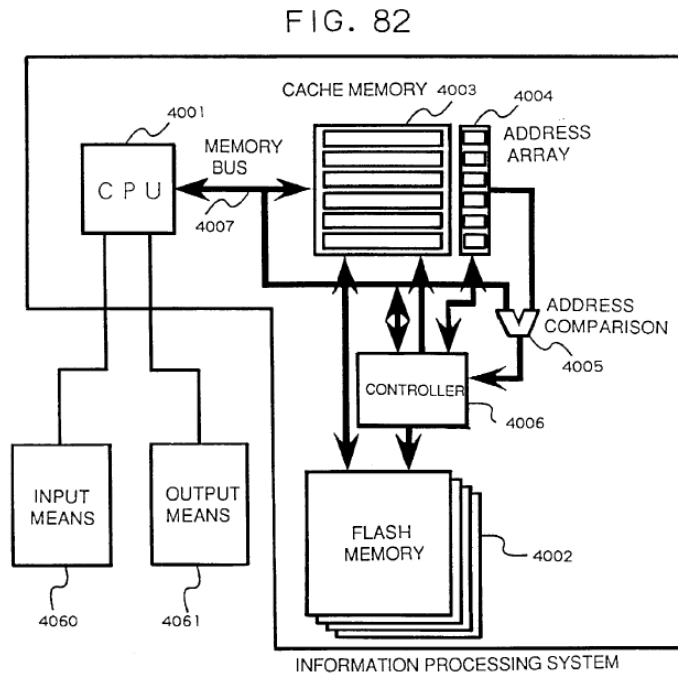


Figure 82 depicts a schematic block diagram of an embodiment of an information processing system using a flash memory as a main memory.

Ex. 1005, 17:1–3, Fig. 82.

Tobita’s information processing system as shown above in Figure 82 includes central processing unit (CPU) 4001; flash memory 4002, which is “a large-capacity nonvolatile memory storing the programs, data, etc., handled by the CPU 4001”; cache memory 4003, which is “a volatile memory temporarily storing data such as data transferred from the flash memory and write data from the CPU 4001”; and controller 4006, which “controls the information processing system so that accurate data can be accessed at high speed as much as possible in response to an access request made by the CPU 4001.” *Id.* at 45:49–46:20.

We further discuss below the disclosure of Tobita in connection with the parties' arguments.

2. *Independent Claim 1: “wherein the controller . . . selects and moves data that has been longest in the volatile memory without alteration from the volatile to the non-volatile memory”*

Independent claim 1 requires, in relevant part, “wherein the controller . . . selects and moves data that has been longest in the volatile memory without alteration from the volatile to the non-volatile memory.” Ex. 1001, 17:24–18:1. The parties dispute, *inter alia*, whether Petitioner’s cited evidence adequately supports Petitioner’s contention that Tobita discloses or teaches this “longest in the volatile memory without alteration” limitation. *See, e.g.*, Prelim. Resp. 42–44; Pet. 59–60.

Petitioner contends Tobita discloses or teaches this limitation because Tobita uses a “least recently used” (LRU) approach to destage⁴ files:

In terms of which files are destaged, Tobita uses an LRU approach. *Id.*, ¶192. Tobita specifically discloses that “‘access history,’ which is information indicating in what sequence the CPU has accessed the cache memory, is stored corresponding to each address registered in the address array 4004.” Ex[1005], 47:59-63. The access history “information indicat[es] relative oldness of addresses last accessed” in the cache memory 4003. *Id.*, 48:1-2. It is this “oldest” data that “may be erased from the cache memory 4003.” *Id.*, 48:2-6, 12:9-20. In short, the controller uses “access history information” to identify the “oldest” address accessed, “deletes the address,” and “further transfers data in said volatile storage means corresponding to the

⁴ “Destaging,” according to Petitioner, is an operation in which a controller selects certain data in a cache (volatile storage) and moves it to non-volatile storage. *See* Pet. 57; *see also id.* at 11–13 (“Destaging in Write Back Caches”).

address deleted ... to said nonvolatile storage means.” Ex[1005], Cl. 3-4 (61:21-32); Ex[1003], ¶192. Accordingly, the data corresponding to the “address the last access to which is the oldest among recorded addresses” are those that have been longest in the cache memory without alteration. Ex[1003], ¶192.

Pet. 11, 59–60. Petitioner’s declarant makes these same statements verbatim, without more, and with no additional citations to evidence. *See* Ex. 1003 ¶ 192. We find Petitioner’s arguments unpersuasive.

Patent Owner argues “an LRU destaging approach does not select and move data that has been longest in the volatile memory without alteration,” because, “[a]s Petitioner admits, in an LRU approach, ‘the system determines which data has been in the cache the longest without being used (e.g., ***read or overwritten***) and preferentially destages that data over other data in the cache.’” Prelim. Resp. 42 (citing Pet. 11–12). Patent Owner argues that “reading data in cache does not *alter* the data,” as the “data is merely read,” and so “[a]n LRU approach thus selects data that has not been recently used—regardless of whether that data has been altered.” *Id.*

Patent Owner argues “Tobita’s system destages data that has been in the cache the longest without being accessed (e.g., ***read or overwritten***):”

Tobita’s data “accesses” include read accesses and write accesses. EX1005, 47:27-32 (disclosing “a read access” and “a write access”). If a “read access” is made, “data input from the CPU 4001 via the memory bus 4007 is written into the corresponding location in the cache memory 4003.” *Id.*, 47:27-32. In such instance, data is not overwritten—it is merely read. Thus, on a read access, the data in cache is *not altered*.

Id. at 42–43. Patent Owner argues “Tobita’s ‘data replacement algorithm’ selects data that has not been recently *accessed*, regardless of whether such data has been *altered*.” *Id.* at 43 (citing Ex. 1005, 48:2–6). “That is,

Tobita's algorithm does not consider whether data has been altered in determining which data to replace—only whether the data has been accessed.” *Id.* Patent Owner argues “Tobita's algorithm will not select data that has been recently read (i.e., accessed), even if that data has been in cache longer than any other data, and has never been overwritten (i.e., altered).” *Id.* Patent Owner concludes, and we agree for the reasons discussed above, that Petitioner does not explain sufficiently, let alone with particularity, how or why Tobita's LRU destaging approach (i.e., moving data longest in memory without *access*) discloses or teaches moving data longest in memory without *alteration*. *Id.*

For the foregoing reasons, and constrained by the Petition, we are not persuaded that the cited evidence adequately supports Petitioner's contention that Tobita discloses or teaches the limitation “wherein . . . selects and moves data that has been longest in the volatile memory without alteration from the volatile to the non-volatile memory,” as recited in independent claim 1.

3. *Summary*

For the foregoing reasons, we determine that Petitioner has not demonstrated a reasonable likelihood of success in establishing the unpatentability of claim 1, or claims 3 and 7 which depend therefrom, as anticipated by Tobita or obvious over Tobita “alone or in view of the knowledge of a POSITA.”

F. Obviousness of Claims 1, 3, 7, and 8 over the Combination of Harari and Hu and over the Combination of Tobita and Hu

Petitioner contends claims 1, 3, 7, and 8 are unpatentable under 35 U.S.C. § 103 as obvious over the combination of Harari and Hu and over

the combination of Tobita and Hu, both “in view of the knowledge of a POSITA.” Pet. 38–45, 62–69. Patent Owner opposes Petitioner’s contentions. Prelim. Resp. 44–45.

Petitioner does not argue Hu cures any deficiencies discussed above concerning Harari (*see* Section II.D.2) or Tobita (*see* Section II.E.2). *See* Pet. 38–45, 62–69; Prelim. Resp. 44–45 (“Hu does not cure the deficiencies of Harari or Tobita.”). Therefore, for the same reasons discussed above in Sections II.D and II.E, we determine that Petitioner has not demonstrated a reasonable likelihood of success in establishing the unpatentability of claim 1, or claims 3, 7, and 8, which depend therefrom, as obvious over the combination of Harari and Hu or over the combination of Tobita and Hu, in view of the knowledge of a POSITA.

III. CONCLUSION

Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to any of claims 1, 3, 7, and 8 of the ’240 patent under any of its proffered Grounds 1 through 6 (Pet. 2).

IV. ORDER

For the reasons given, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is not instituted for claims 1, 3, 7, and 8 of U.S. Patent No. 7,464,240 B2.

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Patent 7,464,240 B2

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