

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

MYPAQ HOLDINGS LTD.,
Patent Owner.

IPR2022-00307
Patent 7,403,399 B2

Before KRISTINA M. KALAN, DANIEL J. GALLIGAN, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–6, 10, and 13 of U.S. Patent No. 7,403,399 B2 (Ex. 1001, “the ’399 patent”). MyPAQ Holdings Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 6. Pursuant to Board authorization, Petitioner filed a Reply to the Patent Owner Preliminary Response. Paper 8. Patent Owner filed a Sur-Reply to Petitioner’s Reply. Paper 9.

We instituted *inter partes* review of claims 1–6, 10, and 13 of the ’399 patent on the grounds of unpatentability alleged in the Petition. Paper 10 (“Dec.”). After institution of trial, Patent Owner filed a Patent Owner Response. Paper 15 (“PO Resp.”). On August 29, 2022, the same day Patent Owner filed its Response, Patent Owner also filed a Statutory Disclaimer of claims 1–5 and 13 of the ’399 patent, leaving only claims 6 and 10 at issue in this *inter partes* review. Ex. 2019; PO Resp. 1. Petitioner filed a Reply. Paper 18 (“Reply”). Patent Owner filed a Sur-Reply. Paper 19 (“Sur-Reply”). We held an oral hearing on February 23, 2023, and a transcript of the hearing is included in the record. Paper 24 (“Tr.”).

This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 6 and 10, the only claims remaining in this *inter partes* review, are unpatentable.

A. *Related Proceedings*

The parties identify the following district court litigation as a related matter: *MyPAQ Holdings Ltd. v. Samsung Electronics Co.*, No. 6:21-CV-

00398 (W.D. Tex.). Pet. 1; Paper 7, 1 (Patent Owner's updated mandatory notices).

The parties also state that Petitioner has filed petitions regarding other patents held by Patent Owner: IPR2022-00308 regarding U.S. Pat. No. 7,978,489, IPR2022-00311 regarding U.S. Pat. No. 8,477,514, and IPR2022-00312 regarding U.S. Pat. No. 7,675,759. Pet. 1; Paper 7, 1.

B. Real Parties-in-Interest

Petitioner identifies Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC as the real parties-in-interest. Pet. 1. Patent Owner states that the “real party in interest is: MyPAQ Holdings Ltd.” and that “Transpacific IP Group Limited has an ownership interest in MyPAQ.” Paper 7, 1.

C. The '399 Patent

The '399 patent is titled “Active Primary-Sided Circuit Arrangement for a Switch-Mode Power Supply” and is directed to a circuit arrangement that has various components integrated in at least one additional semiconductor chip. Ex. 1001, codes (54), (57). By way of background, the '399 patent explains that “[c]harging devices in the low power range are normally implemented as switch-mode power supplies.” *Id.* at 1:19–20. The '399 patent's “switch-mode power supply has a primary side, which can be connected to a supply voltage, and a secondary side, which can be connected to a consumer.” *Id.* at 1:8–12.

The '399 patent focuses on the arrangement of the components on the primary side of the switch-mode power supply. *See id.* at 2:40–49. Figure 1 is reproduced below.

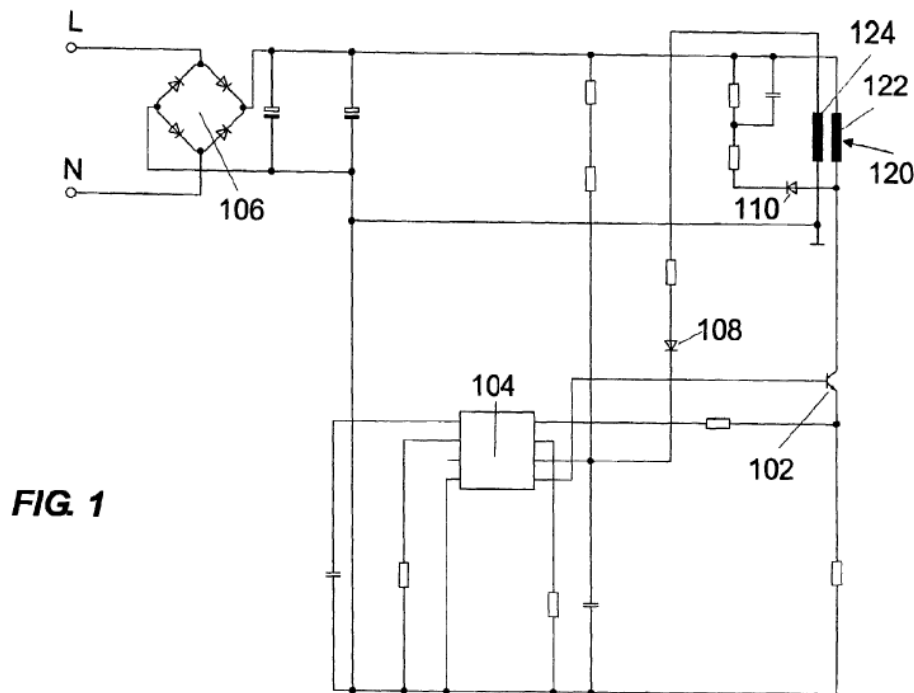


FIG. 1

Figure 1, “in the form of a wiring diagram, shows the circuit diagram of the primary side of a switch-mode power supply with primary regulation.” *Id.* at 1:31–33. Figure 1 shows various components, including converter-transformer 120 (which includes primary-sided winding 122 and auxiliary winding 124), active components, and passive components. *Id.* at 1:30–39. Passive components include “resistors, inductors and capacitors.” *Id.* at 1:36–38. Active components “comprise four single diodes, which form a bridge rectifier 106, the switching transistor 102, an ASIC for pulse width modulation of the primary-sided switching transistor as control circuit 104 of the primary-sided switch 102, an auxiliary voltage diode 108 and a snubber diode 110.” *Id.* at 1:38–44.

The '399 patent arranges components of the primary-sided circuit such that “the control circuit is formed by a first integrated semiconductor chip and that the primary-sided switch and the additional components are

integrated in at least one additional semiconductor chip being separate from the control circuit and arranged on a circuit carrier shared with the control circuit.” *Id.* at 2:48–50. The ’399 patent states that, because the active components “are not executed in a discrete construction . . . but are instead assembled on a shared circuit carrier and, according to an advantageous further development, accommodated in a shared IC housing,” there is “a considerable decrease in the space requirement, as well as a reduction of possible error sources.” *Id.* at 2:58–65.

Figure 2 is reproduced below.

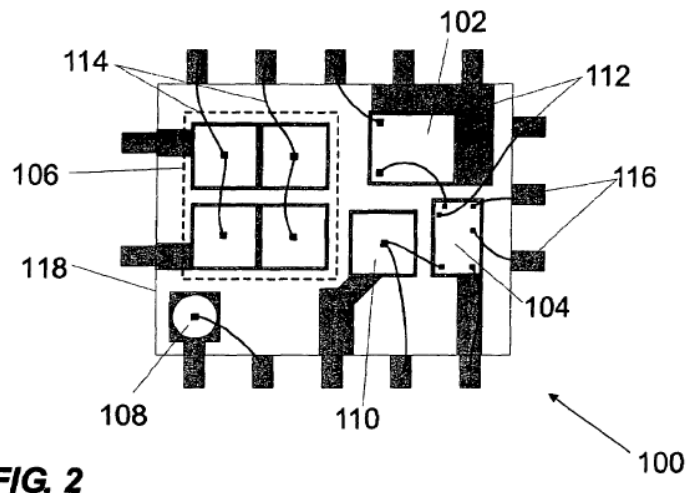


FIG. 2

Figure 2 shows “an active primary-sided circuit arrangement” on a circuit carrier. *Id.* at 4:21–23. In Figure 2, “switching transistor 102, the control circuit 104 (also identified as the control IC), as well as the snubber diode 110, the diodes for the bridge rectifier 106 and the diode for the auxiliary power supply 108 are initially present as separate semiconductor chips, also called dies.” *Id.* at 4:59–64. The “individual semiconductor elements are glued or soldered to the respective areas of the leadframe 112,” i.e., an exemplary circuit carrier, and are “appropriately contacted using bonding wires 114.” *Id.* at 4:43–47, 4:64–66. The semiconductor chips are

contacted to outer terminals 116 via bonding wires 114. *Id.* at 4:66–5:3.
Additionally, shared housing 118 may be “die-cast around the arrangement”
using a casting compound such as an epoxy resin. *Id.* at 4:52–54.

D. Illustrative Claim

Independent claim 1 (now disclaimed) and its dependent claims 6
and 10 are reproduced below.

1[pre] Circuit arrangement for a switch-mode power supply,
wherein the switch-mode power supply has a primary side, which
can be connected to a supply voltage, and a secondary side,
which can be connected to a consumer,

1[a] wherein the circuit arrangement (100) comprises a
primary-sided switch (102), a control circuit (104) for
controlling the primary-sided switch (102) and additional
active, primary-sided components (106, 108, 110),

1[b] wherein said control circuit (104) is formed by a first
integrated semiconductor chip and the primary-sided switch
(102) and the additional components (106, 108, 110), are
integrated in at least one additional semiconductor chip,

1[c] said semiconductor chip being separate from the control
circuit and arranged on a circuit carrier (112) shared with
the control circuit.

Ex. 1001, 6:23–41 (bracketed designations and formatting added by
Petitioner (Pet. 25–31)).

6. Circuit arrangement according to claim 1, wherein a
metallization of the circuit carrier (112) has cooling areas that are
formed for removing heat.

Id. at 6:49–51.

10. Circuit arrangement according to claim 1, wherein the
additional active components (106, 108, 110) are at least
partially combined into a single semiconductor chip and are
monolithically integrated.

Id. at 6:62–65.

E. Instituted Grounds of Unpatentability

We instituted *inter partes* review of claims of the '399 patent on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 5, 10, 13	§ 102 ¹	Zverev ²
4, 6	§ 103	Zverev, Shiraishi ³
4, 6	§ 103	Zverev, Lacap ⁴
1–6, 10, 13	§ 103	Liaw, ⁵ Nam ⁶
1–5, 10, 13	§ 103	Liaw, Lin ⁷
6	§ 103	Liaw, Lin, Shiraishi

Following the disclaimer, the claims and grounds identified in the table below remain in the proceeding:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
10	§ 102	Zverev
6	§ 103	Zverev, Shiraishi
6	§ 103	Zverev, Lacap
6, 10	§ 103	Liaw, Nam
10	§ 103	Liaw, Lin
6	§ 103	Liaw, Lin, Shiraishi

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the '399 patent has an effective filing date prior to the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102 and 103.

² DE 100 43 485 A1, published March 14, 2002 (Ex. 1003). Exhibit 1003 includes a copy of the original document and a certified translation. Ex. 1003, 21; *see* Pet. iv.

³ US 2004/0227547 A1, published November 18, 2004 (Ex. 1007).

⁴ US 5,939,781, issued August 17, 1999 (Ex. 1008).

⁵ US 6,259,618 B1, issued July 10, 2001 (Ex. 1004).

⁶ US 2003/0102489 A1, published June 5, 2003 (Ex. 1005).

⁷ US 5,491,360, issued February 13, 1996 (Ex. 1006).

In support of its unpatentability arguments, Petitioner relies on the declarations of Peter Elenius. Ex. 1002; Ex. 1035. Patent Owner relies on the declaration of Dr. Frank Ferrese to support its opposition. Ex. 2020.⁸ The parties also rely on the deposition transcripts of Mr. Elenius (Ex. 2022) and Dr. Ferrese (Ex. 1036).

II. ANALYSIS

A. Legal Standards

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). A “prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such

⁸ Petitioner argues that Dr. Ferrese’s opinions should be given little, if any, weight. Reply 3. Patent Owner responds that Dr. Ferrese’s opinions are entitled to significant weight. Sur-Reply 2–4. We acknowledge these arguments and, in our analysis, accord Dr. Ferrese’s declaration and testimony the appropriate weight.

that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness, i.e., secondary considerations.⁹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). A decision on the ground of obviousness must include “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). The obviousness analysis “should be made explicit” and it “can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *KSR*, 550 U.S. at 418.

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must demonstrate unpatentability by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (2012) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)).

⁹ Neither Patent Owner nor Petitioner appear to present any evidence directed to secondary considerations. *See* Pet.; PO Resp.; Reply; Sur-Reply.

B. Level of Ordinary Skill in the Art

In our Institution Decision, we adopted Petitioner’s undisputed contention that a person of ordinary skill in the art “would have either (i) a Master of Science in Electrical Engineering, Mechanical Engineering or a related field, or (ii) a Bachelor of Science in Electrical Engineering, Mechanical Engineering or a related field as well as at least two years of experience in the design and/or packaging of power electronics” (Pet. 18 (citing Ex. 1002 ¶ 99)), with the exception of the open-ended phrase “at least,” which expands the range of experience indefinitely without an upper bound. Dec. 8–9.

Patent Owner contends that it “does not dispute part (ii) of the Petition’s definition is sufficient for a POSITA, however for part (i), a Master of Science in Mechanical Engineering alone would not necessarily focus enough on power electronics to qualify as a POSITA.” PO Resp. 13 (citing Ex. 2020 ¶¶ 39–40).

In its Reply, Petitioner agrees with using “the vantage point of a person with expertise in the design and/or packaging of power electronics (through work or otherwise) in addition to either a Bachelor’s or Master’s degree in a relevant field.” Reply 2.

Patent Owner, in its Sur-Reply, notes Petitioner’s agreement that “a POSITA should have expertise in power electronics design or packaging” and argues that the definition should incorporate “the requisite expertise in power electronics design or packaging.” Sur-Reply 2.

We are reluctant to use the parties’ formulation requiring “expertise” in power electronics because it could be read to include an expert level of skill rather than an ordinary level of skill. Accordingly, we modify the

definition set forth in the Institution Decision, so that a person of ordinary skill in the art would have either (i) a Master of Science in Electrical Engineering, Mechanical Engineering or a related field, and experience in the design and/or packaging of power electronics, or (ii) a Bachelor of Science in Electrical Engineering, Mechanical Engineering or a related field as well as two years of experience in the design and/or packaging of power electronics. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that “specific findings on the level of skill in the art . . . [are not required] ‘where the prior art itself reflects an appropriate level and a need for testimony is not shown’” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

C. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. Only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

In the Petition, Petitioner proposes constructions for two limitations. *See* Pet. 18–21. First, Petitioner proposes that the limitation “active . . . components,” as recited in claims 1 and 13, be construed as “non-passive

components including transistors, diodes, and integrated circuits (ICs) for pulse width modulation.” *Id.* at 19. Second, Petitioner proposes that the limitation “wired housing,” as recited in claim 3, be construed as “housing compatible with conventional through-hole technology.” *Id.* at 20. We determined in the Institution Decision that no claim term required express construction. Dec. 8.

In the Response, Patent Owner proposes that the term “monolithically integrated” in claim 10 be construed as “fabricated from a single piece of silicon.” PO Resp. 10. Patent Owner relies on textbook definitions, testimony, and intrinsic evidence to support its proposed interpretation. *Id.* at 10–11 (relying on Ex. 2020 ¶¶ 44–47; Ex. 2023, 1; Ex. 2024, 3; Ex. 1001, 3:41–45, 5:39–44, 3:67–4:3, 5:47–50, Fig. 3). Patent Owner argues that, based on the ’399 patent’s “Fig. 3 and the description of a single silicon die, a person of skill would understand that a single silicon die comprises a single piece of silicon.” *Id.* at 12 (citing Ex. 2020 ¶ 45).

Petitioner proposes that the term “monolithically integrated” means “fabricated from a single piece of semiconductor material (such as silicon).” Reply 16. Petitioner relies on its own expert’s testimony (Ex. 1035 ¶ 6), Patent Owner’s expert’s testimony (Ex. 1036, 16:14–22), and a dictionary definition (Ex. 1037, 483) to support its proposed construction. *Id.* at 16–17.

Patent Owner agrees that “the Board should adopt the construction of ‘monolithically integrated’ as ‘fabricated from a single piece of semiconductor material.’” Sur-Reply 2.

We note the ’399 patent’s example of monolithic integration: Figure 3 shows a “monolithically integrated bridge rectifier” (Ex. 1001, 4:24–25), also referred to as “integrated bridge rectifier circuit 106” (*id.*

at 5:36–37) in which “[i]nstead of the four individual diode chips shown in FIG. 2, all four diodes are integrated on one die in silicon-on-insulator (SOI) technology” such that “a compact construction of the individual constituents of the circuit results from the monolithic integration.” *Id.* at 5:38–44. This contrasts with the “embodiment shown in FIG. 2,” in which “the diodes for the bridge rectifier 106” are “initially present as separate semiconductor chips, also called dies.” *Id.* at 4:61–64. As quoted by Patent Owner: “In SOI technology, one can realise the four diodes in a single die, so that the additional space requirements for the areas on the leadframe, including the insulation gaps in between, are dropped.” *Id.* at 3:67–4:3 (quoted in PO Resp. 12).

In view of the agreement between the parties, we apply the parties’ proposed joint construction of “monolithically integrated” as “fabricated from a single piece of semiconductor material.” We determine that no other claim term requires express construction. *See Vivid Techs.*, 200 F.3d at 803.

D. Summary of Certain Asserted Art

1. Zverev

Zverev is a German patent application publication titled “Switched-Mode Power Supply” and describes the arrangement of “a rectifier arrangement, a switching transistor and a control circuit for controlling the switching transistor.” Ex. 1003, codes (54), (57). Zverev explains that its switched-mode power supply “suppl[ies] DC voltage to a load connected downstream of the switched-mode power supply.” *Id.* ¶ 35. Figure 2 of Zverev is reproduced below.

FIG 2

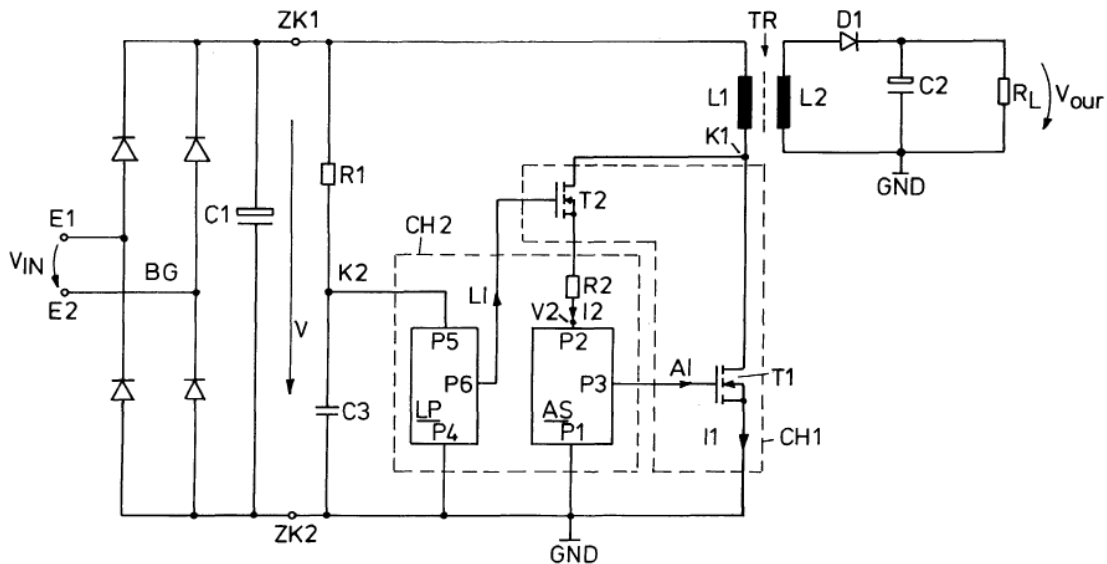


Figure 2 is a circuit diagram of Zverev’s switched-mode power supply. *Id.* ¶ 30. As shown in Figure 2, the “switched-mode power supply has a controllable semiconductor switch T1” which opens or closes to control the application of “supply voltage V to a primary coil L1 of a transformer TR.” *Id.* ¶ 36. “A control circuit AS is provided for controlling the semiconductor switch T1.” *Id.* ¶ 39.

Also shown in Figure 2, “another controllable semiconductor switch T2 is provided.” *Id.* ¶ 42. Semiconductor switch T2 can “supply the control circuit AS with the supply current I2 or supply potential V2 required for standby operation” and can “supply power to the control circuit during normal operation.” *Id.* ¶ 44. Charge pump LP “controls the semiconductor switch T2.” *Id.* ¶ 43.

Additionally, “sense MOSFET T3 can be interconnected with the power transistor T1” (not shown in Figure 2). *Id.* ¶ 48. A sense MOSFET “generates a current measurement signal which is fed to the evaluation circuit” for power management, e.g., a power-saving standby operating

mode or a normal operating mode. *Id.* ¶¶ 17, 41. Sense MOSFET T3 “measures the current (11 [sic]) through the switching transistor (T1).” *Id.* claim 6 (bracketing in provided translation).

Furthermore, Zverev explains that various components of its switched-mode power supply can be integrated on various semiconductor chips. *See id.* ¶¶ 18, 47, 50. In particular, “charge pump LP and the control circuit AS are integrated . . . on a first semiconductor chip CH2” while “MOSFETs T1, T2, T3 are integrated on a second semiconductor chip CH1.” *Id.* ¶ 50; *see id.* Figs. 2, 4. Zverev states that “two semiconductor chips CH1, CH2 can then be interconnected with each other externally and can advantageously be arranged on a single or also several lead frames LF.” *Id.* ¶ 50. “The lead frame(s) LF can then be fitted in a single package G together with the two semiconductor chips CH1, CH2.” *Id.*

2. *Lacap*

Lacap is a US patent titled “Thermally Enhanced Integrated Circuit Packaging System” and is directed to “increased heat dissipation” for integrated circuit packages. Ex. 1008, codes (54), (57). In one embodiment, Lacap’s “thermally enhanced integrated package” is “used with a 64-pin Thin Quad Flatpack Package (TQFP).” *Id.* at 4:55–58. Figure 10 of Lacap is reproduced below.

switching mode power supply (SMPS), and more particularly to a power chip set for an SMPS.” Ex. 1004, code (54), 1:7–9. By way of background, Liaw explains that a power supply circuit “accepts an AC power” and transforms the power input using various circuit components, e.g., transformers, capacitors, windings, resistors, pulse width modulators, and regulators, so that ultimately, “a power supply output voltage is provided.” *Id.* at 1:20–35; *see id.* Fig. 1.

Liaw explains that its “power module 56 for a SMPS comprises a chip set composed of a control unit chip 58 and a high voltage chip 60.” *Id.* at 2:41–44. Liaw states that “high voltage chip 60 contains high voltage circuit elements, while all control circuits contained in the control unit chip 58 being not applied with high voltage.” *Id.* at 2:44–47.

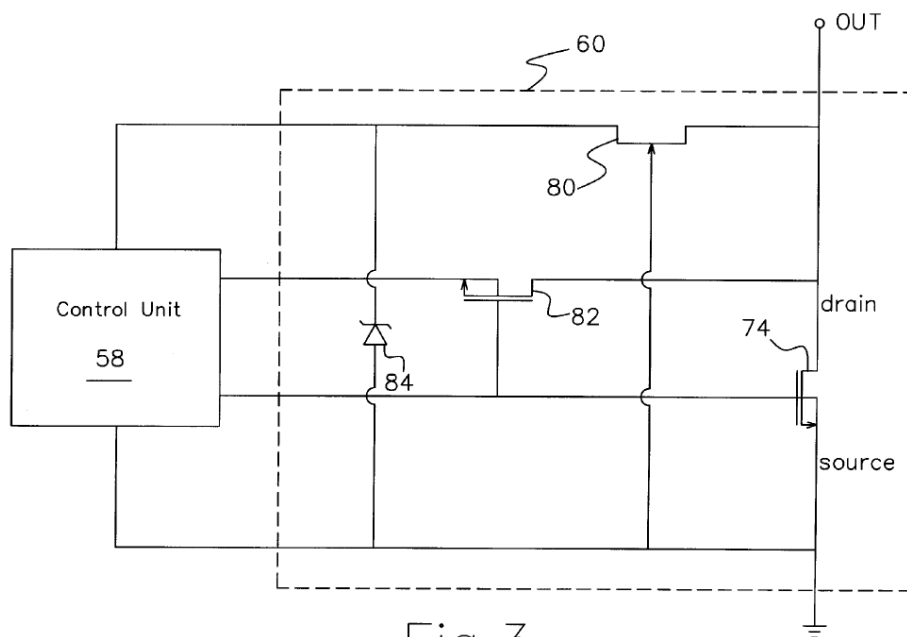


Fig. 3

Figure 3 of Liaw is a circuit diagram of a high voltage chip. *Id.* at 2:34–35. Figure 3 shows high voltage chip 60 “in which a power MOS transistor 74 serves as the switching transistor being turned on/off under the control of the

control signal outputted from the control unit 58.” *Id.* at 3:14–17. High voltage chip 60 includes “junction FET 80 . . . used as the start up element for the control unit 58,” “power MOS transistor 82 serv[ing] as a current sense transistor to detect the drain current of the transistor 74,” and “Zener diode 84 for over voltage protection of the control unit 58.” *Id.* at 3:21–39.

4. *Nam*

Nam is a US patent publication titled “Power Device Having Multi-Chip Package Structure” and is directed to a device in which “the power device, a transistor, which is a switching device, and a control integrated circuit (IC) chip, which is a driving device, are mounted together in a package.” Ex. 1005, codes (54), (57). Figure 4 of Nam is reproduced below.

FIG. 4

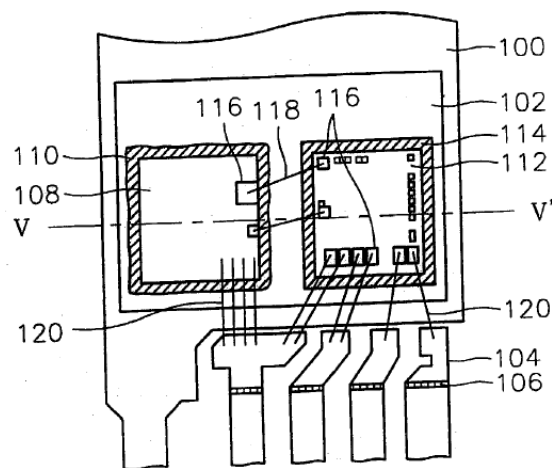


Figure 4 of Nam is a plan view for explaining a power device having a multi-chip package structure. *Id.* ¶ 24. As shown in Figure 4, “power device having a multi-chip package structure . . . includes a lead frame 100 having a chip pad 102, an inner lead 104, and an outer lead (not shown).” *Id.* ¶ 32. Figure 4 also shows “transistor chip 108, which is a switching

device, attached to the chip pad 102 of the lead frame 100 by a conductive adhesive 110.” *Id.* Further, “control integrated circuit (IC) chip 112 . . . is attached on the chip pad 102 of the lead frame 100 by an insulating adhesive tape 114 at the side of the transistor chip 108.” *Id.* The insulating adhesive tape “preserve[s] the insulation of the control IC chip 112 from the transistor chip 108.” *Id.* ¶ 33. “In order to secure a sufficient insulation [to] withstand voltage, the size of the insulating adhesive tape 114 has to be larger than that of the control IC chip 112.” *Id.* ¶ 35. Thus, “it is desirable that distance between the edge of control IC chip 112 and the edge of the insulating adhesive tape 114 is equal to or greater than 100 μm .” *Id.* First gold wire 118 connects “a bond pad 116 of the transistor chip 108 to a bond pad 116 of the control IC chip 112” and second gold wire 120 connects “a bond pad 116 of the transistor chip 108 to a bond pad 116 of the control IC chip 112 to an inner lead 104 of the lead frame 100, respectively.” *Id.* ¶ 32.

E. Petitioner’s Arguments as to Now-Disclaimed Claim 1 – Zverev (Ground 1A)

Petitioner asserts that every element of disclaimed claim 1 is found in Zverev, as set forth in the Petition as follows:

1[pre] *Circuit arrangement for a switch-mode power supply, wherein the switch-mode power supply has a primary side, which can be connected to a supply voltage, and a secondary side, which can be connected to a consumer, (Pet. 25–26 (relying on Ex. 1002 ¶¶ 129–132; Ex. 1003 ¶¶ 1–2, 30, 35–37, 39, 41, 51–52, Fig. 2, claim 1)),*¹⁰

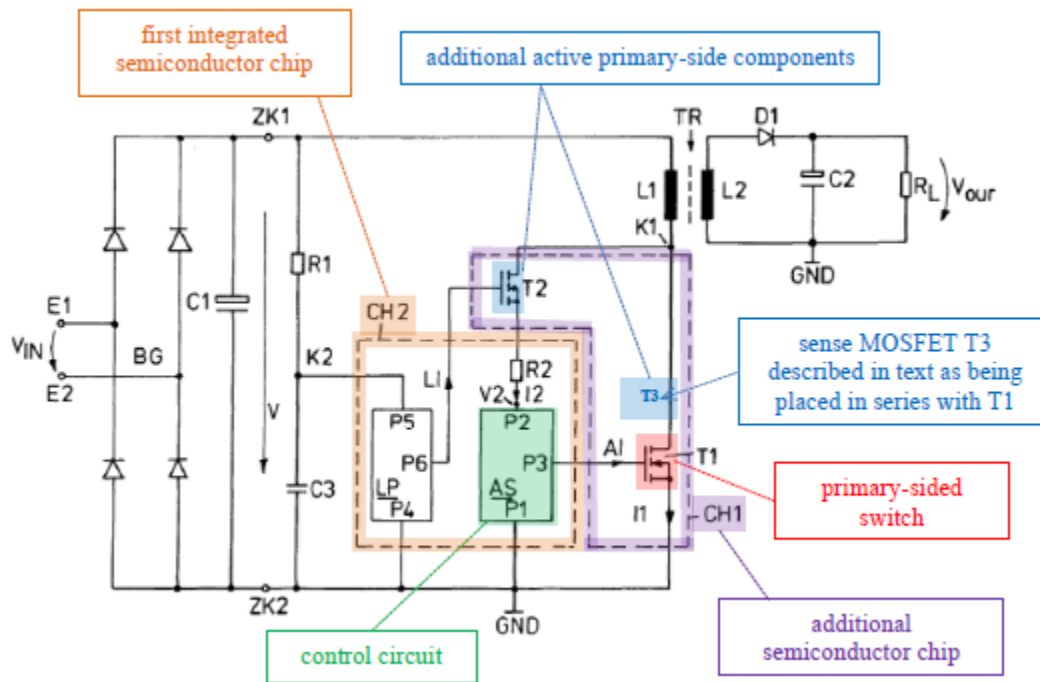
¹⁰ We express no opinion on whether the preamble is limiting.

1[a] *wherein the circuit arrangement (100) comprises a primary-sided switch (102), a control circuit (104) for controlling the primary-sided switch (102) and additional active, primary-sided components (106, 108, 110), (Pet. 26–28 (relying on Ex. 1002 ¶¶ 133–135; Ex. 1003 ¶¶ 11–14, 16–18, 20–21, 32, 36–37, 39–45, 47–50, Figs. 2–4, claims 1–2, 6–8, 14)),*

1[b] *wherein said control circuit (104) is formed by a first integrated semiconductor chip and the primary-sided switch (102) and the additional components (106, 108, 110), are integrated in at least one additional semiconductor chip, (Pet. 28–30 (relying on Ex. 1002 ¶¶ 136–138; Ex. 1003 ¶¶ 18, 20, 32, 47–50, Figs. 2, 4, claim 14)),*

1[c] *said semiconductor chip being separate from the control circuit and arranged on a circuit carrier (112) shared with the control circuit (Pet. 30–31 (relying on Ex. 1002 ¶¶ 139–140; Ex. 1003 ¶¶ 18, 33, 49–50, Fig. 5)).*

Petitioner's contentions are reflected in its annotated version of Zverev's Figure 2, reproduced below.



Zverev’s Figure 2 is a circuit diagram of a switched-mode power supply. Ex. 1003 ¶ 30. In the annotated version of Zverev’s Figure 2, reproduced above, Petitioner identifies control circuit AS on chip CH2 as the claimed “control circuit” that “is formed by a first integrated semiconductor chip.” Pet. 28–29. Petitioner identifies switch T1 as the claimed “primary-sided switch” and switch T2 and sense MOSFET T3 (annotation added by Petitioner) as the claimed “additional active, primary-sided components” and argues that T1, T2, and T3 “are integrated in at least one additional semiconductor chip,” as recited in claim 1, because they are located on chip CH1, rather than chip CH2, which has control circuit AS. *Id.* at 27–29. Petitioner argues that all of these components are in the “primary side” of the power supply, as recited in claim 1, which is connected to supply voltage V. *Id.* at 25–26. Petitioner argues that the load R_L is the claimed “consumer,” to which the components including secondary coil L2 (the

claimed “secondary side”) are attached to deliver power. *Id.* As to limitation 1[c], Petitioner argues that chips CH1 and CH2 are separate chips but can be arranged on the same lead frame (the claimed “circuit carrier”). *Id.* at 30–31; *see* Ex. 1003 ¶ 50 (“These two semiconductor chips CH1, CH2 can then be interconnected with each other externally and can advantageously be arranged on a single or also several lead frames LF. The lead frame(s) LF can then be fitted in a single package G together with the two semiconductor chips CH1, CH2.”).

In its Response, Patent Owner does not dispute these arguments. *See* PO Resp. *passim*.

Based on Petitioner’s contentions and evidence, summarized above, we find that Zverev describes the subject matter of disclaimed claim 1.

F. Petitioner’s Arguments as to Now-Disclaimed Claim 1 – Liaw and Nam (Ground 2)

Petitioner asserts that every element of disclaimed claim 1 is found in the combination of Liaw and Nam, as set forth in the Petition as follows:

1[pre] *Circuit arrangement for a switch-mode power supply, wherein the switch-mode power supply has a primary side, which can be connected to a supply voltage, and a secondary side, which can be connected to a consumer, (Pet. 54–56 (relying on Ex. 1002 ¶¶ 191–196; Ex. 1004, 1:7–9, 1:20–40, 2:41–3:39, Figs. 1–3)),*

1[a] *wherein the circuit arrangement (100) comprises a primary-sided switch (102), a control circuit (104) for controlling the primary-sided switch (102) and additional active, primary-sided components (106, 108, 110), (Pet. 56–58 (relying on Ex. 1002 ¶¶ 197–200; Ex. 1004, 2:41–44, 2:48–63, 3:14–25, 3:32–38, Figs. 2, 3, claims 1, 3)),*

1[b] *wherein said control circuit (104) is formed by a first integrated semiconductor chip and the primary-sided switch (102) and the additional components (106, 108, 110), are integrated in at least one additional semiconductor chip*, (Pet. 58–60 (relying on Ex. 1002 ¶¶ 201–203; Ex. 1004, 2:41–66, 3:14–4:16, Figs. 3, 4, claims 1, 3)),

1[c] *said semiconductor chip being separate from the control circuit and arranged on a circuit carrier (112) shared with the control circuit* (Pet. 60–62 (relying on Ex. 1002 ¶¶ 204–207; Ex. 1004, 2:16–21, 2:41–47, 3:14–39, 4:53–55, Figs. 2, 3, claims 1, 4; Ex. 1005 ¶¶ 3, 5, 11, 13, 32, 40, code (57), Figs. 4, 5, claims 1, 8)).

More particularly, Petitioner relies on Liaw to disclose all the limitations of claim 1 except for the requirement of the shared circuit carrier (limitation 1[c]), for which Petitioner relies on Nam. Pet. 50–61. Petitioner argues that it was “well known that multiple chips could be packaged together in a multi-chip package” and one of ordinary skill in the art would have been motivated to “combine the circuit arrangement disclosed by *Liaw* (i.e., the control unit chip and high-voltage chip) with the packaging disclosed by *Nam*.” *Id.* at 51–52 (citing Ex. 1002 ¶¶ 93–97, 187, 189). More specifically, Petitioner argues that “a POSITA would have been motivated to arrange *Liaw*’s high-voltage chip 60 (including the switching transistor 74) and control unit chip 58 in the package disclosed by *Nam* in the same manner that *Nam* respectively arranges its transistor chip 108 and control integrated circuit (IC) chip 112.” *Id.* at 53 (citing Ex. 1002 ¶190).

In its Response, Patent Owner does not dispute these arguments. *See* PO Resp. *passim*.

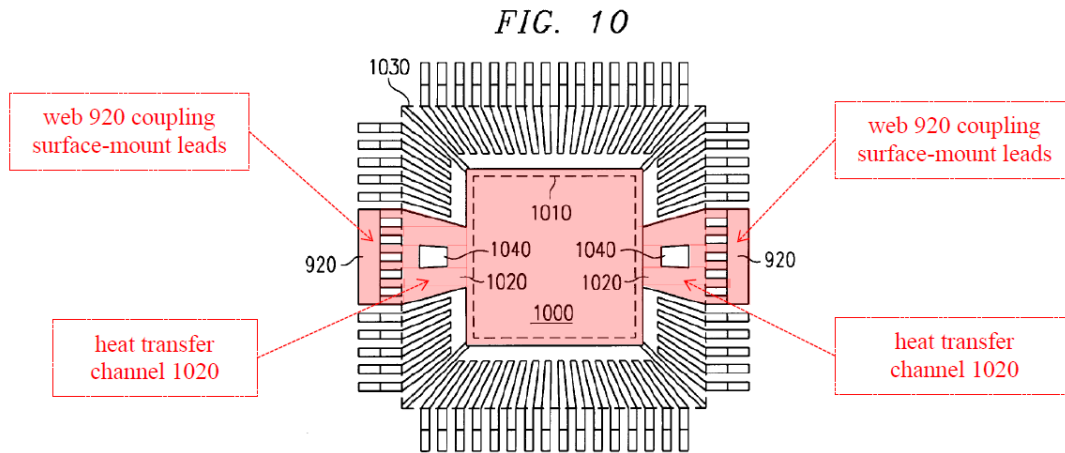
Based on Petitioner’s contentions and evidence, summarized above, we find that the combination of Liaw and Nam teaches the subject matter of disclaimed claim 1 and that a person of ordinary skill in the art would have combined the teachings for the reasons given, with a reasonable expectation of success.

G. Claim 6 – Grounds 1B, 1C, 2, and 3B

Claim 6, which depends from disclaimed claim 1, additionally requires “wherein a metallization of the circuit carrier (112) has cooling areas that are formed for removing heat.” Ex. 1001, 6:49–51. Petitioner argues that claim 6 would have been obvious over Zverev and Shiraishi (Ground 1B), Zverev and Lacap (Ground 1C), Liaw and Nam (Ground 2), and Liaw, Lin, and Shiraishi (Ground 3B). Patent Owner disagrees. PO Resp. 15–19.

1. Ground 1C (Zverev and Lacap)

Petitioner, relying on its Ground 1 arguments for Zverev alone to further argue that Zverev and Lacap would have rendered obvious claim 6, contends that Zverev’s circuit carrier is lead frame LF. Pet. 48. “A POSITA would have understood that such a ‘lead frame LF’ disclosed by *Zverev* is formed of metal.” *Id.* (citing Ex. 1002 ¶¶ 65–71, 178; Ex. 1010, 24; Ex. 1011, 21). Petitioner argues that one of ordinary skill in the art “would have been motivated to modify *Zverev*’s lead frame LF to include the heat transfer channels 1020 as well as the webbed surface-mount leads taught by *Lacap* to improve the thermal characteristics of *Zverev*’s package.” *Id.* at 48–49 (citing Ex. 1002 ¶ 179). Petitioner provides an annotated version of Lacap’s Figure 10, reproduced below.



Pet. 49. Lacap’s Figure 10 is a top cross-sectional view of an integrated circuit package. Ex. 1008, 4:32–35. Petitioner’s annotations include highlighting in pink the “thermally conductive path between die pad 1000 and the top of pins 930” (not called out in Figure 10) as well as web 920 which “increases the heat dissipation from pins 930.” Pet. 49 (quoting Ex. 1008, 5:45–47, 5:15–19; citing Fig. 9 (showing label for pins 930)). According to Petitioner, Lacap’s lead frame includes a “wide heat transfer channel 1020” connecting die pad 1000 to the outer leads, and “heat transfer channel 1020 is typically made of a metal conductor, such as a copper alloy.” *Id.* (citing Ex. 1008, 5:26–28, 5:43–47, 5:31–33, 5:2–4). According to Petitioner, web 920 of Lacap, which is also “typically made of a metal conductor such as a copper alloy” (Ex. 1001, 5:2–4) increases the heat dissipation from pins 930 by increasing the surface area for heat transfer from pins 930 to the ambient environment. Pet. 49 (citing Ex. 1008, 5:15–19). Thus, argues Petitioner, Lacap’s copper-alloy heat transfer channels 1020 and webs 920 serve as cooling areas of the lead frame (i.e. circuit carrier) for removing heat. *Id.* at 50.

Patent Owner argues that neither “Lacap’s heat transfer channel nor web . . . are a metallization *of the circuit carrier* as claimed.” PO Resp. 16. Patent Owner presents an annotated version of Petitioner’s annotated version of Zverev’s Figure 5 (Pet. 31), reproduced below, to argue that “the lead frame is distinct from the pins extending out from the package” and “the web is not part of Zverev’s lead frame (i.e., the circuit carrier) which is inside the package.” PO Resp. 16–17 (citing Ex. 2020 ¶¶ 61–63).

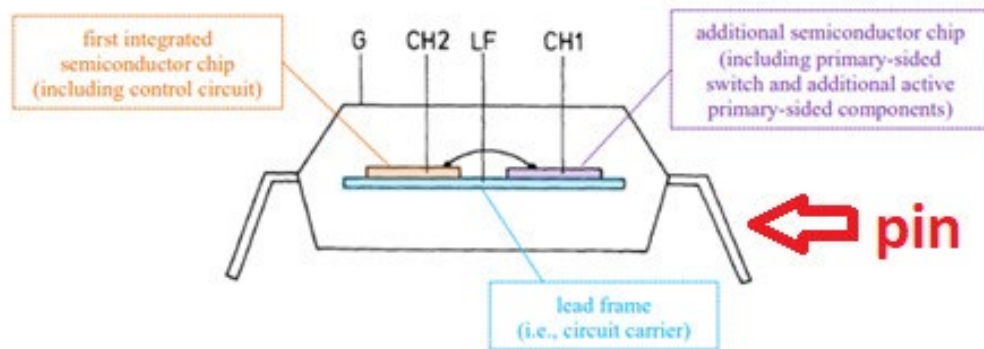


Figure 5 of Zverev “shows a schematic sectional view of an advantageous embodiment example of a package with two embedded semiconductor chips.” Ex. 1003 ¶ 33. Petitioner’s annotations to Zverev’s Figure 5 show lead frame (i.e. circuit carrier) in light blue, and Patent Owner’s annotation points out the pin with a red arrow. Pet. 31; PO Resp. 16. Patent Owner contends, “Lacap’s heat transfer channel is also not part of the lead frame taught by Zverev” because “Lacap teaches that the heat transfer channel connects the die pad to the pins” but “this again is not part of the circuit carrier.” PO Resp. 17. In sum, Patent Owner argues, neither the heat transfer channel nor the web is a metallization of the circuit carrier as claimed. *Id.*

Petitioner replies that Patent Owner’s argument “is based on the false premise that the leads (i.e., pins) of a lead frame, such as disclosed in Lacap, are, in fact, not part of a lead frame in Zverev (or Lacap).” Reply 4–5.

Petitioner explains that a “POSA would have known that the lead frame and its leads (i.e., pins) are fabricated from the same piece of metal at the same time and thus the leads are not distinct from the lead frame,” relying on evidence and testimony about the fabrication process in support of this argument. *Id.* at 5 (citing Ex. 1035 ¶ 15; Ex. 1036, 23:9–24:5). Addressing claim 6’s recitation that a “metallization of the circuit carrier . . . has cooling areas,” Petitioner states that “the way lead frames are manufactured is very consistent. You begin with one piece of metal, and you do a very iterative process of stamping out portions until you are left with, finally, the ultimate lead frame that has the leads as well as the chip carrier portion.” Tr. 11:23–12:15, 13:21–24; *see also* Pet. 9–10; Ex. 1010, 24; Ex. 1011, 21. According to Petitioner, “Lacap and Zverev simply show different views of a lead frame”—a top view in Lacap’s Figure 10, and a side view in Zverev’s Figure 5—and “Zverev’s Fig. 5 is a cross-section through one plane of the package and therefore does not capture how other leads connect to the die pad.” Reply 7–8. One of ordinary skill in the art, according to Petitioner, “would have known that most semiconductor packages connect the die pad to at least one pin to establish a voltage reference for that portion of metal” and, thus, “at the very least, it would have been obvious to a POSA that the die pad would be connected to one (or more) of the leads for this purpose.” *Id.* at 8 (citing Ex. 1035 ¶ 20). Additionally, Petitioner argues, nothing in Lacap “refers to the heat transfer channels as ‘attachments’” and one of ordinary skill in the art “would have understood that the entirety of Lacap’s

lead frame, including the heat transfer channels [1020], was formed from a single piece of metal.” *Id.* at 9 (citing Ex. 1035 ¶¶ 15–16, 22).

Patent Owner responds, first, that Lacap’s web 920 cannot be the claimed heat sink because it is attached to pins outside the package, and “Petitioner still fails to explain how attaching a web to the outside pins renders the web part of the circuit carrier.” Sur-Reply 9. Second, Patent Owner argues that Lacap itself indicates “that the invention is not a standard lead frame as Petitioner alleges.” *Id.* at 10 (citing Ex. 1008, 4:6–8).

On the complete record before us, we are persuaded that the combination of Zverev and Lacap teaches the limitations of claim 6. Preliminarily, concerning the term “metallization,” Petitioner summarizes that “we’ve all . . . understood it to mean that there is essentially a metal part of the circuit carrier that has a cooling area that are formed for removing heat.” Tr. 12:2–4. Patent Owner does not dispute this understanding of “metallization,” and we consider both parties’ arguments and evidence regarding “metallization” in view of this understanding.

Turning to the parties’ arguments, we find that Petitioner argues persuasively that Zverev’s lead frame, or circuit carrier, when combined with Lacap’s heat-dissipating webs and channels, yields “a metallization of the circuit carrier” that “has cooling areas that are formed for removing heat.” Pet. 48–50. Petitioner’s expert supports Petitioner’s assertions. Ex. 1002 ¶¶ 178–183; Ex. 1035 ¶¶ 14–23. Regarding Patent Owner’s arguments based on Zverev’s Figure 5, we credit the testimony that “Zverev’s Fig. 5 is a cross-section through one plane of the package” and “does not capture how other leads connect to the die pad.” Ex. 1035 ¶ 19. Patent Owner’s arguments derive from a narrow interpretation of Zverev’s

Figure 5 cross-section in which the lead frame and pins are depicted with a break between them. An interpretation of Zverev in context, however, indicates that, notwithstanding the slice shown in Figure 5, Zverev's pins are connected to its lead frame. Petitioner has shown that the understood and accepted manufacturing process of a lead frame would result in the metal structures shown and relied upon to meet this element. Reply 5 (citing Ex. 1035 ¶ 15; Ex. 1036, 23:9–24:5); Tr. 13:21–24; Pet. 9–10; Ex. 1010, 24; Ex. 1011, 21. We also credit the testimony of Petitioner's expert that a "POSITA would have known that the majority of semiconductor packages connect the die pad to at least one pin to establish a voltage reference" and "it would have been obvious to a POSITA that the die pad would be connected to one (or more) of the leads for this purpose." Ex. 1035 ¶ 20.

Regarding Patent Owner's argument that Lacap has "attachments to the die pad" that are not part of the lead frame, and therefore the heat transfer channel would not be considered part of the circuit carrier or a metallization of the circuit carrier (PO Resp. 17; Ex. 2020 ¶ 64), we agree with Petitioner that Lacap's heat transfer channels are part of the lead frame in the Zverev-Lacap combination. Ex. 1035 ¶ 22. Lacap "is fabricated using the same tools and equipment as standard, unenhanced integrated circuit packaging." Ex. 1008, 4:4–8. We are persuaded that, understanding the manufacturing process behind Lacap, one of ordinary skill in the art "would have understood that the entirety of Lacap's lead frame, including the heat transfer channels [1020], was formed from a single piece of metal." Reply 9 (citing Ex. 1035 ¶¶ 15–16, 22). We also agree that "Lacap makes clear that its heat transfer channels are an integral part of the lead frame" rather than "attachments." *Id.*

We disagree with Patent Owner’s argument that “Lacap’s web 920 cannot be the claimed heat sink because it is attached to pins outside the package.” Sur-Reply 9. Petitioner identifies Lacap’s heat transfer channels 1020 and webs 920 as cooling areas of the lead frame (i.e. circuit carrier) for removing heat. Pet. 50. We see no claim requirement that the recited cooling areas be located inside an integrated circuit package. Even if there were such a requirement, however, Lacap’s heat transfer channels 1020 are shown *inside* outline 1030 that indicates the limits of the plastic molding 900 in Lacap’s Figure 10. Ex. 1008, 4:32–35, 5:26–28, 5:37–39, Figs. 9, 10 (Figure 9 showing web 920 and plastic molding 900, and Figure 10 showing a top cross-sectional view of Figure 9, showing heat transfer channels 1020 inside outline 1030).

Accordingly, Petitioner has met its burden of demonstrating that the combination of Zverev and Lacap meets the limitations of claim 6. We also find that a person of ordinary skill in the art would have combined the teachings of Zverev and Lacap to “improve the thermal characteristics of Zverev’s package,” with a reasonable expectation of success, as asserted by Petitioner. Pet. 48–49. Based on these findings, and for the reasons discussed above, we conclude that the subject matter of claim 6 would have been obvious based on the combined teachings of Zverev and Lacap.

2. *Ground 2 (Liaw and Nam)*

Petitioner, relying on its claim 1 arguments for Liaw and Nam, argues that this combination also would have rendered obvious claim 6. Pet. 50–62, 66–68. Petitioner argues that one of ordinary skill in the art would have understood that Nam’s lead frame 100 is formed of metal. *Id.* at 66 (citing

Ex. 1002 ¶¶ 65–71, 218). Petitioner’s annotated Figure 4 of Nam is reproduced below.

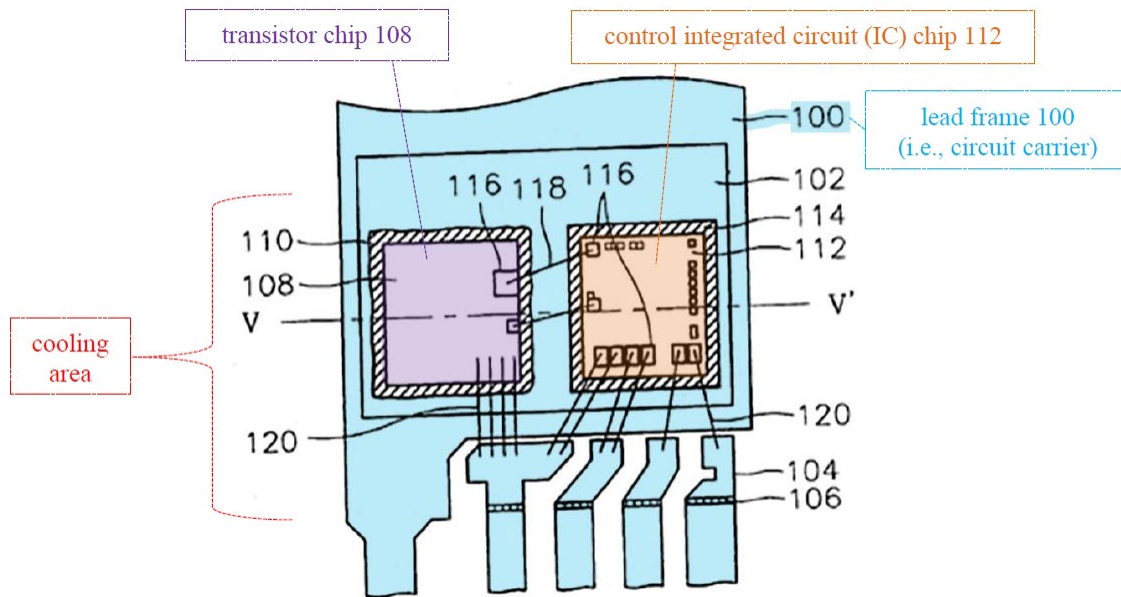


Figure 4 of Nam “is a plan view for explaining a power device having a multi-chip package structure.” Ex. 1005 ¶ 24. Petitioner argues that “chip pad 102 of lead frame 100 (i.e., the circuit carrier) has a large area (i.e., cooling areas) relative to the size of transistor chip 108.” Pet. 66. According to Petitioner, Nam “describes chip pad 102 as part of the lead frame 100,” and a “POSITA would have understood that the continuity of metal provided by lead frame 100 creates a direct thermal path for dissipating heat generated by transistor chip 108.” *Id.* at 67 (citing Ex. 1005 ¶ 32 (describing “lead frame 100 having a chip pad 102”); Ex. 1002 ¶ 219). Additionally, Petitioner argues, a “POSITA would have understood that the exposed portion of *Nam*’s chip pad 102 serves to dissipate heat generated inside the package to the surrounding environment outside the package.” *Id.* at 68 (citing Ex. 1002 ¶ 220).

Patent Owner argues that Nam’s chip pad 102 “is never described as metal—nor does the Petition allege as such.” PO Resp. 18. Patent Owner posits that the chip pad could be ceramic or epoxy, which would not be a “metallization.” *Id.* (citing Ex. 2022, 18:13–25). Patent Owner contends that the “Petition’s only argument that chip pad 102 could be metal is a statement that the ’399 Patent utilizes a large metal surface of the lead frame” but that “Nam never describes its chip pad 102 as metal” and therefore “lacks a metallization of the circuit carrier.” *Id.* at 19 (citing Ex. 2020 ¶ 65).

Petitioner replies that it did “argue in its Petition that Nam’s lead frame is metal.” Reply 10 (quoting Pet. 67 (“A POSITA would have understood that the continuity of ***metal provided by lead frame 100*** creates a direct thermal path for dissipating heat generated by transistor chip 108.”)). Petitioner provides “multiple reasons” that Patent Owner’s “argument that Nam’s lead frame is not metal is wrong”: (1) “Nam discloses a ‘coining’ process used on its lead frame, and a coining process is only used on metals in semiconductor packaging processes” but not used on ceramic or epoxy (*id.* at 10–12 (citing Ex. 1035 ¶¶ 25–29)); (2) “it was well known to a POSA that metals are used to conduct electricity in semiconductor packaging,” and a “POSA would have understood Nam’s disclosure to be discussing a metal lead frame,” particularly in view of Nam’s use of an insulating tape, Nam’s package configuration, and Nam’s metal wire bond (*id.* at 12 (citing Ex. 1035 ¶¶ 30–32)); (3) “Nam’s disclosure of an insulating tape confirms that its lead frame is metal” and “the chip pad of the lead frame is made of a metal” because, “if the chip pad of the lead frame was made of a ceramic or epoxy (which are insulators), then an insulating tape for the control IC chip

would not be needed” (*id.* at 12–13 (citing Ex. 1035 ¶¶ 33–35)); and (4) a “POSA in reviewing Nam’s semiconductor package would have recognized it as a common power package that has the backside of the lead frame exposed for soldering to a PCB or connecting to a heat sink with a thermal interface material” (*id.* at 13 (citing Ex. 1035 ¶¶ 36–38)).

Patent Owner responds that (1) Nam describes 106 as the coining portion, but the Petition relies on chip pad area 102 surrounding transistor 108 as the cooling area, so even if coining portion 106 is metal, that is insufficient to show chip pad 102 is metal; (2) the Reply’s assertion that metals are well known in semiconductor packaging is insufficient; (3) the purpose of insulating adhesive tape is to insulate control chip 112 from transistor chip 108 and says nothing about whether the chip pad is metal; and (4) the Reply’s assertion that it was well known to solder power packages to a PCB is insufficient. Sur-Reply 10–11.

We have reviewed the parties’ arguments and evidence and are persuaded that Petitioner has met its burden by a preponderance of the evidence. The dispute appears to stem from Patent Owner’s assertion that chip pad 102 is separate and distinct from lead frame 100 (PO Resp. 17–19; Sur-Reply 10–11), whereas Petitioner takes the position that chip pad 102 is part of lead frame 100 (Pet. 66–67 (relying on annotated Figure 4 of Nam, highlighting lead frame 100 (including chip pad 102) in light blue); Reply 10–13). We agree with Petitioner’s position that Nam’s chip pad 102 is part of lead frame 100, which Petitioner has persuasively argued are all made of metal. Reply 10; Pet. 67; *see* Ex. 1005 ¶ 32 (discussing “lead frame 100 having a chip pad 102” in reference to Figure 4). Petitioner articulates in the Petition that it relies on chip pad 102 as part of lead

frame 100 as the metallization in claim 6. Pet. 66–68 (citing Ex. 1002 ¶¶ 65–71). The Reply provides additional properly responsive reasons that chip pad 102, as part of lead frame 100, would have been understood to be metal. Reply 10–13 (citing Ex. 1035 ¶¶ 25–38). Petitioner also argues that Patent Owner’s expert agreed that chip pad 102 was metal. *Id.* at 12–13 (quoting Ex. 1036, 29:16–30:12 (“Q. Is it fair to say the chip pad as the lead frame is a metal, as opposed to an insulator in Nam? A. As it relates to Nam . . . I think a POSITA would understand that, yes, the chip frame is metal - - or is a conducting material, which we’re saying, generally, is metal and therefore requires the insulation.”)). Accordingly, Petitioner has met its burden of demonstrating that the combination of Liaw and Nam meets the limitations of claim 6.

As discussed above, we also find that a person of ordinary skill in the art would have combined the teachings of Liaw and Nam with a reasonable expectation of success. We conclude that the subject matter of claim 6 would have been obvious based on the combined teachings of Liaw and Nam.

3. *Grounds 1B and 3B*

Petitioner also argues that claim 6 would have been obvious over the combination of Zverev and Shiraishi (Ground 1B) and Liaw, Lin, and Shiraishi (Ground 3B). Petitioner presents arguments based on Shiraishi as a secondary reference as the basis for its challenge of claim 6 under Grounds 1B and 3B. Pet. 36–42, 82–85. We do not determine the merits of Grounds 1B and 3B. Having determined that Petitioner has met its burden of demonstrating that claim 6 would have been obvious over the combination of Zverev and Lacap (Ground 1C) and Liaw and Nam

(Ground 2), we need not reach the alternative grounds. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Boston Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (nonprecedential) (“We agree that the Board need not address [alternative grounds] that are not necessary to the resolution of the proceeding.”).

H. Claim 10 – Grounds 1A, 2, and 3A

Claim 10, which depends from disclaimed claim 1, further requires that additional active components 106, 108, and 110 “are at least partially combined into a single semiconductor chip and are monolithically integrated.” Ex. 1001, 6:62–65. Petitioner argues that claim 10 was anticipated by Zverev (Ground 1A) and would have been obvious over both Liaw and Nam (Ground 2) and Liaw and Lin (Ground 3A). Patent Owner disagrees. PO Resp. 20–23.

1. Ground 1A (Zverev)

Petitioner, relying on its Ground 1A arguments for Zverev alone to further argue that Zverev anticipated claim 10, contends that Zverev’s “switch T2 and sense MOSFET T3 (collectively, the additional active components)” are “monolithically integrated on the single semiconductor chip CH1,” as shown in annotated Figure 4, reproduced below. Pet. 34–35.

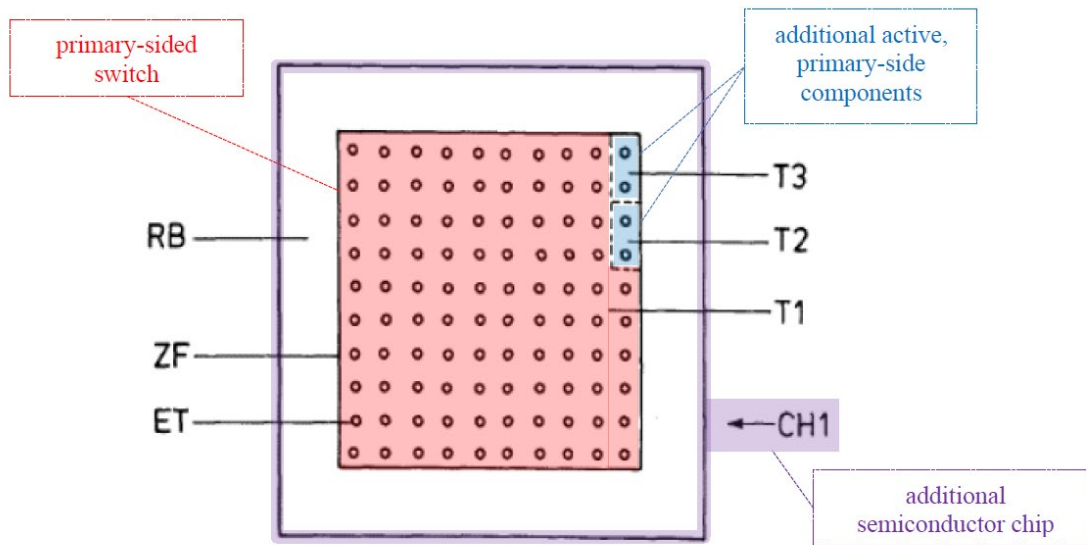


Figure 4 of Zverev “shows in top view a schematic diagram of a cell array ZF in which the power MOSFET T1, the MOSFET T2 acting as a current source, and a sense MOSFET T3 are integrated on a single semiconductor chip CH1.” Ex. 1003 ¶ 47. Referring to recitations of claim 1, Petitioner’s annotations identify Zverev’s cell array ZF (pink) as a “primary-sided switch,” MOSFETs T1 and T2 (blue) as “additional active, primary-side components,” and semiconductor chip CH1 (purple) as an “additional semiconductor chip.” Pet. 35.

Patent Owner argues that “[w]hile Zverev shows a single semiconductor chip, Zverev is silent as to whether that chip is ‘monolithically integrated.’” PO Resp. 21. According to Patent Owner, “monolithically integrated” means “the chip and circuit elements must be fabricated using a single piece of silicon” whereas “integrated alone may encompass other forms of integration such as hybrid integration that forms a circuit on a semiconductor chip with more than one piece of silicon.” *Id.* at 20–21. Without disclosure of the lithographic process used to fabricate

Zverev’s semiconductor chip, Patent Owner argues, “a POSITA would at most understand from Zverev’s single semiconductor chip that circuit elements are placed on a single chip—but with no requirement that the chip is fabricated from a single piece of silicon.” *Id.* at 22 (citing Ex. 2020 ¶¶ 70–72).

Petitioner replies that “Zverev monolithically integrates circuitry in the same die.” Reply 22. Petitioner asserts a skilled artisan would have had this understanding for several reasons: (1) Zverev uses the term “semiconductor chip,” which one of ordinary skill in the art would understand “is referring to a single IC die, not a multi-die package,” instead of using terms such as “multi-chip module, MCM, multi-chip package, or hybrid” that would indicate more than one piece of semiconductor material (*id.* (citing Ex. 1035 ¶ 45)); (2) Zverev expressly distinguishes “chip” from “package” and “explains that two semiconductor chips (i.e. two dies) are arranged in a single package,” which “expressly rejects” Patent Owner’s “underlying argument for validity here—that ‘chip’ and ‘package’ are synonyms” (*id.* at 22–23 (citing Ex. 1035 ¶¶ 46–47)); and (3) Zverev discloses that the switching transistor and the supply device, which are in the same chip, are also in the “same cell array,” which Petitioner argues means “a plurality of single transistors” on a single piece of semiconductor material, such that Zverev’s active components T2 and T3 are “fabricated on the same piece of semiconductor material (i.e. monolithically integrated on the same die))” (*id.* at 23–25 (citing Ex. 1003 ¶¶ 19–20, 47–48, Fig. 4; Ex. 1035 ¶¶ 48–53)).

Patent Owner responds that “[n]othing in the term ‘single semiconductor chip’ alone indicates or requires that the chip be fabricated

from a single piece of semiconductor material.” Sur-Reply 6 (citing Ex. 2020 ¶¶ 70–72). Patent Owner argues that Zverev’s Figure 4 “does not show anything concerning how the array is fabricated and certainly does not show that the array is fabricated from a single piece of semiconductor material.” *Id.* at 7.

Having considered the parties’ arguments and evidence, we are persuaded that Zverev discloses the limitations of claim 10. Petitioner demonstrates persuasively that switch T2 and sense MOSFET T3 are monolithically integrated on a single semiconductor chip CH1. Pet. 34–35; Ex. 1002 ¶ 147–148; Ex. 1003 ¶ 47, Fig. 4. Petitioner also demonstrates persuasively that Zverev’s use of the term “chip” (i.e. a single chip or die) as opposed to “package” (i.e., two chips arranged together) shows that the “single semiconductor chip” is synonymous with “single semiconductor die,” i.e., fabricated from a single piece of semiconductor material. Reply 22–23 (citing Ex. 1003 ¶ 18; Ex. 1036, 50:15–51:11 (Patent Owner’s expert acknowledging this distinction)); *see also* Ex. 1035 ¶¶ 7 (citing Ex. 1001, 4:63–64 as equating semiconductor chips with dies: “separate semiconductor chips, also called dies”), 11. On this point, we credit Petitioner’s expert: the “plain and ordinary meaning” of Zverev’s “integrated on a single semiconductor chip” language “is that there is one piece of semiconductor material (i.e. chip, die) that has the switching transistor, supply device, and/or the sense MOSFET fabricated as an integrated circuit.” Ex. 1035 ¶ 47. In sum, we are persuaded that Zverev “is using ‘chip’ synonymously with ‘die’, i.e., fabricated from a single piece of semiconductor material” rather than synonymously with “package” or any

other terminology that would indicate anything other than fabricated from a single piece of semiconductor material. *Id.*

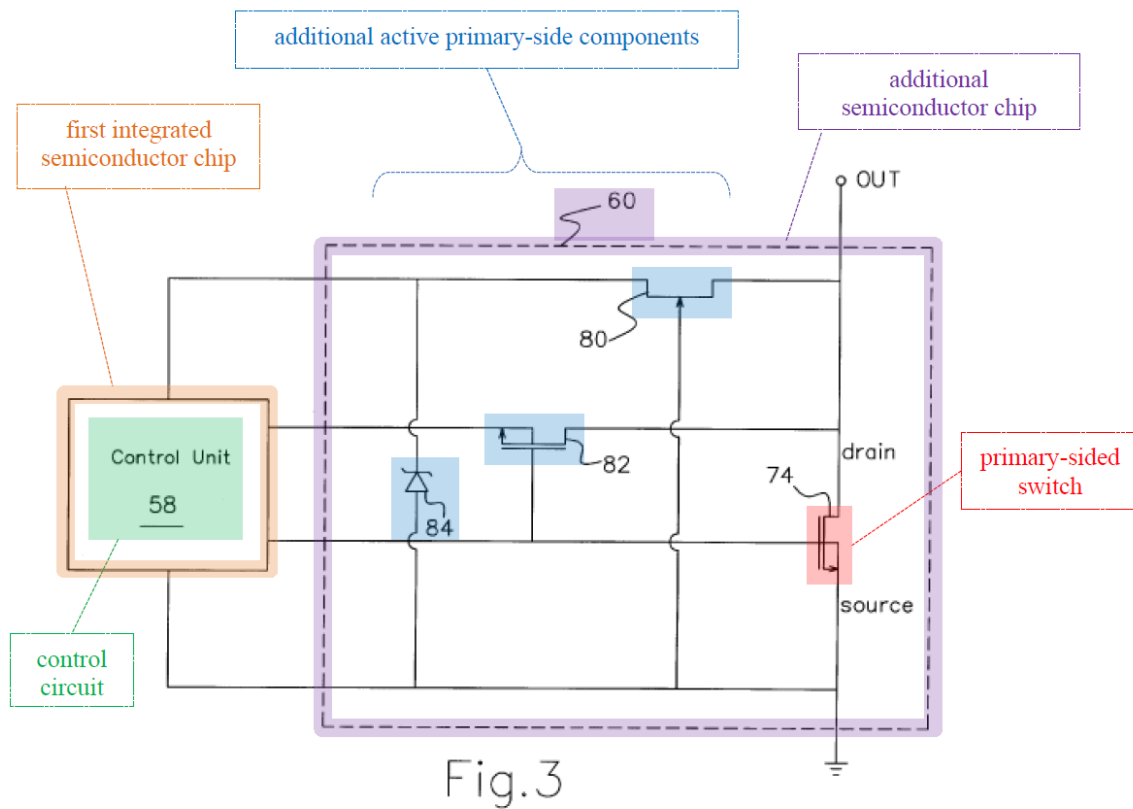
Regarding Patent Owner’s argument that Zverev’s terminology “single semiconductor chip” does not mean “monolithically integrated,” we are persuaded by Petitioner’s evidence and argument to the contrary, as summarized above. Regarding Patent Owner’s argument that nothing about Zverev’s Figure 4 or description shows how Zverev’s cell array is fabricated, we agree with Petitioner’s argument that Zverev’s fabrication process and cell array description show that the additional active components are “monolithically integrated.” Petitioner persuasively argues that Zverev’s “cell array” refers to a “plurality of single transistors” “connected with their load paths and control terminals in parallel to each other,” as described in Zverev, and, therefore, “on a single piece of semiconductor material.” Reply 23–24 (quoting Ex. 1003 ¶¶ 19–20; citing Ex. 1035 ¶¶ 48–49; Ex. 1036, 54:18–55:16). We credit Petitioner’s expert’s reasoning and testimony that, to accomplish Zverev’s configuration of transistors in the same cell array, “these transistors must be on the same piece of semiconductor material.” Ex. 1035 ¶ 49 (citing Ex. 1003 ¶ 20, Fig. 4). We further credit Petitioner’s expert’s testimony that the “details and connections within Figure 4” (Ex. 1003 ¶¶ 47–48) showing and describing the placement of various transistors (i.e. T1, T2, and T3 on chip CH1) teach that T1, T2, and T3 are monolithically integrated on one die. Ex. 1035 ¶¶ 51–52. We have considered Patent Owner’s counterargument that Zverev’s “chip” need not “be fabricated from a single piece of semiconductor material” (Sur-Reply 6–7; Ex. 2020 ¶¶ 70–72), but find this argument lacks supporting evidence and fails to rebut Petitioner’s showing

regarding Zverev's fabrication of a single chip/die with multiple transistors in the same cell array. Accordingly, Petitioner has met its burden of demonstrating that Zverev meets the limitations of claim 6 and, therefore, anticipated claim 6.

2. *Ground 2 (Liaw and Nam)*

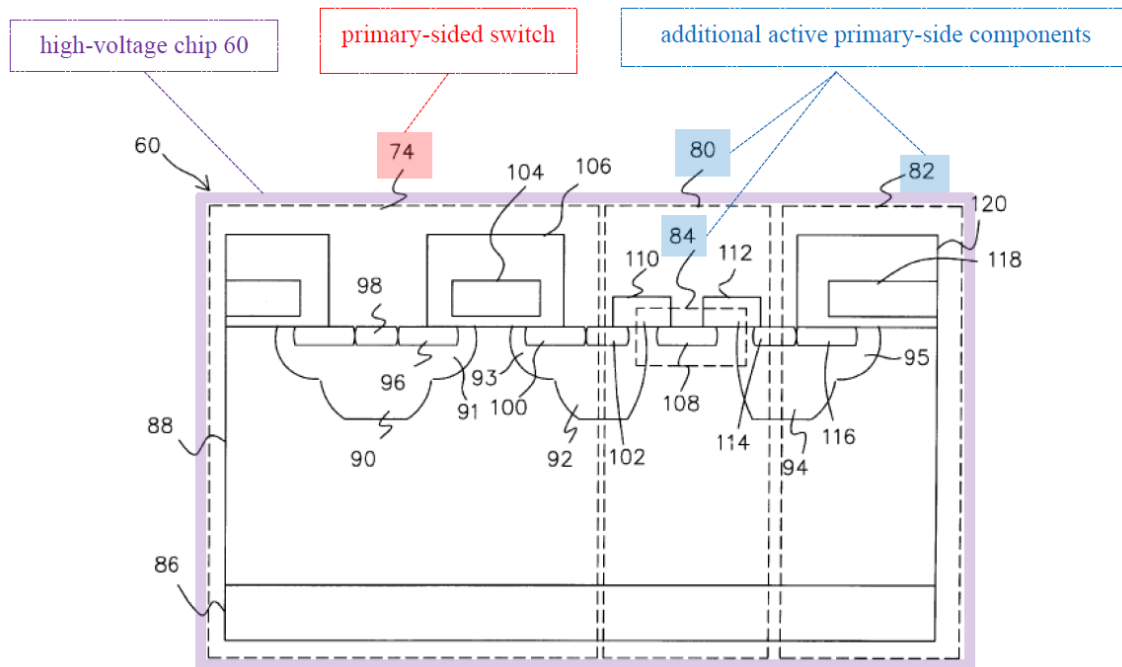
Petitioner relies on its claim 1 arguments for Ground 2 to argue that Liaw and Nam would have rendered obvious claim 10. Pet. 68–70.

Petitioner's annotated Figure 3 of Liaw is reproduced below.



Pet. 69. Figure 3 of Liaw is “a circuit diagram of a high voltage chip.” Ex. 1004, 2:34–35. Petitioner argues that “*Liaw*’s ‘junction FET 80,’ ‘power MOS transistor 82’ (also referred to as a ‘current sense transistor’), and ‘Zener diode 84’” are collectively, the “additional active primary-sided

components” (blue) and are “all monolithically integrated within ‘high-voltage chip 60’ (i.e., a single semiconductor chip)” (purple). Pet. 69. Petitioner further relies on Liaw’s annotated Figure 4, which is reproduced below.



Pet. 70. Figure 4 of Liaw is “a cross-sectional view of the high voltage chip.” Ex. 1004, 2:36–37. Petitioner argues that annotated Figure 4 “shows each of these additional active components monolithically integrated on high-voltage chip 60 with a single substrate 86.” *Id.* (citing Ex. 1004, 3:39–4:16, claims 1, 3; Ex. 1002 ¶ 222).

Patent Owner argues that “Liaw at most discloses a single semiconductor chip and does not disclose that this semiconductor chip is monolithically integrated” and that “a teaching of a single semiconductor chip is insufficient to suggest that the semiconductor chip is monolithically integrated.” PO Resp. 22 (citing Ex. 2020 ¶ 71).

Petitioner replies that Liaw “uses the term ‘single chip,’” which refers to a single die, in contrast to Liaw’s use of a “chip set” packaged in a “module” to refer to two distinct chips. Reply 26. Petitioner contrasts Liaw’s disclosure of its relevant circuitry “integrated on a single chip” (Ex. 1004, 1:15–19, 2:11–15) with Liaw’s disclosure of “two distinct chips” also described as a “chip set” packaged in a “module” (Ex. 1004, 2:16–21). Reply 26. Petitioner argues that “one ‘chip’ of Liaw (i.e., one die) individually contains all the claimed components of claim 10.” *Id.* (citing Ex. 1035 ¶¶ 54–56). “Accordingly, Liaw’s ‘chip’ is a die and thus is monolithically integrated.” *Id.* at 27 (citing Ex. 1035 ¶ 57).

Patent Owner responds that “Liaw’s use of the term ‘single chip’ does not indicate its single chip is fabricated from a single piece of material because a single chip may still be fabricated from multiple pieces of material.” Sur-Reply 8.

We determine that Liaw’s disclosure of how its active components are integrated on a single chip (i.e., die) teaches that Liaw’s additional active components are monolithically integrated. We are persuaded by Petitioner’s arguments explaining how the “relevant circuitry of Liaw is monolithically integrated.” Reply 26–27 (citing Ex. 1004, 1:15–19, 2:11–15). We credit Petitioner’s expert’s interpretation of Liaw: “The only reason for Liaw to state that [the JFET and power MOS transistor] are fabricated in a ‘compatible’ semiconductor ‘process’ is so that they can be integrated on a single chip (die).” Ex. 1035 ¶ 54 (discussing Ex. 1004, 2:11–15). Accordingly, Petitioner has met its burden of demonstrating that Liaw in combination with Nam meets the limitations of claim 10.

As discussed above, we also find that a person of ordinary skill in the art would have combined the teachings of Liaw and Nam, with a reasonable expectation of success. We conclude, therefore, that the subject matter of claim 10 would have been obvious based on the combined teachings of Liaw and Nam.

3. *Ground 3A (Liaw and Lin)*

Petitioner also argues that claim 10 would have been obvious over the combination of Liaw and Lin (Ground 3A). Pet. 81. We do not determine the merits of Ground 3A. Having determined that Petitioner has met its burden of demonstrating that claim 10 would have been anticipated by Zverev (Ground 1A) and would have been obvious over the combination of Liaw and Nam (Ground 2), we need not reach this additional ground. *See SAS Inst. Inc.*, 138 S. Ct. at 1359; *Boston Sci. Scimed, Inc.*, 809 F. App'x at 990.

III. CONCLUSION¹¹

For the reasons discussed above, we determine Petitioner meets its burden of establishing, by a preponderance of the evidence, that the challenged claims are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
10	§ 102	Zverev	10	
6	§ 103	Zverev, Shiraishi ¹²		
6	§ 103	Zverev, Lacap	6	
6, 10	§ 103	Liaw, Nam	6, 10	
10	§ 103	Liaw, Lin		
6	§ 103	Liaw, Lin, Shiraishi		
Overall Outcome			6, 10	

¹¹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

¹² As explained above, because we determine that the challenged claims are unpatentable on other grounds, we decline to address the remaining grounds.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner establishes, by a preponderance of the evidence, that claims 6 and 10 of U.S. Patent No. Patent 7,403,399 B2 are unpatentable; and

FURTHER ORDERED that this is a Final Written Decision; therefore, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 7,403,399 B2

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