

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, DELL TECHNOLOGIES INC.,
and ANKER INNOVATIONS LTD.,¹

Petitioner,

v.

MYPAQ HOLDINGS LTD.,
Patent Owner.

IPR2022-00311
Patent 8,477,514 B2

Before KRISTINA M. KALAN, DANIEL J. GALLIGAN, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Anker Innovations Ltd. filed a motion for joinder and a petition in IPR2022-01134 and has been joined as a petitioner in this proceeding.

I. INTRODUCTION

In this *inter partes* review, Samsung Electronics Co., Ltd. (“Samsung”), Dell Technologies Inc. (“Dell”), and Anker Innovations Ltd. (“Anker”) (collectively “Petitioner”) challenge the patentability of claims 1–20 of U.S. Patent No. 8,477,514 B2 (Ex. 1001, “the ’514 patent”), which is assigned to MyPAQ Holdings Ltd. (“Patent Owner”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine that Petitioner has proven by a preponderance of the evidence that claims 1–20 of the ’514 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) (“In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.”).

A. Procedural History

Samsung and Dell filed a Petition (Paper 3, “Pet.”) challenging claims 1–20 of the ’514 patent on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–12, 14–17, 19, 20	102(a), (b) ²	Chagny ³
1–20	103(a)	Chagny
1–10, 16, 17, 19, 20	102(a), (b)	Hwang ⁴
11, 12, 14–17, 19, 20	103(a)	Hwang, Chagny
18	103(a)	Hwang
13, 18	103(a)	Hwang, Chagny

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011) amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the ’514 patent was filed before this date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

³ Ex. 1004, US 6,873,136 B2, issued March 29, 2005 (“Chagny”).

⁴ Ex. 1006, US 2004/0174152 A1, published September 9, 2004 (“Hwang”).

Pet. 8–9. Patent Owner filed a Preliminary Response. Paper 7. With our authorization, Samsung and Dell filed a reply to the Preliminary Response (Paper 9) addressing discretionary denial issues, and Patent Owner filed a sur-reply (Paper 10). We instituted trial on the asserted grounds of unpatentability. Paper 11 (“Inst. Dec.”), 29.

After institution, Anker filed a motion for joinder and a petition in IPR2022-01134. We joined Anker as a petitioner in this proceeding. Paper 18.

During the trial, Patent Owner filed a Response (Paper 17, “PO Resp.”), Petitioner filed a Reply (Paper 22, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 23, “PO Sur-reply”).

An oral hearing was held on February 24, 2023, a transcript of which appears in the record. Paper 28 (“Tr.”).

Petitioner relies on testimony from Dr. Sayfe Kiaei. Exs. 1002 (Declaration), 1026 (Reply Declaration). Patent Owner relies on testimony from Dr. Frank Ferrese. Ex. 2018. The parties have entered in the record transcripts for depositions of these declarants. Exs. 2020, 2021 (Kiaei Deposition), 1027 (Ferrese Deposition).

B. Real Parties in Interest

Petitioner identifies the following as real parties in interest: Samsung, Dell, Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, Dell Inc., and Anker. Pet. 1; IPR2022-01134, Paper 2 at 1.

Patent Owner identifies itself as the real party in interest and notes that “Transpacific IP Group Limited has an ownership interest in MyPAQ.” Paper 5 at 1; Paper 8 at 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including *MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd.*, 6:21-CV-00398 (W.D. Tex.) (“district court litigation”). Pet. 1; Paper 8 at 1. We are concurrently issuing a final written decision in IPR2022-00312, involving related U.S. Patent 7,675,759 B2. *See* Ex. 1001, code (63) (related application data showing that the ’514 patent is a continuation of a continuation-in-part of Patent 7,675,759 B2).

D. The ’514 Patent and Illustrative Claims

The ’514 patent discloses a power system having a power converter with an adaptive controller that can change an internal operating characteristic (such as switching frequency) of the power converter based on signals about the load to which it provides power. Ex. 1001, code (57), 6:51–7:4, 9:28–38.

Petitioner challenges all 20 claims of the ’514 patent. Pet. 8–9. Claims 1, 6, 11, and 16 are independent. Claims 1 and 6 are illustrative of the claimed subject matter and are reproduced below.

1. A power converter coupled to a load, comprising:
 - a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and
 - a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.
6. A power system, comprising:
 - a power system controller configured to provide a signal characterizing a power requirement of a processor system; and
 - a power converter coupled to said processor system, comprising:

a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and

a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.

II. ANALYSIS

A. *Principles of Law*

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (citing *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary

considerations, if in evidence.⁵ *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “either (i) a Masters of Science in Electrical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering or an equivalent field as well as at least two years of experience in the design of power electronics.” Pet. 9 (citing Ex. 1002 ¶ 35).

At institution, we found this definition to be consistent with the scope and content of the ’514 patent and the asserted prior art, but we omitted the open-ended phrase “at least” to avoid introducing vagueness as to the amount of experience. Inst. Dec. 12.

Patent Owner does not dispute part (ii) of Petitioner’s proposed skill level, but for part (i), Patent Owner argues that “a Master and Bachelor degree in Electrical Engineering alone would not necessarily focus enough on power electronics to qualify as a POSITA.” PO Resp. 16. Relying on Dr. Ferrese’s testimony, Patent Owner argues that,

[t]o qualify as a POSITA based entirely on education, a person would need to demonstrate a significant focus on power electronics while obtaining their Master and/or Bachelor degrees, for example, through taking higher level courses focused on power electronics, publishing on the topic of power electronics, performing lab work or internships in the field of power electronics, or similar.

PO Resp. 16–17 (citing Ex. 2018 ¶ 45). Patent Owner also argues that “a person with a Master and Bachelor degree in many ‘equivalent fields’ to

⁵ The parties do not present arguments related to objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

Electrical Engineering would not be expected to have any significant exposure to power electronics” and that such a person would need “independent expertise in power electronics (through work or otherwise) to qualify as a POSITA.” PO Resp. 17 (citing Ex. 2018 ¶ 46).

We agree with Patent Owner that some degree of familiarity with power electronics would be necessary for a POSITA given the subject matter at issue, and we understood this to be implicit in part (i) of Petitioner’s definition. To address Patent Owner’s concern, we clarify that a person with a Master of Science in Electrical Engineering or an equivalent field would need experience in power electronics to qualify as a POSITA. We are reluctant to use Patent Owner’s formulation of “some independent *expertise* in power electronics” (PO Resp. 17 (emphasis added)) because it could be read to include an expert level of skill rather than an ordinary level of skill.

Thus, we determine that a POSITA would have had either (i) a Master of Science in Electrical Engineering, or an equivalent field, and experience in power electronics or (ii) a Bachelor of Science in Electrical Engineering or an equivalent field as well as two years of experience in the design of power electronics.

We would reach the same determinations on Petitioner’s patentability challenges in §§ II.D–E below even if we adopted Patent Owner’s assessment of a person with a Master of Science degree and “some independent *expertise* in power electronics (through work or otherwise),” which is a higher level of skill.

C. Claim Construction

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b).

Both parties state that they interpret the claims according to “their ordinary and customary meaning,” and neither party proposes express constructions in the claim construction sections of their papers. Pet. 9; PO Resp. 16. In its arguments against Petitioner’s unpatentability contentions, however, Patent Owner proposes constructions for “system operational state” and “core state.” PO Resp. 18–22, 37–38. We discuss each of these terms below.

1. “System Operational State”

Claim 1 recites “a power converter controller configured to receive a signal from [a] load indicating a system operational state of said load.”

Petitioner contends that a signal indicating the activity level of the processor (load) is a signal “indicating a system operational state of said load,” as recited in claim 1. Pet. 18.

Patent Owner counters that a person of ordinary skill in the art “would understand that the term ‘system operational state’ as it pertains to engineering systems, refers to the way in which the system as a whole is being employed or utilized.” PO Resp. 18 (citing Ex. 2018 ¶ 52). Patent Owner argues that examples of signals indicating system operational states from the ’514 patent show that such “signal[s] indicate[] the current or future operational state of the load in a particular context, not simply the current activity level of the processor.” PO Resp. 18–20 (citing Ex. 1001, 9:14–27; Ex. 2018 ¶ 52). According to Patent Owner, “the system operational state is not merely a measure of power level during a low power state[;] it is a state that is driven by various factors, including external requirements, and is ultimately dependent on the context in which the system is being utilized.” PO Resp. 21 (citing Ex. 2018 ¶ 54).

We do not agree with Patent Owner's interpretation of the term "system operational state of said load." As an initial matter, Patent Owner does not direct us to, and we do not find, a definition of "system operational state" of a load in the '514 patent. As noted above, Patent Owner's proposed definition is that "the term 'system operational state' as it pertains to engineering systems, refers to the way in which the system as a whole is being employed or utilized." PO Resp. 18 (citing Ex. 2018 ¶ 52). Claim 1, however, recites "a system operational state *of said load*" (emphasis added), not the system as a whole. Patent Owner's proposed construction, therefore, is not consistent with the claim language. Patent Owner points to examples disclosed in the '514 patent in an attempt to narrow the meaning of the claim term and, as further discussed below, to distinguish the prior art. *See* PO Resp. 18–20 ("The '514 Patent provides examples of signals indicating system operational states that include signals" (citing Ex. 1001, 9:14–27)). But the '514 patent states that these are non-limiting examples. Ex. 1001, 9:11–23 ("Further examples indicating a system operational state include, without limitation").

One passage cited by Patent Owner states the following:

It should also be taken into account that there are loads with different operating states. For example, a server configured to process financial data may operate at a higher level of criticality during normal business hours, and revert to a lower processing state at another time of day. The aforementioned system may require a higher level of performance from the power converter during such periods of high criticality, which may compromise operating efficiency, but which may admit higher operating efficiency during substantial periods of time in the lower processing state.

Ex. 1001, 5:8–17, *quoted in* PO Resp. 20. Patent Owner argues that this passage "illustrates the difference between operational states and system

activity at a particular moment” because, according to Patent Owner, “[i]n this example, the system operational state may be critical or non-critical depending on the performance constraints at particular time of day.”

PO Resp. 20 (citing Ex. 2018 ¶ 53). We disagree. The ’514 patent passage above effectively correlates processor activity and criticality by saying that, in a period of “high criticality,” the load requires a higher performance level from the power converter than when the load is in a “lower processing state.” Ex. 1001, 5:8–17. Thus, this example shows that a “lower processing state” of a data processing server is a “system operational state” of that server, notwithstanding Patent Owner’s labeling this as a “non-critical” operational state. *See* PO Resp. 20.

Patent Owner argues that “two processors in two different systems may have the same activity level at some point in time” but may be in different system operational states because, for example, speed is critical with one processor and energy efficiency is critical with the other. PO Resp. 21–22 (citing Ex. 2018 ¶¶ 55–56). Similarly, Dr. Ferrese posits an analogy in which two vehicles are traveling at the same speed but one is carrying a person to a hospital and the other is carrying a family on a road trip. Ex. 2018 ¶ 55. Dr. Ferrese states that, even though these two vehicles “in a given instant appear to be operating identically,” they “can actually have significantly different system operational states resulting in different preferences in terms of how they are operated and controlled.” Ex. 2018 ¶ 55. These hypotheticals are not persuasive, as they would introduce subjectivity into the claim construction, requiring inquiry into the purpose or intent of a processor’s operation. Furthermore, these hypotheticals are not helpful in resolving the controversy because Petitioner relies on Chagny’s different activity levels as disclosing different system operational states, as

discussed below in section II.D.2.c. Thus, we need not opine on whether one activity level of a processor could result in multiple system operational states.

In addition, we decline to define the system operational state of a load to include “external requirements,” as urged by Patent Owner (PO Resp. 21), because this ignores the plain language of claim 1, which recites “a system operational state *of said load*” (emphasis added), not states external to the load.

For the reasons discussed above, we determine that a signal “indicating a system operational state of said load” encompasses a signal indicating the activity level of a processor. *See* Ex. 1001, 5:8–17. We need not further construe this claim term to resolve the patentability issues before us. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).⁶

⁶ Our Rules require us to consider “[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record in the *inter partes* review proceeding.” 37 C.F.R. § 42.100(b). Patent Owner entered into the record an email from a law clerk in the district court litigation laying out in a table “preliminary claim constructions” for some terms of the ’514 patent before a *Markman* hearing. Ex. 2028. That district court case was stayed before the court issued its final claim construction determinations. Tr. 11:4–10. We have considered the preliminary claim constructions in Exhibit 2028, and we determine that they do not impact the analysis in this proceeding.

2. “Core State”

Claim 4 depends from claim 1 and recites that the “load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.” Claim 9 depends from claim 6 and recites that the “power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.”

Petitioner contends that “the ‘core state’ as described in the ’514 Patent background specifies the activity level (e.g., the rate at which instructions are executed) of the processor.” Pet. 23 (citing Ex. 1001, 5:44–57; Ex. 1002 ¶ 79).

Patent Owner argues that the “core state (C-state) and performance state (P-state) of a processor are defined in the industry standard titled, ‘Advanced Configuration and Power Interface’ which is incorporated by reference into the ’514 Patent.” PO Resp. 37 (citing Ex. 1001, 5:22–27; Ex. 2022 (Advanced Configuration and Power Interface (ACPI) Specification, Revision 3.0, September 2, 2004)). According to Patent Owner, the ’514 patent “defines ‘core state’ as a ‘C-state’ and uses the terms interchangeably.” PO Sur-reply 22–23 (citing Ex. 1001, 5:44–46, 8:7–9, 9:11–15, 25:28–30, 25:65–26:2, Fig. 12; Ex. 2018 ¶¶ 90–96; Ex. 2020, 66:18–25).

Petitioner counters that the claims recite “a core state,” not “a C-state as defined in ACPI,” and that the ’514 patent provides that “a C-state is merely an *example* of a core state.” Pet. Reply 25 (citing Ex. 1001, 9:12–14).

We agree with Petitioner. Claims 4 and 9 recite “core state,” not “C-state.” The specification of the ’514 patent identifies a “C-state” as a type of “core state.” Ex. 1001, 5:44–46 (“Another processor state indicator,

the core state (‘C-state’) . . .”), 25:28–30 (“Turning now to FIG. 12, illustrated is a diagram of an embodiment of processor core states (‘C-states’) in accordance with the principles of the present invention illustrated.”). Figure 12 of the ’514 patent, which “illustrates a diagram of an embodiment of processor core states in accordance with the principles of the present invention,” includes the caption “ACPI C-STATES – IDLE POWER MANAGEMENT.” Ex. 1001, 8:7–9. That the ’514 patent explains the concept of core states by reference to C-states as defined in ACPI (“ACPI C-states”), however, does not mean that the term “core state” is necessarily limited to ACPI C-states. The specification of the ’514 patent elsewhere shows that the ACPI C-states are merely examples within the broader category of core states. For instance, the ’514 patent states that “examples indicating a system operational state include, without limitation, a signal providing a performance state or a core state of a processor *such as a P-state or C-state.*” Ex. 1001, 9:11–23 (emphasis added). Given the ’514 patent’s description of C-states as exemplary core states, we do not agree with Patent Owner’s argument that the recited “core state” should be limited to ACPI C-states.

We need not further construe the term “core state” to resolve the patentability issues before us. *See Realtime Data*, 912 F.3d at 1375.

*D. Anticipation by Chagny
(Claims 1–12, 14–17, 19, 20)*

Petitioner asserts that Chagny anticipated claims 1–12, 14–17, 19, and 20. Pet. 8, 13–39. Patent Owner opposes. PO Resp. 18–39; PO Sur-reply 6–7, 9–25.

1. Chagny

Chagny discloses a voltage regulator module (“VRM”) that provides a regulated direct current (“DC”) voltage output to power a processor of an information handling system. Ex. 1004, code (57). An embodiment is shown in Figure 2A, which is reproduced below.

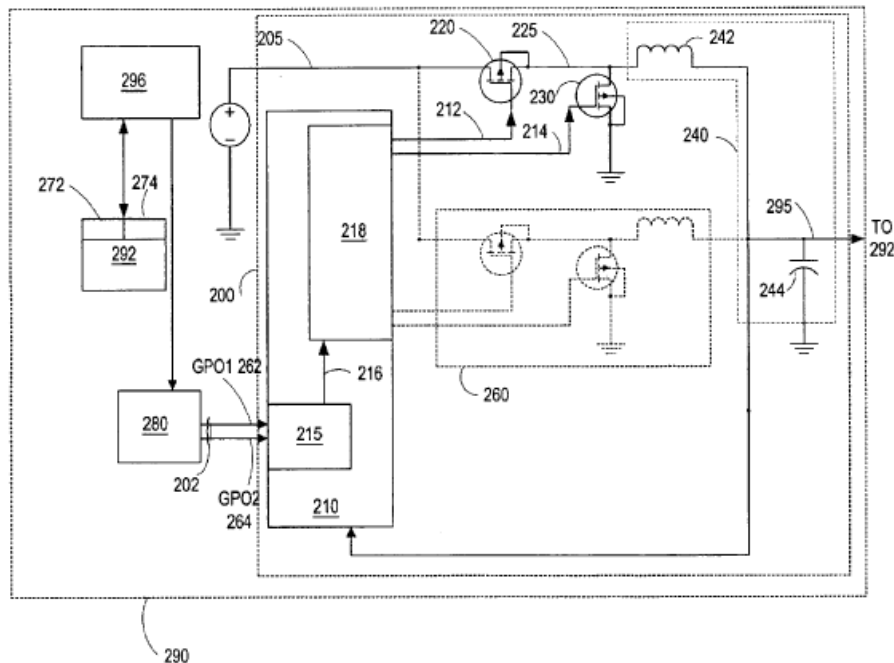


FIG. 2A

In Chagny’s Figure 2A above, VRM 200 receives a DC voltage input 205 and generates a regulated DC voltage output 295, which provides power to processor 292 included in information handling system device 290.

Ex. 1004, 3:52–59. VRM 200 includes, among other things, controller module 210 operable to receive activity input 202 indicative of levels of activity of processor 292 and to select a switching frequency of VRM 200 responsive to activity input 202 so that the switching frequency “dynamically matches the level of activity” of processor 292. Ex. 1004, 3:60–65, 4:66–5:3, 5:9–12.

2. *Claim 1*

a) *Preamble*

Claim 1 is directed to “[a] power converter coupled to a load.”

Petitioner identifies Chagny’s VRM 200 as a “power converter” and argues that “VRM 200 is coupled to provide power to a load including processor 292 and software program 296.” Pet. 13–14 (citing Ex. 1004, 3:54–60, 4:35–37, 7:36–41, Fig. 2A; Ex. 1002 ¶¶ 52–53).⁷

During the trial, Patent Owner did not dispute Petitioner’s contentions for this subject matter. *See* PO Resp. 18–23 (arguments for claim 1); *see also* Paper 12 at 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”); *In re NuVasive, Inc.*, 842 F.3d 1376, 1380–81 (Fed. Cir. 2016) (explaining that the patent owner waived an issue presented in its preliminary response that it failed to renew in its response during trial); Consolidated Trial Practice Guide 52 (Nov. 2019), *available at* <https://www.uspto.gov/TrialPracticeGuideConsolidated> (“Once a trial is instituted, the Board may decline to consider arguments set forth in a preliminary response unless they are raised in the patent owner response.”).

Petitioner’s contentions for the preamble are persuasive. We find that Chagny’s VRM 200 is a power converter because it is “operable to receive a direct current (DC) voltage input 205 and generate a regulated DC voltage output 295.” Ex. 1004, 3:54–56; *see* Pet. 13–14 (discussing this disclosure). This is consistent with the ’514 patent’s description of the operation of power converters. *See, e.g.*, Ex. 1001, 2:67–3:4 (“In an exemplary

⁷ Petitioner and Dr. Kiaei italicize the names of references. We omit this emphasis when quoting Petitioner’s arguments and Dr. Kiaei’s testimony.

application, the power converters have the capability to convert an unregulated dc input voltage such as five volts to a lower, regulated, dc output voltage such as 2.5 volts to power a load.”).

We also find that Chagny’s processor 292 and software program 296 are a “load” to which VRM 200 is coupled because Chagny’s VRM 200 is coupled to and provides power to processor 292 in the same way that the power converter described in the ’514 patent is coupled to and provides power to a microprocessor. *Compare* Ex. 1001, 10:12–15 (“The power converter . . . provides power to a system (not shown) such as a microprocessor coupled to an output thereof.”), *with* Ex. 1004, 3:54–58 (disclosing that “VRM 200 is operable to . . . generate a regulated DC voltage output 295,” which “provides power to a processor 292”).

Based on Petitioner’s persuasive argument and evidence, summarized and addressed above, we find that Chagny describes the subject matter of the preamble.⁸

b) Power Switch

Claim 1 recites that the power converter comprises “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof.”

Petitioner argues that Chagny describes this subject matter because charge switch 220 within VRM 200 is a power switch that conducts for a duty cycle to provide regulated DC voltage output 295 at the output of VRM 200. Pet. 14–16 (citing Ex. 1004, 1:51–59, 5:34–42, 5:44–51, 4:63–65, 6:45–49, Fig. 2A; Ex. 1002 ¶¶ 54–61).

⁸ Because Petitioner has shown that Chagny describes subject matter recited in the preamble, we need not decide whether the preamble is limiting.

Patent Owner does not dispute Petitioner's contentions for this subject matter.

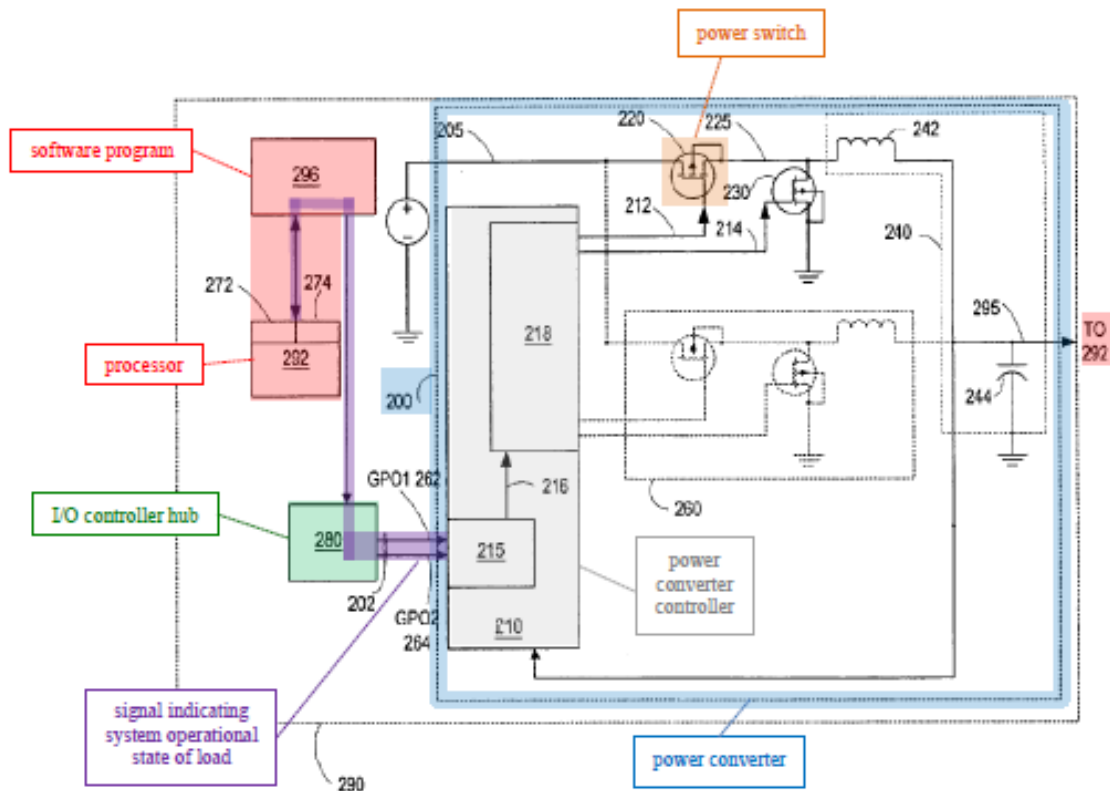
Petitioner's contentions are persuasive. Chagny discloses that power switch 220, controlled by charge control signal 212, is closed (i.e., conducts) during a charge cycle. Ex. 1004, 5:34–40. Chagny explains that “DC voltage input 205 is ‘chopped’ by the charge switch 220 to generate the switched DC voltage output 225,” which is then filtered to generate regulated DC voltage output 295. Ex. 1004, 5:40–42, 5:48–51.

Based on Petitioner's persuasive argument and evidence, we find that Chagny describes “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof.”

c) Power Converter Controller

Claim 1 recites that the power converter comprises “a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.”

Petitioner provides the annotated version of Chagny's Figure 2A reproduced below to illustrate its contentions for this subject matter.



Pet. 17. Chagny's Figure 2A is a diagram of a VRM with a selectable switching frequency. Ex. 1004, 3:17–19. In the annotated version of Chagny's Figure 2A above, Petitioner identifies controller module 210 (gray) within VRM 200 as a power converter controller, and Petitioner illustrates with purple highlighting a signaling path from processor 292 ("load") to software program 296, I/O controller hub 280, and controller module 210 to show "a signal from said load indicating a system operational state of said load." Pet. 17.

Petitioner contends that software program 296 receives a signal from processor 292 indicating the processor's activity level and sends "activity input 202" to controller module 210. Pet. 17–19 (citing Ex. 1004, 4:18–20, 4:35–43, 4:59–67, 5:62–64, Fig. 2A; Ex. 1002 ¶¶ 62–66). Petitioner

contends that “‘activity input 202’ is ‘indicative of the activity level of the processor 292’ (i.e., indicating a system operational state of the load).”

Pet. 18 (citing Ex. 1004, 4:40–43, 5:11–12). Petitioner argues that Chagny’s controller module changes the switching frequency of VRM 200 based on activity input 202 and, therefore, that Chagny discloses “control[ling] an internal operating characteristic of said power converter as a function of said signal.” Pet. 19 (citing Ex. 1004, 3:59–65, 4:46–49, 4:66–5:18; Ex. 1002 ¶¶ 67–69).

Relying on its proposed construction for “system operational state,” Patent Owner argues that “the activity level of Chagny’s processor does not indicate the system operational state.” PO Resp. 22. For the reasons discussed above in section II.C.1, we do not adopt Patent Owner’s interpretation of “system operational state,” and, thus, we do not agree with Patent Owner’s arguments based on its proposed construction.

Chagny discloses that “activity input 202 [is] indicative of the activity level of the processor 292.” Ex. 1004, 5:9–12. Therefore, Chagny’s activity input 202 is a signal indicating the activity level of a processor, which is within the scope of a signal “indicating a system operational state of said load” under the construction set forth above in section II.C.1.

Chagny further explains that “processor 292 loading, usage or activity level will vary depending on the number of instructions executed within a predefined time interval.” Ex. 1004, 4:18–20. Chagny discloses high, medium, and low activity levels. Ex. 1004, 4:31–33. Even applying Patent Owner’s proposed claim construction, Chagny’s low activity level shows how the processor “is being employed or utilized” (PO Resp. 18) consistent with the ’514 patent’s disclosure of a “lower processing state” for a server. Ex. 1001, 5:8–17; *see* above § II.C.1 (discussing this disclosure).

We agree with Petitioner that Chagny's controller module 210 changes the switching frequency of VRM 200 based on activity input 202. *See* Pet. 19 (citing Ex. 1004, 4:46–49, 4:66–5:18; Ex. 1002 ¶¶ 67–69). In particular, Chagny discloses that frequency selector module 215 of controller module 210 “is operable to receive the activity input 202 . . . and select a switching frequency 216 from a plurality of switching frequencies as an output, which dynamically matches the level of activity of the processor 292.” Ex. 1004, 4:66–5:3; *see also* Ex. 1004, 5:9–12 (“Thus the controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.”).

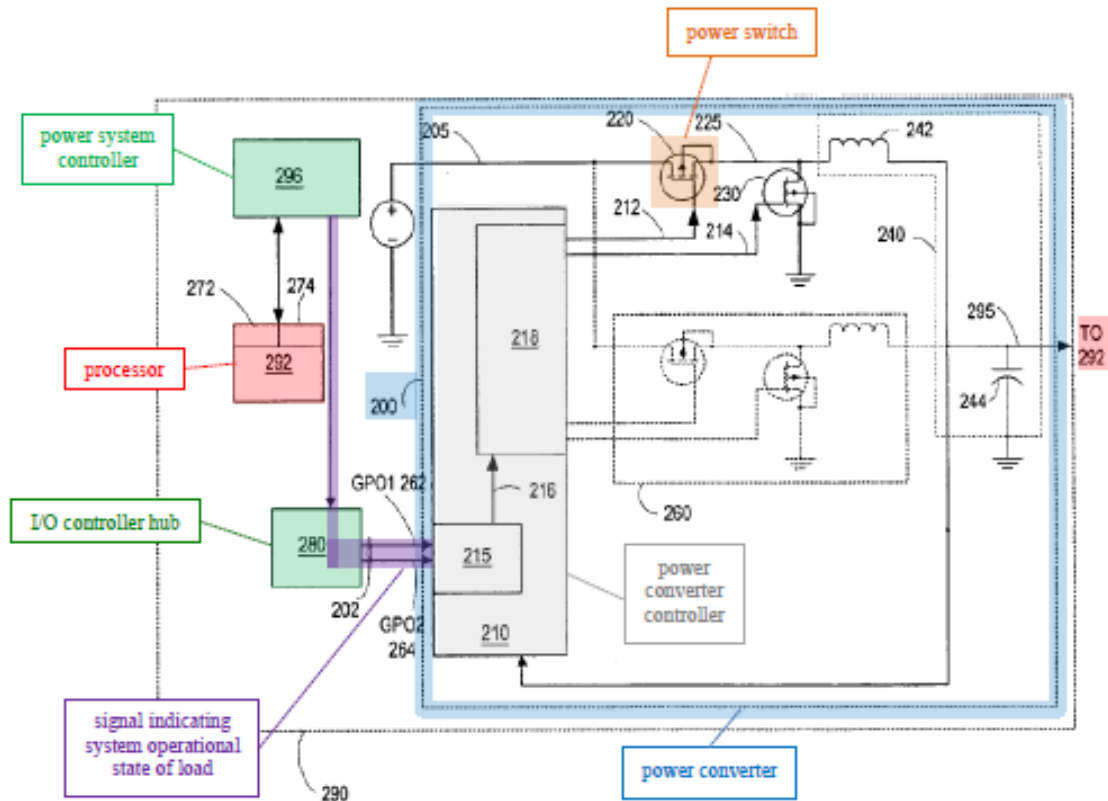
Based on Petitioner's persuasive argument and evidence, we find that Chagny describes “a power converter controller configured to receive a signal from said load indicating a system operational state of said load and control an internal operating characteristic of said power converter as a function of said signal.”

d) Conclusion for Claim 1

For the reasons discussed above and based on Petitioner's contentions and evidence, we find that Chagny describes the subject matter of claim 1 and, therefore, that Chagny anticipated claim 1.

3. Claim 6

Independent claim 6 is directed to a “power system, comprising” “a power system controller” and “a power converter,” which in turn comprises “a power switch” and “a power converter controller.” To illustrate its contentions, Petitioner provides the annotated version of Chagny's Figure 2A reproduced below.



Pet. 25. Chagny’s Figure 2A is a diagram of a VRM with a selectable switching frequency. Ex. 1004, 3:17–19. In the annotated version of Chagny’s Figure 2A reproduced above, Petitioner identifies software program 296 (with or without I/O controller hub 280) (shaded green) as the claimed “power system controller.” Pet. 25–26 & n.4. Petitioner identifies VRM 200 (shaded blue) as the claimed “power converter,” controller module 210 (shaded gray) as the claimed “power converter controller,” and charge switch 220 (shaded orange) as the claimed “power switch.”

Pet. 25–27.

Petitioner argues that Chagny’s software program 296 monitors processor 292 (shaded pink) and generates the activity input, which is a “signal characterizing a power requirement of a processor system,” as recited in claim 6. Pet. 24–26 (citing Ex. 1004, 4:18–20, 4:35–37, 4:40–43, 4:46–61, 5:10–12, 5:62–64, Fig. 2A; Ex. 1002 ¶¶ 86–89).

Petitioner argues that Chagny's VRM 200 is coupled to processor 292 to provide the processor power and, therefore, is a "power converter coupled to said processor system," as recited in claim 6. Pet. 26 (citing Ex. 1004, 3:52–60, Fig. 2A; Ex. 1002 ¶ 90); *see* Ex. 1004, 3:56–59 ("[T]he regulated DC voltage output 295 provides power to a processor 292 included in an information handling system device 290."). For the limitation of claim 6 reciting "a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof," Petitioner refers to its contentions for the same limitation of claim 1. Pet. 27. For the limitation of claim 6 reciting "a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal," Petitioner refers to its contentions for the "power converter controller" of claim 1 and argues that controller module 210 controls the switching frequency ("internal operating characteristic") of VRM 200 based on activity input 202. Pet. 27–28 (citing Ex. 1004, 4:62–5:18; Ex. 1002 ¶¶ 92–94).

Based on Petitioner's persuasive contentions and evidence and for the reasons given for similar subject matter in claim 1, we find that Chagny describes "a power converter" that is "coupled to said processor system" and that has "a power switch" and "a power converter controller" with the functionality for these components recited in claim 6.

Patent Owner argues that Chagny's software program 296 is not the "power system controller" of claim 6. PO Resp. 23–26, 28–32. Patent Owner argues that activity input 202 indicates the level of processor activity but does not "characterize any particular power requirement" and, therefore, that Chagny's software program 296 does not "provide a signal

characterizing a power requirement of a processor system,” as recited of the “power system controller.” PO Resp. 24.

We disagree. Chagny discloses that software program 296 “monitors the processor 292 loading” and, “[b]ased on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292.” Ex. 1004, 4:35–43. Chagny explains that “processor 292 loading, usage or activity level will vary depending on the number of instructions executed within a predefined time interval” and, therefore, that the “demand for power required by the processor 292 is advantageously controlled by limiting the number of instructions executed for a predefined time period.” Ex. 1004, 4:18–20, 5:62–64. Furthermore, as noted above for claim 1, Chagny discloses that frequency selector module 215 of controller module 210 “is operable to receive the activity input 202 . . . and select a switching frequency 216 from a plurality of switching frequencies as an output, which dynamically matches the level of activity of the processor 292.” Ex. 1004, 4:66–5:3; *see also* Ex. 1004, 5:9–12 (“Thus the controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.”). Thus, Chagny discloses that activity input 202 indicates the power required by processor 292; even Patent Owner agrees that a person of ordinary skill in the art “would understand that ‘a signal characterizing a power requirement’ indicates how much power is required.” PO Sur-reply 10 (citing Ex. 1027, 85:10–86:2). We agree with Petitioner’s contentions (Pet. 24–26) and find that Chagny’s activity input 202 is a “signal characterizing a power requirement of a processor system,” as recited in claim 6.

Patent Owner argues that the “the power system controller of the [’514] Patent controls the overall power system,” whereas Chagny’s software program 296 “does not control the power system, and is limited to reporting the activity level of the processor.” PO Resp. 29–30. We disagree. The claimed “power system controller” exerts control over the power system by performing the function recited in the claim, specifically providing a signal to a power converter controller, which controls an internal operating characteristic of the power converter in response to the signal. *See* Inst. Dec. 18; *see also* Ex. 1004, 5:9–12 (“Thus the controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.”). This is consistent with the ’514 patent’s description that the “power system controller . . . induces the power converter to enter a power converter operational state.” Ex. 1001, 26:59–61. Chagny’s software program 296 exerts control in the same manner by providing activity input 202 to frequency selector module 215 of controller module 210, which changes the switching frequency (“internal operating characteristic”) of VRM 200 in response to activity input 202. Ex. 1004, 4:35–37, 4:40–43, 4:62–63, 4:66–5:3, 5:9–12.

Patent Owner also argues that Chagny’s software program 296 is not a power system controller because it runs on device 290, which “corresponds to Chagny’s load.” PO Resp. 30. But as Petitioner points out, “[t]he ’514 Patent includes embodiments where ‘the power system controller’ is constructed as ‘an element’ of a server (i.e., the load).” Pet. 26 n.3 (citing Ex. 1001, 13:12–13, 21:65–22:8, 25:23–27, Fig. 11). We agree with Petitioner because the ’514 patent states that “the power system controller PSC may be constructed as an element of one or more servers SVR,” which

are the loads in Figure 11. Ex. 1001, 22:2–8, 25:24–27, Fig. 11; *see also* Ex. 1001, 13:12–13 (stating that “a power system controller . . . may be constructed as a component of the load”).

For the reasons discussed above and based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claim 6 and, therefore, that Chagny anticipated claim 6.

4. *Claim 11*

Independent claim 11 is directed to a “power system, comprising” “a power system controller” and “a power converter.”

a) Power System Controller

Claim 11 recites that the “power system controller” is “configured to enable operation of components of a processor system to establish a state of power drain thereof” and is “configured to provide a signal to identify operation of said processor system in said state of power drain.”

As with claim 6, Petitioner relies on Chagny’s software program 296 as disclosing the claimed “power system controller.” Pet. 30. Petitioner argues that Chagny discloses that software program 296 sets two bits (UREG_B1 272 and UREG_B2 274) in processor 292 that control the maximum number of instructions that the processor can execute per clock cycle. Pet. 30–31 (citing Ex. 1004, 4:18–20, 5:57–64, 6:3–12; Ex. 1002 ¶¶ 102–103). Petitioner argues that, because processor power demand depends on the processor’s activity level, software program 296 establishes a state of power drain by setting the processor’s activity level. Pet. 31 (citing Ex. 1004, 4:18–20, 5:62–64; Ex. 1002 ¶¶ 102–103).

Patent Owner argues that “the claimed processor system contains a number of components such as memory, hard drives, and specialized circuit cards” and, therefore, that the term “components of a processor system” in

claim 11 “is broader than simply processor 292 and includes a number of peripheral components as well.” PO Resp. 26 (citing Ex. 1001, 13:29–33; Ex. 2018 ¶ 64). According to Patent Owner, Chagny’s software program 296 simply monitors the load “without knowledge of which components of the system are actually drawing power.” PO Resp. 26 (citing Ex. 2018 ¶ 65). Patent Owner further argues that claim 11 “requires that the *operation of the components* of the processor system establish the state of power drain,” meaning that “the claimed power system controller enables operation of processor system components and those components then establish the state of power drain.” PO Resp. 28.

We disagree with Patent Owner’s argument that the “power system controller” is required to have knowledge of which particular components of the processor system are drawing power. Claim 11 recites “a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof” and further recites that the “power system controller [is] configured to provide a signal to identify operation of said processor system in said state of power drain.” Thus, the “state of power drain” refers to the power drain of the processor system as a whole and not the individual power drains of components of the processor system. This is consistent with the ’514 patent specification, which explains that “a power system controller can enable operation of its principal components to establish a state of maximum power drain (e.g., substantially a maximum level of power drain that must be supported by the power system).” Ex. 1001, 13:39–43. This disclosure shows that the power drain measurement relates to what the power system must support, which is the processor system overall, not individual components of the processor system. Thus, we agree with Petitioner that claim 11 does not require

selective enabling of components to establish a separate power drain for each component of a processor system. *See* Pet. Reply 12–13.

We also do not agree with Patent Owner’s argument that claim 11 requires considering “peripheral components.” *See* PO Resp. 26 (citing Ex. 1001, 13:29–33; Ex. 2018 ¶ 64). The passage of the ’514 patent cited by Patent Owner states that a “system such as a personal computer, processor system or a server *is often constructed* with a number of system components such as memory, hard drives, and specialized circuit cards that are specified and installed when the system is assembled for a particular application.” Ex. 1001, 13:29–33 (emphasis added). This passage does not require the “processor system” recited in claim 11 to have any *particular* components. Claim 11 recites “enabl[ing] operation of components of a processor system to establish a state of power drain thereof” and, therefore, also does not recite particular components.

Patent Owner also argues that Petitioner’s position is that “‘processor system’ is limited to the internal components of a processor itself, and not, as discussed in the specification and claims, external components such as memory or hard drives.” PO Sur-reply 12 (citing Pet. Reply 11–12). We disagree. Petitioner’s contention is that a person of ordinary skill in the art would have understood that Chagny’s processor 292 is a processor system with multiple components. Pet. Reply 11–12 (citing Ex. 1026 ¶ 22; Ex. 1002 ¶ 132; Ex. 1015 (1990 publication titled *Microprocessor Data Book*), 4–6, Fig. 1.1). Patent Owner does not dispute, and indeed appears to acknowledge, that there are “internal components of a processor.” *See* PO Sur-reply 13 (“Nothing in the ’514 Patent indicates that ‘processor system’ refers to the internal components of a processor as Petitioners urge.”). We find that a person of ordinary skill in the art would have understood that

Chagny's processor 292 has multiple components, consistent with Petitioner's contention and with the evidence of record. *See* Pet. Reply 11–12; Ex. 1015, 5 (Fig. 1.1 (depicting a CPU with multiple components)); Ex. 1026 ¶ 22 (Dr. Kiaei's testimony, citing Exhibit 1015, that a person of ordinary skill in the art "would have understood that Chagny's processor 292 . . . [is a] processor system[] with multiple components").

Based on Petitioner's contentions, we find that Chagny's software program 296 "enable[s] operation of components of a processor system to establish a state of power drain thereof," as recited in claim 11, by setting UREG_B1 272 and UREG_B2 274 bits in processor 292 "to control the maximum number of instructions executed per clock cycle." Ex. 1004, 5:57–61; *see* Pet. 30–31 (discussing this disclosure). Chagny explains that the "demand for power required by the processor 292 is advantageously controlled by limiting the number of instructions executed for a predefined time period." Ex. 1004, 5:62–64. Given this correlation between instruction execution and power consumption, by controlling the number of instructions that processor 292 can execute, Chagny's software program 296 enables processor 292 (including its constituent components) to establish a state of power drain by operating at a particular level. *See* Ex. 1002 ¶¶ 102 (Dr. Kiaei's testimony that power demand "depends directly on the activity level of processor 292").

Based on Petitioner's contentions, we also find that Chagny's software program 296 "provide[s] a signal to identify operation of said processor system in said state of power drain" by setting activity level bits GPO1 and GPO2 of activity input 202, which "define up to 4 activity levels of the processor 292." Ex. 1004, 4:46–50; *see* Pet. 31–32 (discussing this disclosure); *see also* Ex. 1002 ¶¶ 105–106 (Dr. Kiaei's testimony that "the

activity level identified by the ‘activity input 202’ signal corresponds directly to the state of power drain of the processor system”).

We disagree with Patent Owner’s argument that Chagny’s software program 296 “does not control the power system, and is limited to reporting the activity level of the processor” (PO Resp. 29–30) because, as explained above for claim 6, Chagny’s software program 296 controls the power system by performing the functions recited of the claimed “power system controller.”

Based on Petitioner’s persuasive contentions and evidence and for the reasons discussed above, we find that Chagny describes a “power system controller” that is “configured to enable operation of components of a processor system to establish a state of power drain thereof” and is “configured to provide a signal to identify operation of said processor system in said state of power drain.”

b) Power Converter

Claim 11 recites

a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and to control an internal operating characteristic of said power converter as a function of said power level.

Petitioner’s contentions for this subject matter are similar to its contentions for the “power converter controller” limitations of claims 1 and 6. Pet. 33–36. Petitioner argues that Chagny’s VRM 200 is a power converter and that controller module 210 is a power converter controller. Pet. 33. Petitioner argues that frequency selector module 215 within controller module 210 “senses the activity input 202 signal and thereby the

power level of the state of power drain as indicated by the activity input 202 signal.” Pet. 35 (citing Ex. 1002 ¶ 112). Petitioner contends that Chagny’s controller module 210 controls the switching frequency (“internal operating characteristic”) based on activity input 202, thereby describing “control[ing] an internal operating characteristic of said power converter as a function of said power level,” as recited in claim 11. Pet. 36 (citing Ex. 1004, 4:66–5:18; Ex. 1002 ¶¶ 115–116).

Patent Owner does not dispute Petitioner’s contentions for the “power converter controller” of claim 11. *See* PO Resp.

Based on Petitioner’s persuasive contentions and evidence and for the reasons discussed for similar subject matter in claims 1 and 6, we find that Chagny describes the “power converter” of claim 11.

c) Conclusion for Claim 11

For the reasons discussed above and based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claim 11 and, therefore, that Chagny anticipated claim 11.

5. Claim 16

Independent claim 16 recites a “method of operating a power system” having four steps that correspond to operations recited in claim 11. Petitioner refers to its contentions for claim 11 and argues that Chagny discloses methods for operating a power system. Pet. 38 (citing Ex. 1004, 2:40–43; Ex. 1002 ¶¶ 121–124).

Patent Owner argues that Chagny does not disclose “enabling operation of components of a processor system to establish a state of power drain thereof” for the same reasons given for the corresponding operation recited in claim 11. PO Resp. 25–28. For the reasons explained above in section II.D.4.a, we disagree with this argument.

We agree with Petitioner that its contentions and evidence for claim 11 show that Chagny describes the subject matter of claim 16, and we find, therefore, that Chagny anticipated claim 16.

6. Claims 2, 7, 12, 17

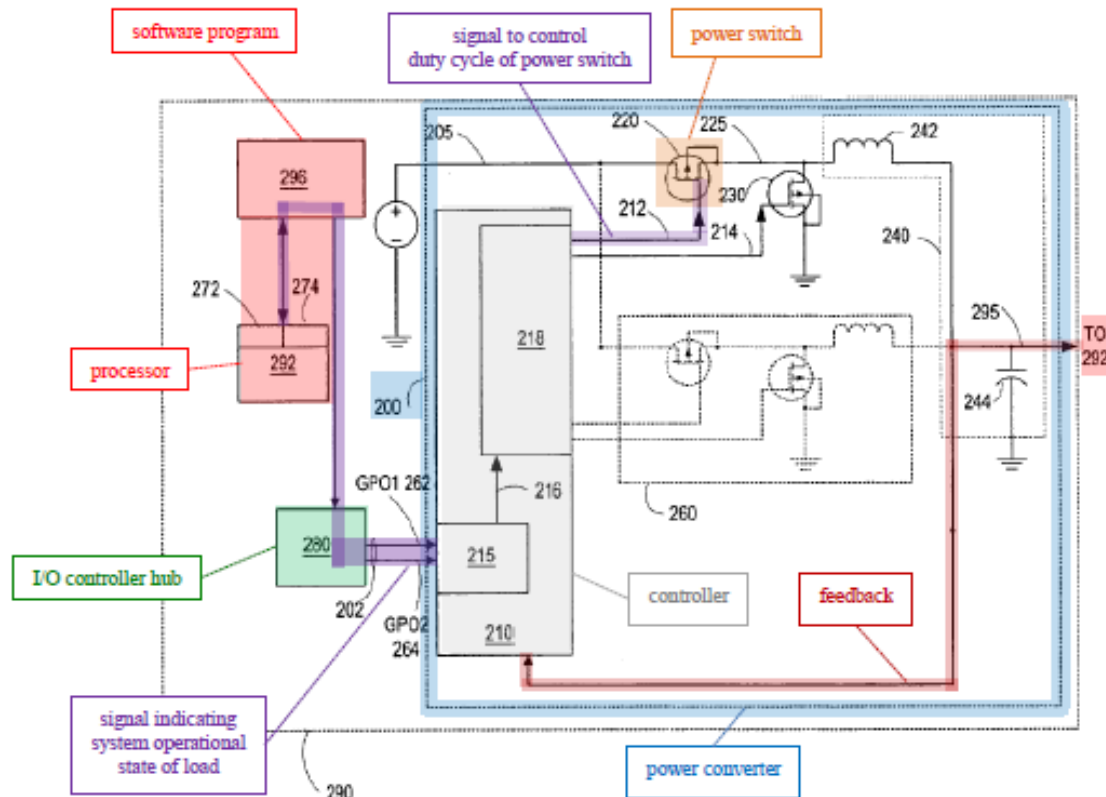
As discussed above, independent claims 1 and 6 each recite that the power converter comprises “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof.” Claims 2 and 7 depend, respectively, from claims 1 and 6, and recite “wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.”

Unlike independent claims 1 and 6, independent claims 11 and 16, from which claims 12 and 17 depend, respectively, do not recite a “power switch.” Claim 12 recites that the “power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof.” Claim 17 recites “inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof.” Chagny discloses this subject matter for the reasons explained in section II.D.2.b.

Similar to claims 2 and 7, claim 12 recites “said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level,” and claim 17 recites “controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.”

a) Petitioner's Arguments

To illustrate its contentions for these claims, Petitioner provides the annotated version of Chagny's Figure 2A reproduced below.



Pet. 20. Chagny's Figure 2A is a diagram of a VRM with a selectable switching frequency. Ex. 1004, 3:17–19. As relevant to the discussion for these claims, in the annotated version of Chagny's Figure 2A reproduced above, Petitioner identifies signal 212 (shaded purple) to charge switch 220 (shaded orange) as a signal to control the duty cycle of the power switch, and Petitioner identifies a connection (shaded pink) from output 295 to controller module 210 as "feedback." Pet. 20.

Petitioner argues that Chagny discloses controlling the duty cycle of charge switch 220 as a function of feedback from output 295 and in accordance with activity input 202. Pet. 20–21 (citing Ex. 1004, 4:62–5:2, 5:34–46, 9:5–7, 10:14–16, Fig. 2A; Ex. 1002 ¶¶ 70–74).

First, as to the requirement to control the duty cycle “as a function of said output characteristic” or “dependent on said output characteristic,” Petitioner refers to its discussion for claim 1 explaining how the duty cycle of charge switch 220 determines the voltage level for output 295. Pet. 21; *see* Pet. 14–16 (explaining that “for a buck power converter, the output voltage is equal to the input voltage times the duty cycle of the high-side switch”). Petitioner relies on Chagny’s disclosure that “controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200.” Ex. 1004, 4:63–65, *cited in* Pet. 21. Petitioner argues that,

[b]ecause it is the duty cycle of charge switch 220 that determines the output voltage, and because Chagny explicitly states that controller module 210 regulates the DC output voltage as a function of the feedback, a [person of ordinary skill in the art] would have understood that controller module 210 is configured to control the duty cycle of charge switch 220 as a function of the feedback from the regulated DC voltage output 295 (i.e., as function of said output characteristic).

Pet. 21 (citing Ex. 1002 ¶ 72). Thus, Petitioner argues, Chagny discloses controlling the duty cycle “as a function of” or “dependent on” output 295 (“said output characteristic”). Pet. 21.

Second, as to the requirement to control the duty cycle “in accordance with said signal” or “said power level,” Petitioner relies on Chagny’s disclosure that frequency selector module 215 receives activity input 202 and selects switching frequency 216 to match the activity level of processor 292 and that FET driver module 218 receives switching frequency 216 and generates charge control signal 212 having that frequency. Ex. 1004, 4:66–5:3, 5:28–31, *cited in* Pet. 21. In particular, Chagny discloses that “FET driver module 218 is operable to receive the selected value of the switching

frequency 216 and generate the charge and discharge control signals 212 and 214, each having the switching frequency 216.” Ex. 1004, 5:28–31. Chagny further discloses that charge control switch 220 responds to charge control signal 212 by generating switched DC voltage output 225 having switching frequency 216. Ex. 1004, 3:66–4:2, 6:46–49, Fig. 3 (step 340). Figure 2A shows that frequency selector module 215 and FET driver module 218 are part of controller module 210. Ex. 1004, 4:62–63. Based on these disclosures, Petitioner argues that Chagny discloses controlling the duty cycle of charge switch 220 “in accordance with” activity input 202, which is the “signal” of claims 1 and 6 and represents the “power level” in claims 11 and 16. Pet. 21, 37.

b) Patent Owner’s Arguments

Patent Owner argues that “activity input 202 sets the switching frequency, not the duty cycle,” that switching frequency and duty cycle “are separate concepts,” that “the duty cycle is independent of the frequency,” and that “Chagny does not even discuss duty cycles.” PO Resp. 33 (citing Ex. 2018 ¶ 82; Ex. 1004, 5:28–31, 4:66–5:3; Ex. 2020, 65:6–15, 86:23–87:18).

In its Sur-reply, Patent Owner argues that Petitioner “cannot rely on knowledge of a POSITA to prove anticipation by Chagny.”

PO Sur-reply 17. Patent Owner also argues that “Chagny does not discuss how the conduction period is determined or what the duty cycle is.”

PO Sur-reply 19.

c) Analysis

As an initial matter, there is no dispute that the “duty cycle is a ratio represented by a conduction period of a power switch to a switching period thereof.” Ex. 1001, 2:57–59; *see* Tr. 42:1–10 (Patent Owner’s counsel

agreeing with the definition of duty cycle set forth in the '514 patent). In other words, the duty cycle is the “ratio of on-time to the total switching period.” Ex. 1002 ¶ 38. We find that Chagny describes a duty cycle because Chagny discloses that charge switch 220 is turned on and off. *See, e.g.,* Ex. 1004, 5:38–40 (“The opening and closing of the charge and discharge switches 220 and 230 is controlled by the charge and discharge control signals 212 and 214 respectively.”). Patent Owner agrees that charge switch 220 is turned on and off. *See* Tr. 43:23–44:1 (Q: “Is Patent Owner disputing that there is a conduction time in Chagny that the FET is turned on and off?”; A: “The FET is turned on and off, yes, so that’s correct.”); *see also* Tr. 45:11–12 (Patent Owner’s counsel stating that “it certainly is turning the FET on and off”). Thus, Chagny discloses that power switch 220 has a duty cycle notwithstanding Patent Owner’s argument that “Chagny does not even discuss duty cycles.” *See* PO Resp. 33.

As to Patent Owner’s argument that “activity input 202 sets the switching frequency, not the duty cycle” (PO Resp. 33), we agree with Petitioner that “[t]here is no requirement that said signal indicating system operational state must ‘set’ the duty cycle.” *See* Pet. Reply 19–20. Petitioner contends that, because the duty cycle of charge switch 220 determines the output voltage and because that output voltage is then used as feedback to regulate the output voltage (Ex. 1004, 4:63–65), a person of ordinary skill in the art would have understood that the duty cycle of charge switch 220 is controlled “as a function of the feedback from the regulated DC voltage output 295 (i.e., as function of said output characteristic).” Pet. 21 (citing Ex. 1002 ¶ 72; Ex. 1009, 17–18).

As to Patent Owner’s argument that Petitioner “cannot rely on knowledge of a POSITA to prove anticipation by Chagny”

(PO Sur-reply 17), we understand that Petitioner is relying on what a person of ordinary skill in the art would have understood from Chagny's disclosure. This is appropriate and indeed necessary because "[a]nticipation is established when 'one skilled in the art would reasonably understand or infer from the prior art reference's teaching that every claim [limitation] was disclosed in that single reference.'" *CRFD Research, Inc. v. Matal*, 876 F.3d 1330, 1338 (Fed. Cir. 2017) (quoting *Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192–93 (Fed. Cir. 2003)). We also credit Dr. Kiaei's un rebutted testimony that, "for a buck power converter, the output voltage is equal to the input voltage times the duty cycle of the high-side switch (referred to as charge switch [220] in Chagny)." Ex. 1002 ¶ 57. As noted above, Chagny discloses that "controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200." Ex. 1004, 4:63–65, *cited in* Pet. 21. Thus, we find that Chagny discloses controlling the duty cycle as a function of the output voltage in order to regulate the output voltage as part of the feedback loop.

As to Patent Owner's argument that "Chagny does not discuss how the conduction period is determined or what the duty cycle is" (PO Sur-reply 19), the claims do not recite any particular value for the duty cycle, and Patent Owner does not dispute Petitioner's arguments and Dr. Kiaei's testimony as to how the duty cycle is controlled to regulate the output voltage, as discussed in the previous paragraph.

As for controlling the duty cycle "in accordance with" the signal "indicating a system operational state" or the power level, Petitioner's contention is that charge and discharge control signals 212 and 214 have the switching frequency 216 that is selected based on activity input 202 and,

therefore, that Chagny discloses controlling the duty cycle “in accordance with” activity input 202 based on the relationship between frequency and period of the duty cycle. Pet. 21 (citing Ex. 1004, 4:66–5:2, 5:34–46; Ex. 1002 ¶ 73); Pet. Reply 20 (citing Ex. 1026 ¶ 31). The switching frequency is the inverse of the switching period. Ex. 1026 ¶ 31. We credit Dr. Kiaei’s un rebutted testimony that, “[a]s a matter of simple math, the duty cycle can therefore also be described as a function of both the conduction period and the *switching frequency*.” Ex. 1026 ¶ 31. By disclosing setting the switching frequency and, thus, the switching period, Chagny discloses that the duty cycle is controlled “in accordance” with activity input 202, upon which the switching frequency is based.

In sum, we find persuasive Petitioner’s contentions for claims 2, 7, 12, and 17. We find that Chagny discloses controlling the duty cycle of charge switch 220 as a function of the feedback from the regulated DC voltage output 295 based on Chagny’s disclosure that “controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200.” Ex. 1004, 4:63–65. We also find that Chagny discloses controlling the duty cycle of charge switch 220 in accordance with the signal indicating the system operational state or the power level based on Chagny’s disclosure that frequency selector module 215 receives activity input 202 and selects switching frequency 216 to match the activity level of processor 292 and that FET driver module 218 receives switching frequency 216 and generates charge signal 212 having that frequency. Ex. 1004, 4:66–5:3, 5:28–31.

For the reasons discussed above and based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claims 2, 7, 12, and 17 and, therefore, that Chagny anticipated these claims.

7. Claims 3, 8, 14, 19

Claims 3, 8, and 14 depend, respectively, from claims 1, 6, and 11 and recite “wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.” Claim 19 depends from claim 16 and recites “wherein said controlling said internal operating characteristic comprises occurs over a period of time.”

Petitioner argues that Chagny discloses dynamically changing the switching frequency in response to activity input 202, which may be periodically updated. Pet. 22 (citing Ex. 1004, 4:43–45, 4:66–5:3, 5:9–12). Petitioner contends that a person of ordinary skill in the art “would have understood that Chagny’s power converter controller is configured to adjust the switching frequency over a period of time as the processor loading (and thus activity input 202) changes.” Pet. 22 (citing Ex. 1004, 4:18–20, 5:65–66; Ex. 1002 ¶¶ 75–77).

Patent Owner argues that “the ’514 Patent is clear that it is beneficial to adjust operating characteristics over gradual periods of time” whereas “Chagny’s controller module 210[] causes an instant response to the activity input that causes a change in the frequency.” PO Resp. 35 (citing Ex. 1001, 16:52–17:14; Ex. 2018 ¶¶ 83, 86). Claims 3, 8, 14, and 19, however, do not recite a “gradual” time period or any specific time period at all. As Petitioner correctly points out (Pet. Reply 22–23), the ’514 patent explains that the timescales for changing operating characteristics vary, giving as an example that “the switching frequency of a power conversion stage or the timing delay between power switch conduction intervals can be readily changed on a much faster time scale, ultimately on a cycle-by-cycle basis.” Ex. 1001, 16:52–61. Thus, we disagree with Patent Owner’s argument that changes have to be gradual.

Petitioner’s contentions are persuasive. Chagny discloses that “activity input 202 may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis.” Ex. 1004, 4:43–45. Chagny discloses that “controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.” Thus, Chagny discloses adjusting the switching frequency over a period of time. As activity input changes, the switching frequency changes accordingly.

For the reasons discussed above and based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claims 3, 8, 14, and 19 and, therefore, that Chagny anticipated these claims.

8. Claims 4, 9

Claim 4 depends from claim 1 and recites “wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.” Claim 9 depends from claim 6 and recites “wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.”

Petitioner argues that the core state “specifies the activity level (e.g., the rate at which instructions are executed) of the processor” and that Chagny’s disclosure of various activity levels (low, medium, high) for its processor describes the subject matter of claim 4. Pet. 23–24 (citing Ex. 1001, 5:44–61; Ex. 1004, 4:23–30, 4:43–49, 6:3–4; Ex. 1002 ¶¶ 79–82). For claim 9, Petitioner argues that “the processor power requirement depends on the activity level of the processor.” Pet. 28 (citing Ex. 1004, 4:18–20, 5:62–64; Ex. 1002 ¶¶ 97–98).

Patent Owner argues that, as a matter of claim construction, the recited “core state” should be limited to ACPI C-states. *See* PO Resp. 37; PO Sur-reply 22–23. We disagree for the reasons given in section II.C.2.

Patent Owner also argues that Chagny “does not teach using C-states or P-states to define the system operational state” and that “it is not possible for the system of Chagny to ascertain the P-state or C-state based on its signal 202 indicative of processor activity level.” PO Resp. 38. Putting aside whether the recited “core states” are limited to ACPI C-states, Patent Owner’s arguments are not commensurate in scope with claims 4 and 9. For example, claim 1 recites “a power converter controller configured to receive a signal from said load indicating a system operational state of said load,” and dependent claim 4 recites “wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.” Claim 4 does not recite that the “core state” itself needs to be reported to the power converter controller or that the power converter controller must be able to “ascertain” the core state of the processor. Rather, there is a signal “indicating a system operational state of said load,” and the “system operational state is dependent on . . . a core state.” Similarly, claim 6 recites “a power system controller configured to provide a signal characterizing a power requirement of a processor system,” and dependent claim 9 recites that the “power requirement . . . is dependent on . . . a core state.” Thus, claim 9 also does not require the system to know or determine the core state.

Patent Owner characterizes the core states of the ’514 patent as follows:

The core state (or C-state) in the ’514 Patent is either a sleep mode (where the activity level of the processor is zero) or (in

state C0), “full operational level” (when the activity level of the processor can be anything). At best, a core state discloses that the activity level of the processor is zero because the system is in sleep mode. Thus, Chagny’s activity level is not a core state as required by claims 4 and 9.

PO Resp. 39 (citing Ex. 1001, 5:44–54). Thus, according to Patent Owner, an operational processor has a core state different from a processor in sleep mode.

We are persuaded by Petitioner’s contention for claim 4 that “the activity level of processor 292 (i.e., system operational state of the load) at any of the activity levels disclosed by Chagny (e.g., low, medium, high) is dependent on at least a core state of the processor 292.” Pet. 23–24 (citing Ex. 1002 ¶¶ 80–81). We agree because the activity levels (low, medium, and high (Ex. 1004, 4:23–30)) show that Chagny’s processor is in an operational core state “when the activity level of the processor can be anything,” according to Patent Owner. *See* PO Resp. 39. Thus, Chagny’s activity level (“system operational state”) is “dependent on” the processor being in an operational “core state.” Similarly, for claim 9, Chagny shows that the processor’s power demand is based on the processor’s activity level (Ex. 1004, 4:18–20, 5:62–64), as discussed for claim 6, and, therefore, the power requirement for Chagny’s processor is dependent on an operational core state.

For the reasons discussed above and based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claims 4 and 9 and, therefore, that Chagny anticipated these claims.

9. Claims 5, 10, 15, 20

Claims 5, 10, 15, and 20 depend, respectively, from claims 1, 6, 11, and 16 and recite “wherein said internal operating characteristic is selected

from the group consisting of: . . . a switching frequency of said power converter.” Petitioner refers to its discussion of the “power converter controller” limitation of claim 1, in which Petitioner identifies Chagny’s switching frequency 216 as the recited “internal operating characteristic.” Pet. 19, 24. Patent Owner does not dispute Petitioner’s contentions for these claims. We find that Chagny’s switching frequency 216 describes “a switching frequency of said power converter.”

Based on Petitioner’s contentions and evidence, we find that Chagny describes the subject matter of claims 5, 10, 15, and 20 and, therefore, that Chagny anticipated these claims.

*E. Obviousness Based on Chagny
(Claims 1–20)*

Petitioner asserts that claims 1–20 would have been obvious over Chagny. Pet. 8, 40–44. As the Court of Appeals for the Federal Circuit has stated, “a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for ‘anticipation is the epitome of obviousness.’” *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983) (citing *In re Fracalossi*, 681 F.2d 792 (CCPA 1982)). Because we find that Chagny anticipated claims 1–12, 14–17, 19, and 20, we also conclude that the subject matter of claims 1–12, 14–17, 19, and 20 would have been obvious based on the teachings of Chagny.

Claims 13 and 18 are the only claims included in this obviousness ground that are not in the Chagny anticipation ground. Claims 13 and 18 depend, respectively, from claim 11 and 16 and recite “wherein said signal is provided upon startup of said processor system.”

Petitioner argues that a person of ordinary skill in the art “would have found it obvious that the generation and provision of Chagny’s activity

input 202 signal (i.e., said signal) would occur throughout the operating time of Chagny’s information handling system device 290, including upon startup.” Pet. 43–44 (citing Ex. 1002 ¶¶ 138–140). In support of this contention, Petitioner relies on Chagny’s disclosure that “activity input 202 may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis.” Ex. 1004, 4:43–45, *cited in* Pet. 43. Petitioner argues that “startup of information handling system device 290 as a whole[] would be among the ‘event basis’ or ‘on-demand basis’ upon which Chagny updates and provides the activity input 202 signal (i.e., provides said signal).” Pet. 44 (citing Ex. 1004, 4:40–45; Ex. 1002 ¶ 140).

In its Response, Patent Owner generally alleges that Petitioner’s obviousness contentions improperly gap-fill missing limitations with the knowledge of a person of ordinary skill in the art, but Patent Owner does not directly respond to Petitioner’s articulated reasoning with respect to claims 13 and 18. PO Resp. 40–41 (citing *DSS Tech. Mgmt. Inc. v. Apple Inc.*, 885 F.3d 1367, 1377 (Fed. Cir. 2018); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1274–75 (Fed. Cir. 2017); *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016)).

We find Petitioner’s obviousness contentions for claims 13 and 18 persuasive. Claim 11 recites that the power system controller is “configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain,” and we find Chagny describes this subject matter for the reasons discussed above in section II.D.4.a. Claims 13 and 18 recite the time at which the signal is provided, specifically “upon startup.” Petitioner’s contention is simply that it would have been obvious for Chagny’s activity

input 202 to be provided throughout the operation of Chagny's system 290, including upon startup. Pet. 43–44. Petitioner's contention is persuasively supported by Dr. Kiaei's testimony (Ex. 1002 ¶ 140) and Exhibit 1007 (US Patent 6,748,545 B1 ("Helms")).

Patent Owner specifically addresses Petitioner's evidence for claims 13 and 18 for the first time in its Sur-reply and argues that "it is not clear what the relevance of EX1007 [(Helms)] is." PO Sur-reply 24. We disagree.

Dr. Kiaei explains, relying on Helms, that "it was well known in the art that a microprocessor would send control signals to an adaptive power supply coupled to that microprocessor as soon as the microprocessor was powered up to a level where its control signal was valid." Ex. 1002 ¶ 140 (citing Ex. 1007, 3:57–64, 4:28–40, 4:50–58, Fig. 3). Helms explains that "[p]ersons of skill in the art are familiar with the power-good signal," which "is asserted and maintained" after "power is initially applied to a computer system" and when "the voltage rails in the system are stable." Ex. 1007, 4:50–55.

As noted above, Chagny discloses that "activity input 202 may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis." Ex. 1004, 4:43–45. Dr. Kiaei testifies that a person of ordinary skill in the art "would have found it obvious that the startup of Chagny's processor 292 (during the startup of information handling system device 290 as a whole) would be among the 'event basis' or 'on-demand basis' upon which Chagny updates and provides the activity input 202 signal (i.e., provides said signal)." Ex. 1002 ¶ 140. Indeed, Chagny's disclosure that activity input 202 may be updated as frequently as "once every millisecond" suggests essentially continuous updating during

operation, which would begin at startup, consistent with Dr. Kiaei's testimony that activity input 202 would be provided "throughout the operating time of Chagny's information handling system device 290, including upon startup." Ex. 1002 ¶ 140.

This is not a situation in which Petitioner has merely made an unsubstantiated assertion of obviousness. *See DSS Tech.*, 885 F.3d at 1377 (relying on "ordinary creativity" "as a wholesale substitute for reasoned analysis and evidentiary support"). Rather, Petitioner provides articulated reasoning with ample supporting evidence to show that, in the context of Chagny, it would have been obvious to provide activity input 202 upon startup of the processor.

Patent Owner also argues that Petitioner incorrectly interprets "upon startup" to mean "thereafter." PO Sur-reply 25 (citing Pet. Reply 27). This argument appears to be directed to the grounds based on Hwang based on Patent Owner's citation of page 27 of the Reply, which addresses Hwang. To the extent this argument is directed to Petitioner's contentions with respect to Chagny, we disagree. Claim 11, from which claim 13 depends, recites that the power system controller is "configured to enable operation of components of a processor system to establish a state of power drain thereof, said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain." Thus, the base claim recites that the components establish a state of power drain, which must take place before there is "a signal to identify operation of said processor system in said state of power drain." The '514 patent confirms this order of operations, explaining as follows:

Upon power-up of such a system, or during its continued operation, a power system controller can enable operation of its

principal components to establish a state of maximum power drain (e.g., substantially a maximum level of power drain that must be supported by the power system). The power system controller can be configured to provide a signal to the power system to identify operation of the system in such a state of a maximum power drain.

Ex. 1001, 13:39–46. Thus, the claims and the specification of the ’514 patent both demonstrate that “upon startup of said processor system” in claims 13 and 18 includes the time period after the components have been enabled to establish a state of power drain.

Based on Petitioner’s contentions and evidence, we conclude that the subject matter of claims 1–20 would have been obvious based on the teachings of Chagny.

F. Remaining Grounds

As noted above in § I.A, Petitioner presents additional challenges to the claims in this proceeding based on Hwang, alone and in combination with Chagny. Because we determine that all challenged claims are unpatentable as discussed above, we need not separately assess the patentability of these claims based on the remaining grounds in this proceeding. 35 U.S.C. § 318(a) (“If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d).”); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (nonprecedential) (“We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.”).

III. CONCLUSION⁹

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that claims 1–20 of the ’514 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–12, 14–17, 19, 20	102(a), (b)	Chagny	1–12, 14–17, 19, 20	
1–20	103(a)	Chagny	1–20	
1–10, 16, 17, 19, 20	102(a), (b)	Hwang ¹⁰		
11, 12, 14–17, 19, 20	103(a)	Hwang, Chagny		
18	103(a)	Hwang		
13, 18	103(a)	Hwang, Chagny		
Overall Outcome			1–20	

⁹ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

¹⁰ As explained above, because we determine that the challenged claims are unpatentable on other grounds, we decline to address the remaining grounds based on Hwang alone or on Hwang in combination with Chagny.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–20 of the '514 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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