

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SENSOR ELECTRONIC TECHNOLOGY, INC.,
Petitioner,

v.

LITE-ON TECHNOLOGY CORPORATION,
Patent Owner.

IPR2022-00396
Patent 8,829,549 B2

Before JONI Y. CHANG, LYNNE E. PETTIGREW, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

CHANG, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Sensor Electronic Technology, Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review (“IPR”) of claims 1–5, 7, 9, 18, and 20 (“the challenged claims”) of U.S. Patent No. 8,829,549 B2 (Ex. 1001, “the ’549 patent”). Paper 1 (“Pet.”), 1. Lite-On Technology Corporation (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”).

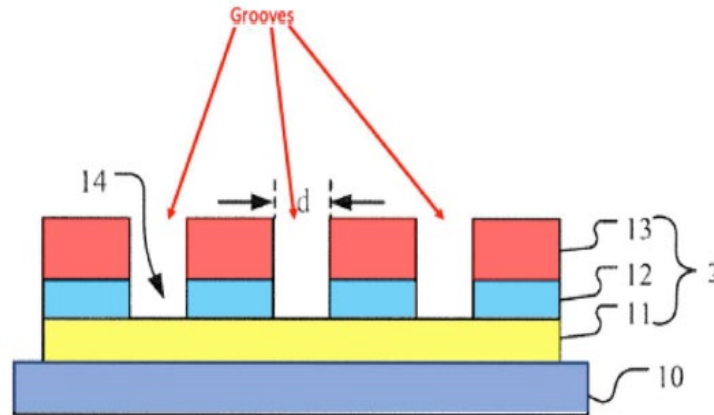
Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons stated below, we determine that Petitioner has not established a reasonable likelihood that it would prevail with respect to any of the challenged claims. We hereby decline to institute an *inter partes* review in this proceeding.

A. Related Matters

The parties indicate that the ’549 patent is involved in *Sensor Electronic Technology, Inc. v. Lite-On Technology Corporation*, Case No. 6:21-cv-00322-ADA (W.D. Tex. 2021). Pet. 89; Prelim. Resp. 4.

B. The ’549 Patent

The ’549 patent discloses a light emitting diode (“LED”) including a first doped layer, a light emitting layer, a second doped layer and a substrate. Ex. 1001, code (57). Figure 2 of the ’549 patent is reproduced below with annotations added by Patent Owner. Prelim. Resp. 19.



Annotated Figure 2 above is a cross-sectional view of a semiconductor device. Ex. 1001, 3:35–36. Semiconductor layer 2 includes first doped layer 11 (yellow), light emitting layer 12 (light blue), and second doped layer 13 (red), formed on substrate 10 (dark blue). As shown, a plurality of grooves 14 penetrate through second doped layer 13 and light emitting layer 12, exposing a partial surface of first doped layer 11.

C. Illustrative Claim

Of the challenged claims, claims 1 and 18 are independent.

Claims 2–5 and 7 depend from claim 1. Claim 20 depends from claim 18.

Claim 1 is illustrative:

1 A light emitting diode, comprising:

[1.1] a substrate;

[1.2] a first doped layer, disposed on the substrate;

[1.3] a light emitting layer, disposed on the first doped layer;

[1.4] a second doped layer, disposed on the light emitting layer;

[1.5] a plurality of first grooves, penetrating through the second doped layer and the light emitting layer, and thus a partial surface of the first doped layer is exposed;

[1.6] an insulating layer, disposed over a part of the second doped layer and extending to the sidewalls of the plurality of first grooves;

[1.7] a first contact, set in the plurality of first grooves and electrically connected to the first doped layer; and

[1.8] a second contact, set on the second doped layer and electrically connected to the second doped layer;

[1.9] *wherein from a top view of the light emitting diode, one end of at least one of the plurality of first grooves extends to the edge of the first doped layer.*

Ex. 1001, 8:59–9:46 (emphasis and bracketed matters added).

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 8)¹:

	Claims Challenged	35 U.S.C. §	References
1	1, 4, 5, 7, 18, 20	103(a)	Yasuda ²
2	2, 3	103(a)	Yasuda, Lee ³
3	1, 4, 5, 7, 9, 18, 20	103(a)	Yasuda, Lumileds ⁴

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the ’549 Patent was filed before this date, we refer to the pre-AIA version of § 103. Ex. 1001, code (22).

² U.S. Application Pub. No. 2009/0159902 A1, published on June 25, 2009 (Ex. 1003).

³ U.S. Application Pub. No. 2011/0070674 A1, published on March 24, 2011 (Ex. 1005).

⁴ M.R. Krames et al., “High-Power III-Nitride Emitters for Solid-State

	Claims Challenged	35 U.S.C. §	References
4	1, 5, 7, 18, 20	103(a)	Krames ⁵
5	4, 9	103(a)	Krames, Lumileds
6	2, 3	103(a)	Krames, Lee

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b) (2021). Under this standard, the words of a claim generally are given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Here, we find that it is necessary to construe only the claim term identified below for our determination of whether to institute a review. *See Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy,

Lighting,” phys. stat. sol. (a) 192, No. 2, 237–245 (2002) (Ex. 1004).

⁵ U.S. Application Pub. No. 2002/0171087 A1, published on November 21, 2002 (Ex. 1006).

and only to the extent necessary to resolve the controversy.” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

“extends to the edge of the first doped layer”

Element 1.9 of claim 1 recites:

wherein from a top view of the light emitting diode, *one end of at least one of the plurality of first grooves extends to the edge of the first doped layer.*

Ex. 1001, 7:47–49 (emphasis added). Patent Owner argues that the term “extends to the edge of the first doped layer” should be construed as “extends to a sidewall of the first doped layer.” Prelim. 18–20. According to Patent Owner, the figures of the ’549 patent show that an “edge” of the “first doped layer” refers to a vertical edge or sidewall of the n-type semiconductor layer of the LED device. *Id.*

Figure 1 of the ’549 patent is reproduced below.

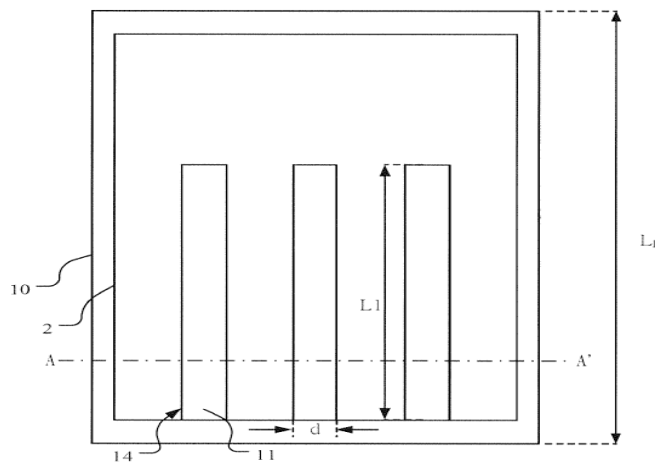


Figure 1 of the ’549 patent is a top view of the semiconductor device. Ex. 1001, 3:33–34. The Specification discloses that “[r]eferring to FIG. 1, in a preferred embodiment, one end of each first groove 14 extends to the edge of the semiconductor layer 2.” *Id.* at 4:38–40. Other embodiments of

the '549 patent also show a device having at least one groove that extends to a sidewall of semiconductor layer 2. Ex. 1001, Figs. 3–9. The Specification discloses that, by extending the first grooves to the edges of the second doped layer and the light emitting layer, “the current can spread evenly over the first doped layer through the first contact to improve the problem of current crowding and achieve the uniform distribution of current” in the LED. *Id.* at 3:4–8. Patent Owner contends that a person of ordinary skill in the art would have understood that the claim phrase “extends to the edge of the first doped layer” means “extends to a sidewall of the first doped layer.” Prelim. Resp. 20 (citing Ex. 2001 ¶ 98). In view of the claim language and the Specification, we agree with Patent Owner.

Through its prior art arguments, Petitioner argues that the term “extends to the edge of the first doped layer” does not require the grooves to extend to a sidewall of the first doped layer because that construction would be consistent with the infringement allegations made by Patent Owner in the district court proceeding. Pet. 24–28, 74.

We are not persuaded by Petitioner’s argument. As the Federal Circuit has explained, “extrinsic evidence by definition is not part of the patent and does not have the specification’s virtue of being created at the time of patent prosecution for the purpose of explaining the patent’s scope and meaning” and “extrinsic evidence . . . generated at the time of and for the purpose of litigation . . . can suffer from bias that is not present in intrinsic evidence.” *Phillips*, 415 F.3d at 1318. Petitioner implicitly acknowledges that the claim term may reasonably be construed to require a

groove that extends to the sidewall of the first doped layer by presenting obviousness contentions to cover that contingency. *See* Pet. 28, 75.

In light of the claim language and the Specification, we agree with Patent Owner’s proposed claim construction and adopt it by construing “extends to the edge of the first doped layer” as “extends to a sidewall of the first doped layer.”

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁶ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art;

⁶ Neither party presents evidence or arguments regarding objective evidence of non-obviousness in the instant proceeding.

prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation marks omitted).

Here, Petitioner asserts that a person of ordinary skill in the art of the ’549 patent would have had “a Bachelor’s Degree in electrical engineering, materials science, physics, or a similar discipline.” Pet. 6–7. And such an artisan also would have had “one to two years of experience in the field of LED with knowledge of device semiconductor design needed to form a p-n junction or diode, the materials involved with the fabrication of an LED device, as well as LED packaging design.” *Id.* (citing Ex. 1007 ¶¶ 32–33).

Patent Owner asserts that a person of ordinary skill in the art of the ’549 patent would have had “at least an undergraduate degree in electrical engineering (or similar discipline with an electrical and/or semiconductor emphasis) and two or more years of experience in LED device design, fabrication and packaging,” or alternatively, “a master’s degree with at least a year of experience in those fields, or an equivalent combination of education and experience.” Prelim. Resp. 4 (citing Ex. 2001 ¶¶ 71–72). However, Patent Owner does not point out any meaningful difference between the parties’ assessments. We note that the open-ended language “at least” in Patent Owner’s assessment may cause certain ambiguity.

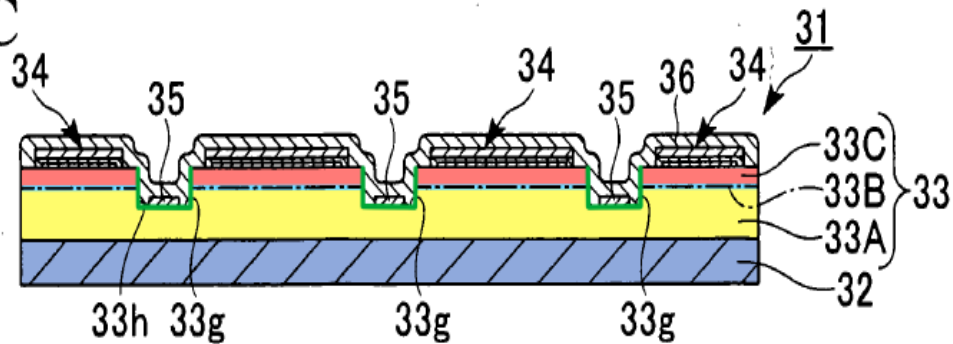
For purposes of this Decision, we adopt the level of ordinary skill as articulated by Petitioner because, based on the current record, this proposal appears to be consistent with the ’549 patent, prior art of record, and supported by the testimony of Jack Josefowicz, Ph.D.

D. Summary of the asserted prior art references

1. Yasuda (Exhibit 1003)

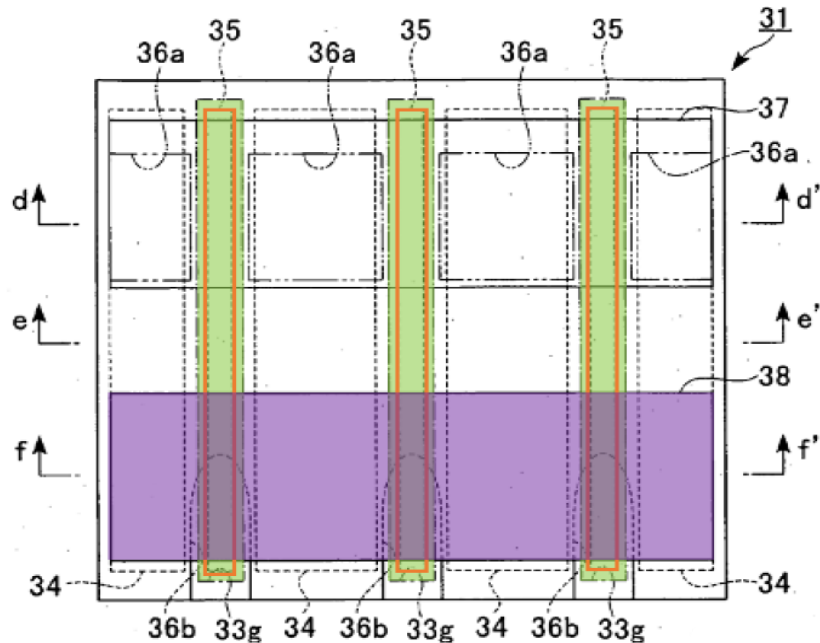
Yasuda discloses a flip-chip type semiconductor light-emitting device. Ex. 1003, Code (57). Figure 5C of Yasuda is reproduced below with annotations added by Petitioner. Pet. 15.

FIG. 5C



Annotated Figure 5C above shows a cross-sectional view of flip-chip type semiconductor light-emitting device 31. Ex. 1003 ¶ 58. Light-emitting device 31 includes substrate 32 (dark blue) and semiconductor layer 33 that includes n-type semiconductor layer 33A (yellow), light emitting layer 33B (light blue with single dashed and dotted line), and p-type semiconductor layer 33C (red). *Id.* ¶¶ 172–175. Recess 33g (green), penetrating p-type semiconductor layer 33C and light-emitting layer 33B to expose n-type semiconductor layer 33A, is provided at a plurality of sites. *Id.* ¶ 176.

Figure 5A of Yasuda is reproduced below with annotations added by Petitioner. Pet 18.

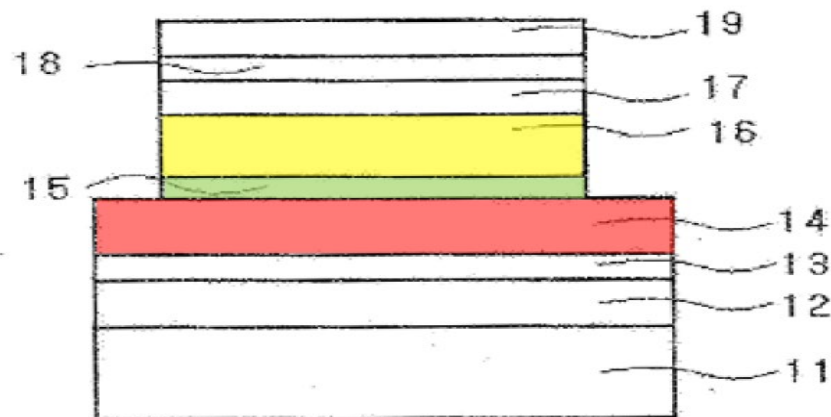


Annotated Figure 5A above shows a bottom view⁷ of light-emitting device 31. Ex. 1003 ¶ 172. As shown, negative electrodes 35 (orange) are formed in recesses 33g (green) and connected to negative electrode pad 38 (purple). *Id.* ¶¶ 179, 188.

2. Lee (Exhibit 1005)

Lee discloses a gallium nitride-based compound semiconductor device. Ex. 1005, Code (54). Figure 1 of Lee is reproduced below with annotations added by Petitioner. Pet. 44.

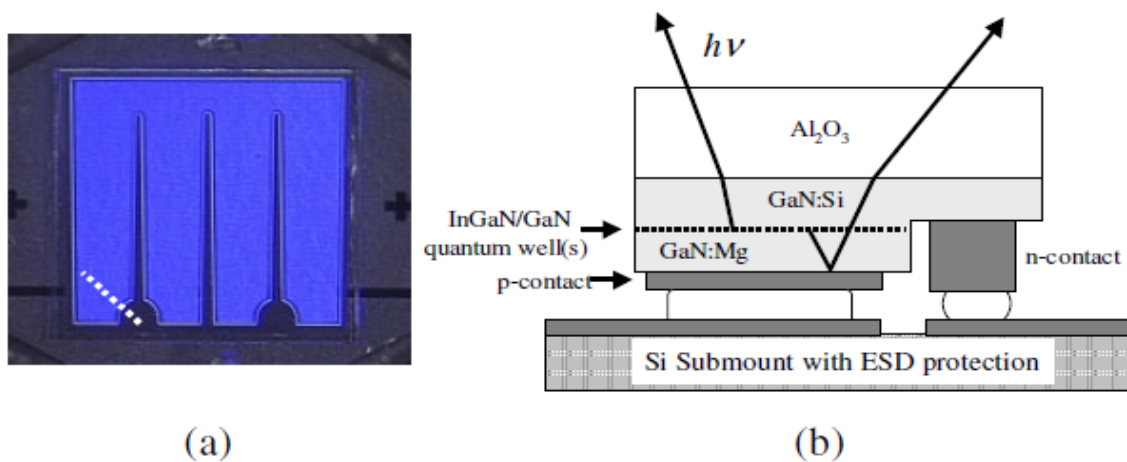
⁷ The bottom view means a top down view of Figure 5C, which shows a flip-chip before it is flipped.



Annotated Figure 1 of Lee above shows a semiconductor device. Ex. 1005 ¶ 22. As shown, the device includes n-type GaN layer 12, active layer 13, and p-type GaN layer 14 (red) formed sequentially on substrate 11. *Id.* ¶ 23. Then, a multi-layered ohmic electrode layer is formed on p-type GaN layer 14 by depositing sequentially contact metal layer 15 (green), Ag layer 16 (yellow), Ru layer 17, Ni layer 18, and Au layer 19. *Id.* ¶¶ 23–27.

3. Lumileds (Exhibit 1004)

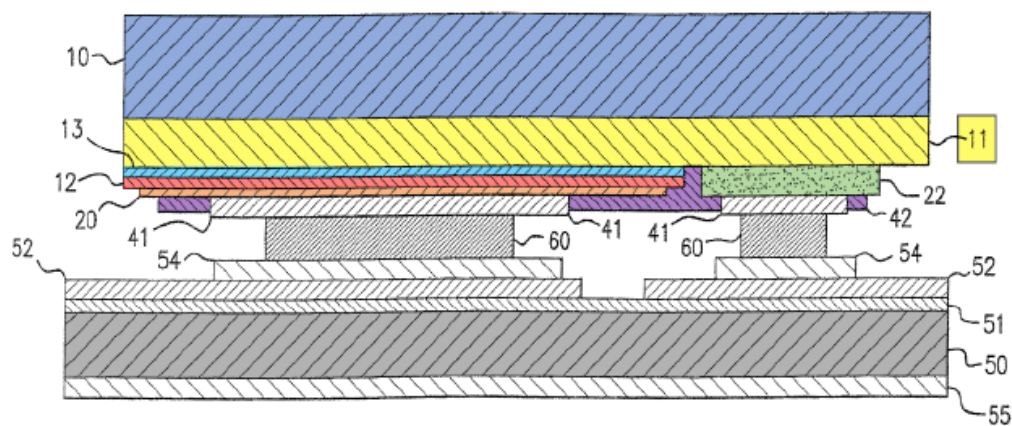
Lumileds discloses a high-power LED device. Ex. 1004, 240. Lumileds discloses “an interdigitated contact design” that “separates the large area of the chip into segmented areas, or cells, wherein uniform current spreading and low series resistance is achieved.” *Id.* Figures 2(a) and 2(b) of Lumileds are reproduced below.



Figures 2(a) and 2(b) show a high-power LED flip-chip bonded onto a Si submount. *Id.* Figure 2(a) (left) is the top view of the LED chip showing the interdigitated contact design (looking through the sapphire substrate). *Id.* Figure 2(b) is a cross-section view corresponding to the dashed line shown in Figure 2(a).

4. Krames (Exhibit 1006)

Krames discloses a large-area, high-power LED chip. Ex. 1006 ¶ 43. Figure 6(b) of Krames is reproduced below with annotations added by Petitioner. Pet. 74.



Annotated Figure 6(b) above is a sectional view of a light-emitting device in an inverted configuration. Ex. 1006 ¶¶ 44–45. The light-emitting device includes transparent superstrate 10 (dark blue), n-type semiconductor layer 11 (yellow), active region 13 (light blue), p-type semiconductor layer 12 (red), n-electrode fingers 22 (green), p-electrode metallization 20 (orange), and dielectric passivating layer 42 (purple). *Id.*

E. Obviousness over Yasuda alone or in view of Lee

Petitioner asserts that claims 1, 4, 5, 7, 18, and 20 are unpatentable under § 103(a) as obvious over Yasuda (Ground 1). Pet. 8–42. Petitioner also asserts that claims 2 and 3 are unpatentable under § 103(a) as obvious over Yasuda in view of Lee (Ground 2). *Id.* at 42–48. Patent Owner argues that Yasuda does not disclose “any grooves that extend to the edge of the first doped layer,” as required by the claims. Prelim. Resp. 21–33. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that claims 1, 4, 5, 7, 18, and 20 would have been obvious over Yasuda alone or that claims 2 and 3 would have been obvious over Yasuda in view of Lee.

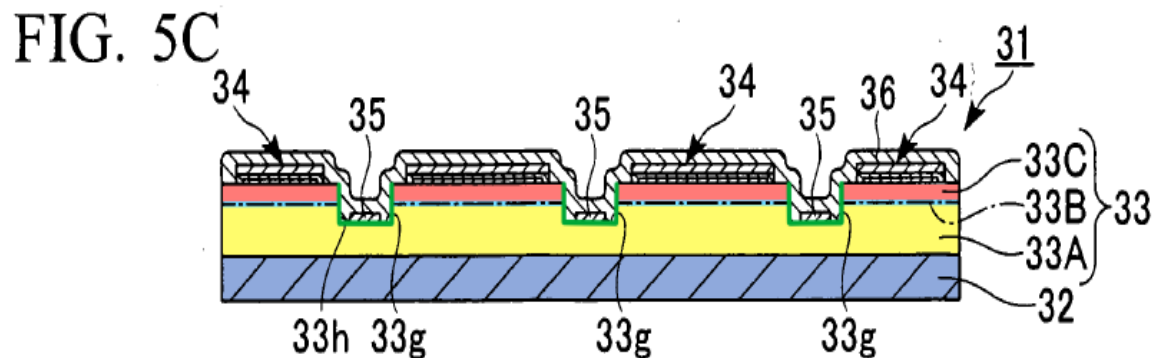
Element 1.9 of claim 1 recites:

wherein from a top view of the light emitting diode, one end of at least one of the plurality of first grooves extends to the edge of the first doped layer.

Ex. 1001, 7:47–49 (emphasis added). Element 18.11 of claim 18 recites the same limitation. *Id.* at 8:56–58. By virtue of their dependency, claims 2–5, 7 and 20 each require this limitation. As discussed above in Section II.A, we adopt Patent Owner’s proposed claim construction, construing “extends to

the edge of the first doped layer” as “extends to a sidewall of the first doped layer.”

Petitioner asserts that Yasuda discloses the claimed “light emitting diode.” Pet. 10–31. Figure 5C of Yasuda is reproduced below with annotations added by Petitioner. *Id.* at 15.



Annotated Figure 5C above shows a cross-sectional view of semiconductor light-emitting device 31. Ex. 1003 ¶ 58. Petitioner asserts that Yasuda’s device 31 includes substrate 32 (dark blue) and semiconductor layer 33 that includes n-type semiconductor layer 33A (yellow) (“first doped layer”), light emitting layer 33B (single dashed and dotted line) (“light emitting layer”), and p-type semiconductor layer 33C (red) (“second doped layer”).

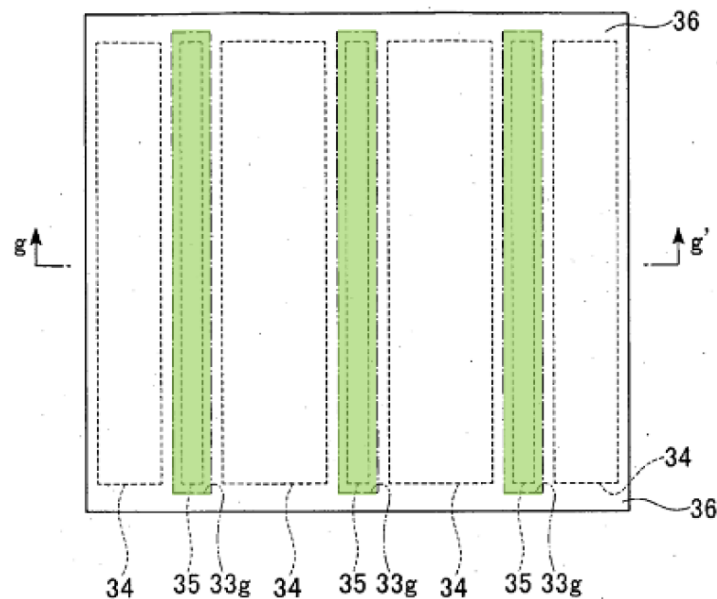
Pet. 10–31. Positive electrode 34 is formed on p-type semiconductor layer 33C, and insulator film 36 is formed to cover semiconductor layer 33, positive electrode 34, and negative electrode 35. *Id.*

For Elements 1.9 and 18.11, Petitioner advances several theories, relying only on Yasuda. *Id.* at 23–31.⁸ First, Petitioner argues that Yasuda discloses the limitation recited in these elements because, as shown in Figure 6A, “the grooves extend to the end of the chip on either end.” *Id.* at 23 (citing Ex. 1007 ¶ 83). Petitioner also argues that a relevant artisan would have understood that “the grooves of Yasuda extend to the edge of the first doped layer or n-type semiconductor layer because Figure 5A does not show any n-type semiconductor layer extending beyond the border of the grooves 33g,” citing to Dr. Josefowicz’s testimony for support. *Id.* at 24 (citing Ex. 1007 ¶ 84).

Petitioner’s arguments and Dr. Josefowicz’s testimony are conclusory and not supported by Yasuda. Petitioner does not show persuasively that either Figure 5A or Figure 6A of Yasuda discloses a groove extending to the end of the chip or to the edge of the first doped layer, as alleged by Petitioner. Figure 6A of Yasuda is reproduced below with annotations added by Petitioner. *Id.*⁹

⁸ Petitioner relies on the same arguments and evidence for Element 18.11 as it presents for Element 1.9. Pet. 39. Here and below, our citations for both elements are to the section of the Petition that addresses Element 1.9.

⁹ Petitioner and Dr. Josefowicz incorrectly cite Yasuda’s Figure 5A instead of Figure 6A as support for the annotated figure below. Pet. 24; Ex. 1007 ¶ 83.



Annotated Figure 6A above shows a bottom view of a light-emitting device. Ex. 1003 ¶ 59. Petitioner highlights recesses 33g in green. Pet. 23. Petitioner does not show persuasively that, in Yasuda’s Figure 6A, “the grooves extend to the end of the chip on either end.” *Id.* Petitioner does not direct us to support in Yasuda’s text for that assertion. In our view, Figure 6A is more accurately characterized by Patent Owner’s declarant, Dr. Michael Lebby, who testifies that “recesses 33g shown in green in the annotated Figure 6A do not extend to the edge of the chip rather just short of it.” Ex. 2001 ¶ 109. Similarly, Petitioner fails to show persuasively that recesses 33g shown in green in Petitioner’s annotated Figure 5A (reproduced in Section II.D.1) extend to the edge of the chip. Ex. 1003, Fig. 5A.

Moreover, Petitioner fails to show that Figure 5A of Yasuda shows the edge of the first doped layer, as recited in the claim. We agree with Dr. Lebby’s testimony that “Figure 5A provides no information one way or the other regarding the extent of the semiconductor layer or where the

purported ‘edge’ is located.” Ex. 2001 ¶¶ 111–113. In short, Yasuda does not support Petitioner’s argument that recesses 33g in Figures 5A and 6A extend to the edge of the n-type semiconductor layer.

Second, Petitioner argues that “[e]ven if the grooves of Yasuda do not fully extend to the sidewall of the n-type semiconductor layer, *the grooves extend far enough to reach the edge.*” Pet. 24 (emphasis added). According to Petitioner, “[t]he disclosure of Yasuda is consistent with the infringement allegations made by Patent Owner which show grooves that do not extend to the sidewall of the n-type semiconductor layer.” *Id.* at 24–28.

Petitioner’s arguments are unpersuasive. As discussed in our claim construction analysis in Section II.A above, we reject Petitioner’s argument that the term “extends to the edge of the first doped layer” does not require the grooves to extend to a sidewall of the first doped layer. Rather, in light of the claim language and the Specification, we agree with Patent Owner’s proposed claim construction and adopt it by construing “extends to the edge of the first doped layer” as “extends to a sidewall of the first doped layer.” In addition, Petitioner’s argument that Yasuda’s “grooves extend far enough to the edge” is inconsistent with the express claim language that requires extending a groove to the edge of the first doped layer. In short, Petitioner fails to show that at least one of Yasuda’s recesses “extends to the edge of the first doped layer,” as required by the claims.

Finally, Petitioner argues that, to the extent that Elements 1.9 and 18.11 require a groove to extend to a sidewall of the first doped layer, “such a modification would be obvious to one of ordinary skill in the art.” Pet. 28 (citing Ex. 1007 ¶¶ 89–96). Petitioner contends that Yasuda’s Figures 1A

and 11A show “a groove that extends to the sidewall of the n-type semiconductor layer with a recess 103g exposing the semiconductor layer 103b.” *Id.* at 28–29 (citing Ex. 1003 ¶¶ 5, 7, 9, 110, 116). According to Petitioner, “Yasuda also teaches that the design of Figures 1A and 11A mak[es] it possible for electric current to flow effectively despite a small forming region of the negative electrode 105.” *Id.* (citing Ex. 1003 ¶ 9). Petitioner argues that a relevant artisan would “have been motivated to apply Figure 1A’s teaching of a recess extending to the sidewall of the n-type semiconductor layer to Figure 5A’s embodiment of Yasuda” because extending a recess to the border of the n-type layer would improve current flow and “increase the performance of the LED chip by increasing the contact area between electrode and the n-type semiconductor layer.” *Id.* 30–31 (citing Ex. 1007 ¶¶ 89–96).

Petitioner’s arguments and Dr. Josefowicz’s testimony are not sufficiently supported by Yasuda or other objective evidence. Petitioner’s analysis rests on impermissible hindsight. An obviousness analysis must provide a sufficient and specific reasoning to guard against the impermissible use of hindsight, even for a structurally simple claimed invention, as here. *See KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[O]bviousness grounds cannot be sustained by mere conclusory statement; instead, there must be some articulated reasoning with some underpinning to support the legal conclusion of obviousness.”); *see also id.* at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.”)).

Notably, Petitioner fails to show that Yasuda discloses extending a groove to a sidewall of the first doped layer. Figures 1A and 11A of Yasuda are reproduced below with annotations added by Dr. Lebby, highlighting the notched portion (recess) in each figure in green. Ex. 2001 ¶ 116.

FIG. 11A

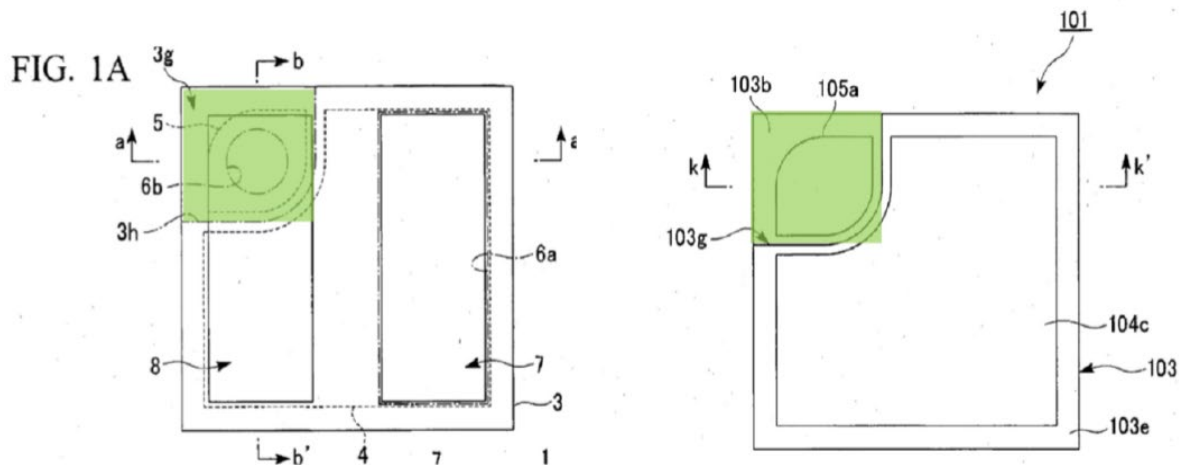


Figure 1A (left) shows the bottom view of a flip-chip type light-emitting device, Yasuda's first embodiment. Ex. 1003 ¶ 54. Figure 11A (right) is the bottom view of a conventional flip-chip type light-emitting device. *Id.* ¶ 64. Yasuda discloses that “[a]s shown in FIG. 1A, the notched portion 3g is provided in the vicinity of one corner among four corners of the semiconductor layer 3 which is approximately rectangular when viewed from above.” Ex. 1003 ¶ 110. Petitioner fails to show that Yasuda's Figures 1A and 11A disclose a groove. We agree with Dr. Lebby's testimony that the notched portion in Figure 1A is “a cut out from a corner of the LED and does not represent a groove.” Ex. 2001 ¶ 121; *compare* notched portion 3g of Yasuda Figures 1A and 11A, *with* grooves 14 in Figures 1, 3–9 of the '549 patent and grooves 33g in Figure 5A or 6A of Yasuda. In short, Petitioner fails to show that the notched portion in each of

Figures 1A and 11A discloses a groove, much less a groove that extends to the edge of the first doped layer, as required by the claims.

Petitioner also fails to show support for its contention that Yasuda discloses extending a groove to a sidewall of the n-type layer would improve current flow or “increase the performance of the LED chip by increasing the contact area between electrode and the n-type semiconductor layer.”

Pet. 30–31 (citing Ex. 1003 ¶ 9; Ex. 1007 ¶¶ 93–96). Petitioner’s reliance on paragraph 9 of Yasuda (reproduced below) is misplaced.

On the other hand, as shown in FIG 11A, the electrode area of the negative electrode 105 is approximately one tenth that of the positive electrode 104. This is because the negative electrode 105 is bonded to an n-type semiconductor layer (n-GaN layer 103b) which has relatively high electric conductivity, thereby making it possible for electric current to flow effectively despite a small forming region of the negative electrode 105.

Ex. 1003 ¶ 9. Nothing in this paragraph suggests extending a groove to the edge of the n-type semiconductor layer. We agree with Dr. Lebby, who testifies that “what paragraph 9 of Yasuda refers to is that the n-type semiconductor layer 103b has a higher electrical conductivity than the p-type semiconductor layer, and as a result, the negative electrode 105 shown in Figure [11A] electrically connected to the n-type semiconductor layer (e.g., 103b shown in Figure 11A) is made much smaller than the positive electrode 104 but still maintains effective current flow in the overall device.” Ex. 2001 ¶ 118. Dr. Lebby also testifies that a relevant artisan would have understood that “this passage is teaching balancing the sizes of the positive and negative electrodes so that their electrical conductivity matches in order to maintain a consistent current flow through the device

from the negative electrode to the positive electrode to compensate for their differences in electrical conductivity.” *Id.* We credit Dr. Lebby’s testimony because it is consistent with Yasuda’s disclosure. Ex. 1007 ¶ 9. Therefore, Yasuda does not support Petitioner’s arguments or Dr. Josefowicz’s testimony that extending a groove to a sidewall of the n-type layer would improve current flow or “increase the performance of the LED chip by increasing the contact area between electrode and the n-type semiconductor layer.” Pet. 28–31 (citing Ex. 1003 ¶ 9; Ex. 1007 ¶¶ 93–96). Thus, we are not persuaded by Petitioner’s argument that a person of ordinary skill in the art would have been motivated to modify Figure 5A’s embodiment of Yasuda by providing grooves that extend to the sidewall of the n-type semiconductor layer.

For the foregoing reasons, we find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 1, 4, 5, 7, 18, and 20 would have been obvious over Yasuda. For Ground 2, Petitioner relies on Lee to teach the limitations expressly recited in claims 2 and 3. Pet. 42–48. Lee is not cited by Petitioner for curing the deficiency in connection with Element 1.9. *Id.* Accordingly, we also find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 2 and 3 would have been obvious over Yasuda and Lee.

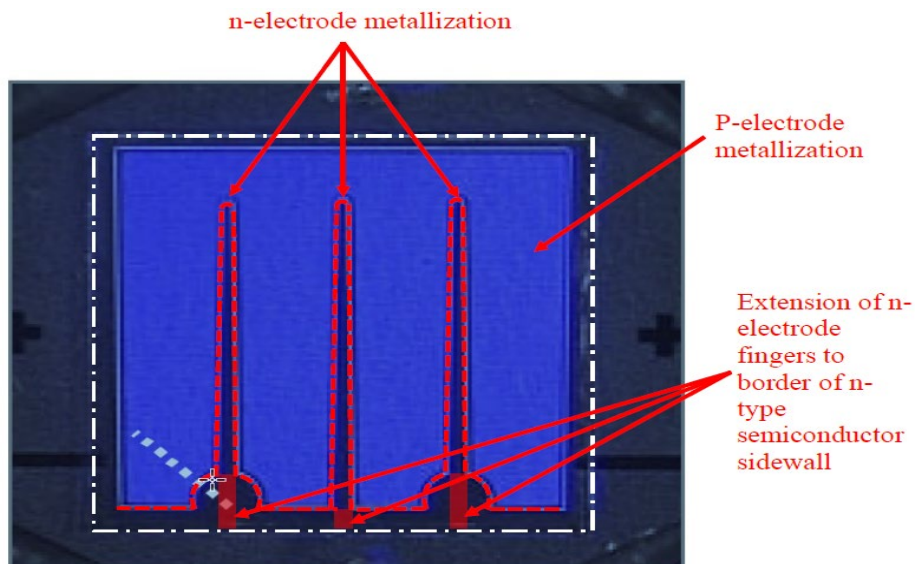
F. Obviousness over Yasuda in view of Lumileds

Petitioner asserts that claims 1, 4, 5, 7, 9, 18, and 20 are unpatentable under § 103(a) as obvious over Yasuda in view of Lumileds (Ground 3).

Pet. 42–60. Patent Owner argues that Yasuda in view of Lumileds does not disclose “any grooves that extend to the edge of the first doped layer.”

Prelim. Resp. 49–60. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that claims 1, 4, 5, 7, 9, 18, and 20 would have been obvious over Yasuda in view of Lumileds.

As discussed above in Section II.E, we find that Petitioner has not shown that Yasuda alone teaches or suggests Elements 1.9 and 18.11. Petitioner further argues that these elements would have been obvious over Yasuda in view of Lumileds. Pet. 52–57, 60. Petitioner contends that “the grooves in Lumileds extend to and come in contact with the sidewall of the n-type semiconductor layer as they extend into the area labeled ‘Extension of n-electrode fingers to border of n-type semiconductor sidewall’” shown in Figure 2(a) of Lumileds annotated by Petitioner. *Id.* at 54–56 (citing Ex. 1004, 240, Fig. 2; Ex. 1007 ¶¶ 146–152). Petitioner’s annotated Figure 2(a) of Lumileds is reproduced below. *Id.* at 54.



Petitioner's annotated Figure 2(a) of Lumileds above shows the top view of a high-power LED flip-chip. *Id.*; Ex. 1004, 240. According to Petitioner, its annotated Figure 2(a) shows that "the interdigitated contact design" with "a p-electrode metallization layer in blue that has been surrounded by and interspersed with n-electrode metallization layer in black and enclosed in red." Pet. 53. Petitioner asserts that "[a]ll of the darker areas shown in the plan view, including those extending beyond the p-type metallization[,] would be understood to correspond to the n-type semiconductor layer made accessible by etching through the p-type semiconductor layer and active layer to the n-type semiconductor material," citing to Dr. Josefowicz's testimony for support. *Id.* at 55–56 (citing Ex. 1007 ¶¶ 149–150).

Petitioner's arguments and Dr. Josefowicz's testimony, including Petitioner's annotations to Figure 2(a), lack sufficient objective evidentiary support. Figure 2(a) of Lumileds is reproduced below without Petitioner's annotations.

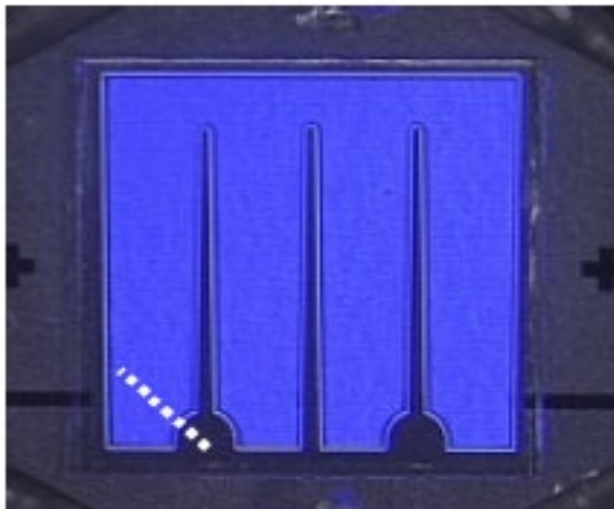


Figure 2(a) of Lumileds above shows a top view of the LED chip with a p-contact metallization shown in blue. Ex. 1004, 240, Fig. 2(a). The black areas include all other layers that are not the p-contact metallization—namely, the p-type semiconductor layer, active layer, n-type semiconductor layer, and n-contact metallization. *Id.* Notably, the actual Figure 2(a) of Lumileds does not show the semiconductor layers or the red areas that Petitioner labels “[e]xtension of n-electrode fingers to border of n-type semiconductor sidewall.” *Compare id. with* Pet. 54.

Moreover, Figure 2(b) (reproduced above in Section II.D.3) shows that p-contact metallization does not cover portions of the p-type semiconductor layer and active layer. Ex. 1004, 240, Figs. 2(a)–(b). Therefore, Petitioner fails to show that the darker areas shown in Figure 2(a) “correspond to the n-type semiconductor layer made accessible by etching through the p-type semiconductor layer and active layer to the n-type semiconductor material.” Pet. 55–56.

Lumileds is silent as to the extent of the n-type semiconductor layer. Ex. 1004, 240, Figs. 2(a)–(b). We agree with Dr. Lebby that “[t]he p-contact metal does not disclose any information regarding the arrangement or extent of the underlying semiconductor layers,” and that “Figure 2(a) therefore does not provide any information one way or the other as to the extent or arrangement of the underlying n-type semiconductor layer or where the purported ‘edge’ of such layer is located in Figure 2(a).” Ex. 2001 ¶ 133. We credit Dr. Lebby’s testimony because it is consistent with Lumileds. Ex. 1004, 240, Figs. 2(a)–(b).

In addition, Petitioner's reliance on the following language in Lumileds is misplaced:

The large area of the chip puts stringent requirements on the current spreading in the GaN:Si layers beneath the active region. It is impossible to spread current uniformly over the full distance of the chip through a GaN:Si layer of only a few microns in thickness. Therefore, an interdigitated contact design is employed. This design separates the large area of the chip into segments areas, or cells, wherein uniform current spreading and low series resistance is achieved.

Ex. 1004, 240. Lumileds is silent as to whether the grooves come in contact with a sidewall of the n-type semiconductor layer. *Id.* This disclosure in Lumileds is directed to the benefits related to the contact design that separates the large area of the chip into segments areas, not extending a groove to a sidewall of the n-type semiconductor layer. *Id.*

Accordingly, we find insufficient evidentiary support for Petitioner's argument and Dr. Josefowicz's testimony that "the grooves in Lumileds extend to and come in contact with the sidewall of the n-type semiconductor layer as they extend into the area labeled '[e]xtension of n-electrode fingers to border of n-type semiconductor sidewall.'" On this record, Petitioner's argument and the corresponding testimony appear to be based on mere speculation or conjecture. Pet. 56; Ex. 1007 ¶ 150. "The legal conclusion of obviousness must be supported by facts" and we may not "resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies." *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). As the Federal Circuit has explained, "legal determination of obviousness . . . should be based on evidence rather than on mere speculation or conjecture." *Alza Corp. v. Maylan Labs., Inc.*, 464 F.3d 1286, 1290 (Fed. Cir. 2006); see

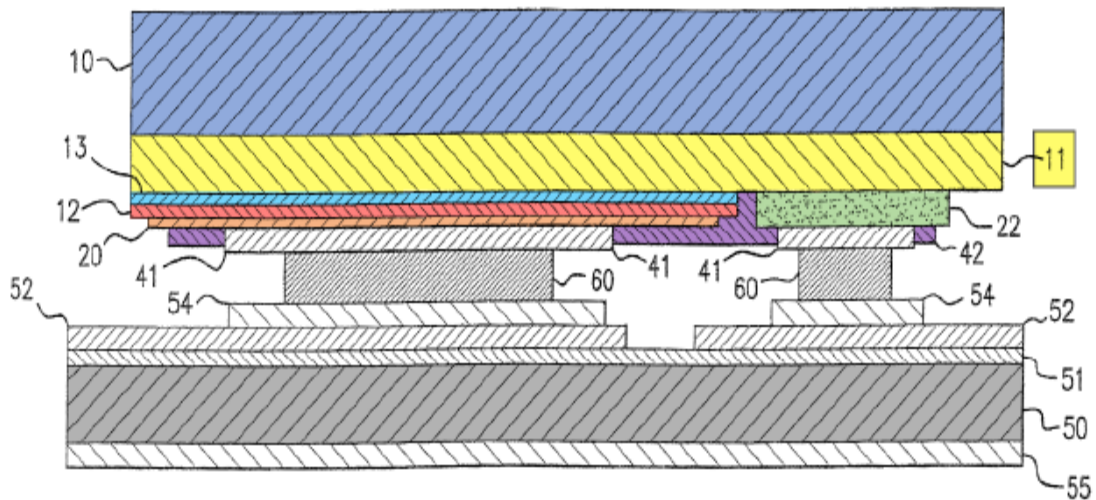
also Star Sci., Inc. v. R.J. Reynolds Tobacco Co., 655 F.3d 1364, 1375–76 (Fed. Cir. 2011) (noting that prior art’s “speculative and tentative disclosure of what ‘might’ or ‘may’ [explain the cause of the desired effect] does not sufficiently direct or instruct one of skill in the art”).

For the foregoing reasons, we find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 1, 4, 5, 7, 9, 18, and 20 would have been obvious over Yasuda and Lumileds.

G. Obviousness over Krames alone or in view of other references

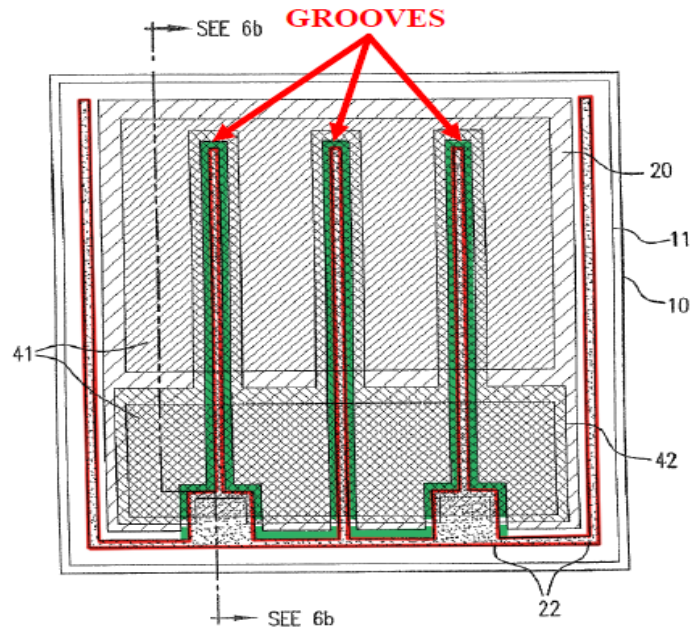
Petitioner asserts that claims 1, 5, 7, 18, and 20 are unpatentable under § 103(a) as obvious over Krames (Ground 4). Pet. 61–85. Petitioner also asserts that claims 4 and 9 are unpatentable under § 103(a) as obvious over Krames in view of Lumileds (Ground 5), and that claims 2 and 3 are unpatentable under § 103(a) as obvious over Krames in view of Lee (Ground 6). *Id.* at 85–95. Patent Owner argues that Krames does not disclose any grooves that extend to the edge of the first doped layer. Prelim. Resp. 36–38. For the reasons provided below, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing in showing that claims 1–5, 7, 9, 18, and 20 are unpatentable.

Petitioner asserts that Krames discloses Elements 1.9 and 18.11. Pet. 74–76, 84. Figure 6(b) of Krames is reproduced below with annotations added by Petitioner. *Id.* at 74.



Annotated Figure 6(b) above is a sectional view of a large-area, high-power LED in an inverted configuration. Ex. 1006 ¶¶ 43–44. Petitioner asserts that the light-emitting device includes transparent superstrate 10 (dark blue) (“substrate”), n-type semiconductor layer 11 (yellow) (“first doped layer”), active region 13 (light blue) (“light emitting layer”), p-type semiconductor layer 12 (red) (“second doped layer”), n-electrode fingers 22 (green) (“first contact”), p-electrode metallization 20 (orange) (“second contact”), and dielectric passivating layer 42 (purple) (“insulating layer”). Pet. 64–76.

Figure 6(a) of Krames is reproduced below with annotations added by Petitioner. *Id.* at 75.



Annotated Figure 6(a) above shows the plan view of the LED chip.

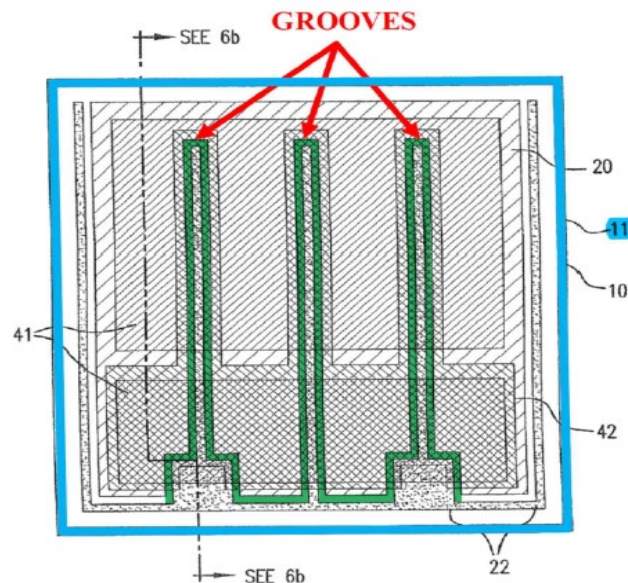
Ex. 1006 ¶¶ 44–45. As shown, n-electrode 22 (red) is formed within the grooves (green). According to Petitioner, Krames discloses that the large area of the device ($>400 \times 400 \mu\text{m}^2$) requires n-electrode 22 “fingers” interposing the p-electrode metallization 20 “to spread current uniformly throughout the device.” Pet. 67 (citing Ex. 1006 ¶ 44). Petitioner asserts that the locations of the three central fingers in n-electrode 22 fingers corresponds to the location of the grooves. *Id.* at 68 (citing Ex. 1007 ¶¶ 172–174).

Petitioner advances two theories. *Id.* at 74–76, 84. First, Petitioner argues that Krames discloses Elements 1.9 and 18.11 because “[t]he grooves extend to the edge of the n-type semiconductor layer 11, which corresponds to the locations of the n-electrode fingers marked in red in Figure 6(a).” *Id.*

at 74 (citing Ex. 1007 ¶ 186). According to Petitioner, “[a]s described for ground 1, this interpretation is consistent with Patent Owner’s infringement contentions.” *Id.* Petitioner avers that a relevant artisan would have understood that “the n-electrode fingers would be coextensive with the boundaries of the n-semiconductor layer and the green grooves extend to the boundaries of the n-electrode fingers 22.” *Id.* at 75 (citing Ex. 1007 ¶ 186).

As discussed in our claim construction analysis in Section II.A and our analysis for Ground 1 in Section II.E above, we reject Petitioner’s argument that the term “extends to the edge of the first doped layer” does not require the grooves to extend to a sidewall or an edge of the first doped layer. Rather, in light of the claim language and the Specification, we agree with Patent Owner’s proposed claim construction and adopt it by construing “extends to the edge of the first doped layer” as “extends to a sidewall of the first doped layer.”

Furthermore, Petitioner’s arguments and Dr. Josefowicz’s testimony are conclusory and not supported by Krames. Figure 6(a) of Krames is reproduced below with annotations added by Dr. Lebby. Ex. 2001 ¶ 136.



Annotated Figure 6(a) above shows the plan view of the LED chip.

Ex. 1006 ¶¶ 44–45. Figure 6(a) does not support Petitioner’s contentions because the end of the grooves (green) do not reach the edge of n-type semiconductor layer 11 (blue). In short, Petitioner fails to show that Krames discloses grooves extending to the edge of the first doped semiconductor layer, as required by Elements 1.9 and 18.11.

Second, Petitioner argues that, to the extent that these elements require that the grooves touch the sidewalls of the n-type semiconductor layer, such a modification would have been obvious in view of the knowledge of a person of ordinary skill in the art. Pet. 75. Citing to Dr. Josefowicz’s testimony for support, Petitioner argues that a relevant artisan would have understood that “extending the grooves of Krames to the sidewalls of the n-type semiconductor layer would have increased the performance of the LED chip by increasing the contact area between the n-type semiconductor layer and n-electrode,” and “[t]hat would beneficially have resulted in reducing the amount of wasted n-type semiconductor layer

that is not in contact with a n-electrode.” *Id.* at 75–76 (citing Ex. 1007 ¶ 187).

Again, Petitioner’s arguments are nothing more than impermissible hindsight, using the claimed subject matter in the ’549 patent as a roadmap. *See Mintz v. Dietz & Watson, Inc.*, 679 F.3d 1372, 1379 (Fed. Cir. 2012) (“Indeed, where the invention is less technologically complex, the need for *Graham* findings can be important to ward against falling into the forbidden use of hindsight.”).

As discussed above, the ends of the grooves (green) in annotated Figure 6(a) of Krames do not reach the edge of n-type layer 11 (blue), as Petitioner alleges. Krames is silent as to extending a groove to the edge of the first doped layer. Moreover, Petitioner’s reliance on paragraph 44 of Krames is misplaced. Per. 67 (citing Ex. 1006 ¶ 44). This paragraph in Krames is directed to the benefits related to interposing n-electrode fingers with p-electrode metallization. Ex. 1006 ¶ 44. Petitioner does not direct us to evidence in Krames or elsewhere sufficient to support its contention that it would have been obvious to extend a groove to the edge of the first doped layer, as required by Elements 1.9 and 18.11. Hence, Petitioner’s arguments and Dr. Josefowicz’s testimony are conclusory and not supported by Krames.

As discussed above in our analysis for Ground 3 in Section II.F, Petitioner also fails to show that Lumileds discloses grooves extending to the edge of the n-type layer or the benefit of such a feature. The actual Figure 2(a) of Lumileds does not show the semiconductor layers or the red areas labeled “[e]xtension of n-electrode fingers to border of n-type semiconductor

sidewall” added by Petitioner in its annotated figure. Ex. 1004, 240, Figs. 2(a)–(b). Lumileds is silent as to the extent of the n-type semiconductor layer. *Id.* Petitioner’s reliance on the benefits disclosed in Lumileds is misplaced because those benefits are related to the contact design that separates the large area of the chip into segments areas, not extending a groove to a sidewall of the n-type semiconductor layer. *Id.*

For the foregoing reasons, we find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 1, 5, 7, 18, and 20 would have been obvious over Krames. For Ground 5, Petitioner relies on Lumileds to teach the limitations expressly recited in claims 4 and 9. Pet. 85–89. Lumileds is not cited by Petitioner for curing the deficiency in connection with Elements 1.9 and 18.11. *Id.* Accordingly, we also find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 4 and 9 would have been obvious over Krames and Lumileds. For Ground 6, Petitioner relies on Lee to teach the limitations expressly recited in claims 2 and 3. Pet. 90–95. Lee is not cited by Petitioner for curing the deficiency in connection with Elements 1.9 and 18.11. *Id.* Accordingly, we also find that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 2 and 3 would have been obvious over Krames and Lee.

III.CONCLUSION

For the foregoing reasons, the information presented in the Petition and evidence of record do not establish that there is a reasonable likelihood that Petitioner would prevail in challenging claims 1–5, 7, 9, 18, and 20 of the ’549 patent.

IV. ORDER

For the foregoing reasons, it is
ORDERED that the Petition is *denied*, and no trial is instituted.

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