

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TCT MOBILE (US) INC., TCL CHINA STAR OPTOELECTRONICS
TECHNOLOGY CO., LTD., TCL TECHNOLOGY GROUP
CORPORATION, TTE TECHNOLOGY, INC., TCL COMMUNICATION
TECHNOLOGY HOLDINGS LIMITED, and TCT MOBILE, INC.
Petitioner,

v.

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.,
Patent Owner.

IPR2022-00441
Patent 10,777,290 B2

Before DAVID C. McKONE, JENNIFER MEYER CHAGNON, and
NATHAN A. ENGELS, *Administrative Patent Judges*.

CHAGNON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

TCT Mobile (US) Inc., TCL China Star OptoElectronics Technology Co., Ltd., TCL Technology Group Corporation, TTE Technology, Inc., TCL Communication Technology Holdings Limited, and TCT Mobile, Inc. (collectively, “Petitioner”)¹ filed a Petition requesting *inter partes* review of claims 1–3 (“the challenged claims”) of U.S. Patent No. 10,777,290 B2 (Ex. 1001, “the ’290 patent”). Paper 1 (“Pet.”). Semiconductor Energy Laboratory Co., Ltd. (“Patent Owner”)² filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314, which provides that an *inter partes* review may be instituted only upon a showing that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Applying this standard, and upon consideration of the information presented in the Petition and the Preliminary Response, as well as the evidence of record, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one of the challenged claims. Accordingly, we do not institute an *inter partes* review of the ’290 patent.

A. *Related Proceedings*

The parties identify *Semiconductor Energy Laboratory Co. v. TCL China Star OptoElectronics Technology Co.*, 8:21-cv-00554 (C.D. Cal.)

¹ The petitioning parties identify themselves as the real parties-in-interest. Pet. 2.

² Patent Owner identifies itself as the real party-in-interest. Paper 10, 1.

(“the related district court proceeding”) as a related matter involving the ’290 patent. Pet. 2–3; Paper 10, 1.

B. The ’290 Patent

The ’290 patent, titled “Semiconductor Device,” was filed on April 26, 2019, and issued on September 15, 2020.³ Ex. 1001, codes (22), (45), (54). The ’290 patent observes that a prior shift register design uses either n-channel transistors for outputting high-level signals sequentially, or p-channel transistors for outputting low-level signals sequentially. *Id.* at 1:21–33. To address the shortcomings of this prior design, the ’290 patent provides a circuit in which n-channel transistors can output low-level signals sequentially, and a circuit in which p-channel transistors can output high-level signals sequentially. *Id.* at 1:44–53, 2:19–24. Additionally, the ’290 patent aims to reduce circuit scale and power consumption. *Id.* at 1:54–57, 2:24–27.

³ The ’290 patent claims earliest priority through a series of continuation applications to application No. 13/775,854, filed on February 25, 2013. Ex. 1001, code (63). The specific priority date of the challenged claims is not at issue in this proceeding, and we need not make any determination in this regard for purposes of this Decision.

One embodiment of the '290 patent pertains to a display device as depicted, for example, in Figure 12A, which is reproduced below.

FIG. 12A

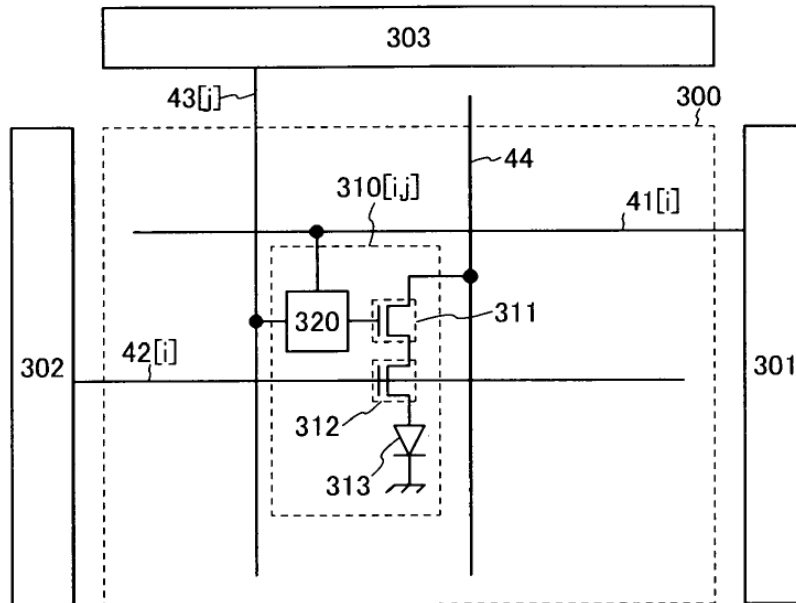


Figure 12A, above, shows a circuit diagram of a display device that includes pixel portion 300, gate driver 301, gate driver 302, and source driver 303. Ex. 1001, 17:9–12. Pixel portion 300 of the display device circuit includes pixels 310, each with two transistors 311, 312, display element 313, and circuit 320. *Id.* at 17:12–15. The display device circuit of Figure 12A may use a shift register circuit for gate driver 302, for example, a shift register circuit comprising the sequential circuit of Figure 2A. *See id.* at 5:65–6:21, 8:29–37, 17:15–17.

Figure 2A of the '290 patent is reproduced below.

FIG. 2A

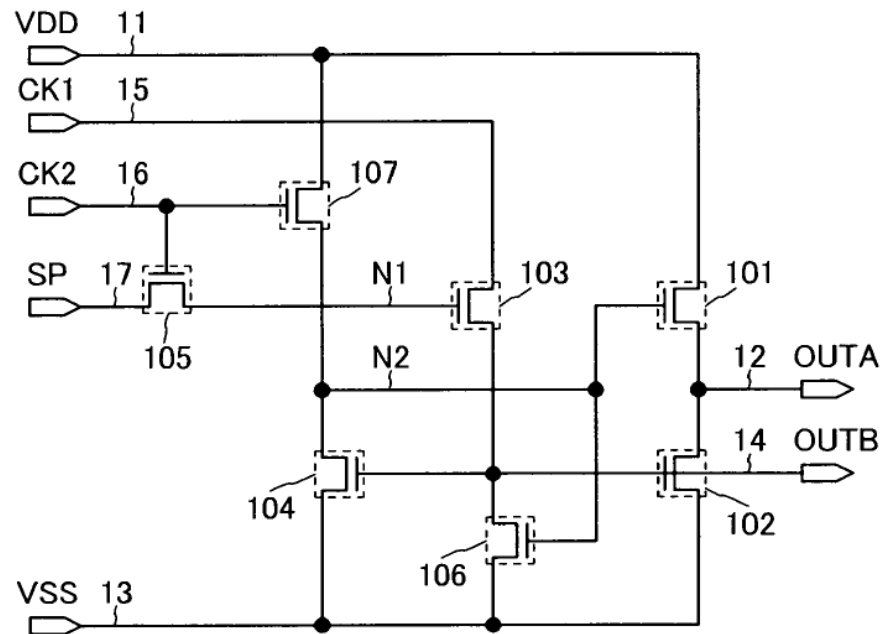


Figure 2A, above, shows a circuit diagram of a sequential circuit that includes seven transistors 101 to 107. Ex. 1001, 5:65–67, 11:43–47. In operation, during a first period of time, an input signal SP is at a high level, a clock signal CK1 is at a low level, and a clock signal CK2 is at a high level. *Id.* at 6:41–43. In this case, the voltage potential of wiring 12 for the output OUTA is the voltage potential of VDD, which is at a high level, while the voltage potential of wiring 14 for the output OUTB is the voltage potential of VSS, which is at the low level. *Id.* at 6:55–57, 7:3–5. In a second period of time, input signal SP is at a low level, clock signal CK1 is at a high level, and clock signal CK2 is at a low level. *Id.* at 7:6–8. Here, wiring 12 has the voltage potential of VSS, so output OUTA is at the low level, while wiring 14 has the potential of VDD, so output OUTB is at the high level. *Id.* at 7:25–27, 7:34–35. In subsequent third and fourth time periods, where SP is low, CK1 is low, and CK2 is high, and SP is low, CK1 is high, and CK2 is

low, respectively, OUTA is high and OUTB is low in both time periods.

Id. at 7:37–39, 7:47, 8:2–6, 8:13, 8:21.

Figure 3 of the '290 patent is reproduced below.

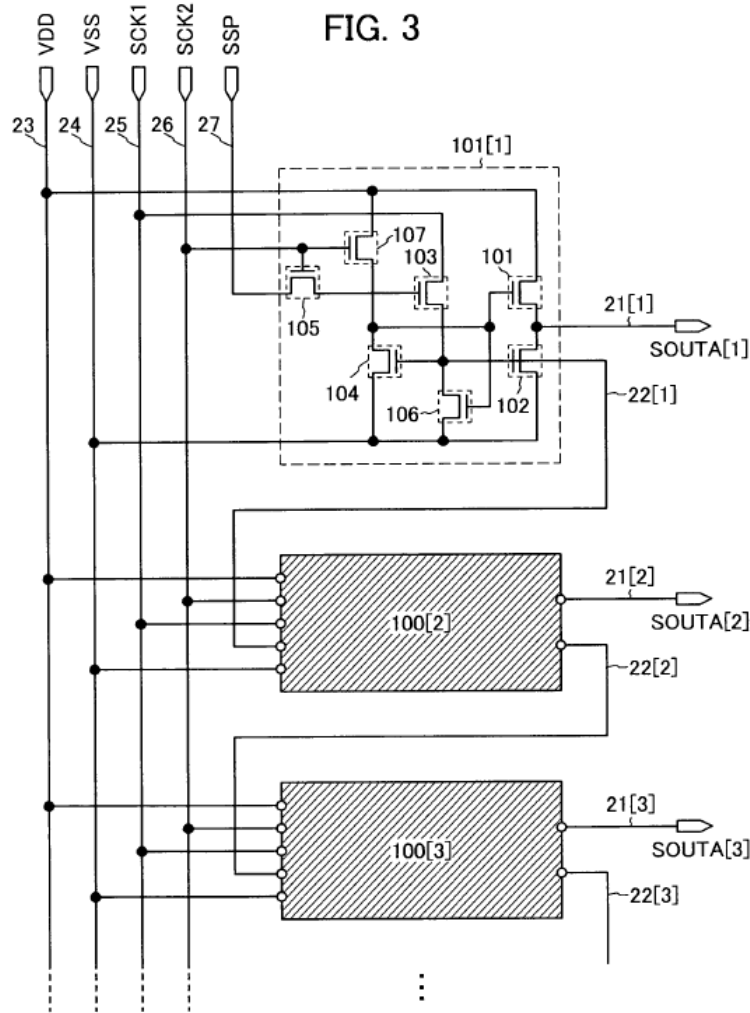


Figure 3, above, shows a circuit diagram of a shift register circuit that uses the sequential circuit depicted in Figure 2A for each of the stages 100(N). Ex. 1001, 8:29–37. Here, each output SOUTA(N) associated with a wiring 21(N) corresponds to OUTA in Figure 2A. *See id.* at 9:17–18.

When the shift register of Figure 3 is implemented in the display device depicted in Figure 12A as gate driver 302, the N wirings 42 in Figure 12 correspond to the N wirings 21 in Figure 3. *See id.* at 18:23–28.

In Figure 12, “gate driver 301 sequentially outputs a signal at the high level to the N wirings 41,” “gate driver 302 sequentially outputs a signal at the low level to the N wirings 42,” and “source driver 303 outputs a video signal to the M wirings 43.” *Id.* at 17:60–64. A video signal is output to a pixel when gate driver 301 outputs a high level signal to its respective wiring 41. *Id.* at 17:65–18:5. By supplying the low level signal on wiring 42, gate driver 302 can turn off transistor 312 in the pixel to solve color deviation or black blurring problems caused by an unintended amount of current flowing through transistor 311. *See id.* at 18:13–22.

C. Illustrative Claim

Each of the challenged claims is independent. Claim 1 of the ’290 patent is reproduced below, and is illustrative of the challenged claims.

1. [1.preamble] A semiconductor device comprising:
 - [1.1] a gate driver; and
 - [1.2] a pixel; and
 - [1.3] wherein the gate driver comprises a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, a sixth transistor, a seventh transistor,
 - [1.4] wherein one of a source and a drain of the first transistor is electrically connected to one of a source and a drain of the second transistor,
 - [1.5] wherein the one of the source and the drain of the first transistor is electrically connected to a first wiring,
 - [1.6] wherein the other of the source and the drain of the first transistor is electrically connected to a first power supply line,

[1.7] wherein the other of the source and the drain of the second transistor is electrically connected to a second power supply line,

[1.8] wherein one of a source and a drain of the third transistor is electrically connected to one of a source and a drain of the fourth transistor,

[1.9] wherein the one of the source and the drain of the third transistor is electrically connected to a gate of the first transistor,

[1.10] wherein the one of the source and the drain of the third transistor is electrically connected to a gate of the sixth transistor,

[1.11] wherein a gate of the third transistor is electrically connected to a second wiring,

[1.12] wherein the other of the source and the drain of the fourth transistor is electrically connected to the second power supply line,

[1.13] wherein one of a source and a drain of the fifth transistor is electrically connected to one of a source and a drain of the sixth transistor,

[1.14] wherein the one of the source and the drain of the sixth transistor is electrically connected to a gate of the second transistor,

[1.15] wherein the other of the source and the drain of the fifth transistor is electrically connected to a third wiring,

[1.16] wherein the other of the source and the drain of the sixth transistor is electrically connected to the second power supply line,

[1.17] wherein one of a source and a drain of the seventh transistor is electrically connected to a gate of the fourth transistor,

[1.18] wherein the one of the source and the drain of the seventh transistor is electrically connected to a gate of the fifth transistor,

[1.19] wherein a gate of the seventh transistor is electrically connected to the second wiring,

[1.20] wherein a first clock signal is input to the second wiring,

[1.21] wherein a second clock signal is input to the third wiring,

[1.22] wherein a ratio of a channel width to a channel length of the first transistor is larger than a ratio of a channel width to a channel length of the third transistor,

[1.23] wherein the ratio of the channel width to the channel length of the first transistor is larger than a ratio of a channel width to a channel length of the fourth transistor,

[1.24] wherein the ratio of the channel width to the channel length of the first transistor is larger than a ratio of a channel width to a channel length of the fifth transistor,

[1.25] wherein the ratio of the channel width to the channel length of the first transistor is larger than a ratio of a channel width to a channel length of the sixth transistor,

[1.26] wherein the ratio of the channel width to the channel length of the first transistor is larger than a ratio of a channel width to a channel length of the seventh transistor,

[1.27] wherein a ratio of a channel width to a channel length of the second transistor is larger than the ratio of the channel width to the channel length of the fourth transistor,

[1.28] wherein the pixel comprises an eighth transistor, a ninth transistor and a light emitting element,

[1.29] wherein one of a source and a drain of the eighth transistor is electrically connected to one of a source and a drain of the ninth transistor,

[1.30] wherein the other of the source and the drain of the ninth transistor is electrically connected to the light emitting element, and

[1.31] wherein a gate of one of the eighth transistor and the ninth transistor is electrically connected to the first wiring.

Ex. 1001, 26:31–27:48 (bracketed identifying labels added, corresponding to the labels used by Petitioner (Pet. 23–95)).

D. The Applied References

Petitioner relies on the following references in the asserted grounds.
Pet. 5, 8.

Reference	Issue Date/ Publication Date	Exhibit
U.S. Patent App. Pub. No. 2008/0079001 A1 (“Umezaki”)	Apr. 3, 2008 ⁴	Ex. 1003
U.S. Patent App. Pub. No. 2008/0013670 A1 (“Lo”)	Jan. 17, 2008 ⁵	Ex. 1004

Petitioner also relies on the Declaration of Jerzy Kanicki, Ph.D.
(Ex. 1002) to support its positions.

⁴ Umezaki is prior art at least under 35 U.S.C. §§ 102(a), (b), (e). See Pet. 5. Petitioner and Patent Owner refer to Umezaki as “the ’001 publication” throughout the Petition and Preliminary Response.

⁵ Lo is prior art at least under 35 U.S.C. §§ 102(a), (b), (e). See Pet. 5. Petitioner and Patent Owner refer to Lo as “the ’670 publication” throughout the Petition and Preliminary Response.

E. The Asserted Grounds

Petitioner sets forth its challenges to claims 1–3 on the following grounds. Pet. 8.

Reference(s)/Basis	35 U.S.C. §	Claims Challenged
Umezaki, Lo	103 ⁶	1–3
Umezaki	102	2

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *See Net*

⁶ The application leading to the ’290 patent claims priority through a series of continuations to an application filed before March 16, 2013 (*see* Ex. 1001, code (63)), thus, patentability is governed by the version of 35 U.S.C. §§ 102 and 103 preceding the Leahy-Smith America Invents Act (“AIA”), Pub L. No. 112-29, 125 Stat. 284 (2011).

MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Although the elements must be arranged or combined in the same way as in the claim, “the reference need not satisfy an *ipsissimis verbis* test,” i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *accord In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990). Further, to be anticipating, a prior art reference must be enabling and must describe the claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. *See Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000); *In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness.⁷ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of

⁷ The parties have not asserted or otherwise directed our attention to any objective evidence of non-obviousness.

ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). However, Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined the prior art references. *See In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

We analyze the asserted grounds of unpatentability in accordance with these principles to determine whether Petitioner has met its burden to establish a reasonable likelihood of success at trial.

B. Level of Ordinary Skill in the Art

We review the grounds of unpatentability in view of the understanding of a person of ordinary skill in the art at the time of the invention. *Graham*, 383 U.S. at 17. Petitioner proposes the following definition for the person of ordinary skill in the art:

a graduate degree in electrical engineering or computer engineering or a similar discipline, with at least three years of relevant industry or research experience, including experience designing or implementing OLEDs in combination with pixel or/and driving circuits.

Pet. 19–20 (citing Ex. 1002 ¶ 26). Patent Owner has not provided an assessment of the level of ordinary skill in the art and does not contest Petitioner’s proposal. *See generally* Prelim. Resp. For purposes of this Decision, we apply Petitioner’s proposed level of ordinary skill in the art, which is consistent with the ’290 patent and the asserted prior art.

C. *Claim Construction*

For this *inter partes* review proceeding claim terms

shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2021). Further, “[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record in the *inter partes* review proceeding will be considered.” *Id.*

Under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc), claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *See Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

Petitioner proposes constructions for two claim terms: “electrically connected” and “transistor.” *See* Pet. 15–19. Patent Owner does not propose any claim constructions at this stage of the proceeding. *See generally* Prelim. Resp.

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). We determine that express construction of the terms identified by Petitioner is not necessary for purposes of this Decision.

D. Overview of the Asserted References

1. Umezaki (Ex. 1003)

Umezaki is titled “Display Device and Electronic Device.” Ex. 1003, code (54). Umezaki recognizes that the state of the art includes “a technique for forming a pixel circuit and a driver circuit including a shift register and the like . . . over the same insulating substrate by using transistors formed of a non-crystalline semiconductor,” which “has been actively developed because the technique greatly contributes to reduction in power consumption and cost.” *Id.* ¶ 4. A shift register according to this technique may comprise a flip-flop, which includes “[a] start signal, a reset signal, a clock signal, a power supply potential VDD, and a power supply potential VSS.” *Id.* ¶ 5. “[A] signal with a potential of VDD is referred to as an H-level signal, and a signal a potential of which is VSS is referred to as an L-level signal.” *Id.* ¶ 7.

Figure 1A of Umezaki, reproduced below, shows an embodiment of a flip-flop. *Id.* ¶ 70.

FIG. 1A

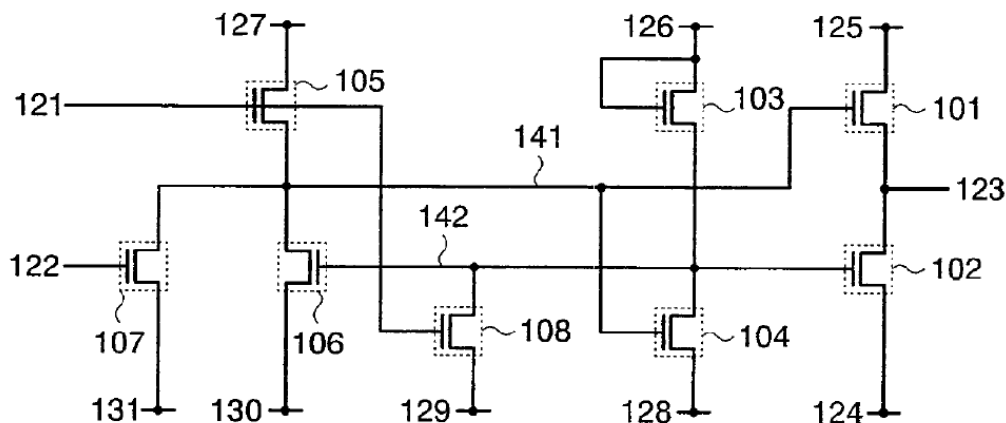


Figure 1A, above, is a circuit diagram of a flip-flop according to an embodiment of Umezaki. *Id.* ¶ 172. As seen in Figure 1A, the flip-flop

includes first to eighth transistors 101 to 108. *Id.* ¶ 172. Wirings 121, 122, 123, and 125 are “a first signal line, a second signal line, a third signal line, and a fourth signal line, respectively.” *Id.* ¶ 176. Wirings 124, 126, 127, 128, 129, 130, and 131 are each power supply lines. *See id.* During operation of the flip-flop, a potential V1 is supplied to wirings 126 and 127 and a potential V2 is supplied to wirings 124, 128, 129, 130, and 131. *Id.* ¶ 178. Further, “[a] signal 221, a signal 225, and a signal 222 . . . are input to the first wiring 121, the fifth wiring 125, and the second wiring 122, respectively. A signal 223 . . . is output from the third wiring 123. . . . [S]ignals 221, 225, 222, and 223 may be referred to as a start signal, a clock signal, a reset signal, and an output signal, respectively.” *Id.* ¶ 179; *see also id.* at Fig. 2 (a timing chart showing the operations of the flip-flop of Fig. 1A).

Figure 5A of Umezaki, reproduced below, shows another embodiment of a flip-flop. *Id.* ¶ 74.

FIG. 5A

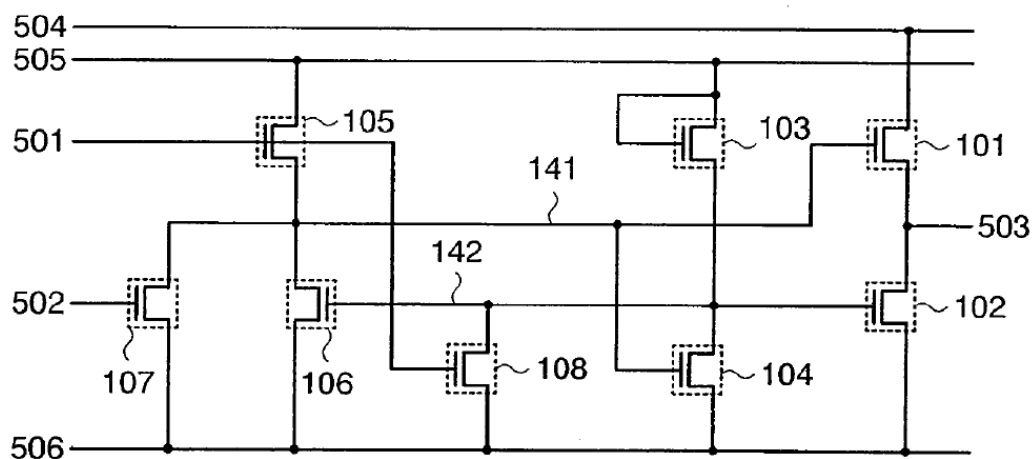


Figure 5A, above, is a circuit diagram of a flip-flop. *Id.* In the embodiment of Figure 5A, the number of wirings is reduced by having multiple transistor

electrodes connect to each of wirings 505 and 506. *Id.* ¶ 205. Here, wirings 501, 502, 503, and 504 correspond to wirings 121, 122, 123, and 125 in the Figure 1A embodiment shown above. *Id.* ¶ 204. Umezaki describes that, in this embodiment, “the number of wirings can be reduced, so that improvement in yield and reduction in layout area can be realized” as well as “improvement in reliability and operation efficiency.” *Id.* ¶ 205.

2. *Lo (Ex. 1004)*

Lo is titled “Shift Register.” *Ex. 1004*, code (54). *Lo* relates “a shift register constructed by amorphous silicon thin-film transistors.” *Id.* ¶ 2. In particular, *Lo* describes a shift register that includes *N* unit stages where the unit stages are connected together in succession. *Id.* ¶ 28.

Figure 3C of *Lo* is reproduced below:

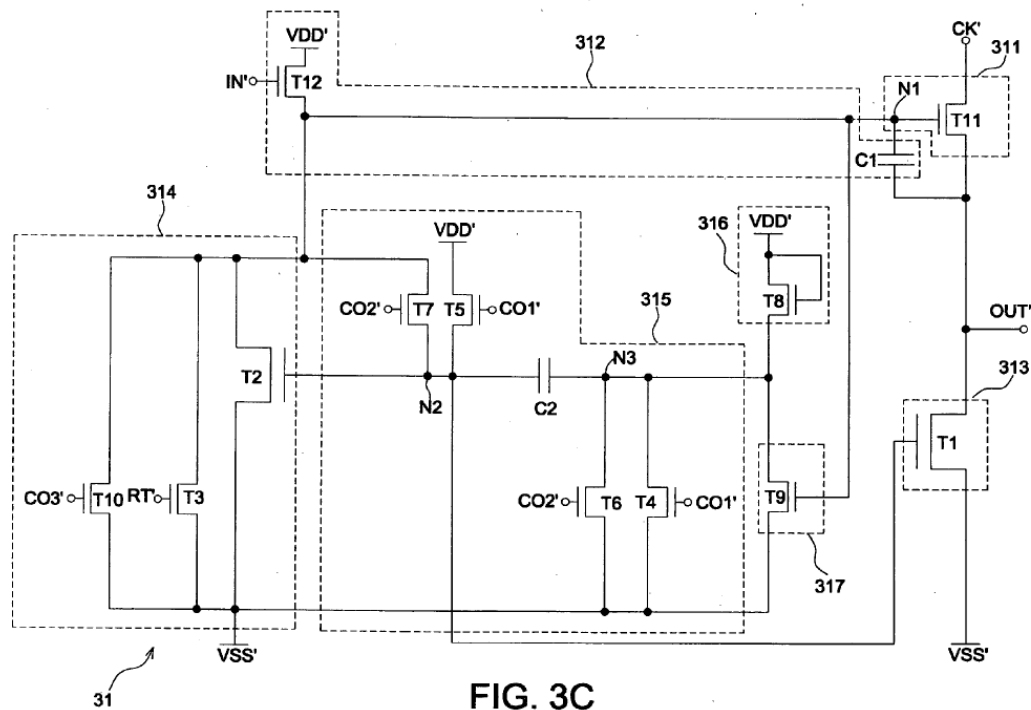


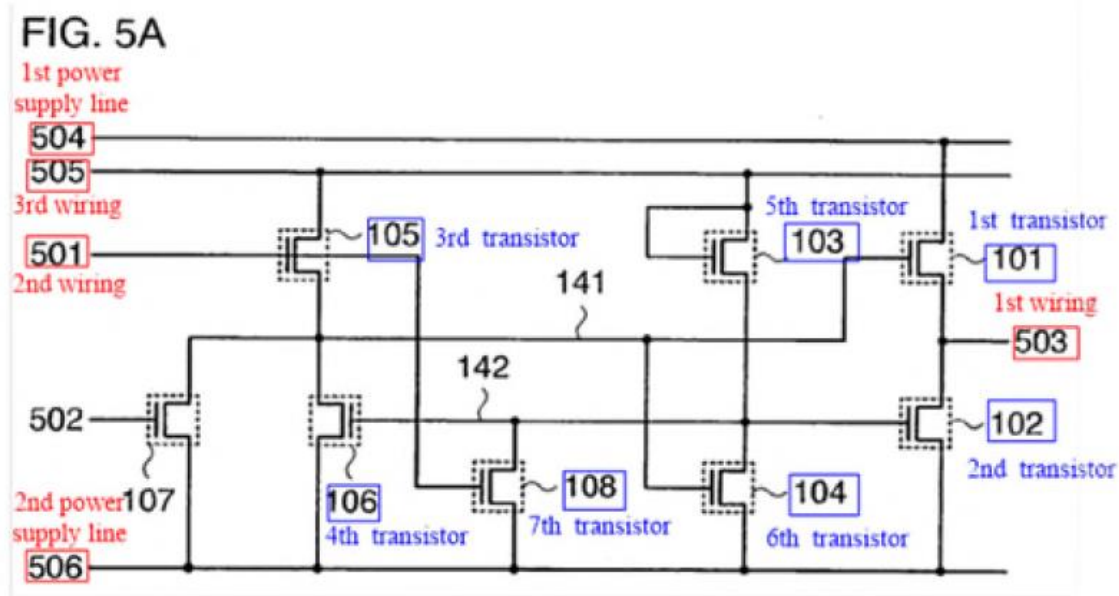
Figure 3C of Lo, above, shows a detailed circuit diagram of a unit stage in a shift register. *Id.* ¶ 23. Figure 3C shows unit stage 31 in which all of the transistors “are a-Si TFTs,” with twelve transistors in total. *Id.* ¶ 32. Unit stage 31 includes “an input terminal IN’, and output terminal OUT’, a feedback control terminal RT’, a clock signal input terminal CK’, a first control signal input terminal CO1’, a second control signal input terminal CO2’, a third control signal input terminal CO3’, a first power voltage terminal VSS’, and a second power voltage terminal VDD’.” *Id.* ¶ 28.

E. Asserted Grounds

Petitioner contends that claims 1–3 would have been obvious in view of Umezaki and Lo. Pet. 20–96. Petitioner also contends that claim 2 is anticipated by Umezaki. *Id.* at 96–101. Patent Owner disagrees, arguing that Petitioner does not show that the asserted references teach or suggest all elements of the challenged claims. Prelim. Resp. 12–30.

1. Independent Claim 1

Petitioner relies on the flip-flop structure of Figure 5A of Umezaki as teaching the seven transistors and various wirings and power supply lines that are recited in claim 1. See Pet. 23–95. Petitioner’s annotated version of Figure 5A is reproduced below (*id.* at 26).



Ex. 1003, Figure 5A (annotated).

Petitioner’s annotated Figure 5A, above, is a circuit diagram of Umezaki’s flip-flop structure with annotations highlighting Petitioner’s mapping to the recited transistors, wirings, and power supply lines of claim 1. *Id.*

Patent Owner focuses its arguments on elements [1.6] and [1.21]. See Prelim. Resp. 12–30. We likewise focus our discussion on these elements.

a) Element [1.6]

Element [1.6] recites “wherein the other of the source and the drain of the first transistor is electrically connected to a first power supply line.” Ex. 1001, 26:42–44. Petitioner relies on Umezaki’s fourth wiring 504 connected to first transistor 101 as teaching this claim element. Pet. 32–33 (citing Ex. 1002 ¶ 143; Ex. 1003 ¶ 206, Fig. 5A).

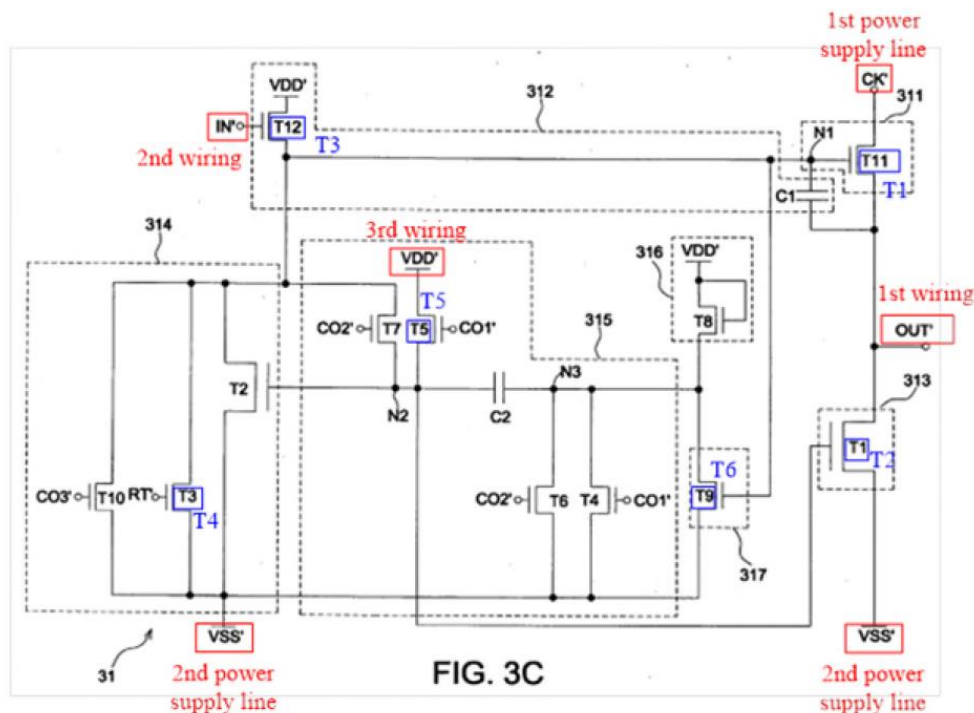
Patent Owner argues that “wiring 504 is not a power supply line at all. It is, instead, a signal line adapted to carry a clock signal.” Prelim. Resp. 13; see *id.* at 13–25. We agree. In Umezaki, fourth wiring 504 of Figure 5A is described as corresponding to fifth wiring 125 of Figure 1A. See Ex. 1003

¶ 204; Prelim. Resp. 15–16. Umezaki describes that signal 225 (i.e., the signal input to fifth wiring 125/fourth wiring 504) is a *clock signal*, and distinguishes the wirings (such as wirings 125, 504) which carry signals from those that supply constant potentials (i.e., the power supply). Ex. 1003 ¶¶ 178–179; Prelim. Resp. 16–17. This distinction is consistent with the description in the ’290 patent itself, which distinguishes between signal lines and power supply lines. Ex. 1001, 4:45–48 (“In this specification and the like, a wiring to which a signal is input may be referred to as a signal line. In addition, a wiring to which a potential is supplied may be referred to as a power supply line.”).

We recognize that Petitioner cites to Umezaki’s disclosure that “[t]he first to eleventh wirings 121 to 131 can be freely connected as long as a flip-flop operates similarly to FIGS. 1A to 1C.” Ex. 1003 ¶ 204 (cited at, e.g., Pet. 25). We agree with Patent Owner, however, that “[t]his disclosure does not stand for the proposition that any input can be arbitrarily applied to any wiring without regard to their impact on the proper and intended operation of the circuit.” Prelim. Resp. 28; *see also* Ex. 1003 ¶ 204 (providing as an example that power supply lines 124, 128, 129, 131, and 131 of Fig. 1A are combined to a single power supply line 506 in Fig. 5A). As Patent Owner notes, Umezaki stresses that the flip-flop must operate similarly to that of Figures 1A to 1C. Prelim. Resp. 28 (citing Ex. 1003 ¶ 204). Petitioner does not explain sufficiently how Umezaki’s fourth wiring 504 is a power supply line or why a person of ordinary skill in the art would have been motivated to input a potential to fourth wiring 504 rather than inputting the disclosed clock signal. *See* Pet. 32 (simply stating that 504 is a power supply line without further explanation). Petitioner also does

not demonstrate that the resulting flip-flop would operate similarly to the circuits in Figures 1A to 1C if such a change was made.

Although Petitioner primarily relies on Lo as “explicitly includ[ing]” the recited “wherein a ratio of a channel width to a channel length of the second transistor is larger than the ratio of the channel width to the channel length of the fourth transistor” (Pet. 22 (“[Umezaki] differs, at most, from the claims by not including the element relating to a single element of claim 1”)), Petitioner also identifies transistors and wirings shown in Lo’s Figure 3C that Petitioner asserts correspond to the seven transistors and wirings and power supply lines recited in claim 1. *See id.* at 26–28. Petitioner’s annotated version of Figure 3C is reproduced below (*id.* at 28).



Ex. 1004, Figure 3C (annotated)

Petitioner’s annotated Figure 3C, above, shows Lo’s unit stage circuit diagram with annotations highlighting Petitioner’s mapping to the transistors, wirings and power supply lines of claim 1. Pet. 28; Ex. 1004

¶ 23. Regarding element [1.6], Petitioner simply states that Lo “teaches the other of the source and the drain of the first transistor T11 (T1 in blue) is electrically connected to the *clock signal input CK* for the purpose of receiving electrical signals.” Pet. 33 (emphasis added). Thus, Petitioner’s reliance on Lo has the same deficiencies as discussed above with respect to Umezaki.

b) Element [1.21]

Element [1.21] recites “wherein a second clock signal is input to the third wiring.” Ex. 1001, 27:15. Petitioner relies on Umezaki’s fifth wiring 505 as teaching the recited third wiring. Pet. 53 (citing Ex. 1002 ¶ 188, Ex. 1003 ¶ 206, Fig. 5A). Petitioner further contends that, based on Umezaki’s disclosure that the wirings “can be freely connected” (Ex. 1003, ¶ 204), “a [person of ordinary skill in the art] reading [Umezaki] would have realized that a clock signal could be input to almost any of the wirings.” Pet. 71 (citing Ex. 1002 ¶ 226); *see id.* at 65–71 (citing Ex. 1002 ¶¶ 218–227; Ex. 1003 ¶¶ 70, 179).

Patent Owner argues that “[i]n reality, . . . [Umezaki] does not disclose that a ‘clock signal’ is input to wiring 505. Rather, [Umezaki] identifies wiring 505 (by description with reference to FIG. 1A) as a ‘power supply line’ to which is supplied a constant potential V1.” Prelim. Resp. 26 (citing Ex. 1003 ¶¶ 176–178); *see id.* at 26–28 (further explaining this argument).

As noted, Petitioner’s contention that wiring 505 could instead receive a clock signal is based on Umezaki’s disclosure that the wirings “can be freely connected” (Ex. 1003 ¶ 204). Pet. 66, 70. As discussed above, we agree with Patent Owner that “[t]his disclosure does not stand for the

proposition that any input can be arbitrarily applied to any wiring without regard to their impact on the proper and intended operation of the circuit.” Prelim. Resp. 28 (citing Ex. 1003 ¶ 204 (emphasizing that the wiring can be “freely connected **as long as a flip-flop operates similarly to FIGS. 1A to 1C.**”)). Petitioner does not explain sufficiently why a person of ordinary skill in the art would have been motivated to supply a clock signal to the disclosed power supply line, nor has Petitioner demonstrated that the resulting flip-flop would operate similarly to the circuits in Figures 1A to 1C if such a change was made. See Pet. 65–71; Prelim. Resp. 29–30.

c) Conclusion as to Claim 1

For the reasons discussed, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that claim 1 would have been obvious in view of Umezaki and Lo.

2. Independent Claims 2 and 3

Independent claims 2 and 3 also recite semiconductor devices, with configurations of transistors and the various wirings and power supply lines that are similar to those recited in claim 1. In particular, each of claims 2 and 3 also recites that “the other of the source and the drain of the first transistor is electrically connected to a first power supply line,” as recited in element [1.6] of claim 1. See Ex. 1001, 27:59–61 (claim 2), 28:42–44 (claim 3).

In the asserted obviousness ground, Petitioner relies on the same teachings of Umezaki and Lo for teaching this element of claims 2 and 3 as those discussed above for claim 1. See Pet. 96. Accordingly, and for the same reasons, we are not persuaded that Petitioner has demonstrated a

reasonable likelihood of prevailing on its assertion that independent claims 2 and 3 would have been obvious in view of Umezaki and Lo.

Similarly, in the asserted anticipation ground, Petitioner simply refers back to its discussion of Umezaki in the obviousness ground, in asserting that Umezaki discloses this limitation. *See* Pet. 97. Accordingly, and for the same reasons discussed above, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its assertion that independent claim 2 is anticipated by Umezaki.

F. Discretionary Denial

Because we deny the Petition on the merits, we do not reach the issue of discretionary denial. *See* Pet. 102–03; Prelim. Resp. 30–36.

III. CONCLUSION

After considering the evidence and arguments presented in the Petition and Preliminary Response, we determine that the record does not demonstrate a reasonable likelihood that Petitioner will prevail with respect to any claim challenged in the Petition. We, therefore, do not institute an *inter partes* review.

IV. ORDER

Accordingly, it is

ORDERED that the Petition is *denied* as to all challenged claims, and no trial is instituted.

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