

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC., LG ELECTRONICS, INC.,
and SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

ARIGNA TECHNOLOGY LTD.,
Patent Owner.

IPR2022-00651
Patent 6,603,343 B2

Before THU A. DANG, GARTH D. BAER, and SHARON FENICK,
Administrative Patent Judges.

DANG, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background*

In response to a Petition (Paper 4, “Pet.”) filed by Apple Inc., LG Electronics, Inc., and Samsung Electronics Co., Ltd. (collectively, “Petitioner”), we instituted *inter partes* review of claims 1 and 2 (the “challenged claims”) of U.S. Patent No. 6,603,343 B2 (Ex. 1001, “the ’343 patent”). See Paper 12 (“Dec. Inst.”). During trial, Arigna Technology Ltd. (“Patent Owner”) filed a Preliminary Response (Paper 15 (“PO Resp.”)), to which Petitioner filed a Reply (Paper 20 (“Pet. Reply”)). In turn, Patent Owner filed a Sur-reply. Paper 21 (“PO Sur-reply”). An oral hearing was held with the parties on July 26, 2023. A transcript of the hearing has been entered into the record. Paper 28 (“Tr.”)

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the record before us, Petitioner has shown by a preponderance of the evidence that claims 1 and 2 of the ’343 patent are unpatentable.

B. *Related Proceedings*

The parties identify the ’343 patent as the subject of *Arigna Tech. Ltd v. TCL Tech. Grp. Corp.*, Case No. 6:22-cv-00217 (W.D. Tex); *Arigna Tech. Ltd v. OnePlus Tech. Shenzhen Co.*, Case No. 6:21-cv-01145 (W.D. Tex.); *Arigna Tech. Ltd v. LG Elecs., Inc. et al.*, Case No. 2:21-cv-0077 (E.D. Tex); *Arigna Tech. Ltd v. Google LLC*, Case No. 6:21-cv-01045 (W.D. Tex.); and *Arigna Tech. Ltd. v. Samsung Elecs. Co. et al.*, Case No. 6:21-cv-00943 (W.D. Tex). Pet. 77; Paper 6, 2 (collectively, “the parallel litigation”).

Patent Owner notes that it has settled all claims regarding the '343 patent with Petitioners LG Electronics and Samsung. PO Resp. 1 n.1.

C. The '343 Patent

The '343 patent, titled "Phase Correction Circuit for Transistor Using High-Frequency Signal," issued on August 5, 2003, from Application No. 10/171,983, with a filing date of June 17, 2002. Ex. 1001, codes (54), (45), (21), (22). According to the '343 patent, the patented invention relates to "a phase correction circuit for a transistor using a high-frequency signal." *Id.* at 1:8–10.

The '343 patent recognizes that a threshold voltage of a gate of a transistor is increased by an increase in the temperature of the transistor, and thus, if the threshold voltage has been increased, a high-level voltage of a control signal supplied to the gate needs to increase so that the transistor can work correctly. *Id.* at 1:13–19. According to the '343 patent, temperature compensation circuits have been proposed to solve the problem by supplying an increased compensation voltage with the increase in temperature of the transistor. *Id.* at 1:23–28. One such temperature compensation circuit is a phase temperature compensation high frequency amplifier that has a circuit functioning as a phase correction circuit, the circuit having a varactor diode and a potential dividing circuit for adjusting a supply voltage of the varactor diode. *Id.* at 2:13–18. According to the '343 patent, the depletion capacitance of the varactor diode changes in simple proportion to the square root of the supply voltage at the step portion, in inverse proportion to the cube root of the supply voltage at the graded junction, and in simple proportion to the increase of its temperature. *Id.* at 2:21–29. Thus,

Figure 1 shows transistor 100 for high-frequency signal, where a gate of the transistor is connected to a control signal line, temperature compensation circuit 10, and phase correction circuit 20. *Id.* at 4:3–6. As shown in Figure 1, a drain of transistor 100 is supplied with supply voltage V_{cc} , a source of transistor 100 is connected to ground, and a drain of transistor 100 is connected to high-frequency circuit 200. *Id.* at 4:6–11. The threshold voltage of transistor 100 increases when the transistor's temperature increases. *Id.* at 4:12–14.

Temperature compensation circuit 10 includes load circuit 11 and resistor 12 connected in series to load circuit 11. *Id.* at 4:18–20. Joint P1 between load circuit 11 and resistor 12 is connected to the gate of transistor 100. *Id.* at 4:21–22. Resistance of load circuit 11 increases together with an increase in temperature, and potential voltage of point P1, which is a compensation voltage supplied to the gate of transistor 100, increases in response to the increase in resistance of load circuit 11. *Id.* at 4:28–33. The change ratio of the compensation voltage to the temperature increase is set to be substantially identical to that of the gate threshold voltage to the temperature increase. *Id.* at 4:33–36. Therefore, transistor 100 always can work correctly, even if the high-level voltage of the control signal does not change by the temperature increase. *Id.* at 4:36–38.

The temperature increase causes an increase in depletion capacitance. *Id.* at 4:39–41. For example, when the compensation voltage (the potential voltage of point P1) is increased, a depletion capacitance between the gate and the source of transistor 100 is increased. *Id.* at 4:41–45. Phase correction circuit 20 includes the reactance component of its impedance to decrease inversely with the increase in depletion capacitance caused by the

temperature increase, and thus, the total capacitance of the depletion capacitance and the reactance component approaches a substantially constant value. *Id.* at 4:46–51. Figure 9 showing the total capacitance is reproduced below:

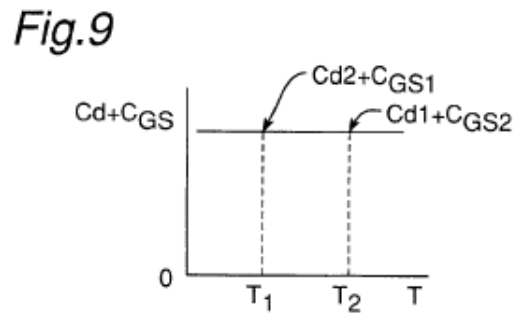


Figure 9 shows a temperature characteristic diagram of the total capacitance of reactance component C_d of the impedance of phase correction circuit 20 and depletion capacitance C_{GS} . *Id.* at 5:30–31. Total capacitance $C_d + C_{GS}$ is maintained constant irrelevant of the temperature. *Id.* at 5:31–32.

D. The Challenged Claims

Of challenged claims 1 and 2, claim 1 is independent, and is reproduced below:

1. A phase correction circuit for a transistor, comprising:

a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal, wherein the circuit element has a reactance that changes with potential difference between the input terminal and the output terminal; and

a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate, wherein a sum of the reactance of the circuit

element and a gate-source reactance of the transistor remains substantially constant.

Ex. 1001, 7:8–8:4.

E. Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 1 and 2 on the following grounds (Pet. 1):

Claims Challenged	35 U.S.C. § ¹	References/Basis
1, 2	103	Jeon '412, ² Jeon IEEE ³
1, 2	103	Yoshimasu, ⁴ Jeon IEEE

Petitioner relies on the Declaration of Sayfe Kiaei, Ph.D. (Ex. 1003) in support of its unpatentability contentions. Patent Owner provides the declaration of Marc E. Herniter, Ph.D. Ex. 2023. Dr. Herniter was cross-examined by Petitioner, and a transcript of his deposition was entered into the record. Ex. 1022.

¹ The Leahy-Smith America Invents Act (AIA), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103, effective March 16, 2013. Because the application from which the '343 patent issued was filed before this date, the pre-AIA version of § 103 apply.

² US Patent No. 6,222,412 B1, issued April 24, 2001, filed October 30, 1997 (Ex. 1005, “Jeon '412”).

³ Jeon, K., Kwon, Y., and Hong, S., *Input Harmonics Control Using Non-Linear Capacitor in GaAs FET Power Amplifier*, 1997 IEEE MTT-S Digest (Ex. 1006, “Jeon IEEE”).

⁴ JP Patent App. No. H4-40702, published February 12, 1992, filed June 6, 1990 (Ex. 1008, “Yoshimasu”).

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In our analysis, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation marks omitted). Furthermore, the prior art itself can reflect the appropriate level of ordinary skill in the art. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Relying on the declaration of Dr. Kiaei, Petitioner contends that a person of ordinary skill in the art (POSITA) at the time of the invention of the '343 patent would have had: 1) “at least a Master of Science Degree in an academic area emphasizing circuit design, such as electrical engineering or an equivalent field (or a similar technical Master’s Degree, or higher degree) with a concentration in circuit design;” or 2) “a Bachelor’s Degree (or higher degree) in an academic area such as electrical engineering with two or more years of work experience in circuit design,” wherein “[a]dditional education in a relevant field, or relevant industry experience may compensate for a deficit in one of the other aspects of the requirements stated.” Pet. 10–11 (citing Ex. 1003 ¶¶ 13, 27).

Patent Owner relies on the declaration of Dr. Herniter and contends that a POSITA at the time of the invention of the '343 patent would have had: 1) “a bachelor’s degree in electrical engineering or a similar field, and

approximately two years of industry or academic experience designing and analyzing integrated circuits;” or 2) “a master’s degree or Ph.D in electrical engineering or an equivalent field, with coursework, thesis, dissertation work, or research experience in integrated circuits.” PO Resp. 9–10 (citing Ex. 2023 ¶ 33).

The parties propose similar levels of ordinary skill in the art and do not directly challenge the other’s proposal. We consider the level of ordinary skill in the art to be reflected by the prior art of record. *See Okajima*, 261 F.3d at 1354–55 (holding that absent evidence to the contrary, “the prior art itself [may] reflect[] an appropriate level” of ordinary skill in the art).

In general, we agree with the areas of agreement in the parties’ proposals. Accordingly, we determine that a person of ordinary skill would have had a bachelor’s degree in electrical engineering or a similar field, and approximately two years of work experience in circuit design; or at least a master’s degree in electrical engineering or an equivalent field, with concentration in circuit design. Our ultimate decision, however, would not change were we to instead adopt outright either party’s proposed definition.

B. Claim Construction

We construe each claim “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2020). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a POSITA at the time of the invention and in the context of the entire patent

disclosure. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

“*reactance*”

Claim 1 recites, *inter alia*, “a circuit element” having “a reactance that changes with potential difference between the input terminal and the output terminal.” Ex. 1001, 7:19–24. Petitioner contends that “no formal claim constructions are necessary in this proceeding.” Pet. 11. Patent Owner acknowledges that it also does not propose any claim construction, but contends that “the burden of proposing and supporting a claim construction demonstrating unpatentability rests *entirely* on the Petitioner.” *See* PO Resp. 14–16. Patent Owner contends that, by not proposing any claim construction, Petitioner’s position “is inconsistent with the rest of the Petition.” *Id.* at 14. In particular, Patent Owner contends that the Petition must fail because Petitioner does not discuss “reactance,” but instead “solely addresses capacitance and argues that is sufficient because it bears some relation to reactance that Petitioner never expressly defines.” *Id.*; *see also* PO Sur-reply 21–25.

In light of the parties’ arguments and evidence, we determine that it is unnecessary to construe “reactance” to resolve the disputed issues before us. *See, e.g., Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that “only those terms need to be construed that are in controversy, and only to the extent necessary to resolve the controversy”)))); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean*

Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review). That is, to resolve the disputed issues before us, we will not enter a claim construction with respect to “reactance.” Instead, we address the term in our discussion of the parties’ explicit arguments with respect to the prior art references. *See supra* § II.D.3.a.iii.

“*phase correction*”

The preamble of claim 1 recites “[a] phase correction circuit for a transistor.” Ex. 1001, 7:18. Patent Owner contends that none of the asserted prior art references “address phase correction for a transistor, much less renders obvious the claimed phase correction circuit.” PO Resp. 27; *see also* PO Sur-reply 2–3. However, Petitioner responds that a “phase correction” circuit is “in the preamble of claim 1” and thus “does not limit the claim.” Pet. Reply 8 (emphasis omitted). According to Petitioner, the term “phase correction” in the preamble is “directed to the purpose and benefits of the claimed circuit and thus does not limit the claim scope.” *Id.*

In light of the parties’ arguments and evidence, we find that it is necessary to determine whether “phase correction” in the preamble of independent claim 1 is limiting.

Patent Owner contends the preamble of claim 1 is limiting because the ’343 patent “teaches and claims circuit configuration specific to phase correction of a transistor in the technological field addressed” (PO Resp. 27), and the preamble “serves to define the invention that is claimed” and is not “simply a description of the prior art” (*id.* at 30 (citing *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1573 (Fed. Cir. 1996))). In particular, Patent Owner contends the ’343 patent relates to a “phase correction circuit for a transistor using a high-frequency

signal . . . used for a radio communication device.” *Id.* at 28 (citing Ex. 1001, 1:13–29). Citing to Dr. Herniter’s testimony for support, Patent Owner contends that, while the prior art addresses “distortion of the waveforms,” the ’343 patent “address[es] the phase of the waveforms. *Id.* at 29 (citing Ex. 1003 ¶¶ 34–86, 107–126, 176–195).

Patent Owner then contends that “providing a ‘phase correction circuit for a transistor’ is necessary to give life and meaning” to claim 1. PO Resp. 30. In particular, Patent Owner contends that claim 1 “expressly recites the circuit arrangement for the transistor being phase corrected (noting the circuit element and control signal line must be connected to the gate of a transistor),” wherein “a phase correction circuit for a transistor gives meaning to the limitation ‘wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.’” *Id.* Patent Owner contends that “[a] POSITA would quantify ‘substantially constant’ as substantially constant enough to achieve the claimed phase correction for the transistor.” *Id.* (citing Ex. 2023 ¶ 40). Thus Patent Owner contends claim 1 “requires that the phase correction circuit maintains ‘a sum of the reactance of the circuit element and a gate-source **reactance of the transistor [to] remain[] substantially constant.**” PO Sur-reply 4 (citing Ex. 1001, 8:2–4).

Petitioner replies that the claim preamble is not limiting and that Dr. Herniter’s testimony does not support otherwise. Pet. Reply 8–11. We agree with Petitioner.

“[A] preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention.” *Catalina*

Marketing Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 809 (Fed. Cir. 2002). Here, claim 1 does not recite any step relating to phase correction, and we do not read any such limitation into the claim.

We agree with Petitioner that the claim body of claim 1 describes a structurally complete invention, i.e., “a transistor, circuit element, voltage control circuit, their corresponding interconnections, and the constant-reactance characteristic—without reliance on the preamble.” Pet. Reply 9; *see* Ex. 1001, 7:18–8:4. In particular, claim 1 recites a “circuit” including, *inter alia*, a “circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an output terminal;” and a “voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate.” Ex. 1001, 7:18–8:4.

Although we agree with Patent Owner that claim 1 “expressly recites the circuit arrangement for the transistor being phase corrected” (PO Resp. 30), we disagree with Patent Owner’s contention that “phase correction circuit gives meaning to the limitation ‘wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.’” *Id.* That is, the body of claim 1 describes a structurally complete invention and “deletion of the preamble phrase [i.e., ‘phase correction’] does not affect the structure . . . of the claimed invention.” *See Catalina*, 289 F.3d at 809. Thus, “phase correction” does not embody an essential component of the invention, but instead, is “simply a descriptive name for the invention that is fully set forth in the bodies of the claims.” *See Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 831

(Fed. Cir. 2003) (preamble term ‘policy caching method’ did not limit claims because it served only as a ‘convenient label for the invention as a whole’).

Accordingly, we disagree with Patent Owner’s contention that “providing a ‘phase correction circuit for a transistor’ is necessary to give life and meaning” to claim 1. PO Resp. 30; PO Sur-reply 3–4. Instead, we determine that “phase correction” in the preamble of claim 1 merely identifies an intended use for the otherwise complete claimed apparatus. “[P]reambles describing the use of an invention generally do not limit the claims because the patentability of apparatus or composition claims depends on the claimed structure, not on the use or purpose of that structure.” *See Catalina*, 289 F.3d at 809. Here, claim 1 is directed to a “circuit” comprising a “circuit element” and a “voltage control circuit,” wherein “phase correction” identifies a use for that circuit. Ex. 1001, 7:18–8:4. In other words, as Petitioner points out, “phase correction is a direct benefit of features that are explicitly recited in the body of claim 1.” Pet. Reply 8–9.

We find that Dr. Herniter’s testimony is entitled to little weight in addressing this issue. In particular, although Dr. Herniter testified that the preamble of claim 1 “is limiting,” he merely testified that “phase correction circuit for a transistor” is referring to “the phase angle between two waveforms.” Ex. 2023 ¶ 107 (citing Ex. 1001, 2:60–64). Dr. Herniter also testified that “[t]his phase correction circuit ‘stabilize[s] a phase of an output signal of the transistor, even if its gate potential is increased by a temperature compensation function, the temperature increase and the other reasons.’” *Id.* ¶ 40 (citing Ex. 1001, 2:59–64). We find testimony as to what the term “phase correction” refers to or what such phase correction

circuit does is not the proper inquiry to determine whether that term in a preamble limits the scope of the claim. Instead, Dr. Herniter’s testimony supports Petitioner’s contention that “phase correction” is an intended use of the claimed circuit. *See id.* ¶ 107 (“[A] purpose of the present invention is to provide a phase correction circuit to stabilize a phase of an output signal of the transistor”).

For the reasons discussed above, we conclude that the preamble of claim 1, reciting a “phase correction circuit for a transistor,” is not limiting.

We also are not persuaded by Patent Owner’s contention that “Petitioner has waived any argument challenging the preamble as non-limiting” because “[t]he Petition does not substantially dispute that the Claim 1 preamble is limiting.” PO Resp. 30. In particular, in the Petition, Petitioner does not affirmatively assert a waiver of the issue but rather argues that “Jeon ’412 discloses a phase correction circuit for a transistor” only “[t]o the extent that the preamble of claim 1 is limiting.” Pet. 24. Patent Owner is correct that Petitioner argues that the recitation “phase correction” in the preamble is not limiting only after Patent Owner asserts that “[t]he preamble of Claim 1 is limiting.” *See* PO Resp. 30–31; Pet. Reply 7–8. However, Petitioner’s underlying legal ground—that claim 1 would have been obvious over Jeon ’412 and Jeon IEEE—does not change, and Petitioner’s arguments are properly responsive to Patent Owner’s contentions and do not raise a new theory of unpatentability.

C. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness.⁵ *See Graham*, 383 U.S. at 17–18.

D. Claims 1 and 2 as obvious over Jeon ’412 and Jeon IEEE (ground 1)

Petitioner contends that a combination of Jeon ’412 and Jeon IEEE renders obvious claims 1 and 2 of the ’343 patent. Pet. 11–45 (ground 1). In particular, Petitioner contends that the circuits of the ’343 patent and Jeon ’412 have substantially similar topology and functionality and that Jeon IEEE describes specifics regarding the voltage control circuit. *Id.* at 14, 20–23.

In response, Patent Owner contends that Jeon ’412 and Jeon IEEE fail to render obvious 1) “wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant” (PO Resp. 17–27), 2) a “phase connection circuit for a transistor” (*id.* at 27–35), and 3) a “voltage control circuit” (*id.* at 37–49). Patent Owner also contends that Petitioner fails to address “reactance” recited in the claims. *Id.* at 52–63. We summarize the asserted prior art below.

⁵ Neither party presents arguments regarding objective evidence of nonobviousness in the instant proceeding.

1. Jeon '412

Jeon '412, titled "Circuit for Controlling Waveform Distortion at a Control Terminal of a Radio Frequency Transistor," relates to a circuit for controlling distortion resulting from nonlinearity of the impedance of a control terminal (gate or base) capacitance of a transistor. Ex. 1005, codes (54), (57). An illustration of Jeon '412's circuit for controlling waveform distortion is depicted in Figure 5, reproduced below.

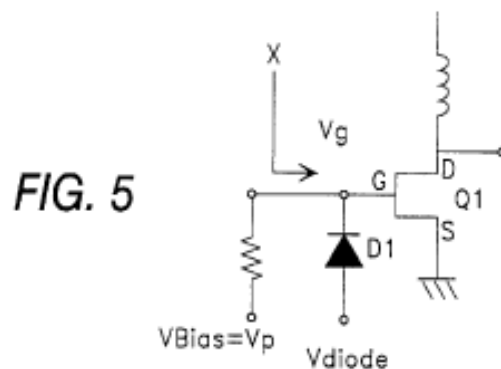


Figure 5 of Jeon '412 shows a schematic diagram depicting a circuit for controlling waveform distortion by employing diode D1. *Id.* at 3:56–57. As shown in Figure 5, gate terminal G of field-effect transistor (FET) Q1 is the anode of a diode fabricated by a gate-source junction, wherein the cathode of diode D1 is connected to gate terminal G of FET Q1. *Id.* at 4:5–7. Gate signal waveform $V_g(t)$ is a combination of gate bias voltage V_p and the gate input signal X . *Id.* at 1:37–40. While the overall gate capacitance is increased in the range above and below V_p , the circuit in Figure 5 increases the capacitance only below V_p and does not increase the capacitance above V_p to control waveform distortion. *Id.* at 4:15–22.

Figure 6 showing such a gate capacitance characteristic is reproduced below:

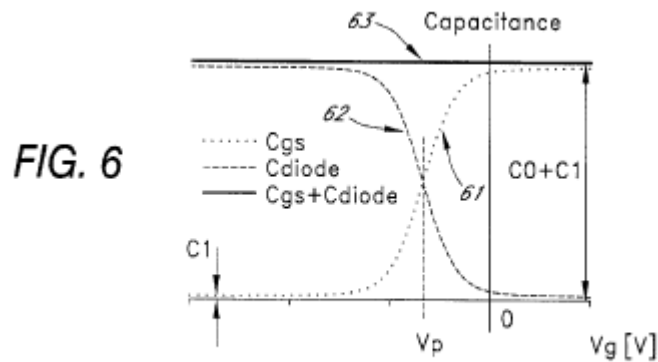


Figure 6 of Jeon '412 depicts a graph showing a typical gate capacitance characteristic when nonlinearity is controlled. *Id.* at 3:40–42. As shown in Figure 6, when anode voltage V_{diode} of diode D1 is 2 times gate bias voltage V_p , the gate capacitance of FET Q1 is represented as solid line 63. *Id.* at 4:7–10. Curve 61 represents capacitance C_{gs} of gate-source junction, curve 62 represents capacitance C_{diode} of diode D1, and curve 63 represents the sum (total capacitance $C_{gs}+C_{diode}$) of curve 61 and curve 62. *Id.* at 4:10–13. As shown in Figure 6, curve 63 has a constant value in the range above and below V_p .

Figure 8A showing Jeon '412's circuit, which controls the gate capacitance of a transistor is reproduced below:

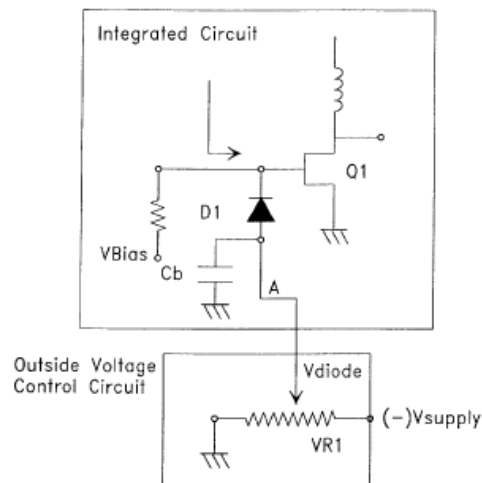


FIG. 8A

Figure 8A of Jeon '412 shows a schematic of a circuit, which controls the gate capacitance of FET Q1 on the outside of the integrated circuit comprising FET Q1. *Id.* at 3:46–48. As shown in Figure 8A, the outside voltage circuit employs variable resistor VR1 to connect to anode A of diode D1 from outside of the integrated circuit, wherein capacitor Cb is also connected to anode A of diode D1. *Id.* at 4:46–50. Variable resistor VR1 is provided in the outside voltage circuit for allowing voltage to change the capacitance of diode D1, and in particular, for adjusting each power supply voltage Vsupply and applying it to anode A of diode D1. *Id.* at 4:57–62.

2. Jeon IEEE

Jeon IEEE, titled “Input Harmonics Control Using Non-linear Capacitor in GaAs FET Power Amplifier,” addresses the effect of gate signal distortion arising from capacitance non-linearity on the power added efficiencies of power amplifiers. Ex. 1006, 1 (“Abstract”). Jeon IEEE proposes connecting a reversed diode to the gate of a FET, where the gate and source part of the FET is modeled as a diode. *Id.* An illustration of Jeon

IEEE's circuit for compensating gate capacitance non-linearity is depicted in Figure 3, reproduced below.

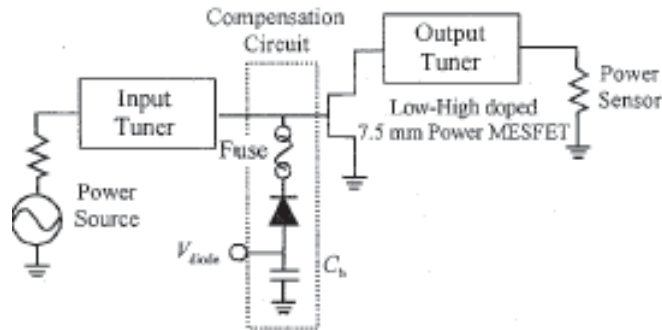


Figure 3 of Jeon IEEE shows a schematic diagram depicting a circuit for compensating gate capacitance non-linearity and setup for load-pull and source-pull. *Id.* at 2 (“New Approach”). As shown in Figure 3, the compensation is carried out by adding a reversed diode between the gate and constant voltage V_{diode} . *Id.* Because the diode junction is connected in the opposite direction with the diode in the gate, the gate sees constant capacitance.

Figure 4 of Jeon IEEE showing the compensated gate capacitance characteristic is reproduced below:

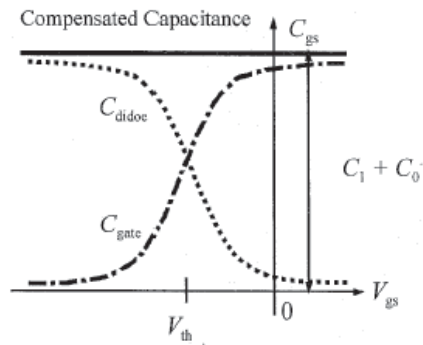


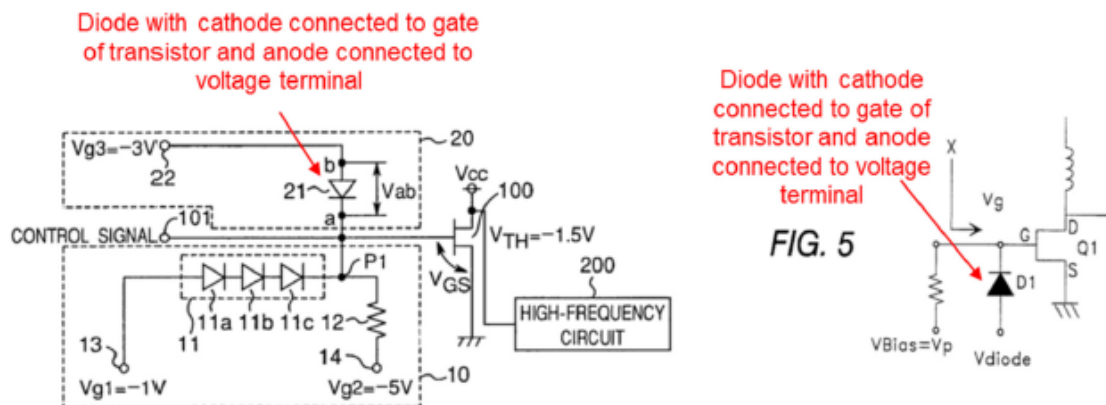
Figure 4 depicts a graph showing compensation of gate capacitance non-linearity using diode capacitance non-linearity. *Id.* As shown in Figure 4,

total capacitance ($C_{gs} + C_{diode}$), i.e., the sum of compensation capacitance C_{gs} and diode capacitance C_{diode} , is constant. *Id.*

3. Analysis

a. Independent Claim 1

Petitioner presents evidence that the respective circuits of the '343 patent and Jeon '412 achieve “substantially the same circuit effect: gate-source capacitances changes in a transistor due to changing gate voltages,” in “substantially the same way: using the compensating capacitance of a diode connected to a gate of the transistor.” *See* Pet. 14 (citing Ex. 1003 ¶¶ 65–66). Petitioner provides side-by-side annotated Figure 1 of the '343 patent and annotated Figure 5 of Jeon '412, as seen below.

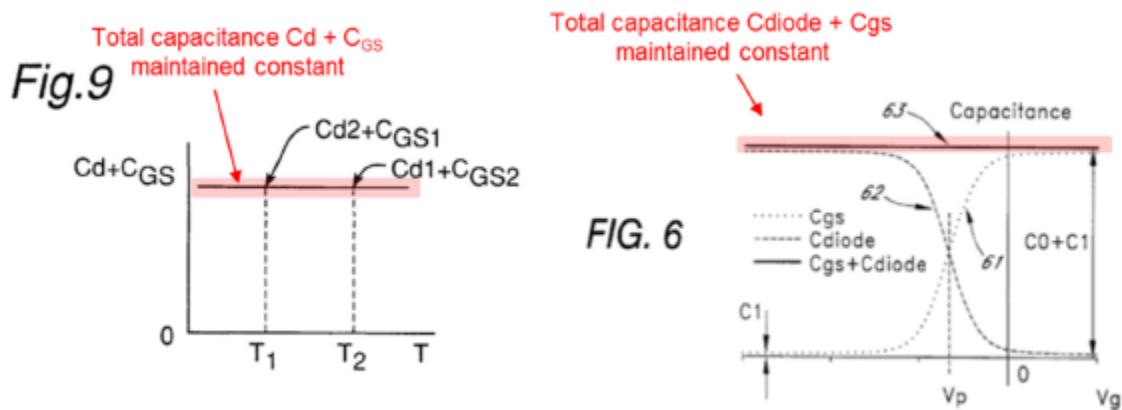


Side-by-side annotated Figure 1 of the '343 patent and annotated Figure 5 of Jeon '412 show circuit diagrams comprising a “diode with cathode connected to gate of transistor and anode connected to voltage terminal.” Pet. 14 (red). According to Petitioner, in the '343 patent, diode 21 has its cathode connected to a gate of transistor 100 and its anode connected to voltage terminal 22. *Id.* (citing Ex. 1001, Fig. 1). Petitioner contends that similarly, in Jeon '412, diode D1 has its cathode connected to a gate of

transistor Q1 and its anode connected to voltage terminal Vdiode. *Id.* (citing Ex. 1005, Fig. 5).

Petitioner also presents evidence that, in the '343 patent, the total capacitance $C_{GS} + C_d$ is maintained constant, wherein similarly, in Jeon '412, the total capacitance $C_{gs} + C_{diode}$ is maintained constant. Pet. 15 (citing Ex. 1001, Fig. 9; Ex. 1005, Fig. 6).

Petitioner provides side-by-side annotated Figure 9 of the '343 patent and annotated Figure 6 of Jeon '412, as seen below.



Side-by-side annotated Figure 9 of the '343 patent and annotated Figure 6 of Jeon '412 show presentation of capacitance graphs wherein “[t]otal capacitance [is] maintained constant.” Pet. 16 (red).

Having reviewed Petitioner’s and Patent Owner’s contentions and supporting evidence in the complete record, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1 and 2 would have been obvious over Jeon '412 and Jeon IEEE for the reasons stated below. We now address in detail Petitioner’s contentions and Patent Owner’s arguments with respect to the limitations of independent claim 1.

i. *Preamble: a “phase correction circuit for a transistor”*

As discussed *supra* § II(B), we conclude that the preamble is not limiting. Petitioner contends that, to the extent that the preamble is limiting, Jeon ’412 discloses a phase correction circuit for a transistor. Pet. 24. In particular, Petitioner points out Jeon ’412 recognizes that, “if the capacitance of gate remains constant without the dependence of the gate voltage, the gate impedance will have a constant value regardless of the applied voltage,” which then “**results in the reduction of the phase distortion.**” *Id.* at 24–25 (citing Ex. 1005, 2:19–27). According to Petitioner, Jeon ’412’s constant value of the gate impedance, “which causes the reduction of phase distortion,” occurs using a circuit for controlling waveform distortion that includes diode D1 shown in Figure 5. *Id.* at 25 (citing Ex. 1005, 3:1–15). Relying on Dr. Kiaei’s testimony, Petitioner then contends that Jeon ’412’s “circuit for controlling waveform distortion,” being connected to a gate of a transistor, “would have been understood by a POSITA as constituting a phase correction circuit for the transistor.” *Id.* (citing Ex. 1003 ¶ 89).

Patent Owner contends “Petitioner conflates what Jeon ’412 refers to as ‘phase distortion’ and ‘waveform distortion’ with phase shift.” *See* PO Resp. 31. Citing to Dr. Herniter, Patent Owner contends that “these are all different concepts.” *Id.* (citing Ex. 2023 ¶¶ 107–26, 176–195). According to Patent Owner, “neither Jeon ’412 nor Jeon IEEE suggests that these waveforms are shifted in phase/time, nor that the solution provided by either reference would correct a phase shift as described by the ’343 Patent.” *Id.* at 33.

Because we conclude that the preamble is not limiting, we need not address whether Petitioner has persuasively shown that the combination of Jeon '412 and Jeon IEEE (ground 1) teaches a “phase correction circuit for a transistor,” as recited in the preamble of claim 1.

Nevertheless, we note Patent Owner’s contention that “phase distortion” and “phase shift” are different concepts (PO Resp. 31) is not commensurate with the claim language. In particular, the claim does not recite “phase shift” correction, but merely “*phase* correction.” See Ex. 1001, 7:18 (emphasis added). Similarly, Patent Owner’s contention that “[n]one of the references Petitioner relies on even recognize the problem being solved by the '343 Patent” (PO Sur-reply 9) is also not commensurate with the claim language.

As Petitioner points out, Jeon '412 recognizes “*phase* distortion” and is directed at correcting this distortion in the phase. Pet. 24–25 (citing Ex. 1005, 2:19–27, 3:1–15) (emphasis added). And Dr. Kiaei testifies that a “circuit for controlling waveform distortion,” being connected to a gate of a transistor, “would have been understood by a POSITA as constituting a phase correction circuit for the transistor.” See Ex. 1003 ¶ 89.

Furthermore, Petitioner also points out that “the phase shift correction in the '343 Patent is caused by maintaining a constant capacitance at a gate of a transistor.” Pet. Reply 13; *see also* Ex. 1001, 7:8–12. Even Dr. Herniter testified that the '343 patent’s constant phase shift stems directly from a constant gate capacitance. Ex. 1022, 90:11–91:2. Thus, Petitioner contends that Jeon '412 and Jeon IEEE disclose circuits that “maintain constant the same total capacitance at the transistor gate (a sum of a diode capacitance C_d and a gate-source capacitance C_{GS}) as in the '343 Patent’s

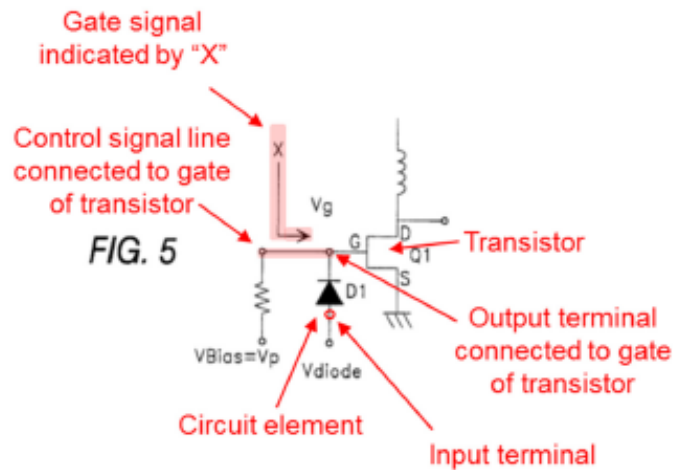
circuit,” and thus, it follows that these circuits, too, “perform phase correction associated with a phase shift.” Pet. Reply 14.

Nevertheless, because we determine that the preamble is not limiting, we need not determine that Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE teaches a “phase correction circuit for a transistor.”

- ii. *“a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal”*

Petitioner presents evidence that Jeon ’412 discloses a circuit element, diode D1, having a cathode connected to a gate terminal of a transistor (FET), and contends that Jeon ’412’s diode D1 is a circuit element having an output terminal connected to a gate of a transistor. Pet. 25 (citing Ex. 1005, 3:65–66; Ex. 1003 ¶ 90). Further, Petitioner presents evidence that Jeon ’412 describes “a line having a ‘gate bias voltage’ and a resistor connected to the gate terminal of the transistor,” wherein the “control terminal” of a transistor can be the “gate or base,” and this line is connected to the gate of the transistor. *Id.* (citing Ex. 1005, 1:10–11, 4:8–9, Fig. 5). Relying on the Dr. Kiaei’s testimony, Petitioner contends that “control of a transistor by a control line connected to the transistor gate is fundamental to the operation of transistors across various common applications, such as switches or amplifiers,” and that a POSITA would have understood the line connected to the gate of the transistor in Figure 5 of Jeon ’412 is a “control signal line.” *Id.* at 26 (citing Ex. 1003 ¶ 91).

To explain its contentions, Petitioner provides an annotated Figure 5 of Jeon ’412, as shown below.



Annotated FIG. 5

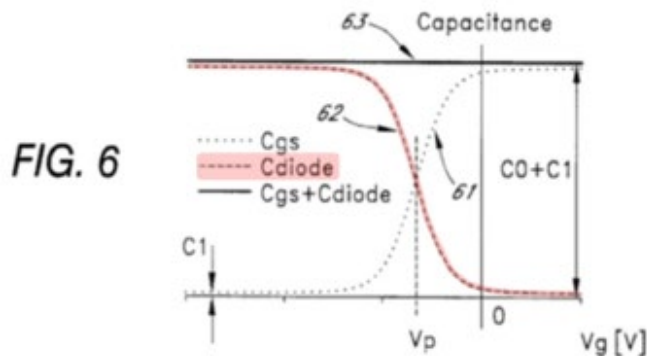
Annotated Figure 5 of Jeon '412 in the Petition shows a circuit diagram comprising a diode with its cathode connected to a gate of a transistor. Pet. 28. According to Petitioner, as shown in annotated Figure 5, Jeon '412's diode is a "circuit element," the cathode terminal of the diode is an "output terminal" that is connected to the gate of the transistor, a "control signal line" is also connected to the gate of the transistor, and the anode terminal of the diode is "an input terminal." *Id.* at 27 (citing Ex. 1003 ¶ 94).

Although Patent Owner does not present arguments in its Response addressing the specific merits of Petitioner's contentions with respect to this claim limitation (*see, generally*, PO Resp; PO Sur-reply), the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Here, as Petitioner points out, Jeon '412 discloses a circuit element (diode D1) having a cathode connected to a gate terminal of a transistor (FET). Pet. 25; *see also* Ex. 1005, 3:65–66, Fig. 5. Further, as shown in Figure 5 of Jeon '412, a line having a gate bias voltage and a resistor are connected to the gate terminal of the transistor. *See* Ex. 1005, 1:10–11, 4:8–9, Fig. 5. Based

on the complete record presented, we determine that Petitioner has persuasively shown that the combination of Jeon '412 and Jeon IEEE teaches “a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal,” as recited in claim 1.

iii. *the circuit element “has a reactance that changes with potential difference between the input terminal and the output terminal”*

Petitioner presents evidence that Jeon '412's circuit element (the diode) has a reactance that changes with potential difference between the input terminal (the anode terminal of the diode) and the output terminal (the cathode terminal of the diode). Pet. 28. Petitioner provides an annotated Figure 6 of Jeon '412, as seen below.



Annotated FIG. 6

Annotated Figure 6 of Jeon '412 in the Petition shows a capacitance graph, with curve 62 (red) representing a capacitance of the diode, and the capacitance of the diode changing with V_g , wherein “ V_g is the voltage at the diode cathode (output terminal).” Pet. 28–29 (citing Ex. 1005, 4:10–13, Figs. 5–6).

Relying on Dr. Kiaei's testimony, Petitioner contends that "the changes in V_g cause changes in the potential difference across Jeon '412's diode," which in turn "create the change in capacitance shown in FIG. 6." Pet. 28–29 (citing Ex. 1004 ¶¶ 42, 95–98). Petitioner references Dr. Kiaei's testimony, in which he testified that a POSITA would have recognized that the diode's change in capacitance (C_{diode}) shown in Figure 6 "represents a well-known characteristic of diodes," namely that "the capacitance of a diode changes with changes in the potential difference between the anode of the diode and the cathode of the diode." *Id.* at 29 (citing Ex. 1003 ¶ 42).

Petitioner then further relies on Dr. Kiaei's testimony to contend that the change in capacitance is "as associated with, equivalent to, or an example of a change in a reactance component in the same direction as the change in capacitance." Pet. 29 (citing Ex. 1003 ¶¶ 43–47). For support, Petitioner points to the prosecution history of the '343 patent, in which, according to Petitioner, the Applicant "conceded" that "**it is well known that a reverse biased diode functions as a capacitor, i.e., a reactance.**" *Id.* (citing Ex. 1002, 4). Petitioner contends that a POSITA would have understood and/or found obvious that Jeon '412's diode is "reversed biased" based on Jeon '412's description of "the voltage levels across its diode as well as the changes in capacitance depicted in FIG. 6," wherein a POSITA would have found it obvious that "a reactance component" of the diode "changes in a manner that corresponds to the changes in capacitance" as shown in Figure 6. *Id.* (citing Ex. 1003 ¶¶ 97, 99).

Petitioner also points out that the '343 patent itself describes "the **reactance component** C_d ," where " C_d " is also described as "the **depletion capacitance** . . . of the diode." Pet. 31 (citing Ex. 1001, 3:41–42, 4:47–48).

That is, in describing the circuit of Figure 1, the '343 patent describes that a “depletion capacitance C_d of the diode 21 decreases inversely with the increase in potential at the gate of the transistor 100 in order that the total capacitance of C_{GS} and C_d reaches a substantially constant value,” which “closely mirrors the language of claim 1,” which recites that “reactance of the circuit element decreases in response to an increase in potential of the gate, wherein the sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.” *Id.* at 31–32 (*comparing* Ex. 1001, 5:36–42 *with* Ex. 1001, 7:27–8:4).

Petitioner further points to Patent Owner’s contentions in the parallel district court litigation in which “Patent Owner identifies a claim mapping in which ‘the circuit element has a reactance component (i.e. capacitance) that changes with potential difference,’” and also contends that the '343 patent specification “identifies the ‘reactance component’ as equivalent to ‘capacitance’ (C_d).” Pet. 32 (citing Ex. 1007, 7, 10).

Accordingly, Petitioner contends that Jeon '412’s disclosure of a capacitance that changes with potential difference is equivalent to or at least renders obvious a disclosure of a reactance or reactance component that changes with potential difference.” Pet. 32 (citing Ex. 1003 ¶¶ 43–47, 99).

In response, Patent Owner argues that “Petitioner failed to address the ‘reactance’ limitations,” and “instead relied solely on teaching regarding capacitance.” PO Resp. 52–53. Patent Owner contends that the word “reactance” never appears in any of Petitioner’s asserted invalidity references. *Id.* at 54 (citing, *generally*, Ex. 1005; Ex. 1006; Ex. 1008). Instead, according to Patent Owner, Petitioner “has repeatedly argued in this proceeding that there is a relationship between capacitance and reactance,”

and “Petitioner argued in the parallel litigation that capacitance was not equivalent to reactance.” *Id.* Thus, Patent Owner contends that, for that theory to succeed, “the Board would have to adopt a construction for reactance that (1) Petitioner had not even expressly proposed . . . , and (2) Petitioner has expressly opposed in the parallel district court proceeding.” *Id.* at 53. According to Patent Owner, “[b]ecause Petitioner’s invalidity grounds would require a construction of ‘reactance’ that is irreconcilable with Petitioner’s positions in the parallel litigation, all of Petitioner’s grounds fail to render obvious the Challenged Claims.” *Id.*

We find Patent Owner’s arguments unavailing. In particular, we disagree with Patent Owner’s contention that, to determine whether Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE renders obvious a circuit element having a reactance, the Board would have to adopt a construction for reactance that Petitioner has not proposed in this proceeding and instead opposed in the parallel district court proceeding. PO Resp. 54. Although Patent Owner focuses on Petitioner’s claim construction arguments in the parallel litigation to assert that Jeon ’412 and Jeon IEEE fail to teach “reactance” (PO Resp. 55–59), Patent Owner does not address the merits of Petitioner’s assertion that, for example, Jeon ’412 “at least renders obvious a disclosure of a reactance.” *See* Pet. 32; *see also generally* PO Resp.; PO Sur-reply.

Here, Petitioner contends, and Patent Owner does not address, that Jeon ’412 discloses that “the changes in V_g cause changes in the potential difference across Jeon ’412’s diode,” which in turn “create the change in capacitance shown in FIG. 6,” wherein a POSITA would have recognized that the diode’s change in capacitance (C_{diode}) shown in Figure 6

“represents a well-known characteristic of diodes.” Pet. 28–29. As Petitioner points out, the ’343 patent similarly discloses “depletion capacitance C_d of the diode 21 decreases inversely with the increase in potential at the gate of the transistor 100 in order that the total capacitance of C_{GS} and C_d reaches a substantially constant value.” *See id.* at 31 (citing Ex. 1001, 3:41–42, 4:47–48).

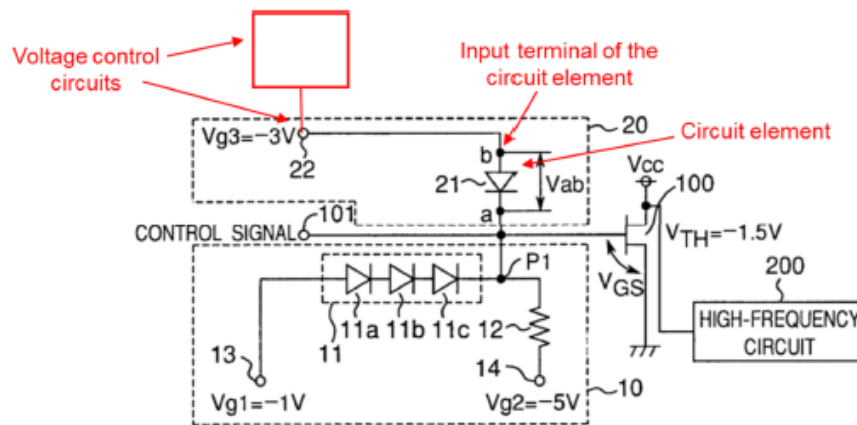
We also find persuasive, on this complete record, Petitioner’s contention, with the support of Dr. Kiaei’s testimony, that a POSITA would have recognized that the change in capacitance is “associated with, equivalent to, or an example of a change in a reactance component in the same direction as the change in capacitance.” Pet. 29 (citing Ex. 1003 ¶¶ 42–47). As Petitioner points out, according to the prosecution history of the ’343 patent, even the Applicant argued that “it is well known that a reverse biased diode functions as a capacitor, i.e., a reactance.” *See* Ex. 1002, 4. And the ’343 patent itself describes “ C_d ” as “the reactance component” as well as “the depletion capacitance . . . of the diode.” *See* 1001, 3:41–42, 4:47–48. In fact, as Petitioner points out, even Dr. Herniter’s testimony does not substantially differentiate between “capacitance” and “reactance.” Pet. Reply 24–25 (citing Ex. 1022, 148:22–23 (“(Q: And your opinions in your declaration do not depend on a definition of ‘reactance’ []? A: My opinions are consistent whether we use ‘capacitance’ or reactance.’)”; Ex. 2023, 36 (“change in gate-source capacitance causes a change in gate-source reactance”), 38 (“the [capacitance] sum of C_{GS} and C_d is constant, independent of voltage and temperature—ultimately resulting in a substantially constant reactance as well”)).

Thus, we are persuaded that a POSITA would have found it obvious that “a reactance component” of the diode “changes in a manner that corresponds to the changes in capacitance” as shown in Figure 6 of Jeon ’412. *See* Ex. 1003 ¶¶ 97, 99.

Based on the complete record presented, we determine that Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE teaches “a circuit element” with an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal, wherein the circuit element “has a reactance that changes with potential difference between the input terminal and the output terminal,” as recited in claim 1.

- iv. “a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate”*

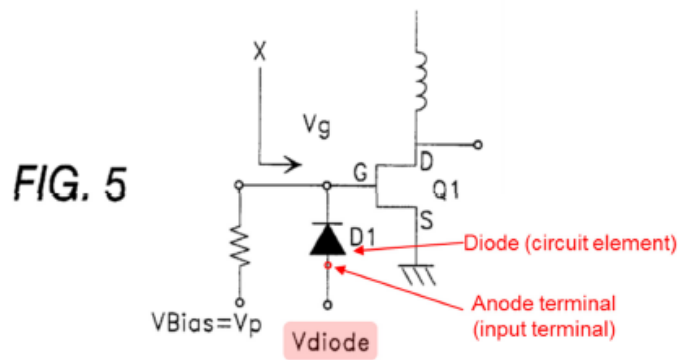
Petitioner presents evidence showing that Jeon ’412 and Jeon IEEE render obvious a voltage control circuit supplying a voltage to the input terminal of the circuit element. Pet. 32–33. Petitioner provides an annotated Figure 1 of the ’343 patent, as seen below.



Annotated FIG. 1

Annotated Figure 1 of the '343 patent as set forth in the Petition shows a circuit diagram with phase correction unit 20. Pet. 33. Petitioner contends that, as shown in annotated Figure 1, an anode of diode 21 is connected with voltage-supplying terminal 22, which is then supplied with constant voltage V_{g3} , wherein a POSITA would have understood that constant voltage V_{g3} “is supplied by a circuit designed to control the voltage at the voltage terminal 22 to maintain the constant voltage V_{g3} .” *Id.* (citing Ex. 1001, 4:60–62, Fig. 1; Ex. 1003 ¶ 100).

Petitioner then presents evidence showing that the combination of Jeon '412 and Jeon IEEE teach “a voltage control circuit supplying a voltage to the input terminal of the circuit element.” Pet. 33. Petitioner provides an annotated Figure 5 of Jeon '412, as seen below.



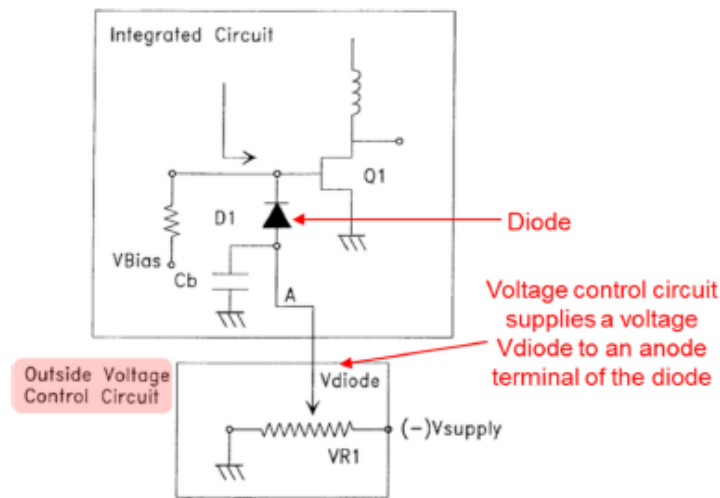
Annotated FIG. 5

Annotated Figure 5 of Jeon '412 in the Petition shows a schematic diagram depicting a circuit employing diode D1. Pet. 33–35. According to Petitioner, annotated Figure 5 shows voltage V_{diode} at the anode terminal (input terminal) of diode D1 (circuit element). *Id.* at 34. Petitioner contends that Jeon '412 describes that voltage V_{diode} “is $2 V_p$,” but “does not explicitly describe that this voltage is ‘supplied’ at the anode terminal.” *Id.* However, relying on Dr. Kiaei’s testimony, Petitioner contends that a POSITA would have understood or found obvious that “voltage V_{diode} has the value $2 V_p$ not by chance but, rather, because that value is being provided by a voltage control circuit supplying a constant voltage of $2 V_p$ to the anode terminal.” *Id.* (citing Ex. 1003 ¶ 101).

Furthermore, Petitioner presents evidence showing that a POSITA would have found it obvious to turn to Jeon IEEE and use the voltage control circuit disclosed in Jeon IEEE to supply voltage V_{diode} needed at the input terminal of Jeon '412’s diode. Pet. 35 (citing Ex. 1003 ¶¶ 102–103). In particular, according to Petitioner, in reference to Figure 3, Jeon IEEE describes that “a ‘constant voltage V_{diode} ’ is ‘set’ at the diode node,” and thus, as described by Dr. Kiaei, “a POSITA would have found it obvious that the ‘constant voltage’ is ‘set’ using a voltage control circuit

connected to the anode of the diode.” *Id.* (citing Ex. 1006, 818; Ex. 1003 ¶¶ 102–103). Petitioner contends that Jeon IEEE also describes that the set voltage can be varied for the purpose of tuning the input matching circuit, and thus, a POSITA would also have understood that “the function of varying of the voltage is performed by a voltage control circuit.” *Id.* at 36 (citing Ex. 1006, 820; Ex. 1005, Fig. 8; Ex. 1003 ¶ 103).

Alternatively, Petitioner presents evidence showing that a POSITA would have found it obvious to incorporate the “**outside voltage control circuit**” of Jeon ’412’s figure 8A into the circuit of Jeon ’412’s Figure 5. Pet. 36–37. Petitioner provides an annotated Figure 8A of Jeon ’412, as seen below.

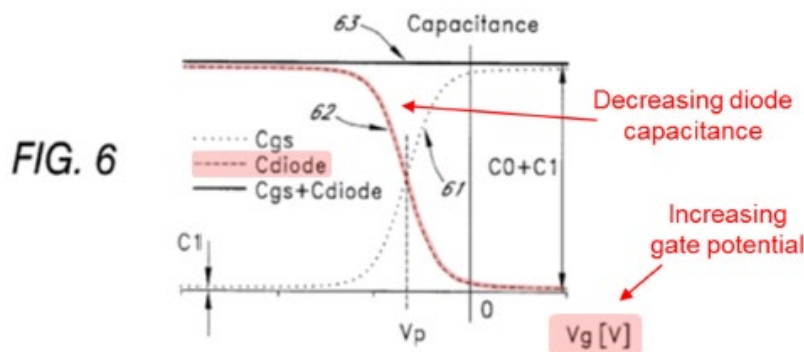


Annotated FIG. 8A

Annotated Figure 8A in the Petition shows a schematic of a circuit with an outside voltage control circuit. Pet. 37. Petitioner contends that Figure 8A shows that the “outside voltage control circuit” is connected to an anode of diode D1 and supplies voltage Vdiode to the anode, wherein variable resistor VR1 can be adjusted to modify “negative” voltage Vsupply, “applying it to anode of diode (D1).” *Id.* (citing Ex. 1005, 4:46–54, 4:57–61; Ex. 1003

¶¶ 104–106). According to Petitioner, a POSITA would have found it obvious to connect the outside voltage control circuit of Figure 8A to the diode anode of Figure 5 as the voltage control circuit. *Id.* at 38.

Petitioner further presents evidence showing that the voltage control circuit as described in Jeon '412 and Jeon IEEE supplies a voltage to the anode of the diode so that “the reactance of the diode decreases in response to an increase in potential of the gate.” Pet. 39. Petitioner provides an annotated Figure 6 of Jeon '412, as seen below.



Annotated Figure 6 of Jeon '412 in the Petition shows a capacitance graph showing diode capacitance C_{diode} , gate-source capacitance C_{gs} , and the sum $C_{gs}+C_{diode}$. Pet. 40. According to Petitioner, as shown in annotated Figure 6 of Jeon '412, as gate potential V_g increases, diode capacitance C_{diode} decreases. *Id.* Petitioner contends that, because the source of the transistor is grounded, “an increase in V_{gs} is equivalent to an increase in the gate bias.” *Id.* (citing Ex. 1003 ¶ 109). According to Petitioner, the inclusion of Jeon IEEE’s voltage control circuit into the circuit of Figure 5 of Jeon '412 “would not have qualitatively altered the decreasing diode capacitance with increasing gate bias” shown in Figure 6 of Jeon '412. *Id.*

Patent Owner responds that “Petitioner has failed to adequately identify the claimed voltage control circuit.” PO Resp. 38–49. Pointing to

the prosecution history, Patent Owner contends that, during prosecution, “the examiner attempted to identify specific components depicted in prior art circuit diagrams that met the claimed voltage control circuit limitation,” but “Petitioner has largely forgone any attempt to do the same here.” *Id.* at 38 (citing Ex. 2004, 10). Patent Owner also points to the district court proceeding where “Petitioner argued that the term ‘voltage control circuit’ was indefinite” (*id.* at 39–40 (citing Ex. 2003, 5–7)). Patent Owner contends that by “attempting to redefine a claim term without proposing an explicit construction,” “Petitioner’s positions in the parallel district court proceeding conflict with its arguments in this proceeding.” *Id.*

Patent Owner further contends that, although Petitioner contends that “a voltage control circuit simply means a terminal,” “an input terminal itself is plainly not a voltage control circuit.” PO Resp. 41. Patent Owner then contends that Petitioner also attempts to argue that the voltage control circuit is “implicit” in Jeon ’412’s Figure 5, which raises “inherency issues.” *Id.* at 42. Although Patent Owner acknowledges that Petitioner is citing to its expert for support, “the cited expert testimony does not address what Claim 1 actually recites,” i.e., “***so that the reactance of the circuit element decreases in response to an increase in potential of the gate.***” *Id.* at 43 (citing Ex. 1003 ¶ 101); *see also* PO Sur-reply 17.

Furthermore, Patent Owner contends that Petitioner’s reliance on Jeon IEEE’s use of a voltage control circuit does not actually teach the limitation. PO Resp. 44. That is, “Petitioner never identifies a circuit in Jeon IEEE which performs the entirety of the claimed limitation.” *Id.* According to Patent Owner, “Petitioner presupposes that it would have been obvious to use some purported voltage control circuit [in Jeon ’412] that it cannot even

expressly identify in Jeon IEEE to supply a specific voltage in a specific location of Jeon '412,” wherein “Petitioner’s expert provides no analysis supporting this sentiment, and instead parrots the same conclusion verbatim.” *Id.* at 45 (citing Ex. 1003 ¶ 103).

Patent Owner also takes issue with Petitioner’s reliance on Jeon '412 Figure 8A’s “outside voltage control circuit,” because being an “outside” circuit “shows that they did not view it as obvious.” PO Resp. 46. Patent Owner then contends that “Petitioner has not carried its burden” to prove that a POSITA would have incorporated Jeon IEEE’s outside voltage control circuit in the claimed manner to form part of the claimed phase correction circuit.” *Id.* at 47. For example, according to Patent Owner, in Figure 8B of Jeon '412, the anode of diode D1 “connects to ground, rather than the Outside Voltage Control Circuit.” *Id.*

We find Patent Owner’s arguments unavailing. In particular, we disagree that “Petitioner has failed to adequately identify the claimed voltage control circuit” in this proceeding. PO Resp. 38–49. Here, relying on Dr. Kiaei’s testimony, Petitioner provides evidence that Jeon '412 discloses voltage $V_{diode} = 2 V_p$ “being provided by a voltage control circuit supplying a constant voltage of $2 V_p$ to the anode terminal.” Pet. 34 (citing Ex. 1003 ¶ 101). Alternatively, we credit Dr. Kiaei’s testimony supporting Petitioner’s argument that Jeon '412’s Figure 8A shows that the “outside voltage control circuit” is connected to an anode of diode D1 and supplies voltage V_{diode} to the anode. *Id.* at 37 (citing Ex. 1005, 4:46–54, 4:57–61; Ex. 1003 ¶¶ 104–106).

Further, we disagree that Petitioner contends “a voltage control circuit simply means a terminal.” PO. Resp. 41. As Dr. Kiaei testified, a POSITA

would have understood or found obvious that, because voltage V_{diode} has a constant value $2 V_p$, that value is being provided by a voltage control circuit supplying a constant voltage of $2 V_p$ to the anode terminal. *See* Ex. 1003 ¶ 101. That is, Dr. Kiaei was not testifying that the terminal is a voltage control circuit, but rather, a POSITA would have understood that “a voltage control circuit” supplies a constant voltage “to the anode terminal.” *Id.* (emphasis added).

Here, Petitioner relies on the *combination* of Jeon '412 and Jeon IEEE, wherein, relying on Dr. Kiaei's testimony, Petitioner contends that a POSITA would have found it obvious to use the voltage control circuit disclosed in Jeon IEEE to supply voltage V_{diode} needed at the input terminal of Jeon '412's diode. Pet. 35 (citing Ex. 1003 ¶¶ 102–103). Petitioner contends that the voltage control circuit in the combined system of Jeon '412 and Jeon IEEE supplies a voltage to the anode of the diode so that “the reactance of the diode decreases in response to an increase in potential of the gate,” as claimed. *Id.* at 39. That is, contrary to Patent Owner's contention that Petitioner merely focuses “on supplying a voltage and ignore[s] the remaining requirements” (PO Sur-reply 16–17), Petitioner relies on the combination of Jeon '412 and Jeon IEEE for “a voltage control circuit that performs all the requirement of Claim 1.” *Id.*

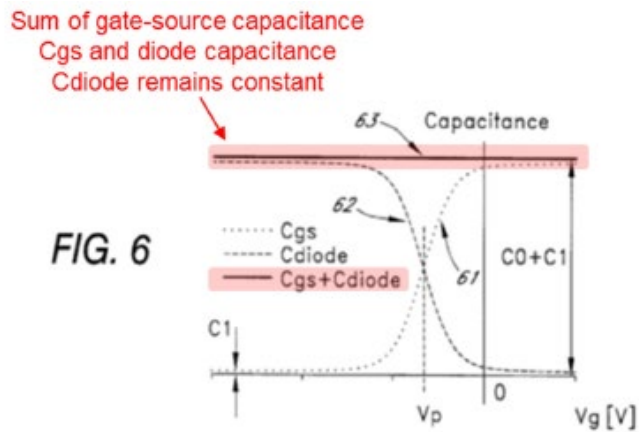
And, as Patent Owner acknowledges, Petitioner also relies on Jeon '412 Figure 8A's “outside voltage control circuit” for rendering obvious a voltage control circuit. PO Resp. 46. We are persuaded by Petitioner's contention that a POSITA would have found it obvious to connect the outside voltage control circuit of Figure 8A to the diode anode of Figure 5 as the voltage control circuit. Pet. 38.

Here, claim 1 requires that “a voltage control circuit” supplies a voltage to the input terminal, and does not preclude an “outside” voltage control circuit as the supplying circuit. *See* Ex. 1001, 7:26–8:2. We are persuaded that a POSITA would have found it obvious to apply a “voltage control circuit” to supply a constant voltage of $2 V_p$ to the anode terminal as shown in Figure 5 of Jeon ’412, so that “the reactance of the diode decreases in response to an increase in potential of the gate.” *See* Pet. 34–39.

Based on the complete record presented, we determine that Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE teaches “a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate,” as recited in claim 1.

- v. *“a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant”*

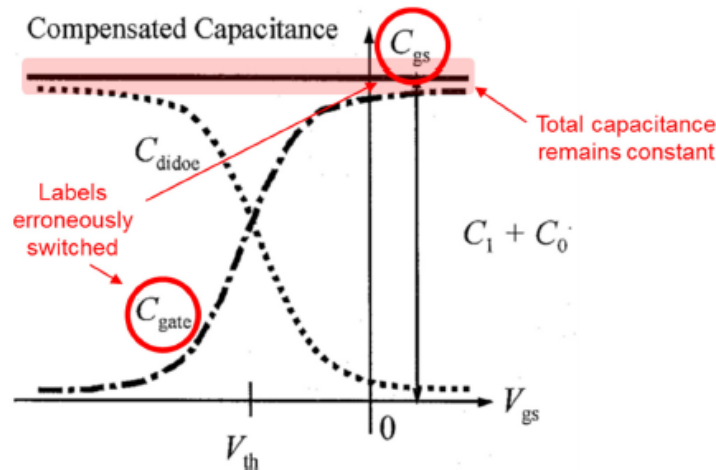
Petitioner provides evidence that, in Jeon ’412, “a sum of the capacitance of the circuit element and the gate-source capacitance of the transistor remains constant.” Pet. 41. Petitioner contends that, accordingly, Jeon ’412 “discloses that a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.” *Id.* To support its contentions, Petitioner provides an annotated Figure 6 of Jeon ’412, as seen below.



Annotated Figure 6 of Jeon '412 in the Petition shows a capacitance graph showing diode capacitance C_{diode} , gate-source capacitance C_{gs} , and the sum $C_{gs} + C_{diode}$. Pet. 42. According to Petitioner, as shown in annotated Figure 6 of Jeon '412, as gate potential V_g increases, diode capacitance C_{diode} decreases. *Id.* Petitioner contends that, as shown, the sum of the capacitance of the gate-source junction (curve 61) and the capacitance of the diode (curve 61) has a constant value (curve 63). *Id.* at 41–42 (citing Ex. 1005, 4:10–13, 4:13–15, Fig. 6). Relying on Dr. Kiaei's testimony, Petitioner contends that Jeon '412's constant gate capacitance that is a sum of C_{diode} and C_{gs} is “an obvious equivalent or example of a constant reactance that is a sum of the reactance of the diode and the reactance of the gate-source junction.” *Id.* at 42 (citing Ex. 1003 ¶ 110).

Petitioner further presents evidence that Jeon IEEE discloses “the same constant sum of the reactance of the circuit element and the gate-source reactance of the transistor as disclosed in Jeon '412.” Pet. 43 (citing Ex. 1006, Fig. 4; Ex. 1003 ¶ 111). Relying on Dr. Kiaei's testimony, Petitioner contends that the inclusion of Jeon IEEE's voltage control circuit

into the circuit of Figure 5 of Jeon '412 “would not have altered the constant reactance sum shown in FIG. 6 of Jeon '412.” *Id.* (citing Ex. 1003 ¶ 111). To support its contention, Petitioner provides an annotated Figure 4 of Jeon IEEE as shown below.



Annotated Figure 4 of Jeon IEEE in the Petition (Pet. 43) shows a capacitance graph showing diode capacitance C_{diode} , gate-source capacitance C_{gs} and the total capacitance at the gate ($C_{gs} + C_{diode}$). *See* Ex. 1006, 2. As shown in annotated Figure 4 of Jeon IEEE, the total capacitance at the gate ($C_{gs} + C_{diode}$) remains constant. *See* Pet. 43.

Patent Owner responds that a POSITA would have understood that the asserted combination “fail[s] to keep the reactance sum substantially constant as claimed when temperature changes,” wherein “none of the prior art even recognizes this problem.” PO Resp. 19. According to Patent Owner, the '343 patent explains that “the change in temperature alters the voltage threshold of the transistor,” wherein “it is desirable to include a temperature compensation circuit which provides a voltage adjustment to compensate for that change in threshold voltage for the circuit to function properly.” *Id.* at 18 (citing Ex. 1001, 1:23–29). Patent Owner contends that

the '343 patent's inventors "realized [that] a voltage adjustment had the undesirable effect of altering the gate-source reactance of the transistor, which created a phase shift in the transistor output signal," and that "to correct for this unwanted phase shift at the transistor, it was necessary to add a circuit element which would balance the change in reactance at the transistor." *Id.* (citing Ex. 1001, 1:63–2:6).

According to Patent Owner, a POSITA would have understood from the specification of the '343 patent that "keeping 'a sum of the reactance of the circuit element and a gate-source reactance of the transistor . . . substantially constant' would have required keeping that sum substantially constant during the operation parameters" described by the '343 patent, "including during changes in temperature." PO Resp. 19 (citing Ex. 2023 ¶¶ 129–130). Patent Owner contends that Jeon '412 and Jeon IEEE do not address "what happens to reactance of the circuit components as temperature changes," and thus, "do not identify or solve the problem addressed by the '343 inventors." *Id.*

We are unpersuaded by Patent Owner's contentions that the asserted combination fails to recognize the problem of "keep[ing] the reactance sum substantially constant as claimed when temperature changes." PO Resp. 19. In particular, as Petitioner points out, "the Challenged Claims do not recite that this reactance sum remains constant with changing temperature," or "any other limitation relating to temperature." Pet. Reply 2. As Petitioner also points out, "although FIG. 1 of the '343 Patent illustrates a 'temperature compensation circuit,' this circuit is not claimed." *Id.* (citing Ex. 1001, Fig. 1). In fact, the '343 patent itself acknowledges that the cause of an increase in gate potential of the transistor is not limited to a temperature

increase. *See* Ex. 1001, 2:60–64 (a purpose of the invention is to “provide a phase correction circuit to stabilize a phase of an output signal of the transistor, even if its gate potential is increased by a temperature compensation function, the temperature increase and the *other reasons*” (emphasis added)).

Here, claim 1 does not recite any temperature changes, but rather recites that “a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.” *See* Ex. 1001, 7:18–8:4. Although Patent Owner points out that claim 1 requires “the sum of the reactance to **remain** substantially constant” (PO Sur-reply 10–11), Petitioner shows that Jeon ’412 discloses that the sum of the capacitance of the gate-source junction (curve 61) and the capacitance of the diode (curve 61) remains at a constant value (curve 63). Pet. 41–42 (citing Ex. 1005, 4:10–13, 4:13–15, Fig. 6); *see* Petitioner’s annotated Figure 6 of Jeon ’412 *supra*. Similarly, Petitioner shows that Jeon IEEE discloses that “total capacitance C_{gs} remains constant as V_{gs} changes.” *Id.* at 42–43 (citing Ex. 1006, 818, Fig. 4); *see* Petitioner’s annotated Figure 4 of Jeon IEEE *supra*.

We credit Dr. Kiaei’s testimony, which is consistent with the complete record, that constant gate capacitance that is a sum of C_{diode} and C_{gs} is “an obvious equivalent or example of a constant reactance that is a sum of the reactance of the diode and the reactance of the gate-source junction.” Ex. 1003 ¶¶ 110–111.

Based on the complete record presented, we determine that Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE teaches “a sum of the reactance of the circuit element and a gate-source

reactance of the transistor remains substantially constant,” as recited in claim 1.

b. Dependent Claim 2

Claim 2 depends from claim 1 and further recites “the circuit element is a diode having an anode as the input terminal and a cathode as the output terminal,” wherein “the cathode of the diode is connected to the gate of the transistor,” and “the voltage control circuit supplies a reverse bias to the anode of the diode.” Ex. 1001, 8:5–10. Petitioner relies on Jeon ’412 in view of Jeon IEEE for teaching the limitations of claim 2, relying on Dr. Kiaei’s testimony for support. Pet. 43–45 (citing Ex. 1006, 817–818; Ex. 1003 ¶¶ 112–113).

Although Patent Owner does not present arguments in its Response addressing the specific merits of Petitioner’s contentions with respect to claim 2 (*see, generally*, PO Resp; PO Sur-reply), the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. Here, Jeon ’412 discloses diode D1 having an anode as the input terminal and a cathode as the output terminal, wherein the cathode is connected to the gate of transistor Q1. *See* Ex. 1005, Fig. 5. We are persuaded by Petitioner’s contention that it would have been obvious to a POSITA “to apply Jeon IEEE’s Vdiode in Jeon ’412 to supply a reverse bias to the anode of the diode D1.” Pet. 45.

Based on the complete record presented, we determine that Petitioner has persuasively shown that the combination of Jeon ’412 and Jeon IEEE (ground 1) teaches “wherein the circuit element is a diode having an anode as the input terminal and a cathode as the output terminal,” the cathode

being “connected to the gate of the transistor,” and “the voltage control circuit supplies a reverse bias to the anode of the diode,” as recited in claim 2.

c. Ground 1 Conclusion

Based on the complete record presented, we are persuaded that Petitioner has demonstrated that the subject matter of claims 1 and 2 would have been obvious over Jeon ’412 and Jeon IEEE (ground 1).

E. Claims 1 and 2 as Obvious over Yoshimasu and Jeon IEEE (Ground 2)

Petitioner contends that, alternatively, Yoshimasu in view of Jeon IEEE renders obvious claims 1 and 2 of the ’343 patent. Pet. 45–67. Because the Jeon ’412-Jeon IEEE combination (ground 1) is dispositive as to challenged claims 1 and 2 (*see supra* § II(D)), we do not reach Petitioner’s challenge of claims 1 and 2 based on obviousness over Yoshimasu and Jeon IEEE. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359 (2018) (holding a petitioner “is entitled to a final written decision addressing all of the claims it has challenged”); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App’x 984, 990 (Fed. Cir. 2020) (non-precedential) (recognizing that “[t]he Board has the discretion to decline to decide additional instituted grounds once the petitioner has prevailed on all its challenged claims”).

III. CONCLUSION⁶

For the foregoing reasons, we determine on the record at hand that Petitioner has demonstrated by a preponderance of the evidence that challenged claims 1 and 2 of the '343 patent are unpatentable.

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2	103	Jeon '412, Jeon IEEE	1, 2	
1, 2	103	Yoshimasu, Jeon IEEE ⁷		
Overall Outcome			1, 2	

IV. ORDER

For the reasons given, it is

ORDERED that, based on the preponderance of the evidence, claims 1 and 2 of the '343 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

⁷ We do not reach this ground because we have determined the challenged claims to be unpatentable under another ground. *See supra* § II(D).

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