

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BMW OF NORTH AMERICA, LLC,
Petitioner,

v.

ARIGNA TECHNOLOGY LIMITED,
Patent Owner.

IPR2021-01531¹
Patent 8,289,082 B2

Before GARTH D. BAER, SHARON FENICK, and IFTIKHAR AHMED,
Administrative Patent Judges.

FENICK, *Administrative Patent Judge.*

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ BMW of North America, LLC, petitioner in IPR2022-00737 was joined as a petitioner in this proceeding. Motions to terminate with respect to original petitioner Volkswagen Group of America, Inc. and additional joinder petitioners Mercedes-Benz Group AG and Mercedes-Benz USA, LLC were granted. Papers 16, 32.

I. INTRODUCTION

A. *Background and Summary*

Volkswagen Group of America, Inc. (“Volkswagen”) filed a Petition (Paper 2, “Pet.”), requesting an *inter partes* review of claims 1–32 of U.S. Patent No. 8,289,082 B2 (Ex. 1001, “the ’082 Patent”). After a determination that Volkswagen would likely prevail with respect to at least one of the claims challenged in the Petition, on March 16, 2022, we instituted an *inter partes* review as to the challenged claims of the ’082 patent. Paper 7 (“Decision on Institution” or “Inst. Dec.”). Patent Owner filed a Response (Paper 10, “PO Resp.”) on June 8, 2022. A Reply to the Patent Owner’s Response (Paper 20, “Pet. Reply”) was filed on September 12, 2022. On November 4, 2022, Patent Owner filed a Sur-reply (Paper 23, “PO Sur-reply”). On December 13, 2022, we held an oral hearing, a transcript of which (Paper 31, “Tr.”) has been entered into the record.

As discussed, Volkswagen initially filed the Petition in this proceeding. After a grant of joinder in IPR2022-00737, BMW of North America, LLC (“Petitioner”), was added as a petitioner in this proceeding. Paper 14. After a grant of joinder in IPR2022-000776, Mercedes-Benz Group AG and Mercedes-Benz USA, LLC, were added as petitioners in this proceeding. Paper 15. After a joint request of Patent Owner and Volkswagen, we terminated the proceeding as to Volkswagen. Papers 11, 12, 16. After a joint request of Patent Owner, Mercedes-Benz Group AG and Mercedes-Benz USA, LLC, we terminated the proceeding as to Mercedes-Benz Group AG and Mercedes-Benz USA, LLC. Papers 29, 30, 32.

B. Real Parties in Interest

Patent Owner has identified only itself as a real party in interest. Paper 5 (Patent Owner's Mandatory Notices), 2; Paper 26 (Patent Owner's Amended Mandatory Notices), 1.

Petitioner BMW of North America, LLC identified BMW of North America, LLC and Bayerische Motoren Werke AG as real parties in interest. IPR2022-00737, Paper 2 (Petition), 81.

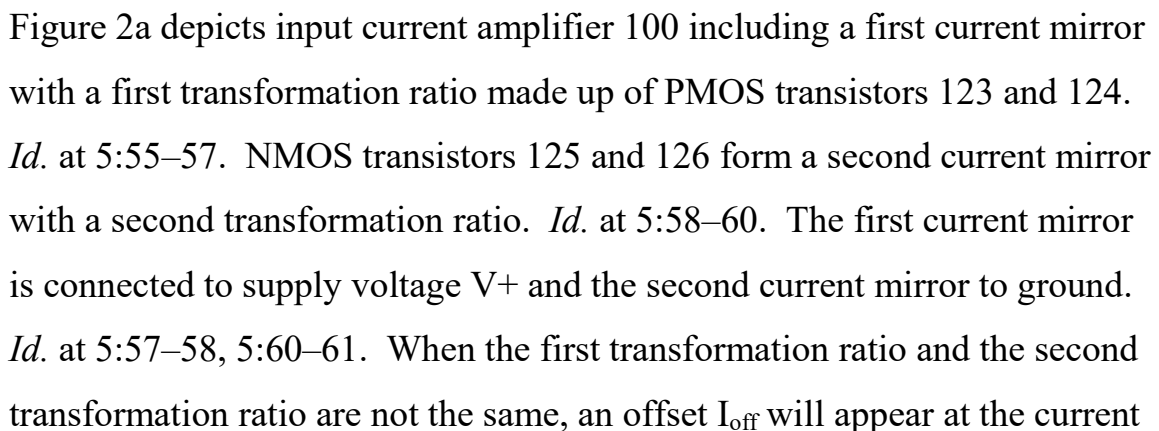
While this proceeding has been terminated as to prior petitioners, we note that Volkswagen Group of America, Inc. had identified itself, Volkswagen AG, Audi AG, Bentley Motors Limited, and Automobili Lamborghini S.p.A. as real parties in interest, and that Mercedes-Benz Group AG and Mercedes-Benz USA, LLC had identified only themselves as real parties in interest. Pet. 81; IPR2022-00776, Paper 2 (Petition), 76.

C. Related Matters

Arigna Technology Limited v. Volkswagen AG et al., Case No. 2:21-cv-00054-JRG-RSP (E.D. Tex.) and ITC Proceeding 337-TA-1267 were identified as related matters. Pet. 81; Paper 5, 2. Additionally, as discussed, joinder was granted in IPR2022-00737 and IPR2022-00776 and these proceedings have been identified as related matters. Paper 26, 1; IPR2022-00776, Paper 2 (Petition), 76–77.

D. The '082 Patent

The '082 patent is directed to the adjustment of an offset of an output current of a current amplifier. Ex. 1001, code (54). The '082 patent explains that a current amplifier takes as input an input current and outputs a current output, which is intended to be I_O , the input current amplified by the current amplification of the current amplifier, but may include an offset current I_{off} , which is an undesirable offset that can be positive or negative in



output of current amplifier 100. In current amplifier 100, output transistor 124 of the first current mirror is connected to current summing node 105 via PMOS transistor 131 and output transistor 126 of the second current mirror is connected to current summing node 105 via NMOS transistor 132. *Id.* at 6:6–11.

Also depicted in Figure 2a is adjusting circuit 200, formed to adjust the offset I_{off} to a minimum, preferably to zero. *Id.* at 6:15–19. Adjusting circuit 200 includes two current sources, controlled current source 210 and constant current source 220. *Id.* at 6:19–21.

Controlled current source 210 generates a controlled current I_1 at its output. *Id.* at 6:42–43. In the embodiment of Figure 2a, controlled current source 210 is connected to NMOS output transistor 126 of the second current mirror in input current amplifier 100 via terminal 204, so the output of NMOS output transistor 126 and output current I_1 of controlled current source 210 are summed in the terminal node. *Id.* at 6:43–52; *see id.* at 1:44–45, 3:60–4:3. In other embodiments, controlled current source is connected to output 102 of input amplifier 100. *Id.* at 6:52–54; *see id.* at 1:44–45, 3:60–4:3. Generally the specification describes that the output I_1 of the controlled current source has an opposite current direction than the output of the current amplifier and is “connected to the current amplifier for impressing the output current of the controlled current source in the current amplifier.” *Id.* at 1:41–43; *see id.* at code (57), 3:23–34, 3:65–4:3, 7:39–41. In other embodiments, controlled current source is connected to current input 101 of current amplifier 100. *Id.* at 1:45–47, 3:35–40, 7:20–23, 7:24–27, 7:31–35.

The specification includes a diagram describing the values to be used for the control signals of switching devices S1, S2, and S3 of the adjusting circuit of Figure 2a, which is shown in Figure 2b, reproduced below.

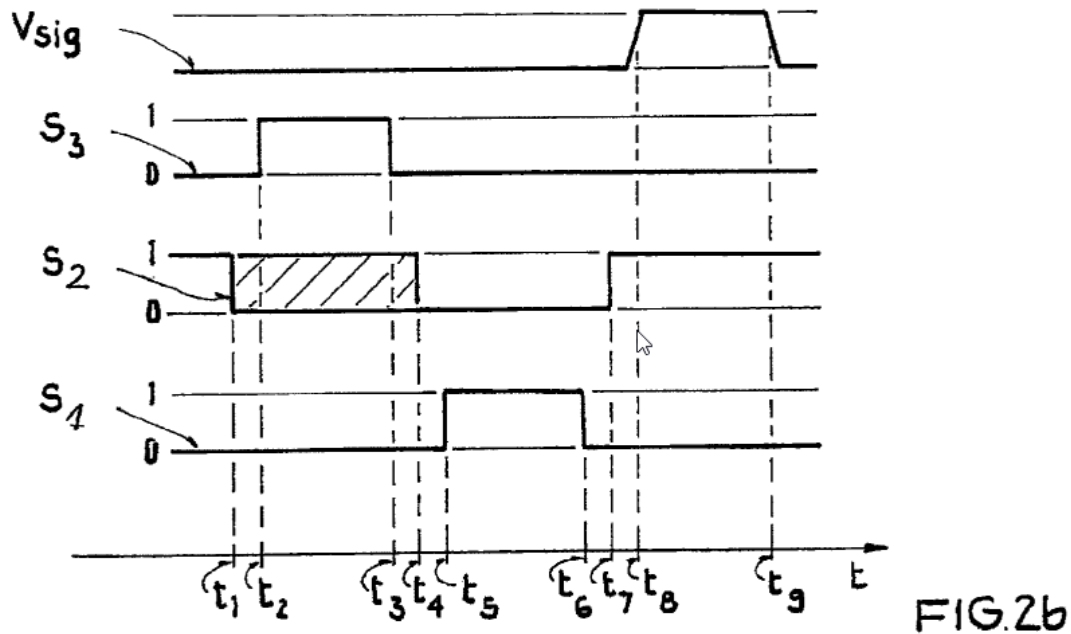


Figure 2b describes the state of the switches S1, S2, and S3 at time points t_1 through t_9 , with where 1 indicates a closed position and 0 indicating an open position. *Id.* at 8:22–9:3. As described with respect to Figure 2b, capacitor 212 is charged between time points t_5 and t_6 , with the switches S2 and S3 in the open position and switch S1 in the closed position. *Id.* at 8:31–40.

When this occurs, the capacitor 212 is connected via first switching device S1 to output 102 of input current amplifier 100, and is charged until the steady state is obtained that can be used to offset the amplifier-intrinsic offset. *Id.* at 8:1–12, 8:38–40.

Constant current source 220 generates a constant current I_2 , which is, in the embodiment of Figure 2a, connected to PMOS output transistor 124 of the first current mirror, so the output current of output transistor 124 is summed with the output of constant current source 220, and connected to

output 102 of current amplifier 100 via PMOS output transistor 124. *Id.* at 6:24–41.

E. Illustrative Claims

Petitioner challenges claims 1–32. Of these, claims 1 and 17 are independent. Claims 1 and 17 are reproduced below with bracketed notations inserted for reference, corresponding to notations used in the Petition.

1. A circuit comprising:
 - [1a] a current amplifier; and
 - [1b] an adjusting circuit configured to correct an offset of an output current of the current amplifier, [1c] the adjusting circuit having a controlled current source and a first switching device,
 - [1d] wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier,
 - [1e] wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop,
 - [1f] wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element,
 - [1g] wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current, and
 - [1h] wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current.

17. A method for correcting an offset of an output current of a current amplifier of a circuit, the method comprising:

- [17a] connecting a controlled current source to an output of the current amplifier via a first switching device, to form a regulation element of a control loop;
- [17b] regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element; and
- [17c] disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current.

Ex. 1001, 10:13–36, 11:44–57.

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–32 would have been unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 11, 13, 14, 16–22, 27, 29–32	103	Soneda ^{2, 3}
1–6, 8–11, 13, 14, 16–22, 24–27, 29–32	103	Soneda, Kozisek ⁴
7, 23	103	Soneda, Palmisano ⁵
7, 23	103	Soneda, Kozisek, Palmisano
12, 15, ⁶ 28, 31	103	Soneda, Gutzki ⁷
12, 15, 28, 31	103	Soneda, Kozisek, Gutzki

² Soneda, JP 62-171212, published July 28, 1987 (Ex. 1005, original at pp. 12–15, translation at pp. 2–11, affidavit of translator at p. 1 (*see* 37 C.F.R. § 42.63(b))).

³ While the grounds chart provided by Petitioner does not list an obviousness ground based on Soneda alone, Petitioner presents obviousness arguments based on Soneda alone. *See, e.g.*, Pet. 12–33 (using Kozisek only in the alternative in arguments relating to limitations 1e and 1g of claim 1). Arguments with respect to certain dependent claims rely solely on Kozisek in combination with Soneda. *See, e.g.*, Pet. 46–47 (arguing claims 8 and 24 based on obviousness over a combination of Soneda and Kozisek).

⁴ Kozisek et al., US 6,049,246, issued Apr. 11, 2000 (Ex. 1006).

⁵ Palmisano, G., Palumbo, G., & Pennisi, S., CMOS CURRENT AMPLIFIERS (1999) (Ex. 1007).

⁶ While Petitioner’s arguments for claims 15 and 31 appear in the discussion relating to obviousness over Soneda and Kozisek, these claims depend from claims 12 and 28 respectively, which are argued with reference to Soneda, Kozisek, and Gutzki. We assume this was a clerical error.

⁷ Gutzki et al., US 7,405,614 B2, issued July 29, 2008 (Ex. 1008).

II. ANALYSIS

A. *Legal Standards*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner must explain with particularity how the prior art would have rendered the challenged claims unpatentable. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”).

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness,

i.e., secondary considerations.⁸ *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art “would have had a minimum of a Master’s degree in electrical engineering or a similar field, and approximately two years of industry or academic experience designing or analyzing electronic circuits,” where “[a]dditional education could substitute for professional experience, and significant work experience could substitute for formal education.” Pet. 6 (citing Ex. 1003 (Declaration of Laurence W. Nagel, Ph.D.) ¶ 50).

Patent Owner argues that a person having ordinary skill in the art would have had “(1) a bachelor’s degree in electrical engineering or a similar field, and approximately two years of industry or academic experience designing or analyzing analog current and/or voltage amplifiers or (2) a master’s degree or Ph.D. in electrical engineering or an equivalent field, with coursework, thesis, dissertation work, or research experience in analog current and/or voltage amplifiers.” PO Resp. 20 (citing Ex. 2011 (Declaration of Dr. Marc E. Herniter) ¶ 29).

Petitioner’s proposed definition, as compared to Patent Owner’s proposed definition, would require a higher degree of education or substitute work experience for a person who had two years of industry or academic experience. *Compare* Pet. 6, *with* PO Resp. 20. Patent Owner’s proposed definition requires that the industry or academic experience be more specifically related to “analog current or voltage amplifiers.” *Compare*

⁸ Neither party presents evidence or argument on the fourth *Graham* factor. We therefore do not consider that factor in this decision.

Pet. 6, *with* PO Resp. 20. Neither party provides substantive argument as to why its proposed level of skill is correct. *See* Pet. 6; PO Resp. 20.

Based on this record, we apply the Petitioner’s proposal for level of ordinary skill in the art at the time of the invention, which is consistent with the level of ordinary skill in the art at the time of the invention as reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). We note, however, that our determinations on patentability would not change if we accepted Patent Owner’s proposed level of skill.

C. Claim Construction

In the Decision on Institution, we construed limitation 1d, which requires that “an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier.” Ex. 1001, 10:19–22; Inst. Dec. 13–16. While this construction was not requested by the parties, we noted that the parties appeared to have conflicting constructions of limitation 1d. Inst. Dec. 13–14 (citing Pet. 16–20; Paper 6 (Patent Owner’s Preliminary Response), 21, 25–30)). We reviewed the intrinsic evidence, and without providing a complete construction, we noted that, for the purposes of institution, we would construe the limitation to not require the connection of the output of the controlled current source to an internal component of the current amplifier. *Id.* at 14–16.

Patent Owner contends that this claim construction is incorrect as ignoring the plain language of the claim. PO Resp. 33–44; PO Sur-reply 2–6. For its part, Petitioner adopts and argues for the preliminary construction in the Decision on Institution. Pet. Reply 2–5.

Because our decision here does not require the resolution of this controversy or the construction of any other claim terms, we do not construe

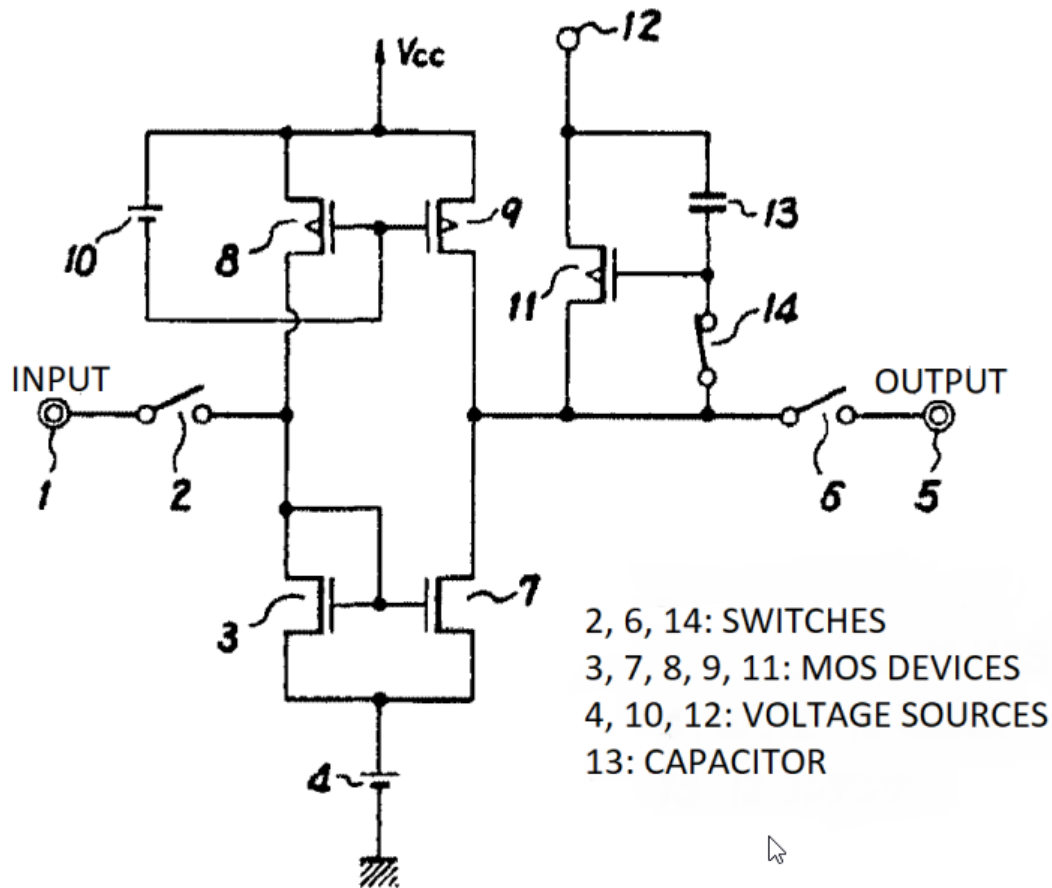
limitation 1d or any other terms in this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Claim 1, Obviousness over Soneda

Petitioner argues that claim 1 would have been obvious over Soneda. Pet. 12–23, 27–30, 32–33. Patent Owner presents several arguments relating to these contentions. PO Resp. 44–56; PO Sur-reply 7–16.

1. Soneda

Soneda describes a current circuit that includes a current amplifier. Ex. 1005, 57–58, Fig. 5. Soneda provides a circuit in which an offset current of the current amplified is eliminated. *Id.* at 58–59. Soneda’s Figure 1, reproduced below, illustrates a current amplifier in a circuit that allows for its output to be unaffected by offset current.



CONNECTION DIAGRAM OF WORKING EXAMPLE
 FIG. 1

The example of Figure 1 includes current amplifier circuitry, including elements 3, 4, and 7–10. *Id.* at 58–59; *see id.* at 57, Fig. 5. Additionally, the example of Figure 1 includes P-type MOS device 11, voltage source 12, capacitor 13, and switch 14. *Id.* at 58.

Soneda describes a blanking interval during which switches 2 and 6 are turned off, and switch 14 is turned on. *Id.* at 59. During this blanking interval, the offset current flows through the device 11 and the capacitor is charged by this offset current. *Id.*

Soneda also describes an operation interval, during which switch 14 is turned off and a current equal to the offset current is supplied from P-type

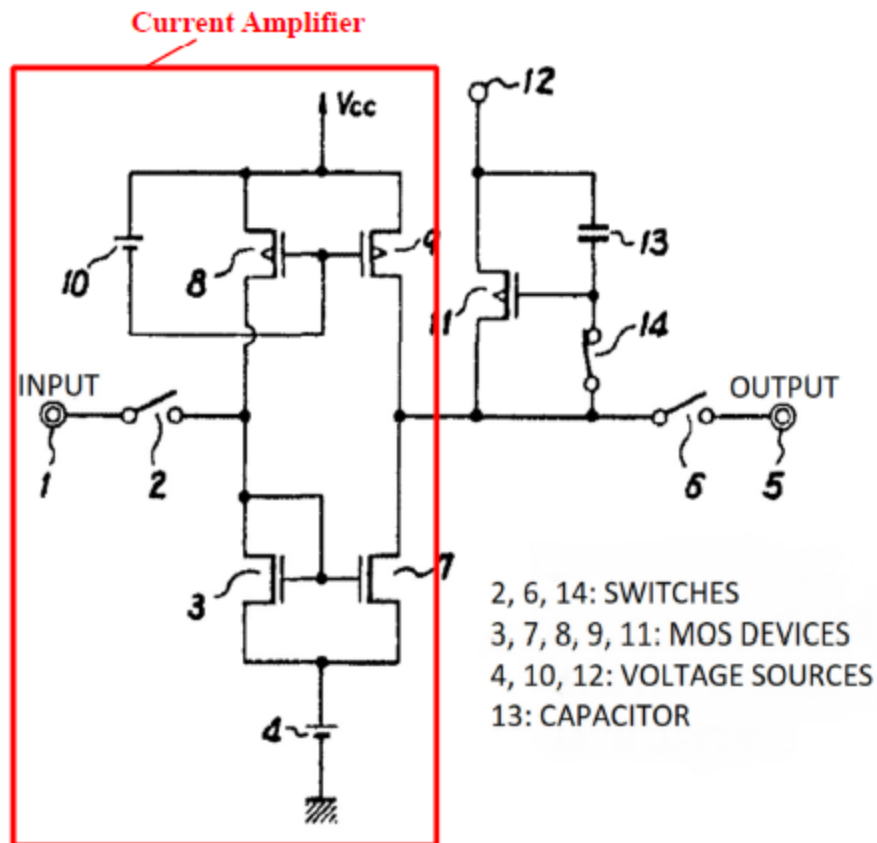
MOS device 11 as “biased by the charging electric potential of the capacitor [13].” *Id.* at 59.

“[A]ccording to this circuit, a current that is equal to the offset current . . . is supplied from the device (11) . . . and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current.” *Id.* at 59.

2. *Claim 1*

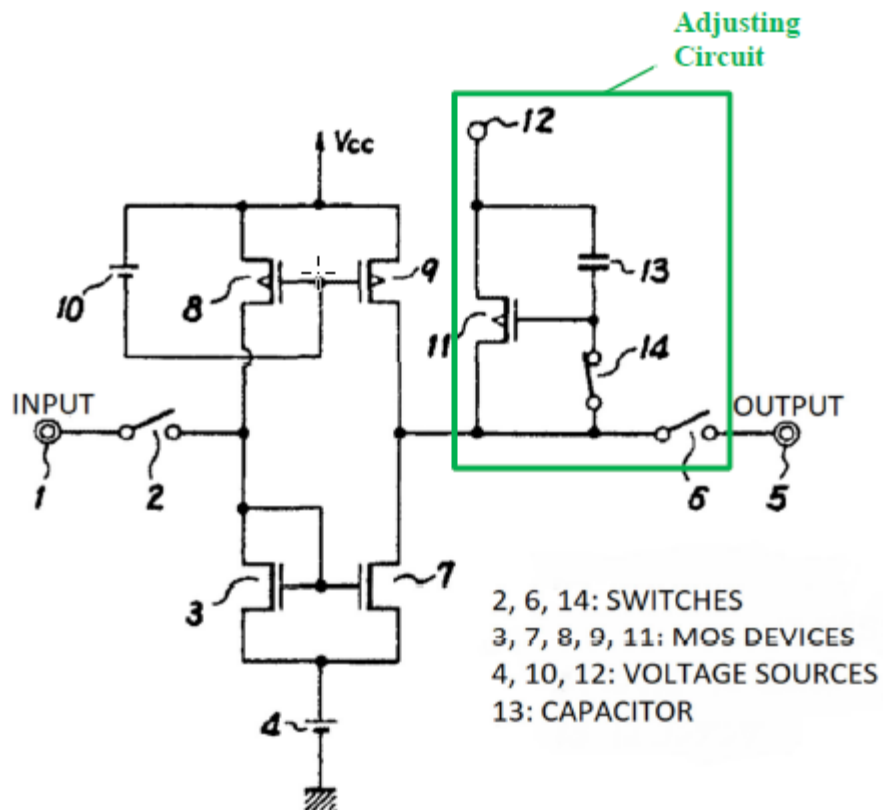
a) Limitations 1a, 1b, 1c, and 1f

We first address Petitioner’s arguments that Soneda teaches or suggests limitations 1a, 1b, 1c, and 1f of claim 1. Petitioner argues that Soneda’s Figure 1 teaches a circuit, and that the circuit comprises a current amplifier as described with reference to Figure 5. Pet. 12–14 (citing Ex. 1005, 57–58, Figs. 1, 5; Ex. 1003 ¶¶ 64–66). Petitioner provides an annotated version of Soneda’s Figure 1, reproduced below, explaining what Petitioner argues is Soneda’s current amplifier, relating this to limitation 1a.



Id. at 14. Petitioner’s annotated Figure 1 shows a red box surrounding elements substantially similar to those in the prior art current amplifier Soneda describes and depicts in Figure 5. *See* Ex. 1005, 57–58, Fig. 5.

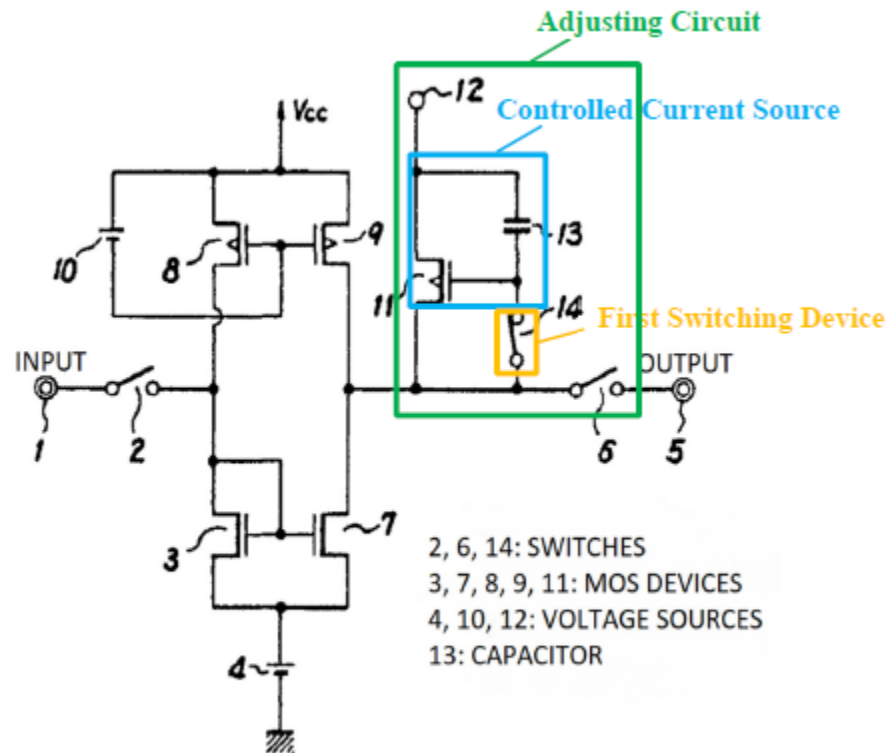
With respect to limitation 1b, Petitioner argues that Soneda’s circuit as shown in Figure 1 includes an adjusting circuit configured to correct an offset of an output current of the current amplifier in Soneda’s circuitry that supplies a current equal to the offset current from Soneda’s P-type MOS device (transistor) 11, and including capacitor 13 and switch 14. Pet. 14–16 (citing Ex. 1005, 59, Fig. 1; Ex. 1003 ¶¶ 67–69). Petitioner provides a second annotated version of Soneda’s Figure 1, reproduced below, to indicate what Petitioner argues is Soneda’s adjusting circuit.



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

Id. at 15. Petitioner's second annotated Figure 1 shows a green box surrounding P-type MOS device 11, voltage source 12, capacitor 13, and switch 14. *See* Ex. 1005, 58–59. Limitation 1c specifies that the adjusting circuit has a controlled current source and a first switching device.

Ex. 1001, 10:16–18. Petitioner argues that transistor 11 and capacitor 13 teach the “controlled current source” of limitation 1c, and that switch 14 teaches the “first switching device” of that limitation. Pet. 16 (citing Ex. 1003 ¶¶ 70–71), as shown in a third annotated version of Figure 1 of Soneda, reproduced below.



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

Id. at 17. Petitioner's third annotated Figure 1 shows a blue box labelled "Controlled Current Source" surrounding P-type MOS device 11 and capacitor 13, and a yellow box labelled "First Switching Device" surrounding switch 14. *Id.*

Petitioner argues that Soneda discloses limitation 1f ("wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element") with reference to these elements. *Id.* at 27. With respect to limitation 1f, Petitioner argues that Soneda teaches an operation interval in which switch 14 is turned off, and that one of ordinary skill would understand that during this interval, the controlled current source acts as a holding element to hold the offset current of the current amplifier. *Id.* at 27–29 (citing Ex. 1005, 58–59; Ex. 1003 ¶¶ 89–92).

b) Limitation 1d

With respect to limitation 1d, requiring that “an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier,” Petitioner cites Soneda’s disclosure that an offset current flows through device 11 and is supplied from device 11. *Id.* at 19 (citing Ex. 1005, 59, Fig. 1; Ex. 1003 ¶ 75). Petitioner additionally cites Soneda’s teaching that the drain of device 11 “is connected to a connection midpoint between [MOS devices] (7) (9).” *Id.* (citing Ex. 1005, 58; Ex. 1003 ¶ 76). Patent Owner disputes this, by arguing that Soneda does not show the production of an output current of the controlled current source “in the current amplifier” as required in limitation 1d. PO Resp. 31–38, 40–49; PO Sur-reply 7–12. Because, as discussed below, we find Petitioner has failed to meet the burden of establishing the unpatentability of claim 1 for other reasons, we do not reach these arguments.

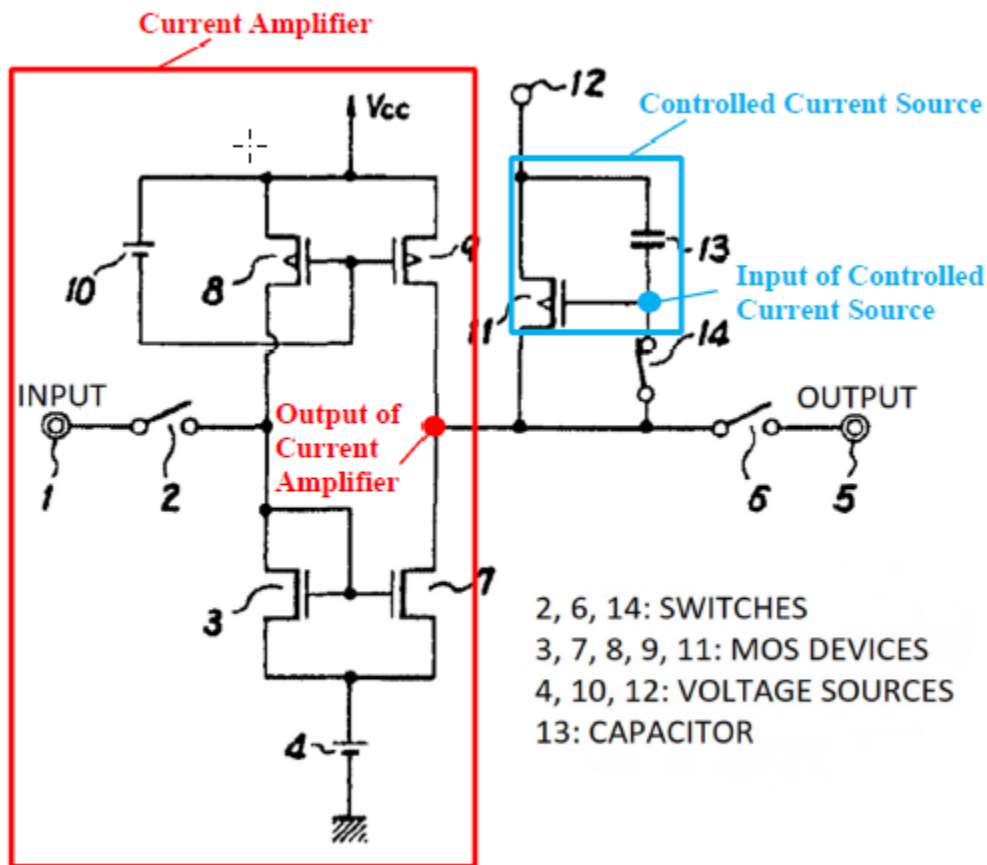
c) Limitations 1e and 1g

(1) Parties’ Positions

Limitation 1e requires that “an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop.” Ex. 1001, 10:23–26. Limitation 1g requires that “the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current.” *Id.* at 10:30–33.

With respect to these two limitations, Petitioner argues that Soneda explains, “during [Soneda’s] blanking interval, the switch 14 (first switching device) is turned on, . . . and the controlled current source and the current

amplifier form a control loop” and that this control loop “is shown in [an annotated version of Soneda’s] Figure 1,” provided in the Petition and reproduced here:



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

Pet. 21–22 (citing Ex. 1005, 58, 59; Ex. 1003 ¶¶ 78, 80). This annotated figure shows the red outline of the asserted current amplifier from an earlier annotated version of Soneda’s Figure 1, the blue outline of the controlled current source from another earlier annotated version of the figure, and includes additional markings of the input of the controlled current source and the output of the current amplifier. *Id.*

In explaining its assertions regarding limitation 1g, Petitioner again references the blanking interval of Soneda, contending that “the controlled

current source (transistor 11 and capacitor 13) acts as a regulation element of the control loop to establish an output current from the controlled current source to be equal to the offset current ΔI_{DC} of the current amplifier.” *Id.* at 30 (citing Ex. 1003 ¶ 94).

Patent Owner argues that “Petitioner fails to identify any control loop” and “Petitioner provides no discussion of what it contends actually constitutes the control loop.” PO Resp. 54–55. Patent Owner discusses possible definitions of a control loop, including describing a feedback control loop as an arrangement in which there is “a closed path with two branches, one direct and the other providing feedback, with one or more mixing points arranged in a manner that an output quantity is maintained within specified parameters.” *Id.* at 51–52 (quoting Ex. 2009, 278; citing Ex. 2010, 422). Patent Owner describes a feedback loop it asserts is present in the Figure 2a embodiment of the ’082 patent. *Id.* at 49–50 (citing Ex. 1001, Fig. 2a; Ex. 2011 ¶¶ 95–99).

In response, Petitioner argues that Patent Owner imposes an (unclaimed) concept of a “classical control loop” on the “control loop” recited in the claim and that Patent Owner improperly faults Petitioner for not showing how Soneda teaches or suggests that “classical control loop.” Pet. Reply 8–9. Petitioner agrees that claim 1 requires a “control loop” and describes similarities between the charging of Soneda’s capacitor to the offset current value during the blanking interval and the charging of capacitor 212 in the Figure 2a embodiment of the ’082 patent, which biases the transistor to generate a current opposed to the offset, which occurs between times t_5 and t_6 . *Id.* at 10–12 (citing Ex. 1001, 7:45–53, 7:58–65, 8:1–21, 9:20–23; Ex. 1005, 58, Ex. 1003 ¶¶ 45, 55). Petitioner argues that “[t]he control loop in Soneda comprises a PMOS device, or transistor, (11)

and a capacitor (13).” *Id.* at 11–12 (citing Ex.1005, 58, Fig. 1; Ex. 1003 ¶ 55). Petitioner argues that this is “the same ‘control loop’ as claimed by claim[] 1 . . . and taught by the ’082 patent’s specification.” *Id.* at 12–13 (citing Ex. 1003 ¶¶ 78–80).

(2) *Analysis*

We agree with Patent Owner that Petitioner has not met the burden of showing how Soneda teaches or suggests limitations 1e and 1g.

As Patent Owner argues, Petitioner has not clearly asserted or met its burden to prove what in Soneda teaches or suggests the “control loop” of limitations 1e and 1g. PO Resp. 53–55. In the Petition, Petitioner argues that “the controlled current source and the current amplifier form a control loop” and describes this as “shown” in an annotated Figure 1 of Soneda. Pet. 21. But this annotated figure does not include any annotations indicating what elements are in the control loop, and no loop can be seen formed by the identified controlled current source and the current amplifier in this annotated figure. In its Reply, Petitioner shifts to an argument that “[t]he control loop in *Soneda* comprises a PMOS device, or transistor, (11) and a capacitor (13).” Pet. Reply 11. We recognize that by using the term “comprising,” which in a claim-interpretation context has an open-ended nature, Petitioner may not be arguing that only these two elements of Soneda are included in the control loop. However, Petitioner still does not make clear what it argues is a control loop. While Petitioner protests that “Patent Owner wrongly faults the Petition for not mapping the teaching of *Soneda* . . . to what it calls the ‘classical control loop,’” we agree with Patent Owner that Petitioner, which has the burden of showing with particularity why the challenged claims are unpatentable, has not identified anything in Soneda

that teaches a control loop under any definition. Pet. Reply 8; PO Sur-reply 12.

Additionally, with respect to the identification of the transistor and capacitor of the controlled current source as the control loop (Pet. Reply 11), as Patent Owner notes, claim 1 requires (limitation 1g) that the controlled current source at least at times is “acting as a regulation element in the control loop” (Ex. 1001, 10:30–31). PO Resp. 52. An identification of elements within the controlled current source as the only elements in the control loop is not consistent with the requirement that the controlled current source acts as a regulation element in control loop. *Id.* at 55; PO Sur-reply 15–16. Rather, an argument that the controlled current source and the current amplifier form a control loop (Pet. 21) appears more consistent with this limitation, however it is not clearly described or supported with evidence by Petitioner. Petitioner argues that the ’082 patent discloses that its control loop is formed when the first switching device S1 closes and the output of the adjusting circuit is connected to the input of the controlled current source and the capacitor 212 is charged to a specific current. Pet. Reply 10–11 (citing Ex. 1001, 7:45–53, 7:58–65, 8:1–21, Fig. 2a). Petitioner contends that Soneda teaches “this same circuit and method for cancelling offset.” *Id.* at 11–12 (citing Ex. 1005, 58, Fig. 1). But, as Patent Owner shows, the method described in the ’082 patent includes the controlled current source 210 acting as a regulation element in a loop that includes additional elements, including elements of the current amplifier. PO Resp. 49–50. This distinction is not persuasively addressed by Petitioner or its identification of only elements of Soneda’s transistor 11 and capacitor 13 as included in the control loop. *See* Pet. Reply 9–10 (discussing the “stage of operation” in which a capacitor is charged until a steady state is

achieved, as opposed to elements of a control loop formed by connecting an input of the controlled current source to an output of the current amplifier).

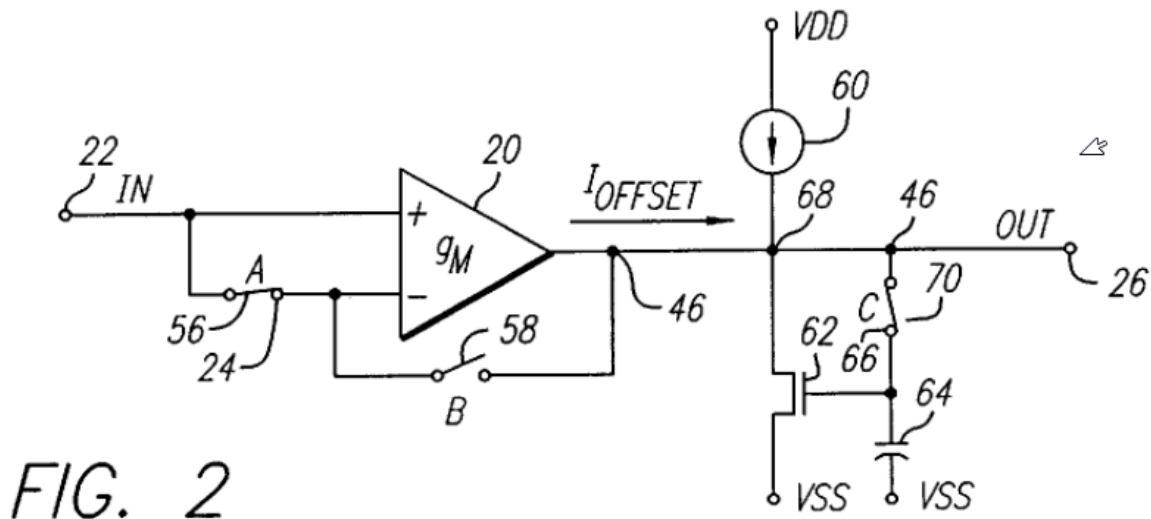
For these reasons, we conclude that Petitioner has not met its burden to prove by a preponderance of the evidence that Soneda teaches the elements of claim 1.

E. Claim 1, Obviousness over Soneda and Kozisek

Petitioner additionally argues that claim 1 would have been obvious over a combination of Soneda and Kozisek. Pet. 12–37. Patent Owner presents several arguments relating to these contentions. PO Resp. 44–56, 60–71; PO Sur-reply 7–17, 20–29.

1. Kozisek

Kozisek describes an adjusting circuit for use with a differential amplifier to correct for an offset current. Ex. 1003, code (57), 1:5–10. This circuit supplies an offset current having a magnitude equal and opposite to the output offset current of an amplifier. *Id.* at 5:52–54. Figure 2, reproduced below, is a schematic drawing of a circuit including a differential amplifier and circuitry to supply an offset cancellation current to the output of that differential amplifier. *Id.* at 4:20–23, 5:27–37.



In Figure 2, amplifier 20 has an output including a current offset, and a current copier circuit including current source 60, transistor 62, and storage capacitor 66 functions to source current or sink current in order to offset that offset current. *Id.* at 5:52–63. Current source 60 sources a fixed amount of current. *Id.* at 6:1. Transistor 62 is biased to sink an amount of current that is greater than, less than, or equal to the amount of current sourced by current source 60, in order to eliminate the current offset. *Id.* at 5:30–37, 6:6–10, 6:22–29. The degree to which transistor 62 conducts current is controlled by storage capacitor 62. *Id.* at 6:6–10.

In a first phase, which Kozisek terms “cancellation mode” or “programming mode,” first switch 56 is closed to null the input to the amplifier 20, second switch 58 is opened to disconnect the feedback loop, and third switch 70 is closed to allow the current copier circuit to sense and null out any output current offset at output node 46. *Id.* at 6:16–22, 6:38–39. In this way, the voltage at node 46 and thus at first terminal 66, will drift until transistor 62 is biased to supply a current (along with current source 60) exactly balances any output offset current from amplifier 20. *Id.* at 6:23–31.

After this mode is performed, circuitry is switched to the normal mode of operation by opening third switch 70, opening first switch 56, and closing second switch 58. *Id.* at 6:39–43. The normal operation of amplifier 20 can occur, and the offset cancellation current set in the prior mode continues to be supplied by transistor 62 and the rest of the current copier circuitry. *Id.* at 6:12–15, 6:47–53.

2. *Claim 1*

Petitioner’s arguments with respect to the obviousness of claim 1 over Soneda and Kozisek are substantially similar, with respect to the issues

discussed in our analysis above, to the arguments made with respect to Soneda alone, and Petitioner argues that Kozisek's controlled current source and Soneda's are "substantially similar." Pet. 23–24, 31–32; Pet. Reply 12–13.

Patent Owner argues, as it did with respect to Soneda alone, that Petitioner does not identify a control or feedback loop in Kozisek. PO Resp. 55–56; PO Sur-reply 16–17.

For the same reasons discussed with respect to the obviousness of claim 1 over Soneda alone, we conclude that Petitioner has not met its burden to prove by a preponderance of the evidence that a combination of Soneda and Kozisek teach the elements of claim 1.

F. Additional Claims / Grounds

With respect to the obviousness of independent claim 17, the Petition argues the obviousness with reference to the arguments regarding claim 1, including specifically the arguments relating to limitations 1e and 1g. Pet. 34–37. In arguments relating to a claim construction dispute, Petitioner specifically argues that limitation 17b of claim 17 is co-extensive with limitations 1d and 1e of claim 1. Pet. Reply 5–6.

With respect to the obviousness of dependent claims 2–16 and 18–32, for each of the grounds asserted against these claims, Petitioner's argument relies on its arguments with respect to the obviousness of claim 1 or claim 17 over Soneda or Soneda and Kozisek. Pet. 37–81. None of the additional arguments or references include any additional details relating to the subject matter of limitations 1e and 1g. Therefore, for the same reasons discussed with respect to the obviousness of claim 1 over Soneda, we conclude that Petitioner has not met its burden to prove by a preponderance of the

evidence that claim 17 or dependent claims 2–16 and 18–32 are obvious over the asserted prior art.

III. CONCLUSION

Petitioner has not shown, by a preponderance of the evidence, that any of claims 1–32 of the '082 patent are unpatentable.

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–6, 11, 13, 14, 16–22, 27, 29– 32	103	Soneda		1–6, 11, 13, 14, 16–22, 27, 29–32
1–6, 8– 11, 13, 14, 16– 22, 24– 27, 29– 32	103	Soneda, Kozisek		1–6, 8–11, 13, 14, 16–22, 24–27, 29–32
7, 23	103	Soneda, Palmisano		7, 23
7, 23	103	Soneda, Kozisek, Palmisano		7, 23
12, 15, 28, 31	103	Soneda, Gutzki		12, 15, 28, 31
12, 15, 28, 31	103	Soneda, Kozisek, Gutzki		12, 15, 28, 31
Overall Outcome				1–32

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–32 of the '082 patent are not unpatentable;
and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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