

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., and
GLOBALFOUNDRIES U.S. 2 LLC,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES, LLC,
Patent Owner.

IPR2022-00763
Patent 6,291,861 B1

Before CHRISTOPHER M. KAISER, JULIA HEANEY,
and BRIAN D. RANGE, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

INTRODUCTION

A. Background

GlobalFoundries Inc., GlobalFoundries U.S. Inc., and GlobalFoundries U.S. 2 LLC (collectively, “Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–12, 16–20, 22, and 24 of U.S. Patent No. 6,291,861 B1 (Ex. 1001, “the ’861 patent”). Katana Silicon Technologies LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a) (2020). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

After considering the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail with respect to at least one challenged claim. Accordingly, we do not institute an *inter partes* review of any challenged claim.

B. Related Matters

The parties identify two related matters. First, the ’861 patent has been asserted in *Katana Silicon Technologies LLC v. GlobalFoundries Inc. et al.*, No. 6-22-cv-00191 (W.D. Tex.). Pet. 8; Paper 4, 1. Second, Patent Owner notes that IPR2022-01083 involves the same parties. Paper 4, 1.

C. The Asserted Grounds of Unpatentability

Petitioner contends that claims 1–12, 16–20, 22, and 24 of the ’861 patent are unpatentable based on the following grounds (Pet. 13–94):¹

Claims Challenged	35 U.S.C. §	References/Basis
1, 3–7, 9–12, 17, 18	103(a)	JP848 ²
2, 4	103(a)	JP848, Watanabe ³
8, 9, 16	103(a)	JP848, 1994 NTRS ⁴
17	103(a)	JP848, JP406 ⁵
19, 20, 22	103(a)	JP533, ⁶ JP406
24	103(a)	JP533, JP406, JP436 ⁷

D. The ’861 Patent

The ’861 patent, titled “Semiconductor Device and Method for Producing the Same,” issued on September 18, 2001. Ex. 1001, codes (45), (54). It “relates to a semiconductor device in which a source/drain region occupies a reduced area so as to decrease the parasitic capacitance and parasitic resistance of the source/drain region.” *Id.* at 1:7–11.

¹ Petitioner also relies on a declaration from Jack C. Lee, Ph.D. Ex. 1003.

² JP H03-74848, published Mar. 29, 1991 (Ex. 1006, certified English translation at Ex. 1005).

³ US 5,723,379, issued Mar. 3, 1998 (Ex. 1007).

⁴ Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, 1994 (Ex. 1025).

⁵ JP H05-218406, published Aug. 27, 1993 (Ex. 1013, certified English translation at Ex. 1012).

⁶ JP H03-27533, published Feb. 5, 1991 (Ex. 1011, certified English translation at Ex. 1010).

⁷ JP H03-268436, published Nov. 29, 1991 (Ex. 1015, certified English translation at Ex. 1014).

According to the patent, “smaller insulation gate type field effect transistors (FETs) become more susceptible to [various] problems.” *Id.* at 1:14–20. “One method for solving such problems has been to reduce the junction depth of the source/drain regions adjoining a channel region of a transistor.” *Id.* at 1:21–23. This “can be realized by, for example, a structure in which source/drain regions (stacked diffusion layers) are stacked on both sides of a gate electrode.” *Id.* at 1:23–27. When this is done, however, “it is difficult to reduce the area occupied by the source/drain regions.” *Id.* at 1:28–2:10.

The ’861 patent seeks to solve this problem by describing a “semiconductor device” with “a gate oxide film, a source/drain region, and an electrode which is electrically coupled to the source/drain region,” with “the active region [being] in contact with the gate oxide film at a first face, a portion of the source/drain regions being located above the first face,” and with “the electrode [being] in contact with the source/drain region at a second face, the second face constituting an angle with respect to the first face.” *Id.* at 2:13–23.

E. Illustrative Claim

Claims 1–12, 16–20, 22, and 24 of the ’861 patent are challenged. Claims 1 and 19 are independent and illustrative. We reproduce them below:

1. A semiconductor device comprising a device separation region and an active region,
the semiconductor device including a gate having a gate dielectric film and a side wall spacer, a source/drain, and a contact which is electrically coupled to the source/drain,

wherein the active region is in contact with the gate dielectric film at a surface of the active region coincident with a first surface, a portion of the source/drain being located above the first surface; and

wherein the contact is in contact with the source/drain at a source/drain surface defining a second surface, the second surface passing through a segment connecting a first point on the source/drain surface in contact with the device separation region to a second point on an edge of the source/drain surface in contact with the side wall spacer, constituting an angle with respect to the first surface.

Ex. 1001, 26:62–27:12.

19. A semiconductor device, comprising:

a gate dielectric film provided beneath a gate electrode on a substrate, said gate electrode and gate dielectric film sandwiched by a pair of vertical insulating film walls, said gate dielectric film and gate electrode having an equal width as viewed in a cross-sectional plane; and

a pair of source/drains, each of the source/drains having a vertical face that meets a corresponding vertical insulating film wall so as to sandwich said gate dielectric film, gate electrode, and vertical insulating film walls therebetween, and having a first continuous angular face that slopes downward from a junction with its vertical face and corresponding vertical insulating film wall to a corresponding device separation region.

Ex. 1001, 28:32–45.

ANALYSIS

A. Claim Construction

Petitioner argues that no claim terms require express construction.

Pet. 12. Patent Owner also does not propose express construction of any term. Prelim. Resp. 16–17.

Id. at 17, Fig. 7(e). Figure 7(e) depicts an embodiment of JP848's semiconductor device. *Id.* at 8. The device is built on "silicon substrate" 1, and it includes "source and drain diffusion layers of a low impurity concentration" 9, "silicon oxide film" 6 surrounding "gate electrode" 5, "sidewall spacer" 33 above layers 9 and next to film 6, "interlayer insulating film" 12 covering most of the device, and "metal wiring layer" 13 in contact with spacer 33. *Id.* at 4, 9, 16, Fig. 7(e).

2. Analysis

Among other limitations, claim 1 of the '861 patent recites "a contact which is electrically coupled to the source/drain" that "is in contact with the source/drain at a source/drain surface." Ex. 1001, 26:62–27:12. Claims 2–12 and 16–18 all depend directly or indirectly from claim 1. *Id.* at 27:13–28:31. Accordingly, all of the claims Petitioner challenges as obvious over combinations of prior art based on JP848 incorporate the limitations of claim 1. 37 C.F.R. § 1.75(c). Therefore, to show the obviousness of any of these claims, Petitioner must show that the asserted prior art teaches or suggests "a contact which is electrically coupled to the source/drain" that "is in contact with the source/drain at a source/drain surface."

In each of the grounds based on JP848, Petitioner relies on element 13 of Figure 7(e) of JP848 to teach the "contact" of claim 1. Pet. 24–25, 29–30, 45, 55–65, 67–68. Petitioner also relies on the combination of elements 9 and 33 of Figure 7(e) of JP848 to teach the "source/drain" of claim 1. *Id.* at 22–24, 29–30, 45, 55–65, 67–68. In particular, Petitioner argues that "the lower portion of contact 13 is electrically coupled to the source/drain 33, 9" and that "contact 13 is formed over the curved sidewall surface of the

polysilicon layer 33 of the source/drain, and therefore it is ‘*in contact with*’ [the source/drain] as claimed.” *Id.* at 24–25, 29–30.

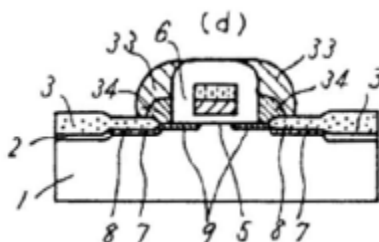
On the present record, we are not persuaded that Petitioner has shown sufficiently that element 33 is part of the source/drain region of JP848. Accordingly, we are not persuaded that Petitioner has shown sufficiently that JP848 teaches a contact that is in contact with a source/drain region.

We note first that JP848 describes element 9 of Figure 7(e) as a “source and drain diffusion layer[]” or as a “low-concentration impurity layer.” Ex. 1005, 4, 12, 13. In contrast, element 33 is described as a “sidewall spacer . . . of polycrystalline silicon” or as “[h]igh-concentration sidewall wiring.” *Id.* at 9, 16. Thus, elements 9 and 33 are described as having both differing purposes (“source and drain diffusion layer” vs. “sidewall spacer”) and differing impurity concentrations (“low-concentration” vs. “[h]igh-concentration”).

Petitioner argues that, despite these differences, JP848 teaches that elements 9 and 33 are both part of the source and drain. Pet. 23–24. Specifically, Petitioner argues that “JP848 discloses that the semiconductor device includes ‘[**layer**] **33 of polycrystalline silicon** [that] . . . increas[es] the effective length of the low-concentration layers of the **source and the drain.**’” *Id.* at 23 (quoting Ex. 1005, 9) (alterations and emphases in original).

But this quotation elides language present in JP848 that changes the meaning significantly. Contrary to Petitioner’s argument that layer 33 “increas[es] the effective length of the low-concentration layers of the source and the drain,” *id.* (emphasis removed), JP848 states that, when “sidewall spacer 33 of polycrystalline silicon has a varying impurity

concentration” due to “low-concentration portion 34 [having been] formed,” the varying impurity concentration itself, not sidewall spacer 33, “increas[es] the effective length of the low-concentration layers of the source and the drain.” Ex. 1005, 9. JP848 illustrates an embodiment with such “varying impurity concentration” in Figure 7(d), reproduced below:



Id. at 9, 16, Fig. 7(d). Figure 7(d) depicts an embodiment of the invention of JP848. *Id.* The device in Figure 7(d) is similar to that in Figure 7(e), but Figure 7(d) depicts an additional layer interposed between “source and drain diffusion layers of a low impurity concentration” 9 and “sidewall spacer” 33. *Id.* at 4, 9, 16, Fig. 7(d). This additional layer is labeled as element 34, which is described as “low-concentration portion” or “[l]ow-concentration sidewall wiring.” *Id.* at 9, 16, Fig. 7(d).

Thus, some embodiments of the device disclosed in JP848, such as the embodiment depicted in Figure 7(e), have layers 9 and 33 that are in contact with one another, while other embodiments, such as the one depicted in Figure 7(d), have an additional layer 34 between layers 9 and 33. When this additional layer is present, the “varying impurity concentration” across the combination of layers 33 and 34 “increas[es] the effective length of the low-concentration layers of the source and the drain.” *Id.* at 9. In a device with layer 34 present, therefore, there might be a sense in which the source and drain regions extend some distance above layer 9 of JP848. It is not clear, at least without some additional explanation, whether that extension above

layer 9 reaches to the furthest extent of layer 33, or whether it reaches only to the interface between layers 33 and 34, or whether it extends some other distance. Petitioner does not offer any explanation for why we should choose any of these options over any of the others. Pet. 21–25.

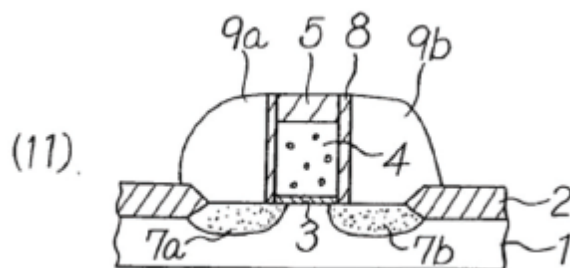
More importantly, JP 848 makes clear that the extension of the source and drain regions above layer 9—however far that extension is—occurs only when layer 34 is present. Ex. 1005, 9. Layer 34 is present in the embodiment depicted in Figure 7(d), but not in the embodiments depicted in Figures 7(c) and 7(e). *Id.* at 16, Figs. 7(c), 7(e). Petitioner relies on Figures 7(c) and 7(e), not on Figure 7(d), to teach or suggest the “contact which is electrically coupled to the source/drain” that “is in contact with the source/drain at a source/drain surface” of the claims of the ’861 patent. Pet. 14–68. Petitioner does not explain why, in light of the disclosure in JP 848 of a benefit exhibited only in the presence of layer 34, a person of ordinary skill in the art would have understood the benefit in question to be exhibited regardless of the absence of layer 34. *Id.* Accordingly, we are not persuaded that Petitioner has shown sufficiently that JP 848 teaches or suggests a contact that is in contact with a source/drain region, as recited in the challenged claims.

C. Asserted Obviousness Based on JP533

Petitioner argues that claims 19, 20, and 22 of the ’861 patent would have been obvious over the combination of JP 533 and JP 406 and that claim 24 would have been obvious over the combination of JP 533, JP 406, and JP 436. Pet. 69–94. In each case, Patent Owner disagrees. Prelim. Resp. 33–40.

1. JP533

JP533 “relates to a semiconductor device and its manufacturing method wherein a gate electrode is formed – with an interposing gate insulating film – between a source region and a drain region formed on a semiconductor substrate.” Ex. 1010, 2. Figure 2(11) of JP533, reproduced below, depicts one embodiment of the invention of JP533:



Id. at 9, Fig. 2(11). Figure 2(11) depicts an embodiment of JP533’s semiconductor device. *Id.* at 5–6. The device is built on “silicon semiconductor substrate” 1, and it includes “source region” 7a, “drain region” 7b, “oxide film” 8 (also referred to as “insulating film” 8), “gate electrode” 4, “source electrode” 9a, and “drain electrode” 9b. *Id.* Electrodes 9a and 9b are located generally above and in contact with the upper surfaces of regions 7a and 7b, respectively, and each has a vertical surface in contact with a portion of film 8. *Id.* at 9, Fig. 2(11).

2. Analysis

Among other limitations, claim 19 of the ’861 patent recites “a pair of source/drains, each of the source/drains having a vertical face that meets a corresponding vertical insulating film wall.” Ex. 1001, 28:32–45. Claims 20, 22, and 24 all depend directly or indirectly from claim 19. *Id.* at 28:46–29:7. Accordingly, all of the claims Petitioner challenges as obvious over combinations of prior art based on JP533 incorporate the

limitations of claim 19. 37 C.F.R. § 1.75(c). Therefore, to show the obviousness of any of these claims, Petitioner must show that the asserted prior art teaches or suggests “a pair of source/drains, each of the source/drains having a vertical face that meets a corresponding vertical insulating film wall.”

In each of the grounds based on JP533, Petitioner relies on element 8 of Figure 2(11) of JP533 to teach the “vertical insulating film wall” of claim 19. Pet. 77, 89. Petitioner also relies on the combination of elements 7a, 7b, 9a, and 9b of Figure 2(11) of JP533 to teach the “pair of source/drains” of claim 1. *Id.* at 75–77, 89. In particular, Petitioner argues that “the source electrode 9a and drain electrode 9b are doped polysilicon” and that, therefore, “JP533 discloses a source region 7a, 9a and a drain region 7b, 9b.” *Id.* at 76–77. Because “JP533’s source/drain regions 9a, 9b, have a vertical face that meets a corresponding vertical insulating film wall 8,” Petitioner argues that JP533 teaches the limitation of the challenged claims requiring “each of the source/drains [to have] a vertical face that meets a corresponding vertical insulating film wall.” *Id.* at 77.

On the present record, we are not persuaded that Petitioner has shown sufficiently that elements 9a and 9b are part of the source and drain regions of JP533. Accordingly, we are not persuaded that Petitioner has shown sufficiently that JP533 teaches “a pair of source/drains” that each have “a vertical face that meets a corresponding vertical insulating film wall.” Ex. 1001, 28:32–45.

We note first that JP533 refers only to regions 7a and 7b as the “source region” and “drain region.” Ex. 1010, 5–6, 9, Fig. 2(11). Regions 9a and 9b are described as the “source electrode” and “drain electrode.” *Id.*

at 5. In addition, the source and drain regions are made from different materials than the source and drain electrodes. The source and drain regions are formed when “impurities are introduced into the surface of semiconductor substrate 1 by ion implantation,” which Petitioner argues is “monocrystalline silicon.” Pet. 75; Ex. 1010, 5. In contrast, the electrodes are formed when “metal layer 9,” which is made of tungsten silicide, aluminum, or “doped polycrystalline silicon,” “is anisotropically etched.” Ex. 1010, 6. This gives the source and drain regions different electrical properties from the electrodes. The source and drain regions are “semiconductor[s],” but the electrodes are “conductive.” *Id.*

Despite these differences, Petitioner argues that the source and drain electrodes of JP533 are, respectively, part of the source and the drain merely because they “are doped polysilicon.” Pet. 76–77. Similarly, Petitioner’s declarant Dr. Lee testifies that “JP533’s device includes a pair of source drain regions 7a, 9a and 7b, 9b,” with no explanation other than “the source electrode 9a and drain electrode 9b are doped polysilicon.” Ex. 1003

¶¶ 233–235. Other than this testimony and the portions of JP533 discussed above, Petitioner does not cite any evidence or explanation to support its argument that a person of ordinary skill in the art would have considered regions 9a and 9b to be part of JP533’s source and drain. Given the differences between the source and drain regions of JP533 and the source and drain electrodes of JP533, Petitioner has not shown sufficiently that a person of ordinary skill in the art would have considered 9a and 9b to be part of JP533’s source and drain.

Accordingly, we are not persuaded that Petitioner has shown sufficiently that JP533 teaches a pair of source/drains that each have a

vertical face that meets a corresponding vertical insulating film wall, as recited in the challenged claims.

CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we determine that Petitioner has not shown a reasonable likelihood that it will prevail in showing that at least one of the challenged claims is unpatentable. Accordingly, we do not institute an *inter partes* review of any challenged claim based on any ground asserted in the Petition.

ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition is denied, and no *inter partes* review is instituted.

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