

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WOLFSPEED, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00854
Patent 8,035,112 B1

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314; 37 C.F.R. § 42.107(e)

I. INTRODUCTION

STMicroelectronics, Inc. (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–3, 6, 7, and 10–16 (“the challenged claims”) of U.S. Patent No. 8,035,112 B1 (Ex. 1001, “the ’112 patent”). The Trustees of Purdue University (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”) to the Petition.

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” For the reasons discussed below, we decline to institute *inter partes* review.

A. Related Proceedings

The parties identify *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.) and *The Trustees of Purdue University v. STMicroelectronics N.V. and STMicroelectronics, Inc.*, No. 6:21-CV-00727 (W.D. Tex.) as related matters. Pet. 3; Paper 4, 1. The parties also identify IPR2022-00724, involving the ’112 patent, as a related matter. *Id.* In addition, Petitioner identifies IPR2022-00252¹ (involving US Patent No.

¹ On June 22, 2022, the Board entered a decision denying institution of *inter partes* review in this proceeding. IPR2022-00252, Paper 13. Petitioner subsequently filed a request for rehearing of that decision. IPR 2022-00252, Paper 14.

7,498,633 B2) as a related matter and Patent Owner identifies IPR2022-00309² (involving the '112 patent) as a related matter. *Id.*

B. Real Parties-In-Interest

Petitioner identifies itself as a real party-in-interest. Pet. 3. Patent Owner identifies itself and the Purdue Research Foundation as real parties-in-interest. Paper 4, 1.

C. The '112 Patent

The '112 patent “relates generally to semiconductor field effect transistors, and more particularly to field effect transistors having self-aligned source contacts.” Ex. 1001, 1:21–23. The '112 patent explains that “[t]he metal oxide semiconductor field effect transistor (MOSFET) is a device used to amplify or switch electronic signals” and “[p]ower MOSFETs are well known for their ability to carry large currents in the on-state while withstanding large breakdown voltages in the off-state.” *Id.* at 1:24–28. According to the '112 patent, misalignment can occur during fabrication of a conventional double-diffused MOSFET (“DMOSFET”), which can cause a reduction in the functional area of a source contact, which in turn increases source resistance and degrades performance. *Id.* at 2:7–18.

The '112 patent describes high voltage power MOSFETs “with self-aligned source contacts and a method for making the same.” *Id.* at 2:24–26. Figure 3 of the '112 patent, reproduced below, depicts a cross-sectional view of cell region 20 of DMOSFET 21. *Id.* at 2:49–50, 3:60–62.

² On September 29, 2022, the Board entered a decision granting Patent Owner’s request for adverse judgement in IPR2022-00309. *See* IPR2022-00309, Paper 18.

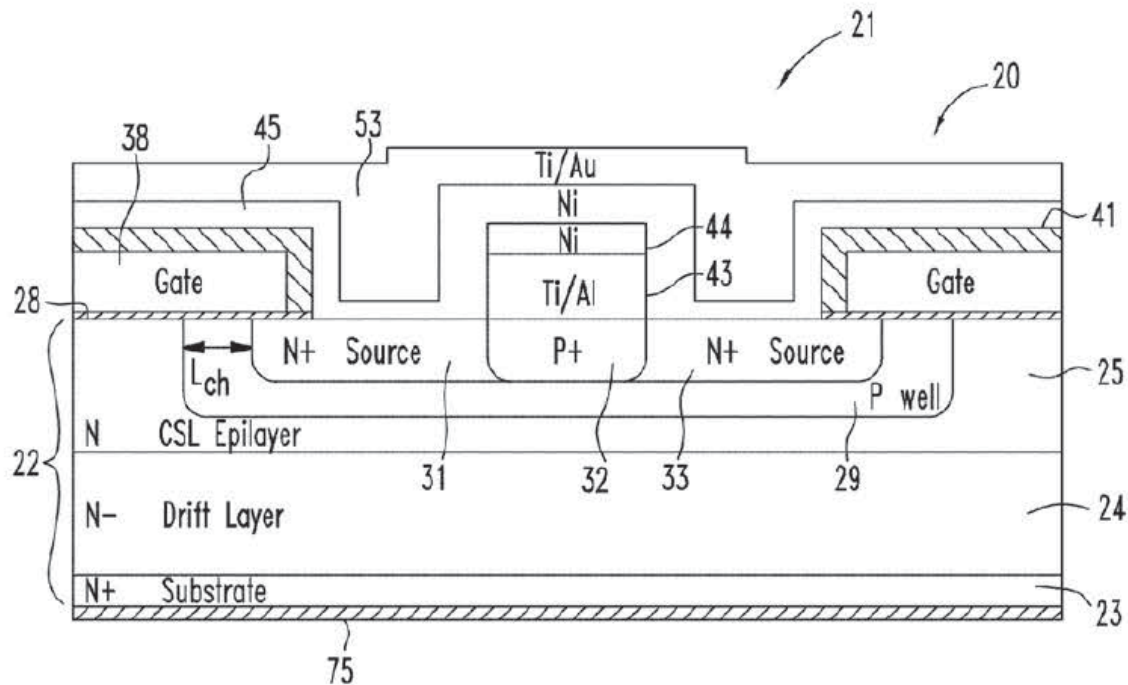


FIG. 3

DMOSFET 21 includes substrate 23 and “a number of semiconductor layers and implants formed on or in the substrate 23,” collectively referred to as substrate body 22. *Id.* at 4:8–11. The ’112 patent states that “[s]ubstrate 23 and the layers and implants are formed from silicon-carbide and doped with N-type or P-type impurities as shown in FIG. 3.” *Id.* at 4:14–16. Drift layer 24 is formed on top of substrate 23 and current spreading epilayer (“CSL”) is formed on top of drift layer 24. *Id.* at 4:24–26. P well 29 is formed in the top of current spreading layer 25. *Id.* at 4:30–31.

The ’112 patent explains that “[f]ormed within P well 29 are two heavily doped N+ implant source regions 31 and 32 on opposing sides of a heavily doped, central implant P+ base 33.”³ *Id.* at 4:51–53. Polycrystalline

³ Figure 3 of the ’112 patent appears to have a typographical error because the reference numerals for the righthand N+ implant source region 32 and the central implant P+ base 33 appear to have been switched with each other.

silicon gate 38 “is surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41.” *Id.* at 5:1–3. Further, “Ni ohmic contact metal 45 is formed over the entire MOSFET 21” and “Ti/Au layer 53 is then formed atop of Ni metal contact 45.” *Id.* at 5:5–7, 5:25–26.

According to the ’112 patent, “[b]ecause gate 38 is completely surrounded by insulating oxide layer 41, its positionment relative to source contacts 31 and 32 is much less critical, and it cannot detrimentally come in contact with any portion of the Ni metal contact 45 due to any mask misalignment during processing.” *Id.* at 5:9–13.

D. Illustrative Claim

Claims 1, 2, and 6 are independent claims. Claim 1 is representative and is reproduced below:

1. A silicon carbide power MOSFET, comprising:
 - a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof;
 - a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions, said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region;
 - a first oxide layer between said first gate lower surface and said upper surface of said drift layer;
 - a second, thicker oxide layer over said top surface and sidewall of said first gate; and
 - a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region.

Id. at 8:23–39.

E. The Asserted Grounds of Unpatentability

Petitioner contends that claims 1–3, 6, 7, and 10–16 of the ’112 patent are unpatentable on the following grounds. Pet. 5.

Ground	Reference(s)	Basis ⁴	Claims Challenged
1	Peters ⁵	§ 102	1–3, 6, 10, 12–14
2	Peters	§ 103	1–3, 6, 7, 10, 12–14
3	Peters, Ghezzi ⁶	§ 103	11
4	Peters, Cooper ⁷	§ 103	1, 13–16
5	Tanimoto ⁸	§ 102	1–3, 6, 7, 10–14
6	Tanimoto	§ 103	1–3, 6, 7, 10–14
7	Tanimoto, Cooper	§ 103	15, 16

Petitioner also relies on a declaration from Jack C. Lee, Ph.D. Ex. 1010.

II. ANALYSIS

A “patent owner may file a statutory disclaimer under 35 U.S.C. [§] 253(a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent. No *inter partes* review will be instituted based on disclaimed claims.” 37 C.F.R. § 42.107(e) (2019).

⁴ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103. Because the ’112 patent has an effective filing date prior to the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of §§ 102, 103.

⁵ DE 198 27 925 A1, published Jan. 21, 1999 (Ex. 1003). Petitioner filed an English language translation of Peters (Ex. 1005).

⁶ US 5,510,281, issued Apr. 23, 1996 (Ex. 1006).

⁷ US 2006/0192256 A1, published Aug. 31, 2006 (Ex. 1007).

⁸ US 2005/0093000 A1, published May 5, 2005 (Ex. 1008).

A disclaimer under 35 U.S.C. § 253(a) is “considered as part of the original patent” as of the date on which it is “recorded” in the U.S. Patent and Trademark Office (“Office”). 35 U.S.C. § 253(a). For a disclaimer to be “recorded” in the Office, the document filed by the patent owner must:

- (1) Be signed by the patentee, or an attorney or agent of record;
 - (2) Identify the patent and complete claim or claims, or term being disclaimed. A disclaimer which is not a disclaimer of a complete claim or claims, or term will be refused recordation;
 - (3) State the present extent of patentee’s ownership interest in the patent; and
 - (4) Be accompanied by the fee set forth in [37 C.F.R.] § 1.20(d).
- 37 C.F.R. § 1.321(a); *see also Vectra Fitness, Inc. v. TNWK Corp.*, 162 F.3d 1379, 1382 (Fed. Cir. 1998) (holding that a § 253 disclaimer is “recorded” on the date that the Office receives a disclaimer meeting the requirements of 37 C.F.R. § 1.321(a), and that no further action is required in the Office for a disclaimer to be “recorded”).

Here, Patent Owner filed a statutory disclaimer of claims 1–16 of the ’112 patent, which includes the challenged claims. Prelim. Resp. 1; Ex. 2001. Based on our review of Exhibit 2001 and Office public records, we conclude that a disclaimer of claims 1–16 of the ’112 patent under 35 U.S.C. § 253(a) was filed with the Office as of September 29, 2021. Based on the information in the public record, we find that the disclaimer complies with the above-listed requirements of 37 C.F.R. § 1.321(a).

Because all challenged claims have been disclaimed under 35 U.S.C. § 253(a), in compliance with 37 C.F.R. § 1.321(a), no *inter partes* review is instituted in this proceeding. 37 C.F.R. § 42.107(e); *General Electric Co. v.*

United Techs. Corp., IPR2017-00491, Paper 9 (PTAB July 6, 2017)
(precedential) (declining to institute *inter partes* review when all challenged claims were disclaimed under 35 U.S.C. § 253(a)). Patent Owner acknowledges that we should deny institution on this threshold procedural ground. Prelim. Resp. 1.

III. CONCLUSION

For the reasons set forth above, we *deny* the Petition and do not institute *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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