

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA CORPORATION and KIOXIA AMERICA, INC.,
Petitioner,

v.

VIASAT, INC.,
Patent Owner.

IPR2022-01067
Patent 8,615,700 B2

Before THU A. DANG, KEVIN F. TURNER, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Kioxia Corporation and Kioxia America, Inc. (collectively, “Kioxia” or “Petitioner”) filed a Petition (Paper 1, “Pet.”) seeking an *inter partes* review of claims 1–4, 8, 10–19, and 23–25 (the “challenged claims”) of U.S. Patent No. 8,615,700 B2 (Ex. 1001, “the ’700 Patent”). Viasat, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 15 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2021). An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

After considering the information presented in the Petition and the Preliminary Response, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing that at least one of the challenged claims is unpatentable, and we do not exercise our discretion to deny institution. Therefore, we grant institution of an *inter partes* review.

Our findings and conclusions below are based on the record developed thus far. This is not a final decision as to the patentability of any challenged claim. Any final decision will be based on the full record developed during trial.

B. *Related Matters*

The parties identify the following district court cases as related matters: *Viasat, Inc. v. Kioxia Corp.*, No. 6:21-CV-01231-ADA (W.D. Tex.) (the “parallel district court litigation”) and *Viasat, Inc. v.*

Western Digital Corp., No. 6:21-CV-01230-ADA (W.D. Tex.). Pet. 1; Paper 5, 1 (Patent Owner’s mandatory notices).

In IPR2022-01126, the ’700 Patent is being challenged by a different petitioner, Western Digital Technologies, Inc. (“Western Digital”).

C. The ’700 Patent (Ex. 1001)

The ’700 Patent was issued from an application filed August 18, 2010. Ex. 1001, code (22). Petitioner contends that the ’700 Patent claims are not entitled to the August 18, 2009 filing date of the provisional application. *Id.* at code (60); Pet. 6. At this stage, Patent Owner does not dispute Petitioner’s contention.

The ’700 Patent discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57), 1:30–31, 2:27–28. According to the ’700 Patent, “[e]ncoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded).” *Id.* at 1:31–33. The data streams are processed at a number of error detection sub-modules, which forward an error-containing portion of the data stream to an error correction module, which corrects the forwarded portion. *Id.* at 1:33–41.

An embodiment is shown in Figure 3, reproduced below.

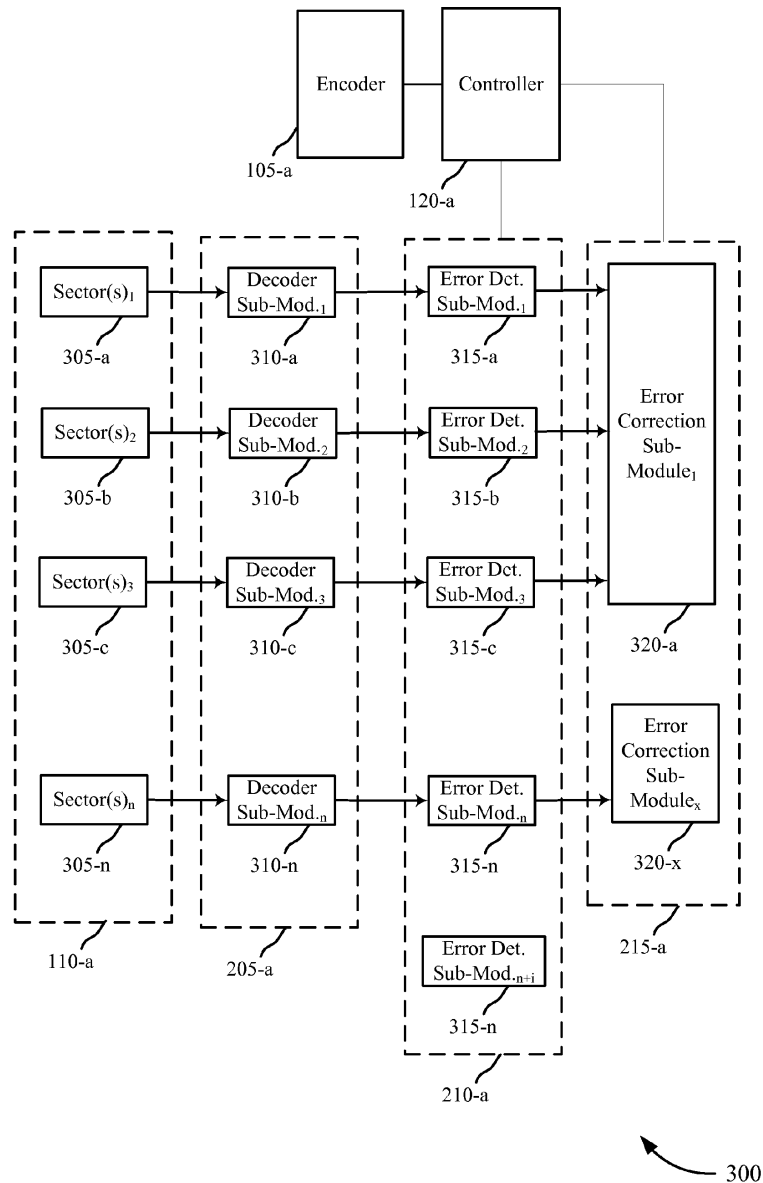


FIG. 3

Figure 3 “is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules.” Ex. 1001, 2:8–10, 6:29–32.

As shown in Figure 3, flash memory decoder system 300 includes flash memory 110-a, decoder module 205-a, error detection module 210-a, error correction module 215-a, controller 120-a, and encoder 105-a.

Ex. 1001, 6:33–37. Flash memory 110-a includes a number of different sets of one or more active sectors 305. *Id.* at 6:39–40. Decoder module 205-a

includes a number of decoder sub-modules 310, each of which may be associated with a different set of sectors 305. *Id.* at 6:40–43. Error detection module 210-a includes a number of error detection sub-modules 315, each of which may be associated with a different set of sectors 305. *Id.* at 6:43–46. For example, encoded data may be read from a set of one or more of sectors 305-a by decoder sub-module 310-a, and processed (e.g., buffered, de-interleaved, and decoded to some extent) to generate a data stream, which may be forwarded to error detection sub-module 315-a. *Id.* at 6:46–52.

According to the '700 Patent, each error detection sub-module 315 evaluates a data stream to determine whether it contains an error and forwards the portion of the stream containing an error to error correction module 215-a. Ex. 1001, 6:61–67. Error correction module 215-a includes a number of error correction sub-modules 320, each of which handles errors from a number of error detection sub-modules 315 and corrects the portions of the data streams containing an error. *Id.* at 6:67–7:7.

D. Illustrative Claims

The '700 Patent includes three independent claims, which are reproduced below with Petitioner's bracketed claim element designations added and paragraphs adjusted.

1. A flash memory decoder comprising:

[1a] a decoding module configured to: receive encoded data from the flash memory; and

[1b] decode the received encoded data to generate a plurality of partially decoded data streams;

[1c] an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel, each error detection

sub-module configured to: receive a different one of the plurality of partially decoded data streams;

[1c] detect whether a portion of the respective received stream contains an error; and

[1e] forward the portion of the respective received stream containing an error to an error correction module; and

[1f] the error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

Ex. 1001, 10:47–65; Pet. 19–27.

15. A system comprising:

[15a] an encoder configured to encode data for storage on a flash memory;

[15b] the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

[15c] a decoder, communicatively coupled with the flash memory, and configured to: retrieve the encoded data from flash memory to generate a plurality of data streams; and

[15d] process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams,

[15e] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[15f] forward the portion of the respective received stream containing an error to an error correction module of the decoder; and

[15g] correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:21–44; Pet. 31–33.

17. A method comprising:

[17a] receiving encoded data from a flash memory comprising a plurality of data streams;

[17b] processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams,

[17c] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[17e] forward the portion of the respective received stream containing an error to an error correction module; and

[17f] correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:49–63; Pet. 33–35.

E. Asserted Challenges to Patentability and Evidence

Petitioner asserts the following challenges to patentability:

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 2, 13–15, 17	102(e)	Lee ²

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the ’700 Patent was issued on an application filed before that date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

² Ex. 1004, US 7,865,809 B1, filed July 1, 2008 and issued January 4, 2011 (“Lee”).

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
4, 8, 19	103(a)	Lee, JO ³
3, 10–12, 16, 18, 23–25	103(a)	Lee, Kim ⁴
1, 13–15, 17	102(e)	Yamaga ⁵
1, 13–15, 17	103(a)	Yamaga
2, 4, 8, 19	103(a)	Yamaga, JO
3, 10–12, 16, 18, 23–25	103(a)	Yamaga, JO, Kim

Pet. 3. Petitioner submits the declaration of Richard Koralek, Ph.D.
Ex. 1002.

II. DISCRETION UNDER 35 U.S.C. § 314(A) BASED ON *FINTIV*

Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 314(a) based on the *Fintiv* factors. Prelim. Resp. 5–13; *see Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv I*”). Petitioner argues the opposite. Pet. 17–18.

In assessing whether to exercise such discretion, the Board weighs the six non-exclusive *Fintiv* factors. *Fintiv I* at 6. Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to

³ Ex. 1007, US 2009/0063934 A1, filed August 27, 2008 and published March 5, 2009 (“JO”). Petitioner asserts that JO is prior art to the ’700 Patent under 35 U.S.C. §§ 102(a) and 102(e). Pet. 10.

⁴ Ex. 1006, US 2010/0241928 A1, filed March 3, 2010 and published September 23, 2010 (“Kim”). Petitioner asserts that Kim is prior art under 35 U.S.C. § 102(e). Pet. 12.

⁵ Ex. 1005, US 8,086,933 B2, filed September 19, 2008 and issued December 27, 2011 (“Yamaga”).

more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* A Memorandum from the Director provides “binding agency guidance” regarding how the Board’s discretion under 35 U.S.C. § 314(a) and the *Fintiv* factors apply to “sample fact patterns.” Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022) (“Interim Procedure”),⁶ 3.

A. Fintiv Factors

1. Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted

Petitioner states that it intends to file a motion to stay the parallel district court litigation “in the event of IPR institution.” Pet. 17. Patent Owner argues that the district court is unlikely to grant a stay. Prelim. Resp. 6–7.

There is no evidence that a stay has been requested or ordered in the parallel district court litigation. We decline to speculate on how the district court would rule on a stay, if one were requested. *Sand Revolution II, LLC v. Cont’l Intermodal Grp.-Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”) (declining to predict whether or not the district court would grant a stay, if requested); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) (“*Fintiv II*”) (explaining that factor 1 generally “does not weigh for or against discretionary denial” when neither party has requested a stay). Accordingly, this factor is neutral.

⁶ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

2. *Proximity of the Court's Trial Date to the Board's Projected Statutory Deadline*

Petitioner states that “a trial date has not yet been set” in the parallel district court litigation. Pet. 17. Patent Owner asserts that, applying the district court’s default timing for patent cases, trial “is currently scheduled to begin around October 2, 2023.” Prelim. Resp. 7. In addition, Patent Owner represents that “the median time to trial in the Western District of Texas is 25.5 months for the year ending December 31, 2021, which would place trial around January 2024.” *Id.*

In this *inter partes* review proceeding, the projected statutory deadline for a final written decision is November 2023. Based on the parties’ representations, it appears that trial in the parallel district court litigation may begin either shortly before or within a few months after the projected statutory deadline for a final written decision in this proceeding. Under these circumstances, this factor weighs neither for nor against the exercise of discretion to deny institution.

3. *Investment in the Parallel Proceeding by the Court and Parties*

Petitioner states that discovery has not commenced in the parallel district court litigation. Pet. 17. Patent Owner states that the parties have exchanged preliminary infringement and invalidity contentions, initial document disclosures, and claim construction briefs; that a claim construction hearing was scheduled for September 30, 2022; that fact discovery was scheduled to commence October 3, 2022; and that final infringement and invalidity contentions are due in November. Prelim. Resp. 9. Neither party filed the district court’s scheduling order, nor provided dates for the close of fact or expert discovery.

Based on the parties' representations, it appears that much work remains to be done in the parallel district court litigation as it relates to invalidity: there is no claim construction order, fact discovery has just begun, expert reports are not yet due, there have been no fact or expert depositions, and substantive motion practice is yet to come. Pet. 17–18; Prelim. Resp. 9; *see Sand Revolution* at 11. Thus, although the parties and the district court have invested some effort in the parallel district court litigation, the bulk of the work to prepare the invalidity case for trial is yet to be done.

We also acknowledge Petitioner's diligence in filing the Petition "only seven weeks" after receiving Patent Owner's preliminary infringement contentions. Pet. 18; Ex. 1010.

Under these circumstances, we determine that this factor weighs slightly against exercising our discretion to deny institution.

4. *Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

In the parallel district court litigation, Petitioner filed a stipulation stating that, if the Board institutes an *inter partes* review in this proceeding, then Petitioner will not pursue in the parallel district court litigation "the specific invalidity grounds" raised in the Petition. Paper 16, 1 (Petitioner's updated mandatory notices); Ex. 1018, 2.

Patent Owner asserts that Petitioner and Western Digital filed joint invalidity contentions in the district court and that "the art asserted in their respective petitions barely overlaps." Prelim. Resp. 10. Patent Owner alleges that Petitioner and Western Digital have coordinated the art they assert in their respective petitions to avoid estoppel in the district court. *Id.* at 3, 10, 12. Patent Owner criticizes Petitioner for not providing a *Sotera-*

style stipulation that covers grounds that could have reasonably been raised in the Petition, including the grounds raised in the Western Digital petition. *Id.* at 2, 10–12; see *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A) (“*Sotera*”).

The Interim Procedure states, “Consistent with *Sotera Wireless, Inc.*, . . . the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure, 3 (footnote omitted; citing *Sotera*). In other words, under the Interim Procedure, a petitioner may avoid discretionary denial of the petition based on a parallel district court litigation by providing a *Sotera*-style stipulation. The Interim Procedure does not, however, make a *Sotera*-style stipulation a prerequisite for institution. Under our informative precedent, an *inter partes* review may be instituted despite the absence of a *Sotera*-style stipulation. *Sand Revolution* at 12 n.5 (instituting *inter partes* review notwithstanding the absence of a stipulation not pursue any ground that could have been reasonably raised in an *inter partes* review).

We find that Petitioner’s stipulation (Ex. 1018) is the same as the one in *Sand Revolution*, where the petitioner stipulated that, if the IPR is instituted, the petitioner will not pursue the same grounds in the district court litigation. *Sand Revolution* at 11–12. In that case, the panel held that petitioner’s stipulation “mitigates to some degree the concerns of duplicative efforts between the district court and the Board as well as concerns of potentially conflicting decisions” and that *Fintiv* factor 4 “weighs marginally in favor of not exercising discretion to deny institution.” *Id.* at 12.

Turning to Patent Owner's assertions about coordination, Patent Owner has not questioned Petitioner's representation that Kioxia is the real party in interest in this proceeding. Pet. 1. Any dispute about the scope of estoppel is premature and would be more appropriately raised before the district court, or any other forum where estoppel may apply, after the issuance of a final written decision.

Consistent with our informative precedent in *Sand Revolution*, we find that this factor weighs marginally against exercising discretion to deny institution under 35 U.S.C. § 314(a).

5. *Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party*

The Petitioner here is a defendant in the parallel district court litigation, and, thus, this factor weighs in favor of exercising our discretion to deny institution under § 314(a). *Fintiv II* at 15 (“Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.”).

6. *Other Circumstances that Impact the Board's Exercise of Discretion, Including the Merits*

Petitioner makes no representation about the strength of the Petition. Patent Owner contends that the merits are “not particularly strong,” asserting that it “identifies multiple weaknesses related to every ground and every independent claim that the Petition challenges.” Prelim. Resp. 13.

According to the Interim Procedure, “*Fintiv* factor six reflects that the PTAB considers the merits of a petitioner's challenge when determining whether to institute a post-grant proceeding in view of parallel district court litigation.” Interim Procedure, 4. The Interim Procedure requires us to determine whether the information presented at the institution stage (1) “is

merely sufficient to meet the statutory institution threshold” or (2) “presents a compelling unpatentability challenge.” *Id.* at 4–5. In the first case, we have “the authority, where warranted, to exercise discretion to deny institution in view of the other *Fintiv* factors,” and in the second case, we do not have such authority. *Id.*

Here, for the reasons discussed below, we determine that the information presented is sufficient to meet the statutory threshold for institution for some of the challenged claims, but does not present a compelling unpatentability challenge. Therefore, consistent with the Interim Procedure, *Fintiv* factor six is neutral.

B. Balancing the Fintiv Factors

After considering the circumstances and facts before us in view of the *Fintiv* factors and the Interim Procedure, we determine that the circumstances presented here do not support exercising our discretion under § 314(a) to deny institution.

III. REASONABLE LIKELIHOOD UNDER 35 U.S.C. § 314(A)

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is anticipated under 35 U.S.C. § 102 only if “each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had a Master’s degree in electrical engineering or an equivalent field and two years of academic or industry experience working with error correction in memory devices.” Pet. 14 (citing Ex. 1002 ¶ 19).

For purposes of the preliminary response, Patent Owner does not dispute Petitioner’s definition of a POSITA. Prelim. Resp. 18.

For purposes of this Decision, we apply Petitioner’s articulation of the level of ordinary skill in the art, which is consistent with the level of skill in the art at the time of the invention as reflected in the asserted prior art.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Below we address the parties' dispute about the meaning of a phrase in claim 1. We do not need to provide an express construction for any other claim terms for purposes of this Decision. Our construction is preliminary, and the parties are invited to address claim construction in their post-institution briefs.

“decode the received encoded data to generate a plurality of partially decoded data streams” (claim 1)

Petitioner contends that this phrase means “buffer the received encoded data, de-interleave the received encoded data, or distinguish error correction bits from information bits in the received encoded data, to generate a plurality of data streams.” Pet. 14–15 (citing Ex. 1002 ¶ 64). As support for this construction, Petitioner relies on the '700 Patent Specification and Patent Owner's district court infringement contention. Pet. 15 (citing Ex. 1001, 6:11–14; Ex. 1010, 9).

Patent Owner argues that this phrase should be construed to mean “process the received encoded data to generate more than one data stream for error detection.” Prelim. Resp. 14. As support for this construction, Patent Owner relies on the '700 Patent Specification. *Id.* at 15 (quoting Ex. 1001, 6:9–14). Patent Owner argues that “‘decode’ requires more than simple buffering.” *Id.* at 17.

The parties rely on the following passage in the '700 Patent:

The decoder module 205 may receive encoded data from flash memory, and process the received encoded data to generate a number of data streams. In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, an[d] thereby generate decoded (or partially decoded) data streams.

Ex. 1001, 6:9–14.

Patent Owner argues that the first sentence quoted above describes what it means to “partially decode.” Prelim. Resp. 14–15. We disagree. Although the sentence describes the function of a decoder module, it does not describe what it means to decode (or partially decode) encoded data. We decline to adopt Patent Owner’s proposed construction because it replaces the claim language “decode the received encoded data to generate a plurality of partially decoded data streams” with a sentence from the Specification that does not describe “decod[ing]” or “partially decoded.” Patent Owner’s proposed construction fails to capture the meanings of these words. Instead, it merely replaces the claim term “decode” with the broader term “process.”

We agree with Patent Owner, however, that “decode” requires more than just buffering. The Specification twice mentions buffering. Ex. 1001, 6:11–14 (quoted above); *id.* at 6:46–50 (“[E]ncoded data may be read from a set of one or more of sectors . . . by a decoder sub-module . . . and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream.”) In each instance, buffering is disclosed along with de-interleaving and decoding as actions performed by a decoder module or sub-module. Nowhere does the Specification define “decode” to mean “buffer” or “de-interleave.”

Patent Owner does not dispute the portion of Petitioner’s construction that defines “decode” to mean “distinguish error correction bits from information bits.” Pet. 14–15. Both parties rely on Patent Owner’s district court infringement contentions, where Patent Owner asserted that the disputed claim limitation is met by the accused products in part because “[a]t a minimum, the ECC bits will be identified, distinguished from, and

associated with the relevant information bits.” Ex. 1010, 9; Pet. 15; Prelim. Resp. 15.⁷

Neither party directs us to intrinsic evidence to support this definition of “decode.” Nevertheless, because this portion of Petitioner’s proposed construction is undisputed at this stage of the proceeding, we adopt it for purposes of our Decision. Accordingly, we construe the phrase “decode the received encoded data” to mean “distinguish error correction bits from information bits in the received encoded data.” Although the term may not be limited to this meaning, no other acceptable definition has been presented on this record. At this stage of the proceeding, we do not construe the phrase “to generate a plurality of partially decoded data streams” because neither party has proposed a construction for that portion of the claim language.

D. Petitioner’s Lee Anticipation Challenge

Petitioner challenges claims 1, 2, 13–15, and 17 as anticipated by Lee. Pet. 19–35. Patent Owner opposes. Prelim. Resp. 18–29. We provide an overview of Lee before turning to our analysis, which focuses on the disputed issues that are relevant under our preliminary claim construction.

1. Lee (Ex. 1004)

Lee discloses data error detection and correction in non-volatile memory devices such as flash memory devices. Ex. 1004, code (57), 1:25–32, 1:65–66. Figures 5A and 5B are reproduced below.

⁷ We understand “ECC” to refer to error correcting codes. Ex. 1002 ¶ 70.

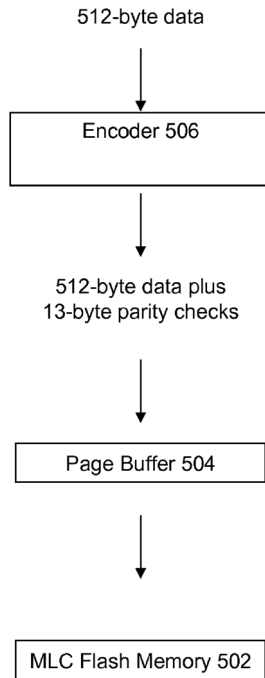


FIG. 5A

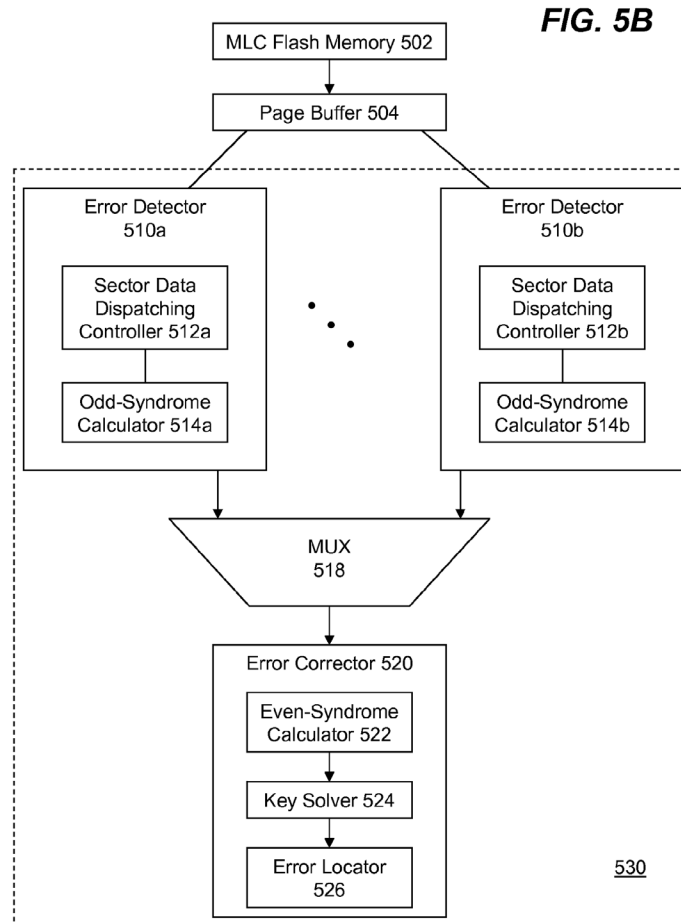


FIG. 5B

Lee’s Figures 5A and 5B show an encoder and a decoder, respectively, in an error corrector of a non-volatile memory device. Ex. 1004, 3:34–39.

As shown in Figure 5A, ECC encoder 506 encodes a chunk of data (e.g., 512-byte sector) to a codeword (e.g., 525-byte data plus ECC or parity checks). Ex. 1004, 8:44–49. Upon creation, the codeword is stored into page buffer 504 then to the non-volatile memory (e.g., MLC flash memory 502). *Id.* at 8:53–55.

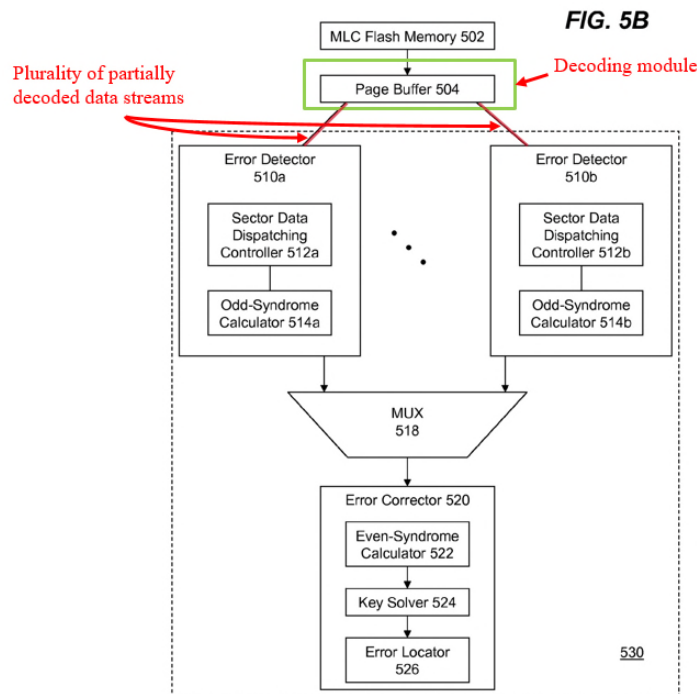
As shown in Figure 5B, error decoder 530 comprises a plurality of data error detectors 510a-b coupled via multiplexer (MUX) 518 to error corrector 520. Ex. 1004, 8:56–61. “Each data error detector 510a-b is configured to process a chunk of data (e.g., 512-byte data sector)” in parallel with the other data error detectors 510a-b. *Id.* at 8:61–65. Data error

detector 510 includes sector data dispatching controller 512 and odd-syndrome calculator 514. *Id.* at 8:65–67. Sector data dispatching controller 512 “is configured for receiving appropriate data sector,” while odd-syndrome calculator 514 “for computing the odd terms of syndrome polynomial of the received codeword.” *Id.* at 8:67–9:4. If “data error detectors 510a-b determine that there is no error in the received data,” then “error corrector 520 stops processing further and moves on to the next chunk of data.” *Id.* at 9:4–6. “If, however, data error detectors 510a-b detect data error in the received data,” then “error corrector 520 is configured to process additional error location and correction.” *Id.* at 9:7–9. According to Lee, “[t]here is only one error corrector 520 for the set of data error detectors 510a-b.” *Id.* at 9:9–11.

2. *Claim 1*

Claim 1 of the ’700 Patent recites “[1a] a decoding module configured to receive encoded data from the flash memory; and [1b] decode the received encoded data to generate a plurality of partially decoded data streams.” Ex. 1001, 10:48–51 (bracketed designations added).

To show claim element [1b], Petitioner provides the following annotation of Lee’s Figure 5B:



Pet. 21. Lee’s Figure 5B shows a decoder. Petitioner’s annotations identify page buffer 504 as a “decoding module” and the lines extending from page buffer 504 to error detectors 510a, b as a “plurality of partially decoded data streams.” *Id.* Petitioner contends that “Lee discloses buffering the received encoded data to generate a plurality of data streams.” Pet. 22.⁸ In addition, Petitioner contends that “[b]ecause Lee’s error detectors 510a-b each process a separate sector of data, the page buffer 504 must necessarily distinguish and associate page-level ECC bits with each set of sector data before sending to error detectors 510a-b.” *Id.* (citing Ex. 1002 ¶ 100; Ex. 1004, 8:61–63).

Patent Owner argues that Lee’s page buffer has no role in the decoding process. Prelim. Resp. 23. Patent Owner disputes Petitioner’s

⁸ When quoting from the Petition, we omit Petitioner’s italicization of the names of the references and drawing sub-references.

contention that Lee’s page buffer distinguishes and associates page-level ECC bits with each sector of data, asserting that “manipulation of the read operations, retrieval of data from the flash memory, and generation of multiple data streams are performed by another component (*e.g.*, sector data dispatching controller 512).” *Id.* at 24. In addition, Patent Owner argues that Petitioner wrongly assumes that Lee’s Figure 5B depicts every process step and component between the flash memory and the decoder and improperly rearranges elements from different embodiments in Lee. *Id.* at 24–25.

As discussed above, we construe the phrase “decode the received encoded data” in claim 1 to mean “distinguish error correction bits from information bits in the received encoded data.” At this stage of the proceeding, we are not persuaded by Petitioner’s contention that Lee’s page buffer 504 performs this function. Petitioner identifies Lee’s page buffer 504 as the “decoding module” of claim 1 (Pet. 20–21), but does not show that page buffer 504 decodes the received encoded data by distinguishing error correction bits from information bits in the received encoded data. Dr. Koralek opines that, “[b]ecause, in at least one example, Lee’s error detectors 510a-b each process a separate sector of data, the page-level ECC bits must be identified and associated with each sector separately so that it can be sent to each error detector 510a-b.” Ex. 1002 ¶ 100 (citing Ex. 1004, 8:61–63). The cited portion of Lee describes data error detector 510a-b, not page buffer 504. Ex. 1004, 8:61–63. Neither Petitioner nor Dr. Koralek direct us to evidence that page buffer 504 performs the function required by our preliminary claim construction.

The parties are invited to address this issue at trial.

3. *Dependent Claims 2, 13, and 14*

At this stage, Patent Owner does not dispute Petitioner’s contention that Lee discloses the limitations of claims 2, 13, and 14, each of which depends from claim 1. We note, however, that Petitioner’s arguments and evidence for dependent claims 2, 13, and 14 (Pet. 29–31) do not remedy the deficiencies in Petitioner’s challenge to independent claim 1, as discussed above.

4. *Claim 15*

Claim element [15c] recites “a decoder, communicatively coupled with the flash memory, and configured to: retrieve the encoded data from flash memory to generate a plurality of data streams.” Ex. 1001, 12:27–30.

Addressing claim element [15c], Petitioner relies on its contentions for claim elements [1a] and [1b] and further contends that “Lee discloses a decoder that receives encoded data from flash memory and generates a plurality of data streams.” Pet. 32 (citing Ex. 1002 ¶¶ 135, 136). According to Petitioner, “a POSITA would understand the ‘sector data dispatching controllers’ of the error detectors would request encoded data from the flash memory.” *Id.* (citing Ex. 1002 ¶ 137; Ex. 1004, 8:58–67).

Patent Owner relies on the same arguments for claim 15 as it presents for claim 1. Prelim. Resp. 27. In addition, Patent Owner argues that Lee’s sector data dispatching controllers 512 do not interact with the page buffer to generate a plurality of data streams. *Id.* at 27–28.

Claim 15 differs from claim 1 in that claim 15 does not recite the phrase, “decode the received encoded data,” for which we provide a preliminary construction. Petitioner presents different contentions for claim 15 than for claim 1. Whereas Petitioner identifies Lee’s page buffer 504 as

the “decoding module” of claim 1 (Pet. 20–22), Petitioner identifies Lee’s decoder 530, including sector data dispatching controllers 512, as the “decoder” of claim 15 (Pet. 32). Furthermore, for claim 15, Petitioner contends that a plurality of data streams is generated by Lee’s decoder 530, not just page buffer 504. *Compare* Pet. 21–22 (addressing claim element [1b]), *with* Pet. 32 (addressing claim element [15c]). On the other hand, for both claim elements [1b] and [15c], Petitioner appears to rely on Lee’s Figure 5B as showing a “plurality of . . . data streams” flowing from page buffer 504 to error detectors 510a, b. Pet. 21 (Petitioner’s annotation of Lee’s Figure 5B for claim element 1); Pet. 32 (addressing claim element [15c] and referencing Petitioner’s contentions for claim element [1b]).

Patent Owner argues that Figure 5B shows a single data stream—not a plurality—going from the sector data dispatching controller. Prelim. Resp. 27–28. At this stage of the proceeding, however, Patent Owner’s argument does not seem to address Petitioner’s position for claim element [15c], which appears to rely on the two lines extending from Lee’s page buffer 504 to error detectors 510a, b as showing a “plurality of data streams” generated by Lee’s decoder. Pet. 21, 32. Furthermore, Patent Owner’s argument for claim element [15c] appears to be contradicted by its argument for claim element [1b]. *Compare* Prelim. Resp. 27 (addressing claim 15: “There is no explanation in [Lee] that the sector data dispatching controllers interact with the page buffers to generate . . . a plurality of streams.”), *with id.* at 24 (addressing claim 1: Lee “explains that . . . generation of multiple data streams are performed by . . . sector data dispatching controller 512.”).

For these reasons, Petitioner’s contention for claim 15 does not appear to suffer from the same deficiencies as Petitioner’s challenge to claim 1 and is sufficient for purposes of institution.

5. *Claim 17*

Claim element [17a] recites “receiving encoded data from a flash memory comprising a plurality of data streams.” Ex. 1001, 12:50–51.

Addressing claim element [17a], Petitioner relies on its contentions for claim elements [1a] and [1b] and further contends that “Lee discloses receiving encoded data from [multi-level cell] MLC flash memory as a plurality of data streams” and “further discloses that the error detectors receive encoded data (i.e., a codeword).” Pet. 34 (citing Ex. 1002 ¶ 149; Ex. 1004, 2:42–44, 8:49–9:4).

Patent Owner relies on the same arguments for claim 17 as it presents for claims 1 and 15. Prelim. Resp. 28. In addition, Patent Owner argues that Lee does not disclose receiving encoded data from a flash memory, where the received encoded data comprises a plurality of data streams. *Id.* at 28–29.

Claim 17 differs from claim 1 in that claim 17 does not recite the phrase, “decode the received encoded data,” for which we provide a preliminary construction. Furthermore, claim 17 is a method claim and does not recite either a “decoding module” as in claim 1 or a “decoder” as in claim 15. For both claim elements [1b] and [17a], Petitioner appears to rely on Lee’s Figure 5B as showing a “plurality of . . . data streams” flowing from page buffer 504 to error detectors 510a, b. Pet. 21 (Petitioner’s annotation of Lee’s Figure 5B for claim element [1b]); Pet. 32 (addressing

claim element [15c] and referencing Petitioner’s contentions for claim element [1b]).

Patent Owner argues that Lee’s Figure 5B shows “only a single arrow coming from the MLC flash memory” and “that single stream is received by the ‘decoding module.’” Prelim. Resp. 29. Patent Owner agrees, however, that Petitioner identifies multiple arrows as corresponding to a “plurality” of data streams. *Id.* (combining Petitioner’s annotations of Lee’s Figure 5B, which identify a “plurality of partially decoded data streams”). Because claim 17 does not recite a decoding module, Petitioner’s contention for claim 17 does not appear to suffer from the same deficiencies as Petitioner’s challenge claim 1 and is sufficient for purposes of institution.

6. Conclusion

We determine that Petitioner has established a reasonable likelihood of prevailing on its challenge to claims 15 and 17 as anticipated by Lee, but has not established a reasonable likelihood of prevailing on its challenge to claims 1, 2, 13, and 14 as anticipated by Lee.

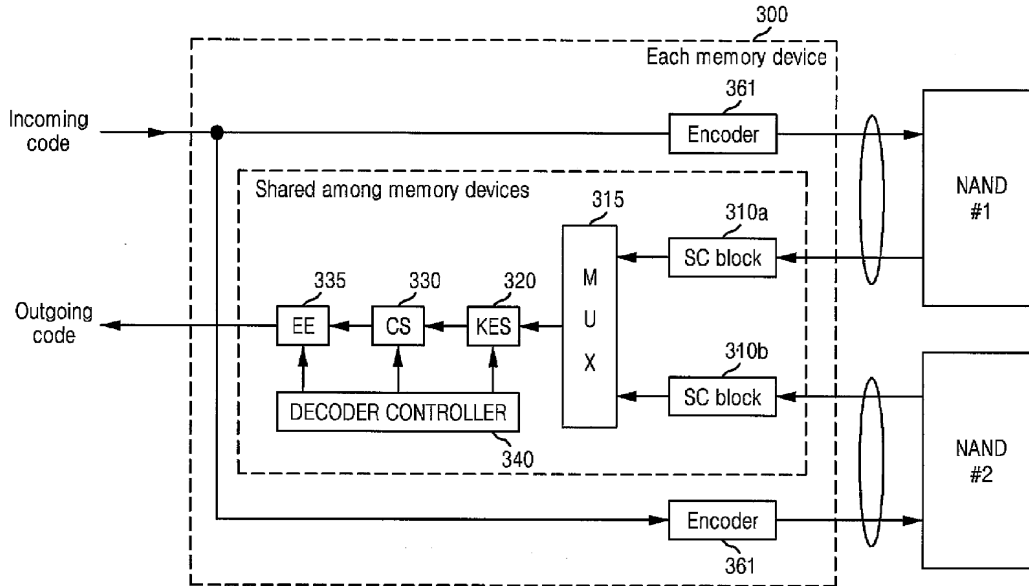
E. Petitioner’s Challenge based on Lee and JO

Petitioner challenges claims 4, 8, and 19 as unpatentable and obvious based on Lee and JO. Pet. 35–39. Patent Owner opposes. Prelim. Resp. 30–35. We provide an overview of JO before turning to our analysis, which focuses on the disputed issues.

1. JO (Ex. 1007)

JO discloses a “multi-channel memory system including error correction decoder architecture.” Ex. 1007, code (54). Figure 3 is reproduced below.

FIG. 3



JO's Figure 3 shows flash memory error correction code (ECC) block 300, which communicates with flash memories NAND #1 and NAND #2 over two communication channels operating in parallel. Ex. 1007 ¶¶ 18, 23, 25. ECC block 300 includes two data encoders 361, one each for communication channel, and two syndrome computation (SC) blocks 310a and 310b, again one for each communication channel. *Id.* ¶ 24. SC blocks 310a and 310b each receive a set of data from a different sector of memory and detect whether or not the data set includes errors. *Id.* ¶¶ 26, 27.

ECC block 300 further includes multiplexer 315, key equation solver (KES) block 320, "Chien" search and error evaluator blocks 330 and 335, and decoder controller 340, all of which are shared by the two communication channels. *Id.* ¶¶ 24, 28. According to JO, "multiplexer 315 multiplexes between the first and second communication channels for locating errors that occur in data sets received from the memory devices via the communication channels." *Id.* ¶ 28. JO further discloses that, "[o]nce

the errors are identified in a data set, then the errors are corrected in a further error correction block not shown in FIG. 3 . . . and the decoded data set may then be sent to a host device.” *Id.*

2. *Claims 4, 8, and 19*

Claim 4 depends from claim 1 and recites “wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.” Ex. 1001, 11:7–10. Claim 8 depends from claim 4. *Id.* at 11:37–41. Claim 19 depends from claim 17 and recites the same limitation as claim 4. *Id.* at 13:1–4.

Petitioner contends that a “POSITA would understand that JO discloses a plurality of error correction sub-modules operating in parallel.” Pet. 36 (citing Ex. 1002 ¶ 169). According to Petitioner, JO discloses systems having two or more channels, “where each pair of channels is associated with a different error correction sub-module.” *Id.* (citing Ex. 1002 ¶ 169; Ex. 1007 ¶ 6, claim 1). Petitioner asserts:

A POSITA would understand that when JO’s system has four (or more) channels, it would include at least four error detection sub-modules and two error correction sub-modules, wherein each error detection sub-module is connected to a different one of the channels, and each error correction sub-module is associated with a unique pair of error detection sub-modules.

Id. (citing Ex. 1002 ¶ 169).

Patent Owner argues that Petitioner makes an “unsupported inference” that, when JO’s system has more than two communication channels, each pair of channels would have its own error correction sub-module. Prelim. Resp. 34. According to Patent Owner, JO discloses “multiple communication channels and yet only has a single error corrector,” and “[t]o

the extent that one wished to add additional channels, . . . a person of skill following Jo’s teachings would simply arrange those channels to feed into the same error corrector.” *Id.* at 35 (citing Ex. 1007 ¶¶ 12, 23, 25, 28, 37, 41, Figs. 3, 6, claim 1).

After considering the parties’ arguments and evidence, we have concerns about the sufficiency of Petitioner’s showing for claims 4, 8, and 19. We are concerned that Petitioner has not sufficiently established that JO discloses “a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules,” as recited in claims 4 and 19. JO’s Figure 2 shows a plurality of error correctors 163, 173, 183, but they are not fewer in number than error detectors 162, 172, 182. Ex. 1007 ¶ 7, Fig. 2. Petitioner does not point to any express disclosure in JO of multiple error correction sub-modules that are fewer in number than the error detection sub-modules. Nor does Petitioner provide sufficient support for its assertion that a POSITA would have understood JO as disclosing this feature.

Petitioner and Dr. Koralek assert that “when JO’s system has four (or more) channels, it would include at least four error detection sub-modules and two error correction sub-modules.” Pet. 36; Ex. 1002 ¶ 169. Patent Owner has a different understanding of JO, namely, that any additional channels (beyond the two shown in JO’s Figures 3 and 6) would feed into the same error corrector. Prelim. Resp. 35. Based on the present record, our preliminary view is that Patent Owner’s understanding more closely aligns with JO’s disclosure. JO repeatedly describes “at least” two communication channels and “at least” two error detectors, but describes only a single error corrector. Ex. 1007 ¶¶ 12, 15, 28, 37, 41, claim 1, Figs. 3, 6. JO uses broad, open-ended language when describing the number of communication

channels and the number of error detectors, but not when describing the number of error correctors. *Id.* The parties are invited to address this issue at trial.

3. *Motivation to combine*

Petitioner contends that a POSITA would have been motivated to combine Lee with JO because the references are from the same field of art and are directed to solving the same problem. Pet. 38. Petitioner contends that “[i]n order to improve throughput and efficiency, a POSITA would have been motivated to include JO’s multiple error correctors, which each correct errors from two or more error detectors, in the system of Lee.” *Id.* (citing Ex. 1002 ¶ 162). Petitioner contends that a POSITA would have expected the combination to be successful because both references disclose error correctors that correct errors from two or more error detection modules operating in parallel. Pet. 39 (citing Ex. 1002 ¶¶ 164, 165).

Patent Owner criticizes Petitioner’s contentions as “too general,” “conclusory,” “cursory,” and inadequate to establish a motivation to combine in view of alleged teaching away in Lee. Prelim. Resp. 31–34 (citing Ex. 1004, 9:9–11). Patent Owner asserts that Petitioner provides “no discussion of how multiple error correction sub-modules would be integrated with Lee’s system.” *Id.* at 33. According to Patent Owner, “adding components to Lee runs counter to Lee’s criticism of the prior art as being ‘complicated hence expensive and not optimized.’” *Id.* (citing Ex. 1004, 1:48–54).

Based on the current record, we provide the following preliminary observations concerning motivation to combine.

First, Petitioner's contention that a POSITA would have been motivated to combine Lee and JO rests on the premise that JO discloses multiple error correctors. As discussed above, Petitioner has not sufficiently established that premise.

Second, although Petitioner and Dr. Koralek assert that a POSITA would have been motivated to include additional error correctors "[i]n order to improve throughput and efficiency," they do not explain how throughput and efficiency would have been improved. Pet. 38; Ex. 1002 ¶ 163. Lee aims to provide "efficient and effective implementation of error correction" and teaches that efficiency is improved by "parallel encoding and error detection," while error correction is conducted sequentially. Ex. 1004, 1:51–54, 2:10–14, 9:13–15, 9:32–34, 13:51–53 (claim 7). JO states that "adding more ECC modules enlarges the size of the integrated circuit[] and increases the number of ECC IP core gates," which "increases the complexity and cost of the flash memory system." Ex. 1007 ¶ 9. JO aims to provide "robust error detection and correction with a more efficient utilization of area and circuitry in a memory controller" and teaches that error correction circuitry is shared by multiple communication channels. *Id.* ¶¶ 10, 28, 33, 41. In view of these teachings, it is unclear whether a desire for improved throughput and efficiency would have motivated a POSITA to add more error correctors. Furthermore, Petitioner and Dr. Koralek do not address whether error correction could have been reliably conducted in parallel by multiple error correctors, rather than serially, as taught by the references. Ex. 1004, 11:20–27, Figs. 12A, 12B; Ex. 1007 ¶¶ 42–50, Fig. 7.

Third, we do not agree that the passage in Lee cited by Patent Owner teaches away from including a plurality of error correction modules. Prelim. Resp. 31, 33. Patent Owner relies on Lee's disclosure that there is "only one

error corrector 520 for the set of data error detectors 510a-b” in Figure 5B. Ex. 1004, 9:9–11. In our preliminary view based on the current record, the quoted passage appears to disclose a ratio of error correctors to error detectors and does not appear to teach away from including multiple error correction modules.

The parties are invited to address the motivation issue at trial.

4. Conclusion

We determine that Petitioner has not established a reasonable likelihood of prevailing on its challenge to claims 4, 8, and 19 based on Lee and JO.

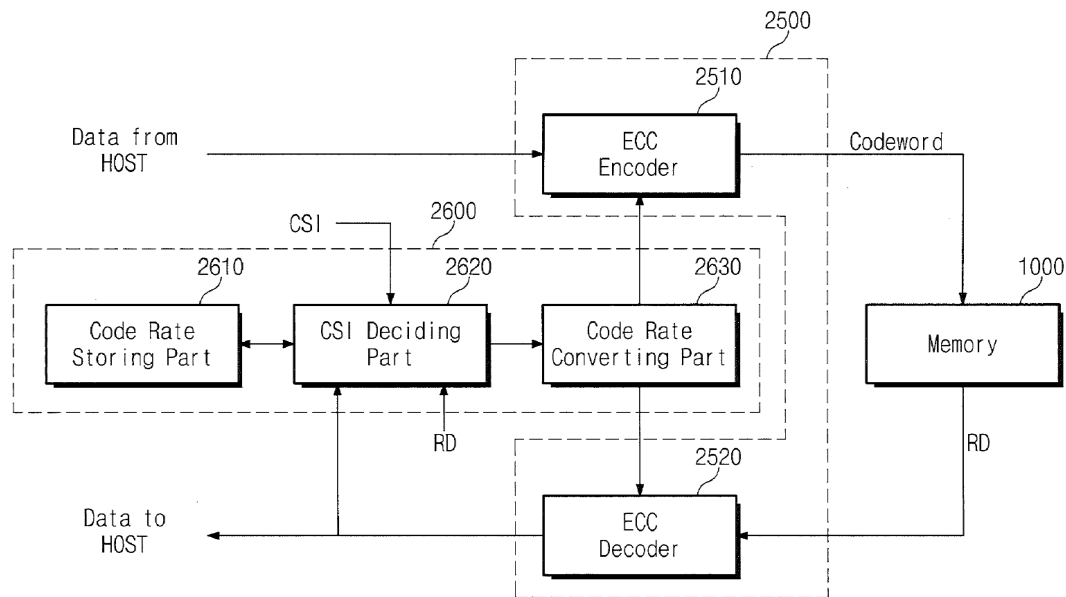
F. Petitioner’s Challenge based on Lee and Kim

Petitioner challenges claims 3, 10–12, 16, 18, and 23–25 as unpatentable and obvious based on Lee and Kim. Pet. 39–49. Patent Owner opposes. Prelim. Resp. 36–38. We provide an overview of Kim before turning to our analysis, which focuses on the disputed issue.

1. Kim (Ex. 1006)

Kim discloses ECC encoding and decoding circuits with code rate selection based on bit error rate detection. Ex. 1006, code (54). Figure 2 is reproduced below.

Fig. 2



Kim's Figure 2 shows ECC encoding and decoding block 2500 and code rate controlling block 2600, which communicate with memory 1000 and a host. Ex. 1006 ¶¶ 10, 32, 33. ECC encoding and decoding block 2500 includes ECC encoder 2510 and ECC decoder 2520. ECC encoder 2510 encodes data from the host to generate a codeword, which is sent to memory 1000. *Id.* ¶ 33. ECC decoder 2520 decodes data read out from memory 1000 and sends the decoded data to the host. *Id.* A code rate of ECC encoder 2510 and a code rate of ECC decoder 2520 are set by code rate controlling block 2600. *Id.*

Kim discloses that criteria for changing the code rate include “wear-leveling information such as a program/erase cycle, a bit error rate (BER), a used time, [and] an error frequency after reading by decoding of an error control code at a read request.” Ex. 1006 ¶ 29.

2. *Motivation to combine*

Petitioner contends that a POSITA would have been motivated to combine Lee with Kim because the references are from the same field of art and address the same challenges. Pet. 48. Petitioner contends that “Kim describes error detection and correction with a dynamically variable detection and correction capacities according to flash memory sector, bit error rate, and memory age.” *Id.* Petitioner asserts that, “[i]n light of Lee’s recognition of the need for more efficient and optimized error correction, a POSITA would have been motivated to implement the dynamic code rate modification of Kim in the flash memory system of Lee to achieve Kim’s stated benefits of improving transmission efficiency and optimizing overhead.” Pet. 48–49 (citing Ex. 1002 ¶ 179; Ex. 1004, 1:50–54).

Patent Owner asserts that Petitioner relies on “generic motivations” and a “naked conclusion.” Prelim. Resp. 36, 38. Patent Owner argues that Petitioner fails to show that Kim’s dynamic code-rate modification is compatible with Lee’s coding system or how Kim’s method could be implemented in Lee’s system. *Id.* at 37. Patent Owner asserts that “Petitioner does not explain how Kim’s code rate controlling block would interact with multiple error detection modules.” *Id.*

After considering the parties’ arguments and evidence, we determine that, for purposes of institution, Petitioner has adequately shown a motivation to combine the teachings of Lee and Kim. Petitioner relies on Dr. Koralek’s opinion that “a POSITA would have been motivated to implement the dynamic code rate modification and error rate monitoring of Kim into the flash memory system of Lee to achieve Kim’s stated benefits of improving transmission efficiency and optimizing overhead.” Ex. 1002 ¶ 178; Pet. 48–49. Dr. Koralek’s opinion appears to be adequately

supported by the cited disclosures of Kim, including Kim’s discussion of the disadvantages of using low code rates (bad transmission efficiency) and constant code rates (difficulty of optimizing the overhead of error control encoding). Ex. 1006 ¶ 5. Further support is provided by Kim’s disclosure that “it is possible to optimize the overhead of the error control encoding by changing a code rate . . . according to a memory state (or, a state of the data processing system).” *Id.* ¶ 31. At this stage of the proceeding, we do not see evidence of incompatibility between the systems of Lee and Kim.

3. Claims 3, 10–12, 16, 18, and 23–25

At this stage, Patent Owner does not dispute Petitioner’s contention that Kim discloses the limitations of claims 3 and 10–12, which depend directly or indirectly from claim 1; claim 16, which depends from claim 15; and claims 18 and 23–25, which depend from claim 17. Pet. 39–47. We note that Petitioner’s arguments and evidence for dependent claims 3 and 10–12 (Pet. 39–45) do not remedy the deficiency in Petitioner’s challenge to independent claim 1, as discussed above.

4. Conclusion

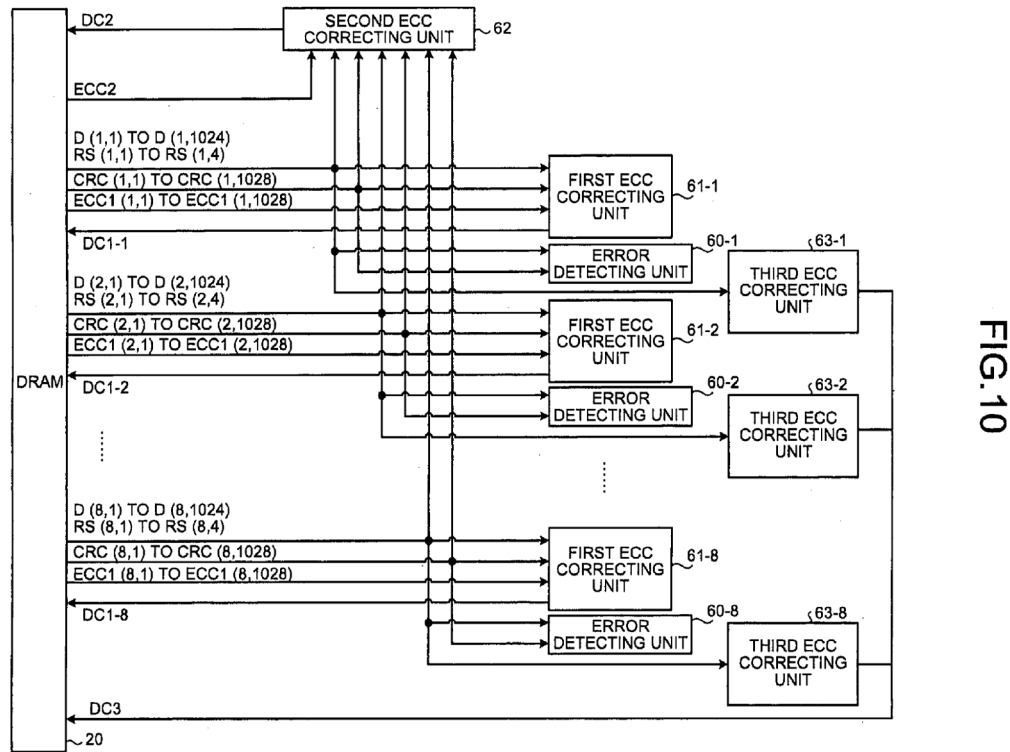
We determine that Petitioner has established a reasonable likelihood of prevailing on its challenge to claims 16, 18, and 23–25 based on Lee and Kim, but has not established a reasonable likelihood of prevailing on its challenge to claims 3 and 10–12 based on Lee and Kim.

G. Petitioner’s Challenges Based on Yamaga Alone

Petitioner challenges claims 1, 13–15, and 17 as anticipated by or obvious in view of Yamaga. Pet. 49–68. Patent Owner opposes. Prelim. Resp. 38–53. We provide an overview of Yamaga before turning to our analysis, which focuses on a disputed issue common to claims 1, 15, and 17.

1. Yamaga (Ex. 1005)

Yamaga discloses an “error correction code (ECC) circuit of a solid state drive (SSD).” Ex. 1005, code (57). Figure 10 is reproduced below.

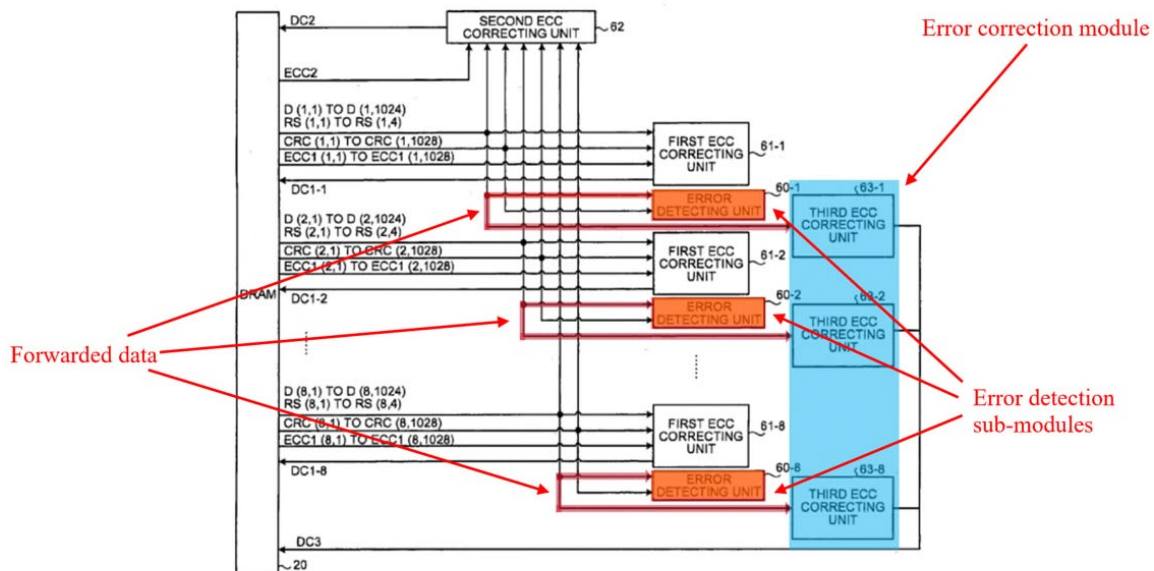


Yamaga’s Figure 10 shows a decoding system in an ECC circuit. Ex. 1005, 3:18–19, 10:15–16. As shown in Figure 10, the ECC circuit communicates with DRAM 20 and includes eight error detecting units 60-1 to 60-8, eight first ECC correcting units 61-1 to 61-8, second ECC correcting unit 62, and eight third ECC correcting units 63-1 to 63-8. *Id.* at 10:18–28.

2. Alleged Anticipation of Claims 1, 15, and 17

Claims 1, 15, and 17 recite that “each error detection sub-module [is] configured to: . . . forward the portion of the respective received stream containing an error to an error correction module” (hereinafter “the forward limitation”). Ex. 1001, 10:54–55, 10:60–61 (claim 1); *id.* at 12:34–35, 38–40 (claim 15); *id.* at 12:54–55, 58–59 (claim 17).

Petitioner contends provides the following annotation of Yamaga's Figure 10 as support for its contention that Yamaga discloses the forward limitation.



Pet. 56. Yamaga's Figure 10 shows a decoding system. Petitioner's annotations identify (1) error detecting units 60-1 to 60-8 as "error detection submodules," (2) third ECC correcting units 63-1 to 63-8 as an "error correction module," and (3) the bidirectional arrows between (1) and (2) as "forwarded data." *Id.* Petitioner contends that "a POSITA would understand [Yamaga's] disclosure and the bidirectional arrows of FIG. 10 . . . to disclose forwarding the portion of the data containing an error from the error detecting units to the third error correcting units." *Id.* (citing Ex. 1002 ¶ 230; Ex. 1005, code (57), 6:61–67). Petitioner contends that Yamaga discloses a multi-step error correction process in which data containing an error is forwarded from the error detecting units to the second error correcting unit and the third error correcting units. Pet. 57 (citing

Ex. 1002 ¶¶ 228–232; Ex. 1005, code (57), 6:61–67). Petitioner relies on the same analysis for claims 15 and 17 as it presents for claim 1. Pet. 67–68.

Patent Owner argues that “Petitioner’s identified ‘error detection sub-modules’ do not ‘forward the portion of the respective received stream containing an error to an error correction module,’” as recited in claims 1, 15, and 17. Prelim. Resp. 45–49. According to Patent Owner, the bidirectional arrows Petitioner identifies in Yamaga’s Figure 10 represent “error information,” not “actual data containing an error.” *Id.* at 46. Patent Owner argues that “Yamaga is explicit that data is never sent directly from the error detecting unit to an error-correcting unit.” *Id.* at 49 (referencing Ex. 1005, 11:67–12:14, Fig. 10).

After considering the parties’ arguments and evidence, we are concerned that Petitioner does not show sufficiently that Yamaga discloses the forward limitation. Based on the current record, Patent Owner appears to be correct that the bidirectional arrows Petitioner identifies in Yamaga’s Figure 10 represent error information, not data containing an error.

Yamaga discloses a first error detection operation in which first error-corrected data blocks are transferred to error detecting units 60-1 to 60-8, which “generate first error information S1 to S8,” which “are transferred to the second ECC correcting unit 62.” Ex. 1005, 11:50–67. According to Yamaga, “[i]f the error detecting units 60-1 to 60-8 detect that errors exist in data blocks D respectively, then the data blocks D before being corrected, but not the first error-corrected data DC1-1 to DC1-8, are transferred to the second ECC correcting unit 62.” *Id.* at 11:67–12:4.

Yamaga discloses a second error detection operation in which second error-corrected data blocks are transferred to “error detecting units 60-1 to 60-8,” which “generate second error information S1 to S8,” which “are

transferred to the third ECC correcting units 63-1 to 63-8, respectively.”

Ex. 1005, 12:39–56. According to Yamaga, “if there are data blocks D in which errors exist as results of detection by the error detecting units 60-1 to 60-8, then the data blocks D before being corrected, but not the second error-corrected data DC 2, are transferred to the third ECC correcting units 63-1 to 63-8 respectively.” *Id.* at 12:56–62.

For both the first and second error detection operations, Yamaga explains that the data before being corrected contains less error than the data that has undergone error correction. Ex. 1005, 12:4–14, 12:62–13:4. Thus, although Yamaga discloses error detecting units that detect whether a received data stream contains an error, at this stage of the proceeding, Petitioner does not direct us to disclosure sufficient to show that Yamaga’s error detecting units forward an error-containing portion of the data stream to an error correction module.

Petitioner cites Yamaga’s Abstract, which discloses:

An error correction code (ECC) circuit of a solid state drive (SSD) performs first error correction on read data using a first error correction code (Hamming code), and further performs second error correction on the result of the first error correction using a second error correction code (BHC code). Furthermore, the ECC circuit performs third error correction on the result of the second error correction using a third error correction code (RS code).

Ex. 1005, code (57); Pet. 55–57. The Abstract does not mention error detecting units and does not disclose the forward limitation.

Petitioner also cites the following disclosure in Yamaga:

First, error correction (first error correction) is performed on a data block D basis (A). Next, column-by-column error correction (second error correction of a first round) is performed on data blocks D in which an error or errors cannot be corrected

(B). Further, row-by-row error correction (third error correction of the first round) is performed on data blocks D in which an error or errors cannot be corrected (C). Column-by-column error correction (second error correction of a second round) is again performed on data blocks D in which an error or errors cannot be corrected (D). Further, row-by-row error correction (third error correction of the second round) is performed on data blocks D in which an error or errors cannot be corrected (E). With these operations, data with no error are decoded (F).

As explained above, in the first embodiment, the error correction (first error correction) is first performed on the data block basis. If there is any data block in which an error cannot be corrected, the column-by-column error correction (second error correction) and the row-by-row error correction (third error correction) are alternately repeated until the error is eliminated, and data with no error are decoded.

Ex. 1005, 6:47–67; Pet. 55. Again, the foregoing passage does not mention error detecting units and does not disclose the forward limitation.

Petitioner also relies on the bidirectional arrows labeled “forwarded data” in its annotation of Yamaga’s Figure 10. Pet. 56. As discussed above, however, Yamaga’s description of the data flow indicates that the bidirectional arrows are not sufficient to support Petitioner’s contention. We have also considered the cited portions of Dr. Koralek’s testimony (Ex. 1002 ¶¶ 228–232), which lacks sufficient support in Yamaga for the same reasons. The parties are invited to address this issue at trial.

3. Alleged Obviousness of Claims 1, 15, and 17

Petitioner contends that Yamaga renders the forward limitation obvious in view of the knowledge of a POSITA. Pet. 57. According to Petitioner, a “POSITA would be motivated to modify Yamaga’s system to:

- (1) include an error detection step prior to the first error correction step; and
- (2) forward the error-containing data from the error detecting unit to the first

error correction unit.” *Id.* (citing Ex. 1002 ¶ 233). Petitioner contends that “including error detection prior to error correction was widely known” and would result in power savings. Pet. 58 (Ex. 1002 ¶¶ 233–239; Ex. 1005, 1:66–2:2, 15:13–23). Petitioner proposes two alternative ways to make this modification. *Id.* “First, data blocks could be read from DRAM 20 into the error detecting units 60-1 to 60-8 prior to any error correction.” *Id.* (citing Ex. 1002 ¶ 237). “Second, . . . additional error detecting units [could be included] between DRAM 20 and first ECC units 61-1 to 60-8.” Pet. 59 (citing Ex. 1002 ¶ 238). In both instances, Petitioner contends that the error detecting units would forward those data blocks containing errors to first ECC correcting units 61-1 to 61-8. *Id.*

Patent Owner argues that “Petitioner’s first modification changes the type of error detection performed by the error detecting units” in Yamaga. Prelim. Resp. 50. According to Patent Owner, “Yamaga expressly teaches away from the Petitioner’s second modification to have the error detecting unit forward data to an ECC correcting unit after error detection.” *Id.* at 51 (citing Ex. 1005, 12:4–10, 12:56–13:4).

After considering the parties’ arguments and evidence, we are not sufficiently persuaded by Petitioner’s contention that a “POSITA would be motivated to modify Yamaga’s system to: (1) include an error detection step prior to the first error correction step; and (2) forward the error-containing data from the error detecting unit to the first error correction unit.” Pet. 57 (citing Ex. 1002 ¶ 233). Although Petitioner asserts that adding an error detection step prior to the first error correction would result in fewer first ECC operations, error detection for a smaller number of data blocks, and power savings (Pet. 58; Ex. 1002 ¶¶ 235–236), Petitioner does not on this record appear to show a sufficient reason or motivation for making the

second proposed modification. Petitioner does not attempt to show that forwarding error-containing data from the error detecting unit to the first error correction unit would provide any advantage over Yamaga's method in which the second ECC correcting unit and third ECC correcting units operate on "the data before being corrected," which "contains less error" than the corrected data. Ex. 1005, 11:50–12:14, 12:39–13:4. The parties are invited to address this issue at trial.

4. Dependent Claims 13 and 14

At this stage, Patent Owner does not separately dispute Petitioner's contention that Yamaga discloses the limitations of claims 13 and 14, which depend from claim 1. Pet. 62–63. We note that Petitioner's arguments and evidence for dependent claims 13 and 14 (Pet. 62–63) do not remedy the deficiencies in Petitioner's challenge to independent claim 1, as discussed above.

5. Conclusion

We determine that Petitioner has not established a reasonable likelihood of prevailing on its challenges to claims 1, 13–15, and 17 based on Yamaga.

H. Petitioner's Remaining Challenges

Petitioner challenges dependent claims 2, 4, 8, and 19 based on Yamaga and JO and dependent claims 3, 10–12, 16, 18, 23–25 based on Yamaga, JO, and Kim. Pet. 68–80. Patent Owner disputes Petitioner's contentions regarding a motivation to combine Yamaga and JO, arguing that Petitioner's combination does not make sense in view of operational differences between the error detectors in the two references. Prelim. Resp. 55–56; *see* Pet. 74 (addressing motivation to combine). At this stage

of the proceeding, it appears that Patent Owner's arguments have some merit. We also note that Petitioner's arguments and evidence for dependent claims 3, 10–12, 16, 18, 23–25 do not appear to remedy the shortcomings in Petitioner's challenges to independent claims 1, 15, and 17 based on Yamaga alone, nor the shortcomings in Petitioner's challenges to dependent claims 4, 8, and 19 based on JO. We determine that Petitioner has not established a reasonable likelihood of prevailing on its challenges to claims 2, 4, 8, and 19 based on Yamaga and JO and dependent claims 3, 10–12, 16, 18, 23–25 based on Yamaga, JO, and Kim.

IV. CONCLUSION

After considering the Petition and the Preliminary Response, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that at least one challenged claim of the '700 Patent is unpatentable. Accordingly, we institute an *inter partes* review of all challenged claims on all grounds asserted in the Petition. 37 C.F.R. §§ 42.107(e), 42.108(a). *See* Guidance on the Impact of SAS on AIA Trial Proceedings (April 26, 2018);⁹ *see also SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

⁹ Available at <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>.

V. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–4, 8, 10–19, and 23–25 of the '700 Patent is instituted commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

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