

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA CORPORATION and KIOXIA AMERICA, INC.,
Petitioner,

v.

VIASAT, INC.,
Patent Owner.

IPR2022-01067
Patent 8,615,700 B2

Before THU A. DANG, KEVIN F. TURNER, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Kioxia Corporation and Kioxia America, Inc. (collectively, “Kioxia” or “Petitioner”) filed a Petition (Paper 1, “Pet.”) seeking an *inter partes* review of claims 1–4, 8, 10–19, and 23–25 (the “challenged claims”) of U.S. Patent No. 8,615,700 B2 (Ex. 1001, “the ’700 Patent”). Viasat, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 15 (“Prelim. Resp.”). We instituted an *inter partes* review. Paper 17 (“Institution Decision” or “Inst. Dec.”).

After institution, Patent Owner filed a Patent Owner Response (Paper 19, “PO Resp.”), Petitioner filed a Reply (Paper 22, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 25, “PO Sur-reply”). We held an oral hearing on August 30, 2023, and a transcript is in the record. Paper 33 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We determine that Petitioner has not shown by a preponderance of the evidence that the challenged claims of the ’700 Patent are unpatentable. Briefly, in summary, Petitioner’s challenges based in whole or in part on Lee do not succeed because Petitioner does not show that Lee discloses a decoding module or the functions of a decoder as recited in the challenged independent claims. Petitioner dropped its Yamaga anticipation challenge, and its challenges based wholly or partially on that reference do not succeed because Petitioner does not show that Yamaga discloses the forward limitation of the challenged claims or that it would have been obvious to modify Yamaga to include an error detection step prior to the first error correction step and to

forward error-containing data from the error detecting units to the first error correcting units.

B. Related Matters

The parties identify the following district court cases as related matters: *Viasat, Inc. v. Kioxia Corp.*, No. 6:21-CV-01231-ADA (W.D. Tex.) (the “parallel district court litigation”) and *Viasat, Inc. v. Western Digital Corp.*, No. 6:21-CV-01230-ADA (W.D. Tex.). Pet. 1; Paper 5, 1 (Patent Owner’s mandatory notices).

In IPR2022-01126, the ’700 Patent is being challenged by Western Digital Technologies, Inc., and Kioxia has been joined as an understudy petitioner.

C. The ’700 Patent (Ex. 1001)

The ’700 Patent was issued from an application filed August 18, 2010. Ex. 1001, code (22). Petitioner contends that the ’700 Patent claims are not entitled to the August 18, 2009 filing date of an earlier provisional application. *Id.* at code (60); Pet. 6. Patent Owner does not dispute Petitioner’s contention.

The ’700 Patent discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57), 1:30–31, 2:27–28. According to the ’700 Patent, “[e]ncoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded).” *Id.* at 1:31–33. The data streams are processed at a number of error detection sub-modules, which forward an error-containing portion of the data stream to an error correction module, which corrects the forwarded portion. *Id.* at 1:33–41.

An embodiment is shown in Figure 3, reproduced below.

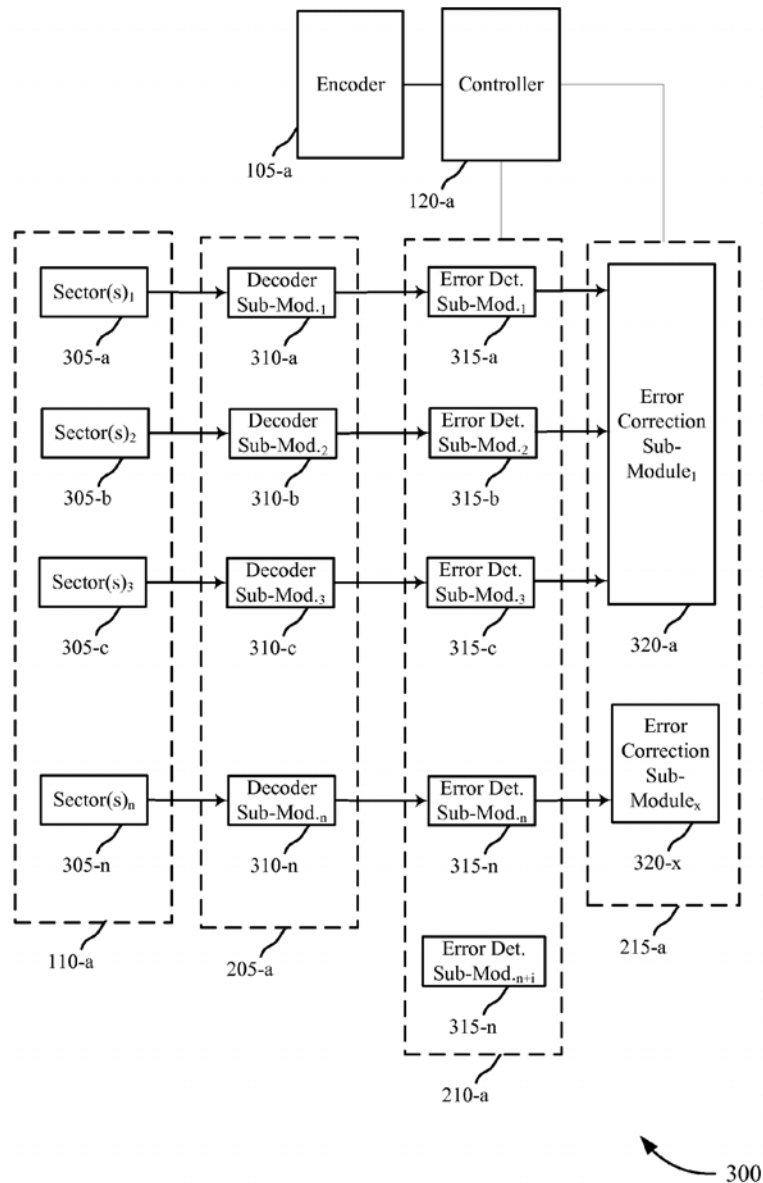


FIG. 3

Figure 3 “is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules.” Ex. 1001, 2:8–10, 6:29–32.

As shown in Figure 3, flash memory decoder system 300 includes flash memory 110-a, decoder module 205-a, error detection module 210-a, error correction module 215-a, controller 120-a, and encoder 105-a. Ex. 1001, 6:33–37. Flash memory 110-a includes a number of different sets of one or more active sectors 305. *Id.* at 6:39–40. Decoder module 205-a

includes a number of decoder sub-modules 310, each of which may be associated with a different set of sectors 305. *Id.* at 6:40–43. Error detection module 210-a includes a number of error detection sub-modules 315, each of which may be associated with a different set of sectors 305. *Id.* at 6:43–46. For example, encoded data may be read from a set of one or more of sectors 305-a by decoder sub-module 310-a, and processed (e.g., buffered, de-interleaved, and decoded to some extent) to generate a data stream, which may be forwarded to error detection sub-module 315-a. *Id.* at 6:46–52.

According to the '700 Patent, each error detection sub-module 315 evaluates a data stream to determine whether it contains an error and forwards the portion of the stream containing an error to error correction module 215-a. Ex. 1001, 6:61–67. Error correction module 215-a includes a number of error correction sub-modules 320, each of which handles errors from a number of error detection sub-modules 315 and corrects the portions of the data streams containing an error. *Id.* at 6:67–7:7.

D. Illustrative Claims

The '700 Patent includes three independent claims, which are reproduced below with Petitioner's bracketed claim element designations added and paragraphs adjusted.

1. A flash memory decoder comprising:

[1a] a decoding module configured to: receive encoded data from the flash memory; and

[1b] decode the received encoded data to generate a plurality of partially decoded data streams;

[1c] an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel, each error detection

sub-module configured to: receive a different one of the plurality of partially decoded data streams;

[1c] detect whether a portion of the respective received stream contains an error; and

[1e] forward the portion of the respective received stream containing an error to an error correction module; and

[1f] the error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

Ex. 1001, 10:47–65; Pet. 19–27.

15. A system comprising:

[15a] an encoder configured to encode data for storage on a flash memory;

[15b] the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

[15c] a decoder, communicatively coupled with the flash memory, and configured to: retrieve the encoded data from flash memory to generate a plurality of data streams; and

[15d] process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams,

[15e] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[15f] forward the portion of the respective received stream containing an error to an error correction module of the decoder; and

[15g] correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:21–44; Pet. 31–33.

17. A method comprising:

[17a] receiving encoded data from a flash memory comprising a plurality of data streams;

[17b] processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams,

[17c] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[17e] forward the portion of the respective received stream containing an error to an error correction module; and

[17f] correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:49–63; Pet. 33–35.

E. Asserted Challenges and Evidence

Petitioner asserts the following challenges to patentability:

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 2, 13–15, 17	102(e)	Lee ²

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the ’700 Patent was issued on an application filed before that date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

² Ex. 1004, US 7,865,809 B1, filed July 1, 2008 and issued January 4, 2011 (“Lee”).

Claims Challenged	35 U.S.C. §¹	Reference(s)/Basis
4, 8, 19	103(a)	Lee, Jo ³
3, 10–12, 16, 18, 23–25	103(a)	Lee, Kim ⁴
1, 13–15, 17	102(e)	Yamaga ⁵
1, 13–15, 17	103(a)	Yamaga
2, 4, 8, 19	103(a)	Yamaga, Jo
3, 10–12, 16, 18, 23–25	103(a)	Yamaga, Jo, Kim

Pet. 3.

F. Testimonial Evidence

The record includes two declarations of Richard Koralek, Ph.D. submitted by Petitioner (Exs. 1002, 1024) and Dr. Koralek’s deposition testimony submitted by Patent Owner (Exs. 2023, 2026). The record also includes the declaration of Nader Bagherzadeh, Ph.D. submitted by Patent Owner (Ex. 2022) and Dr. Bagherzadeh’s deposition testimony submitted by Petitioner (Ex. 1019).

³ Ex. 1007, US 2009/0063934 A1, filed August 27, 2008 and published March 5, 2009 (“Jo”). Petitioner asserts that Jo is prior art to the ’700 Patent under 35 U.S.C. §§ 102(a) and 102(e). Pet. 10.

⁴ Ex. 1006, US 2010/0241928 A1, filed March 3, 2010 and published September 23, 2010 (“Kim”). Petitioner asserts that Kim is prior art under 35 U.S.C. § 102(e). Pet. 12.

⁵ Ex. 1005, US 8,086,933 B2, filed September 19, 2008 and issued December 27, 2011 (“Yamaga”). Petitioner asserts that Yamaga is prior art to the ’700 Patent under 35 U.S.C. § 102(e). Pet. 8.

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is anticipated under 35 U.S.C. § 102 only if “each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented,⁶ objective evidence of

⁶ Here, neither party presents evidence of secondary considerations.

nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had a Master’s degree in electrical engineering or an equivalent field and two years of academic or industry experience working with error correction in memory devices.” Pet. 14 (citing Ex. 1002 ¶ 19).

Patent Owner argues that a POSITA “would have had at least a [bachelor of science degree] in electrical engineering, computer engineering, or computer science or a related field, and at least two years of experience in the design, development, or research of the hardware implementation of error correction systems.” PO Resp. 3 (citing Ex. 2022 ¶¶ 27–31, 64–88). According to Patent Owner, “[a]dvanced education may substitute for experience and vice versa.” *Id.*

The parties' articulations of the level of ordinary skill in the art are similar, and we adopt parts of each party's description of a POSITA's education and experience. We agree with Patent Owner that computer engineering and computer science are relevant fields of study. PO Resp. 3. Our finding is supported by the '700 Patent, which describes systems, devices, methods, and software for forward error correction for a flash memory system, which may be integrated with a computer, server, or other computing device. Ex. 1001, 3:23–30. Although Dr. Koralek testifies that an undergraduate education would not have been sufficient for a person to acquire ordinary skill in the art relating the '700 Patent (Ex. 1024 ¶¶ 7–9), that testimony does not adequately account for the knowledge relating to error correction a person could acquire through practical experience. For this reason, we agree with Patent Owner and Dr. Bagherzadeh that a bachelor of science is the appropriate level of education. PO Resp. 3; Ex. 2022 ¶ 31. We disagree with Patent Owner's assertion that a POSITA's experience would have been limited to "hardware implementation." PO Resp. 3. Our finding is supported by the '700 Patent, which states that "embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof." Ex. 1001, 10:26–28.

For these reasons, we find that a POSITA would have had a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and two years of academic or industry experience in the design, development, or research of error correction in memory devices.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below we address the parties’ dispute about the meaning of one phrase in claim 1. We do not need to provide an express construction for any other claim term for purposes of resolving the controversy before us.

“decode the received encoded data to generate a plurality of partially decoded data streams” (claim 1)

Petitioner contends that this phrase means “buffer the received encoded data, de-interleave the received encoded data, or distinguish error correction bits from information bits in the received encoded data, to generate a plurality of data streams.” Pet. 14–15.

In the Institution Decision, we agreed with Patent Owner that “decode” requires more than just buffering. Inst. Dec. 18. We construed the phrase “decode the received encoded data” to mean “distinguish error

correction bits from information bits in the received encoded data,” which corresponds to a portion of Petitioner’s proposed construction that was not disputed by Patent Owner. *Id.* at 18–19.

Patent Owner agrees with the claim construction in the Institution Decision, arguing that the phrase, “decode the received encoded data,” (1) “cannot be satisfied by mere buffering;” and (2) “can be satisfied by distinguishing error correction bits from information bits in the received encoded data.” PO Resp. 4.

Petitioner disagrees with the Board’s preliminary construction, arguing that Petitioner’s proposed construction is the only one supported by the Specification. Pet. Reply 2–3.

After considering the parties’ submissions, we are persuaded that the construction in the Institution Decision is correct.

First, we agree with Patent Owner that “decode” requires more than just buffering. PO Resp. 4, 6–8; PO Sur-reply 1–2. Nothing in the claim language or the Specification supports that “decoding” can mean mere buffering. Petitioner relies on two sentences in the ’700 Patent.

In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, an[d] thereby generate decoded (or partially decoded) data streams.

Ex. 1001, 6:11–14 (cited at Pet. 15; Pet. Reply 2).

Thus, encoded data may be read from a set of one or more of sectors 305 (e.g., sector(s) 305-a) by a decoder sub-module 310 (e.g., decoder sub-module 310-a), and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream.

Id. at 6:46–50 (cited at Pet. Reply 2).

The sentences quoted above are the only instances where buffering is mentioned in the Specification. In each instance, buffering is disclosed along with de-interleaving and decoding as actions performed by a decoder module or sub-module. The Specification's disclosure that a decoder module can buffer data does not mean that buffering alone can constitute decoding. Nowhere does the Specification define "decode" to mean just "buffer." The Specification's use of the disjunctive, "or," to connect these words (Ex. 1001, 6:11–14) is not enough to redefine the word "decode" to encompass buffering alone. Petitioner agrees that "[t]he '700 Patent does not *define* the word 'decode.'" Pet. Reply 2.

"Absent lexicography or disavowal, we do not depart from the plain meaning of the claims." *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (citing *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)). "The standards for finding lexicography and disavowal are 'exacting.'" *Id.* (quoting *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014)). In this case, defining "decode" to encompass mere buffering would be a departure from the plain and ordinary meaning of the term as understood by a POSITA. Petitioner's expert, Dr. Koralek, agrees that, "aside from the '700 patent, what a person of ordinary skill would understand decode to mean, it would not be just buffering. Decoding might include buffering, but buffering by itself would not be considered decoding to a person of ordinary skill." Ex. 2023, 73:14–20. As Petitioner recognizes, "it is undisputed that 'decoding' is the opposite of 'encoding.'" Pet. Reply 7 (citing Ex. 1019, 56:5–11); *see also* PO Resp. 7 ("The plain meaning of 'decode' implies undoing or reversing some prior encoding."). This undisputed meaning is supported by the expert testimony, as well as dictionary definitions provided

by Patent Owner. Ex. 1024 ¶ 51 (“[A] POSITA would understand that decoding is the inverse operation of encoding.”); Ex. 2022 ¶ 103 (“[A] POSITA would understand that to ‘decode’ generally means to undo or reverse the effects of some previous encoding.”); Ex. 2024 (IBM Dictionary of Computing: “decode: (1) To convert data by reversing the effect of some previous encoding.”); Ex. 2025 (IEEE Dictionary, similar definition); *see* PO Resp. 7 (relying on these definitions); Ex. 2022 ¶ 97 (same).

The ’700 Patent describes “encoding” as “adding parity information” to data to be stored in flash memory. Ex. 1001, 3:46–48.⁷ Mere buffering would not undo or reverse any previous encoding and would not be sufficient, by itself, to constitute decoding. Ex. 2022 ¶ 103. Our finding is supported by a dictionary definition of “buffer” relied upon by both parties’ experts. Ex. 1012 (Microsoft Computer Dictionary, Fifth Edition, 2002: “to use a region of memory to hold data that is waiting to be transferred, especially to or from input/output (I/O) devices such as disk drives and serial ports.”); Ex. 1002 ¶ 218 (quoting this definition); Ex. 2022 ¶ 97 (same); *see also* PO Resp. 13 (citing Ex. 1012).

Second, we agree with Patent Owner that “decoding” can be satisfied by distinguishing error correction bits from information bits in the received encoded data, which is the construction we adopted in the Institution Decision. Inst. Dec. 19; PO Resp. 4. Patent Owner and its expert explain that, in the context of the ’700 Patent, a POSITA would have understood that decoding includes distinguishing error correction bits from information bits. PO Resp. 5–6; Ex. 2022 ¶¶ 104, 105. According to Dr. Bagherzadeh, some

⁷ We understand that “parity information” refers to parity bits or error correction code (“ECC”) bits that are added to data to make a codeword. Ex. 1002 ¶ 70; Ex. 2023, 33:16–34:16.

error correction systems do not require that ECC bits be stored together with the related data bits and that such systems must distinguish the data bits from the ECC bits before performing error detection or correction. Ex. 2022

¶ 104. Dr. Koralek agrees that storing error correction bits at the end of an entire page of information bits, i.e., separately from the related data bits, was a known method of storing encoded data. Ex. 1024 ¶ 46 (citing Ex. 1021⁸). Claim 1 recites that a “decoding module” is configured to “decode the received encoded data to generate a plurality of partially decoded data streams.” Ex. 1001, 10:48–51. Dr. Bagherzadeh explains:

If a given data stream does not include all the ECC bits associated with the data bits in the stream, error detection and correction may not be possible. Thus, where data bits and ECC bits are not stored together, they must be distinguished and associated—and included within the same data stream—in order for error detection and correction to occur.

Ex. 2022 ¶ 105. Dr. Koralek agrees that, when “data coming from a flash memory includes both data bits and error-correction bits, . . . for the purposes of error detection and correction, you have to know which error-correction bits are associated with which data bits.” Ex. 2023, 63:18–64:5.

Petitioner does not disagree that “decoding” can be satisfied by distinguishing error correction bits from information bits in the received encoded data. In fact, that is one of the alternatives in Petitioner’s proposed construction. Pet. 14–15. Instead, Petitioner argues that “[i]t would be improper to limit ‘decoding’ to *only* ‘distinguish[ing]’ between error correction and information bits[] to the exclusion of other examples of

⁸ Micron Technology, Inc., *NAND Flash 101: An Introduction to NAND Flash and How to Design It In to Your Next Product*, Technical Note 29–19 (Rev. B, April 2010) (“Micron”).

‘decoding’ in the specification.” Pet. Reply 2–3 (second alteration in original). Consistent with the Institution Decision, we do not limit the term “decoding” to only distinguishing between error correction and information bits to the exclusion of other examples of decoding. Inst. Dec. 19. But other examples of decoding are not relevant to the parties’ dispute because Petitioner does not attempt to prove its case based on any definition of “decoding” other than mere buffering or distinguishing between error correction and information bits. *See, e.g.*, Pet. 20–22 (addressing claim element [1b] and Lee); Pet. Reply 3–8 (same). Therefore, for purposes of resolving the parties’ dispute in this proceeding, it is unnecessary to include other examples of “decoding” in the claim construction.⁹

For the reasons discussed above, “decoding” is not satisfied by mere buffering. Because the parties agree that “decoding” can be satisfied by distinguishing error correction bits from information bits, that is how we construe “decoding” for purposes of resolving the parties’ dispute in this proceeding. Accordingly, consistent with the Institution Decision, we construe the phrase “decode the received encoded data” to mean “distinguish error correction bits from information bits in the received encoded data.”

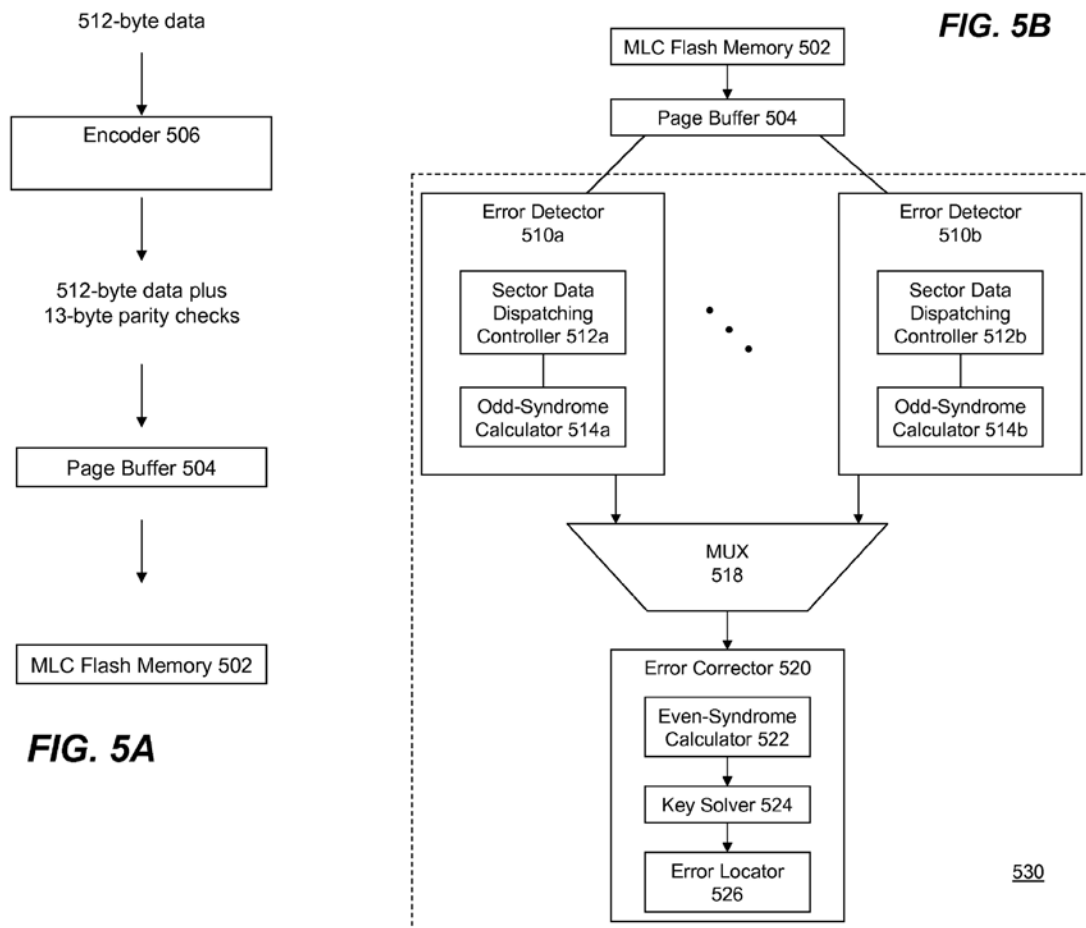
⁹ In our final written decision in the related *inter partes* review, we hold that the term “partially decoded” is broad enough to encompass intra-channel rearrangement (descrambling) and inter-channel rearrangement (de-interleaving). IPR2022-01126, Paper 32 at 15. For purposes of this proceeding, however, it is unnecessary to include these examples of “decoding” in the claim construction because Petitioner does not rely on either of them to prove its unpatentability challenges.

D. Petitioner's Lee Anticipation Challenge

Petitioner challenges claims 1, 2, 13–15, and 17 as anticipated by Lee. Pet. 19–35. Patent Owner opposes. PO Resp. 10–28. We provide an overview of Lee before turning to our analysis.

1. Lee (Ex. 1004)

Lee discloses data error detection and correction in non-volatile memory devices such as flash memory devices. Ex. 1004, code (57), 1:25–32, 1:65–66. Figures 5A and 5B are reproduced below.



Lee's Figures 5A and 5B show an encoder and a decoder, respectively, in an error corrector of a non-volatile memory device. Ex. 1004, 3:34–39.

As shown in Figure 5A, ECC encoder 506 encodes a chunk of data (e.g., 512-byte sector) to a codeword (e.g., 525-byte data plus ECC or parity checks). Ex. 1004, 8:44–49. Upon creation, the codeword is stored into page buffer 504 then to the non-volatile memory (e.g., multi-level cell (“MLC”) flash memory 502). *Id.* at 8:53–55.

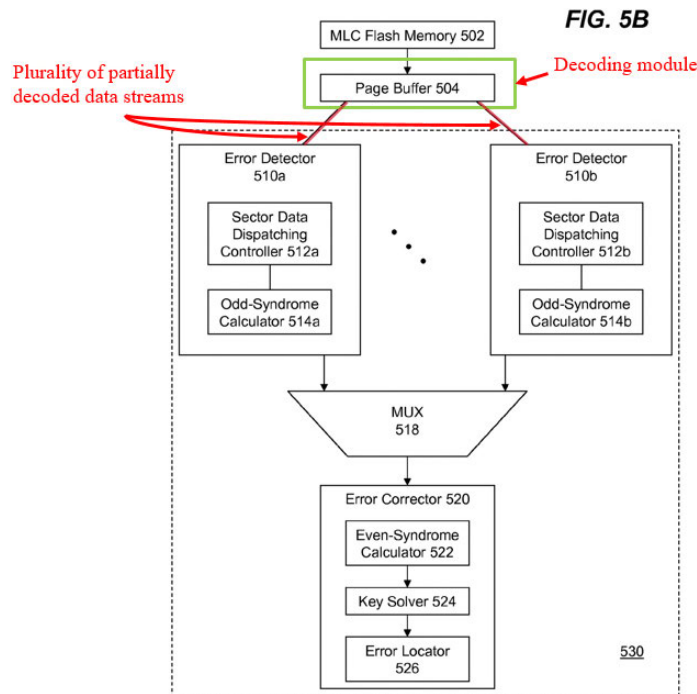
As shown in Figure 5B, error decoder 530 comprises a plurality of data error detectors 510a-b coupled via multiplexer (“MUX”) 518 to error corrector 520. Ex. 1004, 8:56–61. “Each data error detector 510a-b is configured to process a chunk of data (e.g., 512-byte data sector)” in parallel with the other data error detectors 510a-b. *Id.* at 8:61–65. Data error detector 510 includes sector data dispatching controller 512 and odd-syndrome calculator 514. *Id.* at 8:65–67. Sector data dispatching controller 512 “is configured for receiving appropriate data sector,” while odd-syndrome calculator 514 is “for computing the odd terms of syndrome polynomial of the received codeword.” *Id.* at 8:67–9:4. If “data error detectors 510a-b determine that there is no error in the received data,” then “error corrector 520 stops processing further and moves on to the next chunk of data.” *Id.* at 9:4–6. “If, however, data error detectors 510a-b detect data error in the received data,” then “error corrector 520 is configured to process additional error location and correction.” *Id.* at 9:7–9. According to Lee, “[t]here is only one error corrector 520 for the set of data error detectors 510a-b.” *Id.* at 9:9–11.

2. Claim 1

Our analysis focuses on the portion of claim 1 that recites “[1a] a decoding module configured to receive encoded data from the flash memory; and [1b] decode the received encoded data to generate a plurality

of partially decoded data streams.” Ex. 1001, 10:48–51 (bracketed designations added).

To show claim element [1b], Petitioner provides the following annotation of Lee’s Figure 5B:



Pet. 21. Lee’s Figure 5B shows a decoder. Petitioner’s annotations identify page buffer 504 as a “decoding module” and the lines extending from page buffer 504 to error detectors 510a, b as a “plurality of partially decoded data streams.” *Id.* Petitioner contends that “Lee discloses buffering the received encoded data to generate a plurality of data streams.” Pet. 22.¹⁰ In addition, Petitioner contends that “the page buffer 504 must necessarily distinguish and associate page-level ECC bits with each set of sector data before sending [it] to error detectors 510a-b.” *Id.*

¹⁰ When quoting from the Petition, we omit Petitioner’s italicization of the names of the references and drawing sub-references.

Patent Owner argues that Lee's page buffer is simply a passive and temporary data repository, not a "decoding module," as recited in claim 1. PO Resp. 10–13, 17. Patent Owner disputes Petitioner's contention that Lee's page buffer distinguishes and associates page-level ECC bits with each sector of data. *Id.* at 14–17.

For the reasons discussed above, we do not adopt Petitioner's proposed construction that "decoding" can be met by mere buffering. For the same reasons, we are not persuaded by Petitioner's contentions concerning Lee's disclosures to the extent they rely on this construction. Pet. 20–22; Pet. Reply 3–4.

As discussed above, we construe the phrase, "decode the received encoded data," to mean "distinguish error correction bits from information bits in the received encoded data." We are not persuaded by Petitioner's contention that Lee's page buffer 504 performs this function. Pet. 22. Petitioner identifies Lee's page buffer 504 as the "decoding module" of claim 1 (Pet. 20–21), but does not show that page buffer 504 decodes the received encoded data by distinguishing error correction bits from information bits in the received encoded data.

Petitioner contends that Lee's page buffer 504 "must necessarily" distinguish error correction bits from information bits because, according to Petitioner, "[i]n some cases, there is one set of ECC data for a page including several data sectors" and "Lee's error detectors 510a-b each process a separate sector of data." Pet. 22 (citing Ex. 1002 ¶ 100; Ex. 1004, 7:46–61, 8:61–63). Petitioner relies on Dr. Koralek's testimony that "[i]n at least some cases, the ECC data is . . . generated at the page level, i.e., for a page of data that includes multiple data sectors." Ex. 1002 ¶ 100 (citing Ex. 1004, 7:46–61).

We are not persuaded that Lee discloses page-level encoding, as asserted by Petitioner and Dr. Koralek. Pet. 22; Pet. Reply 4–5; Ex. 1002 ¶ 100; Ex. 1024 ¶¶ 45–47; *see* PO Resp. 14 (arguing that Petitioner is “incorrect when it asserts that Lee describes encoding by page and decoding by sector.”). Petitioner and Dr. Koralek rely on the following description in Lee: “The generated ECC 321 is appended to the original data as an ECC page 322 (i.e., a data segment containing (Page+ECC) bytes).” Ex. 1004, 7:57–59; Pet. 22; Pet. Reply 4; Ex. 1002 ¶ 100; Ex. 1024 ¶ 47. We agree with Patent Owner and Dr. Bagherzadeh that the above-quoted sentence describes Lee’s Figures 3A and 3B, which show sector-level encoding, not a separate page-level encoding embodiment, as Petitioner contends. PO Resp. 15; Ex. 2022 ¶ 123; *see* Tr. 59:12–15 (Petitioner’s contention). The reference numerals in the quoted sentence refer to Lee’s Figures 3A and 3B, not a separate embodiment. Ex. 1004, 7:57–59, Figs. 3A, 3B (reference numerals 321, 322); *see* Tr. 58:17–24 (Petitioner agrees that the quoted sentence references Figures 3A and 3B).

Because it aligns with Lee’s disclosure, we credit Dr. Bagherzadeh’s testimony that “Lee’s description of ‘ECC page 322’ as ‘a data segment containing (Page + ECC bytes),’ . . . merely refers to the fact that this page includes eight sectors, each of which contains both data and ECC bits.” Ex. 2022 ¶ 123 (quoting Ex. 1004, 7:58–59). Petitioner and Dr. Koralek agree that Lee’s Figure 3B shows sector-level encoding, not page-level encoding. Tr. 59:9–11 (“JUDGE ROESEL: And that sort of page level encoding is not shown in Figures 3A and 3B. Is that right? MR. SILLIMAN: That is correct.”); *see also* Pet. Reply 4 (asserting that Figure 3B shows information bits stored contiguously with ECC bits);

Ex. 1024 ¶¶ 46, 47 (same); Ex. 2026, 183:13–21 (same). Accordingly, Petitioner has not shown that Lee discloses page-level encoding.

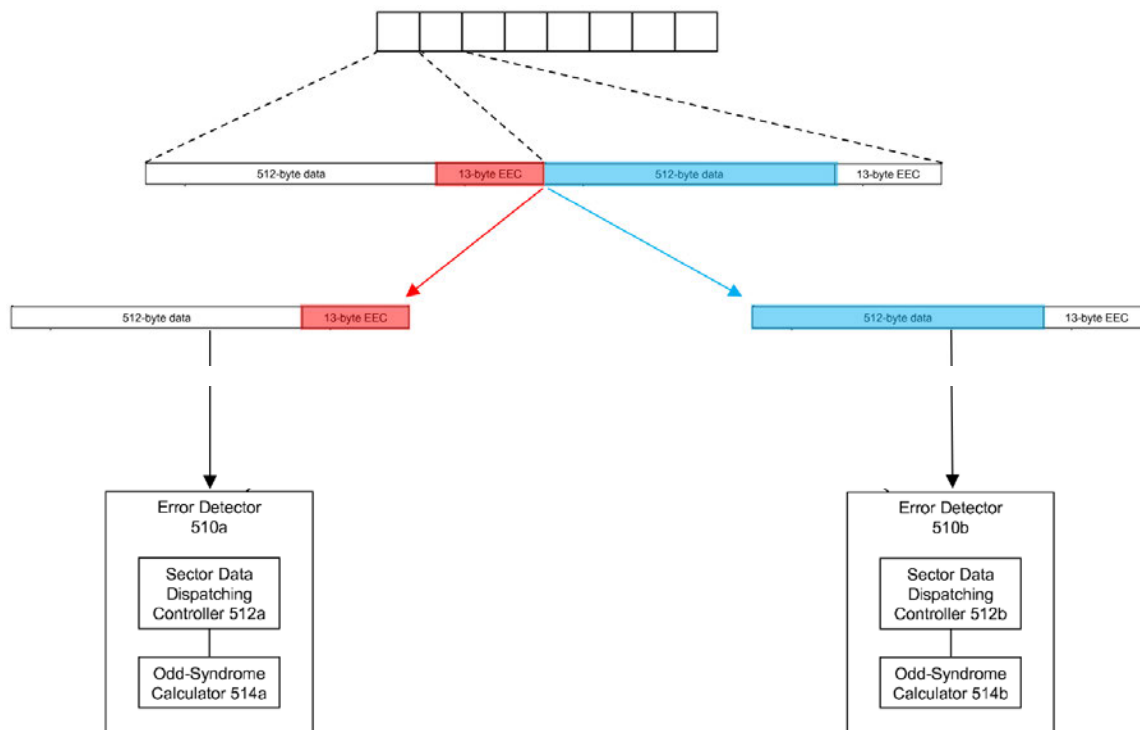
For the first time in the reply brief, Petitioner contends that “[s]toring ECC bits on a page-level rather than by sector was known before the ’700 Patent” and relies on Dr. Koralek’s opinion that “page-level encoding would have been an obvious implementation in view of Lee’s teachings.” Pet. Reply 4; Ex. 1024 ¶ 45. Petitioner’s contention presents a new theory of unpatentability based on new evidence¹¹ that exceeds the proper scope of a reply brief under 37 C.F.R. § 42.23(b). For that reason, we need not consider it.¹² Petitioner’s contention is not persuasive in any event. The challenge before us is anticipation, not obviousness. Petitioner’s new theory is not enough to show that Lee “must necessarily” distinguish error correction bits from information bits in the received encoded data, as asserted in the Petition (Pet. 22) and required by our claim construction.

¹¹ The new evidence includes Exhibit 1021 and paragraphs 45 to 47 of Dr. Koralek’s supplemental testimony, Exhibit 1024.

¹² *Yita LLC v. MacNeil IP LLC*, 69 F.4th 1356, 1366–67 (Fed. Cir. 2023) (stating “the Board acts within its discretion when it declines under section 42.23(b) to consider a new theory of unpatentability raised for the first time in reply” and holding that petitioner’s reply argument that a claim limitation would have been an obvious modification was a “meaningfully distinct contention” from the petition’s argument that the limitation was taught by the reference and that the new theory was not within the scope of a proper reply); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369–70 (Fed. Cir. 2016) (affirming Board’s decision not to consider an argument made on reply because in the original petition the challenger argued only that a reference disclosed a limitation, while in the reply the challenger argued that a relevant artisan would have considered it obvious to modify that reference to arrive at the limitation).

Furthermore, Petitioner presents no rationale for modifying Lee’s disclosure to include page-level encoding and sector-level decoding.

Petitioner’s reply brief also presents a new theory of inherent disclosure. Relying on Dr. Koralek’s testimony, Petitioner argues that Lee discloses “‘distinguishing’ error correction bits from information bits by separating the sectors of data via the page buffer.” Pet. Reply 5; Ex. 1024 ¶¶ 48–50. As support for this new theory, Petitioner and Dr. Koralek present the following modified compilation of Lee’s Figures 3B and 5B:



Pet. Reply 6; Ex. 1024 ¶ 49. Lee’s Figure 3B shows ECC data structures, and Figure 5B shows a decoder. Petitioner’s modified compilation shows adjacent codewords of a data sector being transmitted to error detectors 510a and 510b. Dr. Koralek testifies that the operation of Lee’s Figure 3B and 5B embodiments “requires the error correction information (red) . . . of the first codeword to be separated from, and therefore distinguished from, the

information bits (blue) . . . of the second codeword.” Ex. 1024 ¶ 49 (quoted at Pet. Reply 6).

Petitioner’s modified compilation of Lee’s Figures 3B and 5B and the related testimony of Dr. Koralek (Ex. 1024 ¶ 49) are new argument and new evidence that exceed the proper scope of a reply under Rule 42.23(b).¹³ Even if it were proper, Petitioner’s new theory of inherent disclosure is not persuasive. Claim 1 recites “a decoding module configured to . . . decode the received encoded data.” Ex. 1001, 10:48–51. Petitioner identifies Lee’s page buffer 504 as the “decoding module” (Pet. 20–21), but fails to show that the page buffer “decode[s]” by distinguishing error correction bits from information bits in the received encoded data. Petitioner does not show that page buffer 504 is the component responsible for separating adjacent codewords or distinguishing error correction bits from information bits in the received encoded data. Petitioner points to nothing in Lee that ascribes this function to the page buffer.

The evidence instead shows that Lee’s error detector, not the page buffer, is responsible for separating adjacent codewords. Dr. Bagherzadeh testifies that, according to a POSITA’s understanding of Lee, data is read from the page buffer “one sector at a time” and “[t]he error detector will have an address” for that sector and make an “address request” based on “some indexing mechanism” so that “error detector 510[A] you get the address location 100, error detector[5]10B you get the location 110 and so on.” Ex. 1019, 110:6–111:14; *see also* Ex. 2022 ¶ 125 (When responding to a request for a given sector of data from the page buffer, “[t]he page buffer does not need to determine which bits are ECC bits versus data bits. It

¹³ *See Yita*, 69 F.4th at 1366; *Intelligent Bio-Sys.*, 821 F.3d at 1369–70.

simply needs to provide the requested sector which—due to the organization of data that Lee discloses in Figure 3—will already include both data and ECC bits.”); *id.* ¶ 130 (in Lee, the “organization of data into ‘sectors’ means that no decoding or processing is necessary to distinguish ECC bits from data bits.”). Dr. Koralek provided similar testimony about the functionality of Lee’s page buffer, error detectors, and the sector dispatching controllers. Ex. 2023, 116:18–117:7 (“[E]ach of these sector data dispatching controller[s] is asking for a particular one of those sectors along with its ECC bytes[,] and the page buffer . . . sends out the requested data sector plus the associated ECC bytes.”). The foregoing expert testimony is consistent with Lee’s disclosure that “error detector 510 comprises a sector data dispatching controller 512 . . . configured for receiving appropriate data sector.” Ex. 1004, 8:65–9:4. Accordingly, we find that Lee’s page buffer does not distinguish error correction bits from information bits in the received encoded data, as argued by Petitioner. Pet. Reply 5–6.

Next, Petitioner argues that “Lee’s page buffer ‘distinguishes’ by virtue of storing information in the encoding format.” Pet. Reply 7 (citing Ex. 1024 ¶ 51). Petitioner relies on Dr. Koralek’s testimony that a “POSITA would understand that receiving and storing data in the arrangement set out by the encoding process is sufficient to ‘distinguish’ between the different types of bits, and therefore, also sufficient to ‘decode.’” Ex. 1024 ¶ 51. We disagree. Receiving and storing data in a particular format is mere buffering, which does not satisfy our claim construction for “decode.” Our finding is supported by Dr. Bagherzadeh’s testimony that Lee’s page buffer 504 is “merely a form of temporary storage, such as SRAM or DRAM” that maintains “the structure and integrity of the original data bits” and “receives requests for data and responds to those requests by providing

the data that has been requested,” without decoding. Ex. 2022 ¶¶ 78, 109–119. Although Dr. Koralek asserts that “buffers are capable of actively managing data” and can “include circuits that make decisions about where data is sent” (Ex. 1024 ¶¶ 19–22), this testimony is not sufficient to show that Lee’s page buffer distinguishes error correction bits from information bits in the received encoded data, as provided in our claim construction.

In sum, Petitioner does not persuade us that Lee’s page buffer—the component Petitioner identifies as the “decoding module”—is configured to “decode the received encoded data,” which we construe to mean “distinguish error correction bits from information bits in the received encoded data.” Petitioner does not show that Lee’s page buffer participates in the decoding process rather than simply acting as a passive repository for temporarily storing data. For these reasons, Petitioner does not show that Lee anticipates claim 1.

3. Dependent Claims 2, 13, and 14

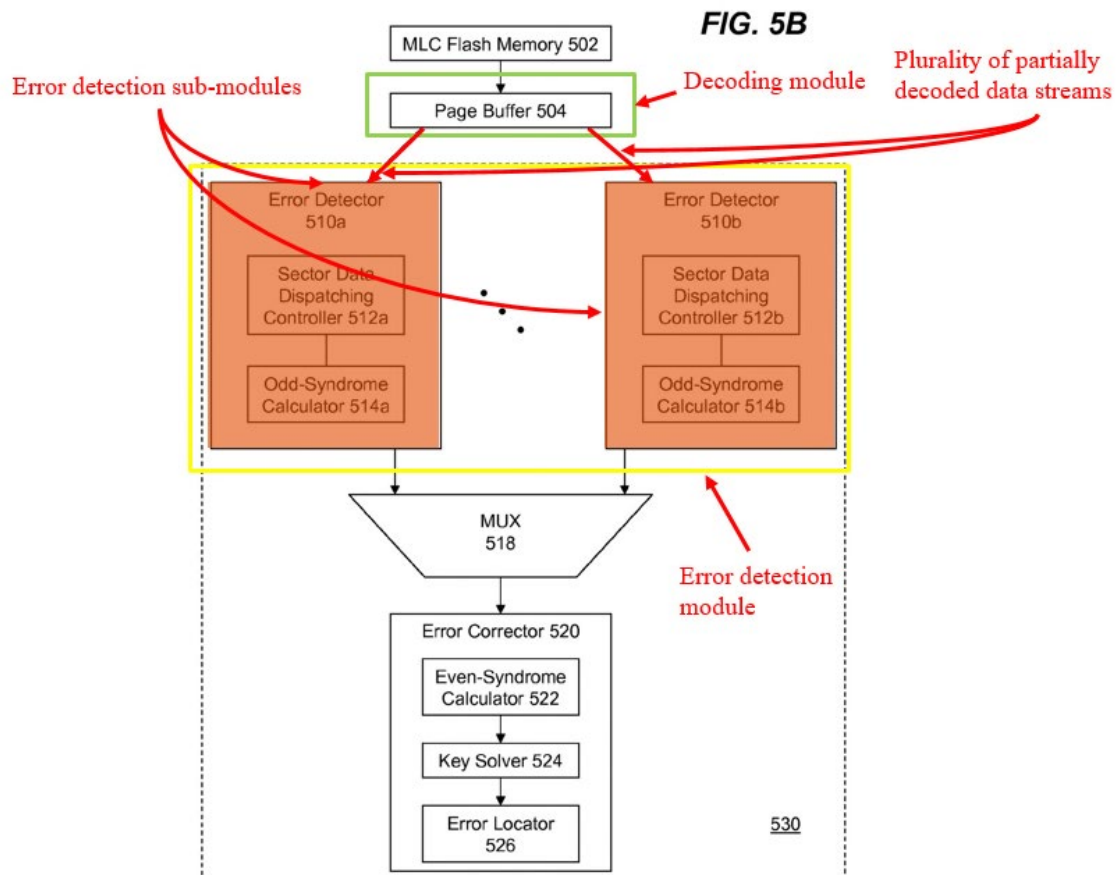
Claims 2, 13, and 14 each depend from claim 1. Petitioner’s arguments and evidence for these dependent claims (Pet. 29–31) do not remedy the deficiencies in Petitioner’s challenge to independent claim 1. Accordingly, Petitioner does not show unpatentability of dependent claims 2, 13, and 14 for the same reasons discussed above for claim 1.

Petitioner’s challenge to claim 14 does not succeed for an additional reason. Claim 14 depends from claim 1 and recites: “wherein, [14a] the error detection module comprises the decoding module; and [14b] the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.” Ex. 1001, 12:16–20 (bracketed text added).

Addressing claim element [14a], Petitioner contends that “a POSITA would understand that the detection module of Lee may comprise the decoding module” because “Lee discloses a decoder and error detector as overlapping components” and the disclosed operations may be carried out by software on a general-purpose computer. Pet. 30–31.

Patent Owner argues that Petitioner fails to show that the structure Petitioner identifies as the “error detection module”—Lee’s error detectors 510a and 510b—comprises the structure Petitioner identifies as the “decoding module”—Lee’s page buffer 504. PO Resp. 26–28.

We agree with Patent Owner. The Petition includes the following annotation of Lee Figure 5B to illustrate its contentions for claim 1.



Pet. 23. Lee's Figure 5B shows a decoder. As shown by Petitioner's annotations, Petitioner identifies Lee's page buffer 504 as the "decoding module" and Lee's error detectors 510a and 510b as the "error detection module." *Id.* The green and yellow boxes Petitioner draws around these structures do not overlap. Although Lee's Figure 5B shows error detectors 510a and 510b as part of decoder 530 and Petitioner accurately asserts that Lee's error detector and decoder are "overlapping components" (Pet. 30), Petitioner does not show that these error detectors 510a and 510b comprise Lee's **page buffer 504**, which Petitioner identifies as the "decoding module." Pet. 21–23. Petitioner does not show that a POSITA would view Lee's page buffer as part of Lee's error detection module.

For this additional reason, Petitioner does not show that Lee anticipates claim 14.

4. *Claim 15*

Our analysis focuses on claim element [15c], which recites "a decoder, communicatively coupled with the flash memory, and configured to: retrieve the encoded data from flash memory to generate a plurality of data streams." Ex. 1001, 12:27–30.

For claim element [15c], Petitioner relies on its contentions for claim elements [1a] and [1b] and further contends that "Lee discloses a decoder that receives encoded data from flash memory and generates a plurality of data streams." Pet. 32. According to Petitioner, "a POSITA would understand the 'sector data dispatching controllers' of the error detectors would request encoded data from the flash memory." *Id.*

Patent Owner argues that Lee's sector data dispatching controllers do not retrieve data from flash memory, that Petitioner's claim 15 arguments

contradict its claim 1 arguments, and that Petitioner identifies components outside Lee's decoder that retrieve data from flash memory. PO Resp. 20–24.

We are not persuaded by Petitioner's arguments for claim element [15c]. Petitioner contends that Lee discloses a “decoder” as recited in claim 15, namely decoder 530 including sector dispatching controllers 512. Pet. 32; Ex. 1002 ¶¶ 135–137. Petitioner does not, however, show that Lee's decoder 530 “retrieve[s] the encoded data from flash memory to generate a plurality of data streams,” as recited in claim 15. We agree with Patent Owner and Dr. Bagherzadeh that Lee's decoder 530 retrieves data from page buffer 504, not from flash memory 502. PO Resp. 20; Ex. 2022 ¶ 132. That is what is shown in Lee's Figure 5B, which depicts an arrow from a box labeled, “MLC Flash Memory 502,” terminating in another box labeled, “Page Buffer 504” and two lines from the latter terminating in boxes labeled “Error Detector 510a” and “Error Detector 510b.” Petitioner agrees with our understanding of Lee's Figure 5B. The Petition asserts that, “[a]s shown in FIG. 5B, the data processed by the error detectors 510a-b is received *from the page buffer 504.*” Pet. 22 (emphasis added). Dr. Koralek makes the same assertion. Ex. 1002 ¶ 99.

Petitioner argues that claim 15 does not require that the decoder retrieve the encoded data *directly* from flash memory and “nothing in the claim prevents intermediary components.” Pet. Reply 11–12. We disagree. Petitioner's argument is contrary to the plain language of claim 15, which recites that “a decoder . . . configured to: retrieve the encoded data *from flash memory . . .*” The claim requires that the encoded data be retrieved from flash memory, not from some intermediary component between the

decoder and the flash memory. Petitioner directs us to no support in the Specification for its interpretation of claim 15. The figures of the '700 Patent do not show intermediary components between the decoder and the flash memory. Ex. 1001, Figs. 1, 3, 4. Nor does the description suggest the possibility of intermediary components. Instead, as part of method 500 performed by the system of Figures 1, 3, or 4, the '700 Patent discloses that “[a]t block 505, encoded data from a flash memory is received.” *Id.* at 8:47–48.

Petitioner argues that, even if the claims require that the decoder retrieve data directly from flash memory, “a POSITA would have understood Lee’s page buffer to be included in the ‘decoder’ of Claim 15.” Pet. Reply 10 (citing Ex. 1024 ¶ 63). Petitioner’s reply argument is inconsistent with the Petition and the original Koralek declaration, which identify Lee’s decoder 530 as the “decoder” of claim 15. Pet. 32; Ex. 1002 ¶ 136. Moreover, Petitioner’s argument is premised on equating Lee’s page buffer with the decoding module of the '700 Patent, a proposition we do not accept for the reasons discussed above for claim 1. *See* Pet. Reply 12 (arguing that “Lee’s page buffer (‘decoding module’) would be understood to be part of the ‘decoder’”).

For these reasons, Petitioner does not show that Lee anticipates claim 15.

5. *Claim 17*

Our analysis focuses on claim element [17a], which recites “receiving encoded data from a flash memory comprising a plurality of data streams.” Ex. 1001, 12:50–51.

Addressing claim element [17a], Petitioner relies on its contentions for claim elements [1a] and [1b] and further contends that “Lee discloses receiving encoded data from MLC flash memory as a plurality of data streams” and “further discloses that the error detectors receive encoded data (i.e., a codeword).” Pet. 34.

Patent Owner argues that Petitioner “does not explain how or why the *single* data stream emanating from ‘flash memory 502’ in [Lee] Figure 5B comprises ‘a *plurality* of data streams.’” PO Resp. 25. Patent Owner also argues that Petitioner’s arguments for claim 17 are inconsistent with its argument for claims 1 and 15. *Id.*

We are not persuaded by Petitioner’s arguments for claim element [17a]. Petitioner agrees that claims 15 and 17 “stand and fall together” with respect to receiving encoded data from a flash memory. Tr. 20:18–21. We therefore determine that Petitioner does not show that Lee discloses claim element [17a] for the same reasons as discussed above for claim element [15c]. We add the following to address Petitioner’s arguments for claim 17.

Whereas claim 17 recites “receiving encoded data from a flash memory comprising a *plurality* of data streams,” Lee Figure 5B shows that a *single* stream of data is transmitted from flash memory. Petitioner does not dispute this fact. Pet. Reply 13 (“the initial data stream from flash memory to the page buffer is a single arrow in FIG. 5B” (citing PO Resp. 24–26)).

Petitioner contends, “there is nothing preventing data comprising a plurality of data streams from being represented by the single arrow of Figure 5B.” Pet. Reply 13 (citing Ex. 1024 ¶ 67). Neither Petitioner nor Dr. Koralek provide any explanation or objective support for this contention. Lee’s Figure 5B depicts a single arrow from a box labeled, “MLC Flash

Memory 502,” terminating in another box labeled, “Page Buffer 504,” and a pair of lines from the latter terminating in boxes labeled “Error Detector 510a” and “Error Detector 510b.” Petitioner identifies this pair of lines as disclosing a “plurality of partially decoded data streams.” Pet. 21, 23. Logically, the single arrow from the flash memory to the page buffer represents a single data stream, not a plurality of data streams. In this regard, we credit Dr. Bagherzadeh’s testimony that a “POSITA would understand the one line emanating from Flash Memory 502 to depict a single data stream, not a plurality of data streams.” Ex. 2022 ¶ 136.

For these reasons, Petitioner does not show that Lee anticipates claim 15.

6. Conclusion

Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 13–15, and 17 are unpatentable as anticipated by Lee.

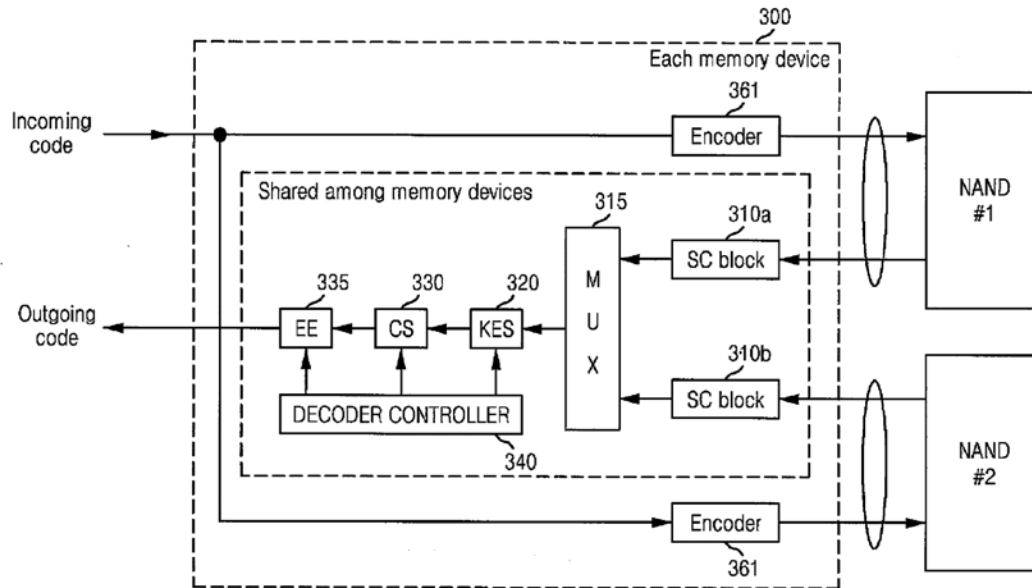
E. Petitioner’s Challenge based on Lee and Jo

Petitioner challenges claims 4, 8, and 19 as unpatentable based on Lee and Jo. Pet. 35–39. Patent Owner opposes. PO Resp. 28–34. We provide an overview of Jo before turning to our analysis.

1. Jo (Ex. 1007)

Jo discloses a “multi-channel memory system including error correction decoder architecture.” Ex. 1007, code (54). Figure 3 is reproduced below.

FIG. 3



Jo’s Figure 3 shows flash memory error correction coder (“ECC”) block 300, which communicates with flash memories NAND #1 and NAND #2 over two communication channels operating in parallel. Ex. 1007 ¶¶ 18, 23, 25. ECC block 300 includes two data encoders 361, one each for communication channel, and two syndrome computation (SC) blocks 310a and 310b, again one for each communication channel. *Id.* ¶ 24. SC blocks 310a and 310b each receive a set of data from a different sector of memory and detect whether or not the data set includes errors. *Id.* ¶¶ 26, 27.

ECC block 300 further includes multiplexer 315, key equation solver (“KES”) block 320, “Chien” search and error evaluator blocks 330 and 335, and decoder controller 340, all of which are shared by the two communication channels. Ex. 1007 ¶¶ 24, 28, Fig. 3. According to Jo, “multiplexer 315 multiplexes between the first and second communication channels for locating errors that occur in data sets received from the memory devices via the communication channels.” *Id.* ¶ 28. Jo further discloses

that, “[o]nce the errors are identified in a data set, then the errors are corrected in a further error correction block not shown in FIG. 3 . . . and the decoded data set may then be sent to a host device.” *Id.*

2. *Claims 4, 8, and 19*

Claim 4 depends from claim 1 and recites “wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.” Ex. 1001, 11:7–10. Claim 8 depends from claim 4. *Id.* at 11:37–41. Claim 19 depends from claim 17 and recites the same limitation as claim 4. *Id.* at 13:1–4.

Petitioner contends that a “POSITA would understand that Jo discloses a plurality of error correction sub-modules operating in parallel.” Pet. 36. According to Petitioner, Jo discloses systems having two or more channels, “where each pair of channels is associated with a different error correction sub-module.” *Id.* Petitioner asserts:

A POSITA would understand that when Jo’s system has four (or more) channels, it would include at least four error detection sub-modules and two error correction sub-modules, wherein each error detection sub-module is connected to a different one of the channels, and each error correction sub-module is associated with a unique pair of error detection sub-modules.

Id.

Patent Owner argues that Jo does not disclose a plurality of error correctors operating in parallel and fewer in number than the error detectors, as required by claims 4, 8, and 19, and that to the extent one wished to add channels, a POSITA following Jo’s teachings would have arranged the additional channels to feed into the same error corrector. PO Resp. 29–30.

Patent Owner additionally argues that Petitioner fails to show a motivation to combine Lee and Jo. *Id.* at 31–33.

Petitioner’s arguments and evidence for dependent claims 4, 8, and 19 (Pet. 35–39) do not remedy the deficiencies in Petitioner’s challenge to independent claims 1 and 17. Accordingly, Petitioner does not show unpatentability of dependent claims 4, 8, and 19 for the same reasons as discussed above for claims 1 and 17.

Petitioner’s challenge to dependent claims 4, 8, and 19 does not succeed for the following additional reasons.

a) Jo’s teachings

Petitioner relies on Jo to teach the limitations of claims 4, 8, and 19 (Pet. 35–38), but does not show that Jo teaches “a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules,” as recited. Jo’s Figure 2 shows a plurality of error correctors 163, 173, 183, but they are not fewer in number than error detectors 162, 172, 182. Ex. 1007 ¶ 7, Fig. 2. Petitioner does not point to any express disclosure in Jo of multiple error correction sub-modules that are fewer in number than the error detection sub-modules. Nor does Petitioner provide sufficient support for its assertion that a POSITA would have understood Jo as disclosing this feature.

Petitioner and Dr. Koralek assert that “when Jo’s system has four (or more) channels, it would include at least four error detection sub-modules and two error correction sub-modules.” Pet. 36; Ex. 1002 ¶ 169. Patent Owner and Dr. Bagherzadeh have a different understanding of Jo, namely, that any additional channels (beyond the two shown in Jo’s Figures 3 and 6) would feed into the same error corrector. PO Resp. 30; Ex. 2022

¶¶ 142–144. In our view, Patent Owner’s understanding more closely aligns with Jo’s disclosure. Jo repeatedly describes “at least” two communication channels and “at least” two error detectors, but describes only a single error corrector. Ex. 1007 ¶¶ 12, 15, 28, 37, 41, claim 1, Figs. 3, 6. Jo uses broad, open-ended language when describing the number of communication channels and the number of error detectors, but not when describing the number of error correctors. *Id.*

The parties agree that Jo’s Figures 1 and 2 show the prior art, and Figures 3, 4, and 6 show an improvement. PO Resp. 29; Pet. Reply 14. According to Petitioner, “[a]lthough Jo only shows two channels when discussing its improved design, Jo recognizes that more than two channels may be used (e.g., in prior art systems), and therefore, more than one error correction sub-module would be used.” Pet. Reply 14 (citing Ex. 1007, Figs. 1–4); Ex. 1024 ¶¶ 69, 70). We are not persuaded. Petitioner’s reply argument addresses what “would be used,” not what Jo actually teaches. Petitioner’s challenge is based on a combination of Lee and Jo, not a combination of Lee and a modification of Jo.¹⁴ To the extent Petitioner argues that connecting multiple channels to a single error corrector would cause a “bottleneck” (Pet. Reply 15), that is an argument for modifying Jo’s teachings, not an argument that supports the challenge articulated in the Petition.

Petitioner concedes that, to find for Petitioner on its Jo-based challenges, the Board would need to accept Petitioner’s position that Jo teaches parallelization of the error correction. Tr. 26:9–15. Because we do

¹⁴ Petitioner does not sufficiently show a motivation to modify Jo for the reasons discussed in the following subsection.

not find for Petitioner on that issue, Petitioner's challenges based on Jo in combination with either Lee or Yamaga cannot succeed.

b) Motivation to combine

Petitioner contends that “[i]n order to improve throughput and efficiency, a POSITA would have been motivated to include Jo’s multiple error correctors, which each correct errors from two or more error detectors, in the system of Lee.” Pet. 38. Petitioner contends that a POSITA would have expected the combination to be successful because both references disclose error correctors that correct errors from two or more error detection modules operating in parallel. Pet. 39.

Patent Owner argues that a POSITA “would not parallelize Jo’s Figure 3 and apply it to Lee,” as proposed by Petitioner, because “[b]oth Jo and Lee criticize complicated and costly systems” and Petitioner’s combination “would increase both the complexity and the size of the error-correction circuitry.” PO Resp. 33 (citing Ex. 1004, 1:42–54, Ex. 1007 ¶ 9).

We are not persuaded that Petitioner sufficiently shows a motivation to combine Jo and Lee. Petitioner’s combination of Lee and Jo rests on the incorrect premise that Jo discloses multiple error correctors and “parallelized [error] correction.” Pet. 38; Pet. Reply 18–19. As discussed above, Petitioner has not established that premise. In fact, both Lee and Jo teach just the opposite: a plurality of error detectors operating in parallel and feeding into a single error corrector that operates serially. Ex. 1004, Fig. 5B, 9:9–15, 13:50–52 (claim 7); Ex. 1007, Fig. 3.

Furthermore, although Petitioner and Dr. Koralek assert that a POSITA would have been motivated to include additional error correctors “[i]n order to improve throughput and efficiency,” they do not explain how

throughput and efficiency would have been improved. Pet. 38; Ex. 1002 ¶ 163. Lee aims to provide “efficient and effective implementation of error correction” and teaches that efficiency is improved by “parallel encoding and error detection,” while error correction is conducted sequentially. Ex. 1004, 1:51–54, 2:10–14, 9:13–15, 9:32–34, 13:51–53 (claim 7). Jo states that “adding more ECC modules enlarges the size of the integrated circuit[] and increases the number of ECC IP core gates,” which “increases the complexity and cost of the flash memory system.” Ex. 1007 ¶ 9. Jo aims to provide “robust error detection and correction with a more efficient utilization of area and circuitry in a memory controller” and teaches that error correction circuitry is shared by multiple communication channels. *Id.* ¶¶ 10, 28, 33, 41. In view of these teachings, Petitioner does not show persuasively that a desire for improved throughput and efficiency would have motivated a POSITA to add more error correctors. Furthermore, Petitioner and Dr. Koralek do not address whether error correction could have been reliably conducted in parallel by multiple error correctors, rather than serially, as taught by the references. Ex. 1004, 11:20–27, Figs. 12A, 12B; Ex. 1007 ¶¶ 42–50, Fig. 7.

In the reply, Petitioner argues that a POSITA would “use engineering knowledge to optimize fundamental design tradeoffs such as speed, efficiency, circuit size, and cost” and that “adding error correctors in a 1:2 ratio to error detectors . . . would appropriately balance speed and hardware.” Pet. Reply 19 (citing Ex. 1024 ¶¶ 23–29, 70–76; Ex. 1019, 35:11–22; Ex. 2023,¹⁵ 88:17–89:4). Dr. Koralek provides a new illustration

¹⁵ Although Petitioner cites Exhibit 2022, we understand Exhibit 2023 is the correct citation.

of the proposed combination and a new example of a system with eight channels and four error correctors. Ex. 1024 ¶¶ 74, 75.

We are not persuaded by Petitioner’s reply argument. We credit the testimony of Dr. Bagherzadeh that Petitioner’s proposed combination of Jo and Lee “runs counter to Jo’s teachings on how to design an efficient error correction system.” Ex. 2022 ¶ 141; *see also id.* ¶ 147 (“Petitioner’s proposed combination would add circuitry to one or both” of Jo and Lee, contrary to the teachings of the references). Dr. Bagherzadeh is correct that Petitioner’s proposed modification “would duplicate [the circuitry in Jo Figure 3] counter to the guidance provided in [Jo] of minimizing the circuitry and area for a given flash memory device.” *Id.* ¶ 141. Dr. Koralek concedes that using a “single corrector for all detectors . . . would reduce circuit scale.” Ex. 1024 ¶ 70. Contrary to Jo’s teachings about efficient utilization of area and circuitry, Petitioner’s proposed combination duplicates the circuitry of Jo Figure 3 that Jo teaches can be “shared among memory devices.” *Compare* Ex. 1007 ¶¶ 9, 10, 28, 33, 41, Fig. 3 (Jo), *with* Ex. 1024 ¶ 74 (modification of Jo Figure 3). In view of the prior art teachings, Petitioner fails to show persuasively that a POSITA would combine the teachings of Lee and Jo in the manner proposed by Petitioner.

3. *Conclusion*

Petitioner has not shown by a preponderance of the evidence that claims 4, 8, and 19 are unpatentable based on Lee and Jo.

F. Petitioner’s Challenge based on Lee and Kim

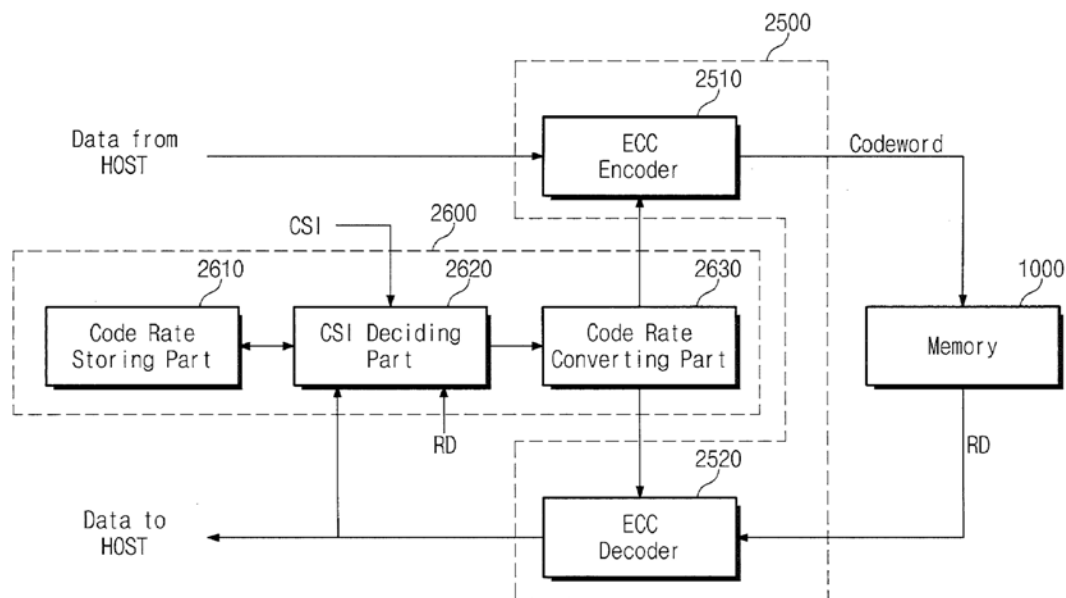
Petitioner challenges claims 3, 10–12, 16, 18, and 23–25 as unpatentable based on Lee and Kim. Pet. 39–49. Patent Owner opposes.

PO Resp. 34–35. We provide an overview of Kim before turning to our analysis.

1. *Kim (Ex. 1006)*

Kim discloses ECC encoding and decoding circuits with code rate selection based on bit error rate detection. Ex. 1006, code (54). Figure 2 is reproduced below.

Fig. 2



Kim's Figure 2 shows ECC encoding and decoding block 2500 and code rate controlling block 2600, which communicate with memory 1000 and a host. Ex. 1006 ¶¶ 10, 32, 33. ECC encoding and decoding block 2500 includes ECC encoder 2510 and ECC decoder 2520. ECC encoder 2510 encodes data from the host to generate a codeword, which is sent to memory 1000. *Id.* ¶ 33. ECC decoder 2520 decodes data read out from memory 1000 and sends the decoded data to the host. *Id.* A code rate of ECC encoder 2510 and a code rate of ECC decoder 2520 are set by code rate controlling block 2600. *Id.*

Kim discloses that criteria for changing the code rate include “wear-leveling information such as a program/erase cycle, a bit error rate (BER), a used time, [and] an error frequency after reading by decoding of an error control code at a read request.” Ex. 1006 ¶ 29.

2. *Claims 3, 10–12, 16, 18, and 23–25*

Petitioner’s arguments and evidence for dependent claims 3, 10–12, 16, 18, and 23–25 (Pet. 39–49) do not remedy the deficiencies in Petitioner’s challenge to independent claims 1, 15, and 17. Accordingly, Petitioner does not show unpatentability of dependent claims 3, 10–12, 16, 18, and 23–25 for the same reasons as discussed above for claims 1 and 17.

Petitioner’s challenge to dependent claims 3 and 18 does not succeed for the following additional reasons.

Claim 3 depends from claim 2, which depends from claim 1. Claim 3 recites “a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory.” Ex. 1001, 11:3–6. Claim 18 depends from claim 17 and recites “dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory.”

Petitioner contends that “a POSITA would understand that Kim’s code rate controlling block 2600 (i.e., read controller) dynamically modifies error detection sub-modules by setting the ECC decoding block to varying code rates that correspond to specific memory sectors.” Pet. 41.

Patent Owner argues that claims 3 and 18 require changing “the error-detection sub-modules *assigned* to certain sectors of flash memory,” and that Kim does not disclose dynamic assignment of error detection sub-modules to specific sectors of memory. PO Resp. 35.

We agree with Patent Owner. The plain language of claims 3 and 18 requires dynamically modifying the assignment of error detection sub-modules to sectors of flash memory. That is also what the Specification describes.

The read controller 420 may dynamically change the components of the decoder 115-b to be used to read different sectors of flash memory 110-b (e.g., in FIG. 3, the assignments of the decoder sub-modules 310, error detection sub-modules 315, and error correction sub-modules 320 may be changed in response to code rate modifications, increased errors, or age).

Ex. 1001, 8:34–40. Petitioner argues that claims 3 and 18 “only require ‘dynamically *modify[ing]*’ the error detection sub-module,” not dynamically assigning or reassigning error detection sub-modules to specific sectors of memory. Pet. Reply 20. We disagree. Petitioner’s claim construction is inconsistent with the claim language and the Specification, as discussed above.

To show the limitations of claims 3 and 18, Petitioner relies on Kim’s disclosure of assigning code rates to memory sectors. Pet. 39–40 (“Kim discloses a ‘code rate controlling block 2600’ (i.e., a read controller) that may select and modify ‘a code rate of a storage area being accessed,’” (citing Ex. 1006 ¶ 30).); Pet. 46 (“Kim discloses that error detection submodules are dynamically modified by being assigned varying code rates on a sector-by-sector basis.”); *see also* Ex. 1002 ¶ 184 (“a POSITA would understand that Kim’s code rate controlling block 2600 (i.e., read controller) dynamically modifies error detection sub-modules by setting the ECC decoding block 2520 to varying code rates that correspond to specific memory sectors.”). Petitioner points to no disclosure in Kim (or any other

prior art) of dynamically changing the assignment of error detection sub-modules to sectors of flash memory.

3. Conclusion

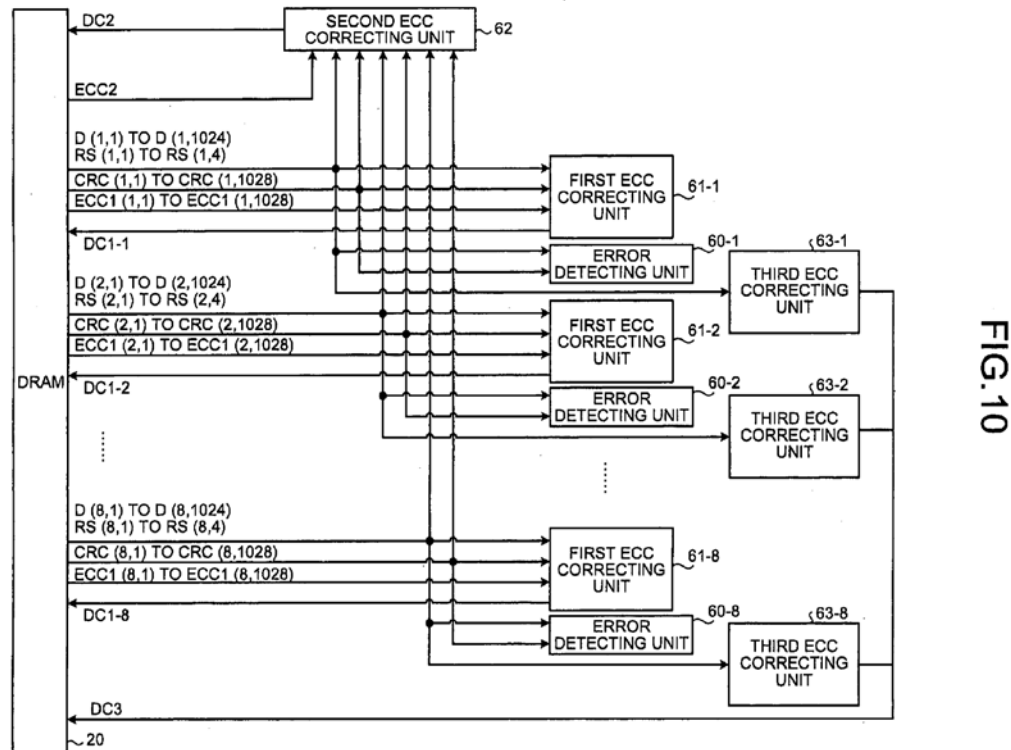
Petitioner has not shown by a preponderance of the evidence that claims 3, 10–12, 16, 18, and 23–25 are unpatentable based on Lee and Kim.

G. Petitioner’s Challenges Based on Yamaga Alone

Although the Petition challenges claims 1, 13–15, and 17 as both anticipated by and obvious in view of Yamaga (Pet. 3, 49–68), Petitioner drops the anticipation challenge in the reply and focuses exclusively on obviousness. Pet. Reply 20. Patent Owner opposes both challenges. PO Resp. 35–60. We provide an overview of Yamaga before turning to our analysis.

1. Yamaga (Ex. 1005)

Yamaga discloses an “error correction code (ECC) circuit of a solid state drive (SSD).” Ex. 1005, code (57). Figure 10 is reproduced below.

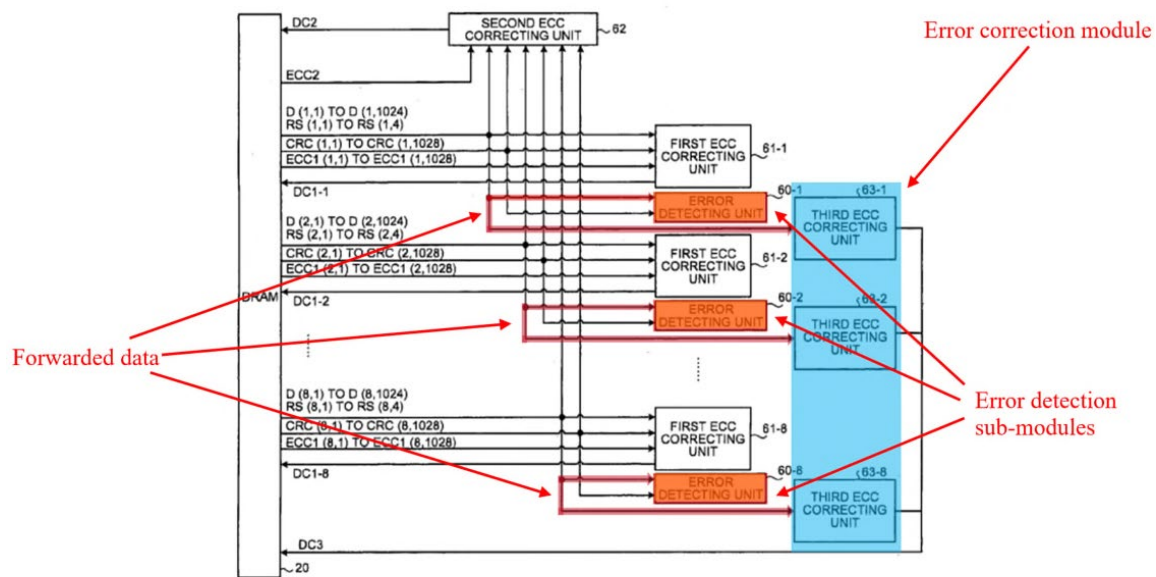


Yamaga’s Figure 10 shows a decoding system in an ECC circuit. Ex. 1005, 3:18–19, 10:15–16. As shown in Figure 10, the ECC circuit communicates with DRAM 20 and includes eight error detecting units 60-1 to 60-8, eight first ECC correcting units 61-1 to 61-8, second ECC correcting unit 62, and eight third ECC correcting units 63-1 to 63-8. *Id.* at 10:18–28.

2. Alleged Anticipation of Claims 1, 13–15, and 17

Claims 1, 15, and 17 recite that “each error detection sub-module [is] configured to: . . . forward the portion of the respective received stream containing an error to an error correction module” (hereinafter “the forward limitation”). Ex. 1001, 10:54–55, 10:60–61 (claim 1); *id.* at 12:34–35, 38–40 (claim 15); *id.* at 12:54–55, 58–59 (claim 17). Claims 13 and 14 depend from claim 1. *Id.* at 12:12–20.

Petitioner provides the following annotation of Yamaga’s Figure 10 as support for its contention that Yamaga discloses the forward limitation.



Pet. 56. Yamaga’s Figure 10 shows a decoding system. Petitioner’s annotations identify (1) error detecting units 60-1 to 60-8 as “error detection submodules,” (2) third ECC correcting units 63-1 to 63-8 as an “error correction module,” and (3) the bidirectional arrows between (1) and (2) as “forwarded data.” *Id.* Petitioner contends that “a POSITA would understand [Yamaga’s] disclosure and the bidirectional arrows of FIG. 10 . . . to disclose forwarding the portion of the data containing an error from the error detecting units to the third error correcting units.” *Id.* Petitioner contends that Yamaga discloses a multi-step error correction process in which data containing an error is forwarded from the error detecting units to the second error correcting unit and the third error correcting units. Pet. 57. Petitioner relies on the same analysis for claims 15 and 17 as it presents for claim 1. Pet. 67–68.

In the Institution Decision, we stated that “Petitioner does not show sufficiently that Yamaga discloses the forward limitation.” Inst. Dec. 39. We agreed with Patent Owner that “the bidirectional arrows Petitioner

identifies in Yamaga's Figure 10 represent error information, not data containing an error." *Id.* We found that "Petitioner does not direct us to disclosure sufficient to show that Yamaga's error detecting units forward an error-containing portion of the data stream to an error correction module." *Id.* at 40.

Patent Owner argues that Petitioner has not demonstrated that Yamaga anticipates claims 1, 13–15, and 17. PO Resp. 35–55. Among other things, Patent Owner argues that Yamaga does not disclose the forward limitation. *Id.* at 35–36, 42–51.

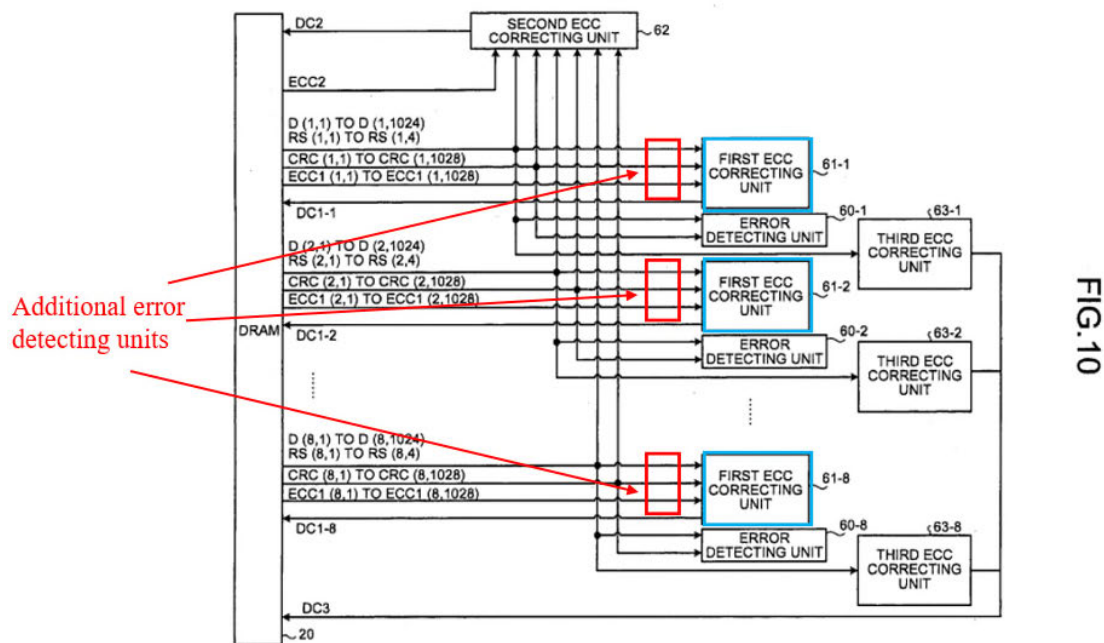
Petitioner does not dispute our preliminary findings as set forth in the Institution Decision (Inst. Dec. 39–41) nor Patent Owner's argument that Yamaga does not disclose the forward limitation. Instead, the reply states that "Petitioner is relying exclusively" on obviousness for challenging claims 1, 13–15, and 17 based on Yamaga. Pet. Reply 20. Accordingly, for the same reasons as stated in the Institution Decision and summarized above, Petitioner does not show that Yamaga anticipates claims 1, 13–15, and 17.

3. Alleged Obviousness of Claims 1, 13–15, and 17

Petitioner contends that Yamaga renders the forward limitation obvious in view of the knowledge of a POSITA. Pet. 57. According to Petitioner, a "POSITA would be motivated to modify Yamaga's system to: (1) include an error detection step prior to the first error correction step; and (2) forward the error-containing data from the error detecting unit to the first error correction unit." *Id.* Petitioner contends that "including error detection prior to error correction was widely known" and would reduce power consumption. Pet. 58. Although the Petition proposes two alternative ways to make this modification of Yamaga (*id.*), Petitioner's reply drops the first

alternative¹⁶ and focuses on the second alternative, which is adding error detecting units between DRAM 20 and first ECC units 61-1 to 60-8.

Pet. 58–59; Pet. Reply 22–23 (arguing obviousness of adding detectors); PO Sur-reply 19 n.1 (observing that Petitioner dropped its first theory); Tr. 20:22–21:13 (arguing obviousness of adding detectors). Petitioner contends that the additional error detecting units would forward the data blocks containing errors to first ECC correcting units 61-1 to 61-8. Pet. 59. Petitioner provides the following illustration of its proposed modification.



Id. Yamaga’s Figure 10 shows a decoding system. Petitioner modifies the drawing by adding three boxes labeled “additional error detecting units” between DRAM 20 and first ECC correcting units 61.

¹⁶ Petitioner’s first alternative was reading data blocks from DRAM 20 into error detecting units 60-1 to 60-8 prior to error correction and forwarding data blocks containing errors from error detecting units 60-1 to 60-8 to first ECC correcting units 61-1 to 61-8 for a first error correction. Pet. 58–59.

Patent Owner argues that Petitioner's obvious theory is hindsight biased, that a POSITA would not have added an additional error detection step to Yamaga, that adding this step and a forwarding step is contrary to Yamaga's teachings and would needlessly duplicate error detection that already exists within the error correctors, and that "adding another error detecting unit would undermine Yamaga's stated goals of reducing power consumption, read time, and circuit scale." PO Resp. 56–60.

We agree with Patent Owner that Petitioner's obviousness theory is hindsight biased and that Petitioner has not proven its contention that a POSITA would have been motivated to modify Yamaga's system to "(1) include an error detection step prior to the first error correction step; and (2) forward the error-containing data from the error detecting unit to the first error correction unit." Pet. 57.

As articulated in the Petition, Petitioner's obviousness case appears to be based on the same false premise as the anticipation challenge. For both challenges, the Petition incorrectly assumes that Yamaga's error detecting units forward data to the first error correction units. Pet. 56–60. The Petition does not assert that the proposed additional error detecting units would function any differently than Yamaga's existing error detecting units. *See* Pet. 59 (modifying Yamaga Figure 10 to show "Additional error detecting units"). Dr. Koralek's initial declaration suggests that the proposed additional error detecting units would function in the same way as Yamaga's existing error detecting units.

[I]n my opinion, a POSITA would be motivated to modify Yamaga's system to include an error detection step prior to the first error correction step, and forward data containing an error from the error detecting unit to the first error correction unit. In my opinion, this modification would have at least been obvious

to try in view of *the error detection already performed* in Yamaga . . .

Ex. 1002 ¶ 240 (emphasis added). Petitioner drops its anticipation challenge (Pet. Reply 20) and does not contest our preliminary finding in the Institution Decision that Yamaga does not disclose that its error detecting units forward an error-containing portion of the data stream to an error correction module. Inst. Dec. 39–41; *see also* PO Resp. 35–36, 42–51 (arguing consistent with our finding). To the extent Petitioner’s obviousness challenge is based on adding another set of error detecting units that function in the same manner as Yamaga’s existing error detecting units (Pet. 59–60), the challenge fails for the same reason. Petitioner fails to show that the additional error detecting units would forward an error-containing portion of the data stream to an error correction module.

We find that the persuasiveness of Petitioner’s Yamaga obviousness challenge and the trustworthiness of Dr. Koralek’s testimony are undermined because they were forced to change positions on multiple technical issues in response to the Institution Decision, the Patent Owner Response, and Dr. Bagherzadeh’s testimony. These issues include (1) whether Yamaga’s error detecting units forward data to the error correction units; (2) whether a POSITA would have modified Yamaga by routing data first to the error detecting units and then to the first ECC correcting units; and (3) whether the proposed additional error detecting units would function in the same manner as Yamaga’s existing error detecting units. After reviewing the testimony of Dr. Bagherzadeh, Dr. Koralek dropped his initial position that Yamaga’s error detecting units forward data to the second and third error correction units. *Compare* Ex. 1002 ¶¶ 228, 230, 231, *with* Pet. Reply 24 (Yamaga’s “second and third

ECC correctors operat[e] on the original, uncorrected data” (citing Ex. 1024 ¶ 35)). Dr. Koralek also dropped his first proposed alternative way of modifying Yamaga. *Compare* Ex. 1002 ¶ 237, *with* Ex. 1024 ¶¶ 79–92 (addressing Yamaga obviousness without mentioning the first alternative). Furthermore, Dr. Koralek’s first declaration suggests that the proposed additional error detecting units would function in the same manner as Yamaga’s existing error detecting units. Ex. 1002 ¶ 240 (quoted above). Dr. Koralek changed positions in his supplemental declaration, agreeing with Dr. Bagherzadeh that the added error detectors would have a different purpose than Yamaga’s existing error detecting units. Ex. 1024 ¶ 86.

Petitioner’s proposed modification of Yamaga appears more akin to a hindsight reconstruction of the claimed invention than an obvious modification of Yamaga’s ECC circuit. Yamaga discloses an error correction system that aims to reduce power consumption and circuit scale without detriment to error correction capability. Ex. 1005, code (57); 2:1–3, 16:40–44. Yamaga accomplishes that objective by providing an ECC circuit that performs three different types of correction coding with different levels of error correction capability. *Id.* at code (57), 3:62–67, 6:26–41. First error correction is performed on a data block basis; second error correction is performed on a column-by-column basis; and third error correction is performed on a row-by-row basis. *Id.* at 6:47–54. Yamaga explains that the second and third error correction steps are performed only when errors are detected in the preceding step, which reduces data read time and power consumption. *Id.* at 12:15–23, 13:10–19, 13:29–41, 14:1–8, 15:13–23. We agree with Patent Owner that “Yamaga describes a carefully choreographed system in which multiple blocks undergo error detection and correction in precise order and with precisely aligned timing.” PO Sur-reply 24 (citing

Ex. 1005, 9:18–13:52). Petitioner does not persuade us that a POSITA would have had a reason to modify Yamaga’s system by adding another error detection step and forwarding data from added error detectors to the first error correction units.

It is undisputed that Yamaga’s ECC correcting units include error detection capability. PO Resp. 59 (“Yamaga’s ‘first ECC correcting units’ already perform error detection on the original data.”); Pet. Reply 21 (“Yamaga teaches that its first ECC corrector is preferably a Hamming decoder, which includes a detection portion and a correction portion.”); Ex. 1024 ¶ 83; Ex. 2022 ¶¶ 171, 175. Petitioner does not explain persuasively why a POSITA would have added additional error detectors before Yamaga’s first ECC correcting units, when those units already have error detection capability. We agree with Patent Owner that “Petitioner’s obviousness theory would needlessly duplicate error detection functions in Yamaga.” PO Resp. 59 (heading). In his reply declaration, Dr. Koralek asserts that “the detecting capabilities of Yamaga’s first ECC correcting units 61-1 to 61-8 are immaterial to the proposed modification.” Ex. 1024 ¶ 87. But Dr. Koralek does not explain why the existing error detection capability of Yamaga’s first ECC correcting units is not adequate to achieve the asserted benefit. As further discussed below, Petitioner does not show that a POSITA would have expected to save power by adding an error detection step and rerouting some of the data to bypass Yamaga’s first ECC correcting units and error detecting units.

Petitioner and Dr. Koralek assert that the proposed modification of Yamaga would result in power savings. Pet. 58; Ex. 1002 ¶¶ 234–236, 240; Pet. Reply 21–23; Ex. 1024 ¶¶ 80–88. Petitioner and Dr. Koralek do not, however, properly compare the power consumption of Yamaga’s

unmodified system with the power consumption of their proposed modified system. The Petition and Dr. Koralek's original declaration make no comparison between the power consumed by the two systems. Instead, Petitioner and Dr. Koralek assert that, with the modification, a smaller number of data blocks would undergo first error correction and error detection after first error correction. Pet. 58; Ex. 1002 ¶¶ 234–236. That reasoning fails to take into account the power consumption of the additional error detectors Petitioner proposes to add to Yamaga's circuit. Pet. 59; Ex. 1002 ¶ 238; *see* PO Resp. 57 ("Petitioner's proposed modification . . . adds a power-consuming error detecting step before the initial error correction is performed."); Ex. 2022 ¶ 174 (Dr. Bagherzadeh: inserting additional error detecting units would not result in any meaningful power savings).

Petitioner's reply evidence fares no better. Petitioner's power savings argument is based on a comparison between the power consumed by a CRC detector, such as Yamaga's error detecting units 60, and a Hamming decoder, such as Yamaga's first error correcting units 61, which Petitioner concedes include a detection portion and a correction portion. Pet. Reply 21–22; Ex. 1024 ¶¶ 82, 83. Petitioner asserts that power would be saved by allowing error-free data to bypass these units. Pet. Reply 21. But that argument assumes, without basis, that the correction portion of Yamaga's first error correcting units 61 operates on *all* the data, rather than just the data containing errors. *Id.*; Ex. 1024 ¶ 82. Petitioner's argument also ignores the power consumed by the SRAM buffers Petitioner and Dr. Koralek propose to add to Yamaga's circuit. For the first time in the reply, Petitioner and Dr. Koralek assert the additional error detecting units would have been CRC detectors and that SRAM buffers would have been

used to forward data from the CRC detectors to the first ECC correcting units. Pet. Reply 22–23; Ex. 1024 ¶¶ 84, 89–92. Even though Petitioner and Dr. Koralek rely on SRAM buffers to show obviousness of the forward limitation (Pet. Reply 23; Ex. 1024 ¶¶ 89–92), they ignore the SRAM buffers in their analysis of power savings. Pet. Reply 21–23; Ex. 1024 ¶¶ 80–88 (asserting that proposed modification would result in lower power consumption, without mentioning SRAM buffers). The oversight is not insignificant. Dr. Koralek agrees that SRAM buffers with capacity sufficient for Yamaga’s data would require 130,000 transistors. Ex. 2026, 225:16–226:17. Petitioner fails to address how adding 130,000 transistors to Yamaga’s circuit would save power. *See* Tr. 53:23–25 (Patent Owner’s argument).

Furthermore, Petitioner’s power savings argument is premised on the assertion that, in the modified circuit, most data blocks would bypass **both** first ECC correcting units 61 **and** error detecting units 60. Pet. Reply 21–23 (discussing motivation to modify Yamaga); Ex. 1024 ¶¶ 82, 84, 87 (same). For purposes of bypassing first ECC correcting units 61, Petitioner and Dr. Koralek propose to add SRAM buffers that forward data from the additional CRC detectors to the first ECC correcting units. Pet. Reply 23; Ex. 1024 ¶¶ 89–92. Petitioner and Dr. Koralek do not, however, propose to add SRAM buffers to Yamaga’s first ECC correcting units. *See* PO Sur-reply 23 (“Petitioner proposes adding SRAM to the detecting units, not the First ECC Correcting Units.”). Yamaga teaches that data is transferred to error detecting units 60 from DRAM 20, **not** from first ECC correcting units 61. Ex. 1005, 11:42–57. Petitioner and Dr. Koralek do not explain how data could bypass error detecting units 60 without adding forwarding

functionality, e.g., SRAM buffers, to the first ECC correcting units. Any such additional SRAM buffers would consume yet more power.

For these reasons, Petitioner does not persuade us that power savings would have motivated a POSITA to add an error detection step to Yamaga's ECC circuit. Petitioner's remaining arguments are similarly unpersuasive. Petitioner argues that "including error detection prior to error correction was widely known." Pet. 58; Ex. 1002 ¶ 239 (citing references); Tr. 61:17–24. Petitioner does not, however, provide a sufficient reason to modify Yamaga to include an additional error detection step, when Yamaga already performs error detection prior to error correction, as Petitioner and Dr. Koralek concede. Pet. Reply 21; Ex. 1024 ¶¶ 37, 83.

Petitioner has no persuasive response to Patent Owner's argument that Petitioner's proposed modification would increase read time, contrary to one of Yamaga's disclosed objectives. PO Resp. 56, 59–60; Ex. 1005, 13:37–38, 15:17–21. Although Petitioner and Dr. Koralek argue that adding a detection step would reduce overall read time (Pet. Reply 25; Ex. 1024 ¶ 88), they do not properly compare the overall read time of Yamaga's unmodified system with the overall read time of their proposed modified system. Dr. Koralek testifies that "reading from DRAM is one of the slower processes in a system – certainly slower than reading same amount of data from an SRAM buffer." Ex. 1024 ¶ 92. If reading from DRAM is the rate-limiting step, as Dr. Koralek suggests (*id.*), then Petitioner fails to show how would the speed/throughput of Yamaga's system be increased by adding error detectors that read data from DRAM. Ex. 1002 ¶ 238 (proposing to "modify Yamaga's system to add an error detecting unit between DRAM 20 and first ECC units 61-1 to 60-8"); Ex. 1024 ¶ 88 (asserting that "the proposed modification would yield a much higher speed/throughput than

Yamaga’s original configuration”). Petitioner and Dr. Koralek provide no persuasive explanation for their position.

Petitioner also has no persuasive response to Patent Owner’s argument that Petitioner’s proposed modification would increase circuit scale, contrary to one of Yamaga’s disclosed objectives. PO Resp. 56, 59–60; Ex. 1005, code (57), 1:66–2:3, 3:62–67, 6:26–30, 14:66–15:12, 16:40–44; PO Sur-reply 24–25. We credit Dr. Bagherzadeh’s testimony that “[i]nserting additional error detecting units would of course *increase* the amount of circuitry consumed by error detection in Yamaga.” Ex. 2022 ¶ 174. Although Dr. Koralek testifies that “Yamaga’s Hamming decoders 61-1 to 61-8 are larger . . . than the CRC circuits 60-1 to 60-8” (Ex. 1024 ¶ 83), that testimony and the corresponding argument from Petitioner (Pet. Reply 22) does not address Patent Owner’s point that Petitioner’s proposed modification would increase circuit scale, contrary to Yamaga’s stated objective.

For these reasons, Petitioner has not shown that a POSITA would have had a reason to modify Yamaga’s system in a way that meets the forward limitation of independent claims 1, 15, and 17. Petitioner’s arguments and evidence for dependent claims 13 and 14 (Pet. 62–63) do not remedy the deficiencies in Petitioner’s challenge to independent claim 1.

4. Conclusion

Petitioner has not shown by a preponderance of the evidence that claims 1, 13–15, and 17 are unpatentable as anticipated by or obvious in view of Yamaga.

H. Petitioner's Remaining Challenges

Petitioner challenges dependent claims 2, 4, 8, and 19 based on Yamaga and Jo and dependent claims 3, 10–12, 16, 18, 23–25 based on Yamaga, Jo, and Kim. Pet. 68–80.

Patent Owner relies on its arguments for the independent claims. PO Resp. 60, 64. In addition, Patent Owner disputes Petitioner's contentions regarding a motivation to combine and reasonable expectation of success for Yamaga and Jo (Pet. 73–75; PO Resp. 61–63) and Petitioner's contentions regarding a motivation to combine Yamaga and Kim (Pet. 80–83; PO Resp. 64–65).

Petitioner's arguments and evidence for dependent claims 2–4, 8, 10–12, 16, 18, 19, and 23–25 do not remedy the shortcomings in Petitioner's challenges to independent claims 1, 15, and 17 based on Yamaga alone (*see* Section G, *supra*), nor the shortcomings in Petitioner's challenge to dependent claims 4, 8, and 19 based in part on Jo (*see* Section E.2.a, *supra*).

Accordingly, Petitioner has not shown by a preponderance of the evidence that claims 2, 4, 8, and 19 are unpatentable based on Yamaga and Jo or that dependent claims 3, 10–12, 16, 18, 23–25 are unpatentable based on Yamaga, Jo, and Kim.

III. CONCLUSION

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 13– 15, 17	102(e)	Lee		1, 2, 13–15, 17
4, 8, 19	103(a)	Lee, Jo		4, 8, 19

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
3, 10–12, 16, 18, 23–25	103(a)	Lee, Kim		3, 10–12, 16, 18, 23–25
1, 13–15, 17	102(e)	Yamaga		1, 13–15, 17
1, 13–15, 17	103(a)	Yamaga		1, 13–15, 17
2, 4, 8, 19	103(a)	Yamaga, Jo		2, 4, 8, 19
3, 10–12, 16, 18, 23–25	103(a)	Yamaga, Jo, Kim		3, 10–12, 16, 18, 23–25
Overall Outcome				1–4, 8, 10–19, 23–25

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not shown that claims 1–4, 8, 10–19, and 23–25 of the '700 Patent are unpatentable; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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