

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., AND
GLOBALFOUNDRIES U.S. 2 LLC,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2022-01083
Patent 7,402,903 B2

Before CHRISTOPHER M. KAISER, JULIA HEANEY,
and BRIAN D. RANGE, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

INTRODUCTION

A. Background

GlobalFoundries Inc., GlobalFoundries U.S. Inc., and GlobalFoundries U.S. 2 LLC (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–3, 6, and 7 of U.S. Patent No. 7,402,903 B2 (Ex. 1001, “the ’903 patent”). Katana Silicon Technologies LLC (“Patent Owner”) filed a Preliminary Response. Paper 6.

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a) (2020). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

After considering the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail with respect to at least one challenged claim. Accordingly, we do not institute an *inter partes* review of any challenged claims on any ground asserted in the Petition.

B. Related Matters

The parties identify one related matter: the ’903 patent has been asserted in *Katana Silicon Technologies LLC v. GlobalFoundries Inc. et al.*, No. 6-22-cv-00191 (W.D. Tex.). Pet. 10; Paper 5, 1.

C. The Asserted Grounds of Unpatentability

Petitioner contends that claims 1–3, 6, and 7 of the '903 patent are unpatentable based on the following grounds (Pet. 14, 16–98):¹

Claim(s) Challenged	35 U.S.C. §	References/Basis
1–3	103(a)	Christensen, ² Yasushi, ³ Lin ⁴
6	103(a)	Christensen, Yasushi, Lin, Wong, ⁵ 1994 NTRS ⁶
7	103(a)	Christensen, Yasushi, Lin, Kasahara ⁷
1–3	103(a)	Shirakawa, ⁸ Shim ⁹
6	103(a)	Shirakawa, Shim, Ren, ¹⁰ Mitani ¹¹
7	103(a)	Shirakawa, Shim, Tuinhout ¹²

¹ Petitioner also relies on declarations from Scott E. Thompson, Ph.D., and Ingrid Hsieh-Yee. Ex. 1003; Ex. 1006.

² US 5,889,306, issued Mar. 30, 1999 (Ex. 1033).

³ JP 2000-156494A, published June 6, 2000 (Ex. 1035; English translation provided as Ex. 1034).

⁴ US 6,483,147 B1, issued Nov. 19, 2002 (Ex. 1054).

⁵ US 6,246,094 B1, issued June 12, 2001 (Ex. 1044).

⁶ Semiconductor Industry Association, *The National Technology Roadmap for Semiconductors*, 1994 (Ex. 1045).

⁷ US 6,337,644 B1, issued Jan. 8, 2002 (Ex. 1050).

⁸ US 6,633,075 B1, issued Oct. 14, 2003 (Ex. 1005).

⁹ US 5,296,394, issued Mar. 22, 1994 (Ex. 1022).

¹⁰ Ren et al., *Implant isolation of GaAs-AlGaAs heterojunction bipolar transistor structures*, 56 APPL. PHYS. LETT. 860 (1990) (Ex. 1026).

¹¹ US 5,019,524, issued May 28, 1991 (Ex. 1027).

¹² Tuinhout et al., *Measurement of Lithographical Proximity Effects on Matching of Bipolar Transistors*, PROC. IEEE 1998 INT. CONFERENCE ON MICROELECTRONIC TEST STRUCTURES, Vol. 11, pp. 7–12, Mar. 1998 (Ex. 1011).

D. The '903 Patent

The '903 patent, titled “Semiconductor Device,” issued on July 22, 2008. Ex. 1001, codes (45), (54). It “relates to a semiconductor device having through plugs, more particularly, to a semiconductor device in which highly reliable through plugs are formed with good productivity.” *Id.* at 1:14–17. According to the '903 patent, there is a demand for “reduction in size and weight of electronic equipment,” which leads to a demand for “downsizing and higher-density design.” *Id.* at 1:19–23. One way to achieve this “is a stacked-type semiconductor device (multichip device) in which semiconductor integrated circuit chips (LSI chips) are three-dimensionally stacked.” *Id.* at 1:23–26. One way of enabling such stacked devices is to form “through plugs electrically connecting a face of the semiconductor substrate in which elements are formed to a rear face side.” *Id.* at 1:27–34. In the design of the '903 patent, “[t]he through plug 15 is constituted of a columnar electric conductor 15a . . . and an insulation layer 15b . . . surrounding the electric conductor 15a.” *Id.* at 6:21–25.

E. Illustrative Claim

Claims 1–3, 6, and 7 of the '903 patent are challenged. Claim 1 is independent and illustrative. We reproduce it below:

1. A semiconductor device comprising:
 - a semiconductor substrate;
 - a plurality of diffusion layer patterns formed on the semiconductor substrate;
 - an insulation film formed between the diffusion layer patterns on the semiconductor substrate to isolate the diffusion layer patterns from one another; and
 - a through plug formed to have a side surface being in contact with one of the diffusion layer patterns, the side

surface being surrounded by the one of the diffusion layer patterns without being in contact with the insulation film, and to pass through the one of the diffusion layer patterns and the semiconductor substrate.

Ex. 1001, 9:50–62.

ANALYSIS

A. Claim Construction

Petitioner argues that no claim terms require express construction. Pet. 13. Patent Owner disagrees, arguing that the term “through plug” needs to be construed. Prelim. Resp. 7–10. We agree with Patent Owner that an express construction of “through plug” is necessary to determine whether or not to institute review.

In an *inter partes* review, we construe a claim in an unexpired patent “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2020). “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

The term “through plug” appears several times in the ’903 patent, and it is used consistently throughout. First, in describing related prior art, the ’903 patent states that “[t]he through plug is constituted of an insulating material covering a sidewall of a through hole and a low electrical resistance

metal material . . . in a columnar shape that is positioned so as to be surrounded by the insulating material and that serves as a conductive member.” Ex. 1001, 1:35–40. In describing its own drawings, reference numeral 15 consistently is used to refer to the “through plug.” *Id.* at 2:37–52. Figures 1A and 1B “are views schematically showing the structure of a semiconductor device (semiconductor chip) according to an embodiment of the present invention.” *Id.* at 5:46–48, Figs. 1A, 1B. In these figures, reference numeral 15 refers to “[a] through plug.” *Id.* at 6:16. This through plug “is constituted of a columnar electric conductor 15a . . . and an insulation layer 15b . . . surrounding the electric conductor 15a.” *Id.* at 6:21–25. Similarly, reference numeral 15 refers to the “through plug” in Figures 1C, 2A, 2B, 3, 4, 5, 6, 7A, and 7B. *Id.* at 6:35–40, 7:10–38, 8:10–17, 8:32–38, 8:65–9:43. Where it is referred to in these same parts of the ’903 patent, the conductive core is discussed as merely a portion of the through plug and is referred to by the reference numeral 15a. *Id.*

Thus, the ’903 patent consistently defines the through plug as having two portions: both a conductive core and a surrounding insulation layer. This is true whether the patent is referring to either of its disclosed embodiments or the prior art. Based on this unambiguous usage, we determine that the ’903 patent defines the term “through plug” as including both a conductive core and a surrounding insulating layer. *See Phillips*, 415 F.3d at 1320–21 (“the specification ‘acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication’” (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996))).

On the present record, no other terms in the challenged claims require express construction. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

B. Asserted Obviousness Based on Christensen, Yasushi, and Lin

Petitioner argues that claims 1–3 would have been obvious over the combination of Christensen, Yasushi, and Lin. Pet. 16–44. Petitioner also argues that claim 6 would have been obvious over the combination of Christensen, Yasushi, Lin, Wong, and 1994 NTRS. *Id.* at 45–53. In addition, Petitioner argues that claim 7 would have been obvious over the combination of Christensen, Yasushi, Lin, and Kasahara. *Id.* at 53–58. Patent Owner disagrees with each argument. Prelim. Resp. 11–15.

1. Christensen

Christensen “relates generally to devices having reduced surface wiring for power source and ground applications. More specifically, the invention relates to silicon-on-insulator devices which use the bulk silicon substrate as a voltage plane for power source and ground applications.” Ex. 1033, 1:5–9. Christensen’s device has a silicon layer on an insulating layer that is on a silicon substrate. *Id.* at 3:33–44, Fig. 9. Transistors are formed on the silicon layer, and they are separated by an isolation volume. *Id.* at 4:3–57. After the transistors are formed, a conductive stud is formed to connect the substrate and the source of one of the transistors. *Id.* at 4:63–5:26.

2. *Yasushi*

Yasushi “relates to a semiconductor device and its manufacturing method and in particular to a structure for fixing the potential of a substrate in a gate finger type MOS transistor and the method for forming the structure.” Ex. 1034 ¶ 1. In Yasushi, “a contact hole is provided that penetrates through source region 7 of transistor 3 and reaches p⁺ layer 10 for fixing the substrate potential. By filling the interior of the contact hole with tungsten layer 14, p⁺ layer 10 . . . and source region 7 are electrically connected.” *Id.* ¶ 55, Fig. 1. Yasushi teaches surrounding tungsten layer 14 by source region 7. *Id.* ¶ 51, Figs. 3, 4.

3. *Lin*

Lin “relates to methods for removing heat from the device layer of Silicon-on-Insulator devices.” Ex. 1054, 1:5–9. In particular, Lin teaches “positioning one or more contacts or conductive plugs (thermally conductive) adjacent and/or within the silicon device layer to draw any heat away from the silicon device layer, through the plugs down into the bulk silicon layer of an SOI substrate.” *Id.* at 3:15–19.

4. *Analysis*

Among other limitations, claim 1 of the '903 patent recites “a through plug.” Ex. 1001, 9:50–62. Each of the other challenged claims depends from claim 1. *Id.* at 9:63–10:29. Accordingly, each of the other challenged claims incorporates the limitations of claim 1. 37 C.F.R. § 1.75(c). Thus, each challenged claim requires a “through plug.” As discussed above, we construe “through plug” in the '903 patent to include both a conductive core and a surrounding insulating layer.

Petitioner argues that the “through plug” of the challenged claims is taught both by Christensen alone and by the combination of Christensen and Lin. Pet. 33–36. We consider each argument separately.

a. Christensen alone

Petitioner argues first that Christensen alone teaches or suggests the “through plug” of the challenged claims. *Id.* at 33–34. Specifically, Petitioner argues that a person of ordinary skill in the art would have understood Christensen’s “conductive stud 34,” which extends through Christensen’s silicon layer 16 and oxide layer 14, to be a through plug. *Id.* (quoting Ex. 1033, 2:20–26, 4:63–5:11, Figs. 8B, 9) (emphasis omitted).

We are not persuaded that the Petition adequately identifies how Christensen teaches or suggests a through plug as that term is used in the ’903 patent. As noted above, the ’903 patent requires a through plug to have both a conductive core and a surrounding insulating layer. It is clear on the current record that Christensen’s “conductive stud” could correspond to the conductive portion of such a through plug. Ex. 1033, 4:66–5:1 (“the stud 34 may comprise any number of conductive materials”). But Petitioner does not show sufficiently that Christensen teaches or suggests the surrounding insulating layer necessary to turn the conductive core into a through plug. First, Petitioner does not allege that Christensen teaches or suggests such a layer. Pet. 33–34. Second, Christensen discloses the use of “conductive materials” and “material[s] which promote[] adhesion to the surrounding oxide such as titanium or titanium nitride.” Ex. 1033, 4:66–5:1, 5:15–20. None of these materials are identified by Christensen as insulators. *Id.* Accordingly, we are not persuaded on the current record that Petitioner has

shown sufficiently that Christensen alone teaches or suggests the through plug of the challenged claims.

b. Christensen and Lin

Petitioner also argues that the combination of Christensen and Lin teaches or suggests the through plug of the challenged claims. Pet. 34–36. Specifically, Petitioner argues that “[t]o the extent [it is determined] that Christensen alone is not sufficient because the conductive stud 34 does not extend all the way through wafer 12, Christensen in view of Lin renders obvious a ‘*through plug*.’” *Id.* at 34. According to this argument, “Lin teaches a backside process for forming ‘a conductive plug through a silicon’ wafer and an insulation layer,” and it would have been obvious to form such a plug “from the backside of the wafer 12 below [Christensen’s] conductive stud 34,” such that the combination of the two structures would form a conductive path all the way through the structure of Christensen’s Figures 8B and 9. *Id.* at 34–35 (emphasis omitted). As with the argument based on Christensen alone, however, this argument does not show sufficiently that the combination of Christensen and Lin teaches or suggests a through plug that has both a conductive core and a surrounding insulating layer. Lin describes its structure as a “conductive plug” and does not describe any insulation surrounding that structure. Ex. 1054, 1:60–64, 3:2–34, 4:23–32, Fig. 7. “The conductive plugs” of Lin “typically compris[e] metal,” which Lin does not describe as an insulator. *Id.* at 3:21–25. Nor does Petitioner allege the presence of a conductive core surrounded by insulation either in Lin itself or in the combination of Lin and Christensen. Pet. 34–36. Accordingly, we are not persuaded on the current record that

Petitioner has shown sufficiently that the combination of Christensen and Lin teaches or suggests the through plug of the challenged claims.

c. Grounds based on additional references

As noted above, Petitioner challenges claims 6 and 7 based on Wong, 1994 NTRS, and Kasahara in addition to Christensen, Yasushi, and Lin. Pet. 45–58. Petitioner does not allege that any of Wong, 1994 NTRS, and Kasahara teaches or suggests the through plug recited in claim 1. *Id.* Accordingly, the addition of these references does not remedy the deficiency in Petitioner’s asserted ground.

C. Asserted Obviousness Based on Shirakawa and Shim

Petitioner argues that claims 1–3 would have been obvious over the combination of Shirakawa and Shim. Pet. 59–84. Petitioner also argues that claim 6 would have been obvious over the combination of Shirakawa, Shim, Ren, and Mitani. *Id.* at 84–92. In addition, Petitioner argues that claim 7 would have been obvious over the combination of Shirakawa, Shim, and Tuinhout. *Id.* at 92–98. In each case, Patent Owner disagrees. Prelim. Resp. 15–25.

1. Shirakawa

Shirakawa “relates to heterojunction bipolar transistors including those connected in parallel and methods for fabricating the same.” Ex. 1005, 1:7–9. Specifically, Shirakawa teaches one or more heterojunction bipolar transistors (HBTs) made from gallium arsenide. *Id.* at 8:39–50. Shirakawa discloses several embodiments of its invention. *Id.* at 8:34–18:25. In the first embodiment, an HBT has a via hole formed through its emitter layer, base layer, and collector layer, as well as through the gallium arsenide substrate, to reach a heat sink layer. *Id.* at 8:66–9:59, Figs. 2A–2E. The

similar fourth embodiment teaches two HBTs connected in parallel, each with an emitter layer, base layer, collector layer and via hole, all hexagonal, rather than rectangular as in the first embodiment. *Id.* at 12:40–64, Figs. 7A–7B. Other than these differences, the HBTs of the fourth embodiment are “the same as . . . the HBT . . . of the first embodiment.” *Id.* at 12:46–47. Shirakawa’s eleventh embodiment teaches high-resistivity device isolation regions that isolate adjacent device active areas from one another. *Id.* at 16:49–17:10, Fig. 18.

2. *Shim*

Shim “relates to a manufacturing method of GaAs metal semiconductor FET (Field Effect Transistor).” Ex. 1022, 1:8–10. Shim teaches “a manufacturing method of a GaAs metal semiconductor FET in which silicon ions of a silicon layer formed on a GaAs substrate are diffused by means of ion-implantation method using little energy and annealing treatment.” *Id.* at 1:34–40. This method is contrasted with a previously known method in which “the source/drain regions of GaAs compound semiconductor devices” are doped with “ion-implantation methods using high energy.” *Id.* at 1:12–16.

3. *Analysis*

Among other limitations, claim 1 of the ’903 patent recites “a plurality of diffusion layer patterns formed on the semiconductor substrate.” Ex. 1001, 9:50–62. Each of the other challenged claims depends from claim 1. *Id.* at 9:63–10:29. Accordingly, each of the other challenged claims incorporates the limitations of claim 1. 37 C.F.R. § 1.75(c). Thus, each challenged claim requires a “plurality of diffusion layer patterns formed on the semiconductor substrate.”

Petitioner argues that the “diffusion layer patterns” of the challenged claims are taught by both Shirakawa alone and the combination of Shirakawa and Shim. Pet. 68–71. We consider each argument separately.

a. Shirakawa alone

Petitioner argues first that Shirakawa teaches “a plurality of . . . layer patterns formed on the semiconductor substrate” and that “Shirakawa renders obvious that [the layer containing these patterns] is a ‘diffusion’ layer.” Pet. 68–70 (emphases omitted). Specifically, Petitioner argues that Shirakawa’s heterojunction bipolar transistors each “ha[ve] a collector layer 3’ with a plurality of patterns,” that these layers are formed on a substrate, that they are created by patterning, and that they are made from a material that “it would have been obvious . . . is a ‘diffusion’ layer that has diffused therein n-type impurities.” *Id.* (emphasis omitted). Patent Owner argues that Petitioner does not show sufficiently that Shirakawa teaches or suggests that the layer in question would have been made using diffusion. Prelim. Resp. 17–19. On the present record, we agree with Patent Owner that Petitioner has not shown sufficiently that it would have been obvious from the teachings of Shirakawa to make Shirakawa’s layer 3’ by diffusion.

We note first that Petitioner is correct that Shirakawa teaches patterning its layer 3 into a plurality of collector layers 3’ and that Shirakawa teaches that these layers are made of n-type gallium arsenide. Ex. 1005, 8:44–55, 9:37–50, 12:40–48, Figs. 1B, 2A, 7A. We are not persuaded, however, that Petitioner has shown sufficiently that Shirakawa alone teaches or suggests that n-type gallium arsenide would have been made via diffusion.

Petitioner argues that “[i]t would have been obvious to a POSITA that ‘n-GaAs’ refers to GaAs doped or diffused with n-type impurities.” Pet. 70 (citing Ex. 1016, 8:7–19; Ex. 1022, 1:5–40; Ex. 1025, 3:49–4:67, 7:62–66). Under this argument, “doped” and “diffused” are synonymous, such that doping gallium arsenide with n-type impurities means diffusing n-type impurities into gallium arsenide. One of the references Petitioner cites does teach producing n-GaAs in this way. Ex. 1022, 1:34–40 (“silicon ions of a silicon layer formed on a GaAs substrate are diffused by means of ion-implantation method using little energy and annealing treatment”). But the other references Petitioner cites teach producing n-GaAs through epitaxial growth rather than through diffusion. Ex. 1016, 8:7–19 (“a highly doped n type GaAs subcollector layer . . . [and other layers] are made to grow above a semiinsulating GaAs substrate . . . by a metal organic vapor phase epitaxial growth method”); Ex. 1025, 4:40–45 (teaching “[f]orming two flat epitaxial layers of gallium arsenide to obtain [a] collector,” including “a layer . . . of the n+ conductivity type and a layer . . . of the n -conductivity type” by “epitaxial growth . . . from the vapour phase or from the liquid phase”). Moreover, Shirakawa itself teaches producing its collector layers by an epitaxial growth process, not through diffusion. Ex. 1005, 9:36–42 (first embodiment “collector layer” is “laminated on top of a semi-insulating GaAs substrate . . . by epitaxial growth process”), 12:47–48 (fourth embodiment made in same way as first embodiment).

Given that the prior art teaches that n-GaAs may be made through processes other than diffusion, and given that Shirakawa teaches using one of these other processes, Petitioner does not persuasively explain why a person of ordinary skill in the art would have, as Petitioner argues, produced

the n-GaAs of Shirakawa through diffusion. Accordingly, we are not persuaded on the current record that Petitioner has shown sufficiently that Shirakawa alone teaches or suggests the “diffusion layer patterns” of the challenged claims.

b. Shirakawa and Shim

Petitioner also argues that, “to the extent [it is] determined that Shirakawa’s disclosure is not sufficient to expressly disclose ‘*diffusion*,’ Shim expressly teaches that ‘silicon ions of a silicon layer formed on a GaAs substrate are **diffused** by means of ion-implantation method using little energy and annealing treatment,’” and that “[i]t would have been obvious to a POSITA to form Shirakawa’s n-GaAs collector layer 3 by a diffusion technique, as Shim teaches.” Pet. 71 (citing Pet. 65–66; Ex.1022, 1:34–40, 3:26–37) (emphases in original). In making this argument, Petitioner relies on its argument that a person of ordinary skill in the art would have combined the teachings of Shirakawa and Shim “because Shim’s diffusion teachings would facilitate the formation of” Shirakawa’s collector layer and “because [Shim’s] ‘method us[es] little energy and annealing treatment.’” Pet. 65–66.

“An invention is not obvious just ‘because all of the elements that comprise the invention were known in the prior art.’” *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013) (quoting *Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1351 (Fed. Cir. 2010)). Instead, “a finding of obviousness at the time of invention requires a ‘plausible rational[e] as to why the prior art references would have worked together.’” *Id.* (quoting *Power-One*, 599 F.3d at 1352). This rationale requires “some articulated reasoning with some rational underpinning” to combine the

known elements in the manner required in the claim at issue. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). “[I]t can be important to” include within this reasoning “a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *Id.*

Here, Petitioner offers two reasons to combine the teachings of Shim and Shirakawa. First, Petitioner argues that “Shim’s diffusion teachings would facilitate the formation of” Shirakawa’s collector layer. Pet. 65–66. On the present record, we do not find this reason sufficiently persuasive. Even though Shim does teach a way to make the n-GaAs that Shirakawa uses, Shirakawa teaches a different way to make the same material, and other prior-art references agree with Shirakawa. Ex. 1022, 1:34–40 (“silicon ions of a silicon layer formed on a GaAs substrate are diffused by means of ion-implantation method using little energy and annealing treatment”); Ex. 1005, 9:36–42 (first embodiment “collector layer” is “laminated on top of a semi-insulating GaAs substrate . . . by epitaxial growth process”), 12:47–48 (fourth embodiment made in same way as first embodiment); Ex. 1016, 8:7–19 (“a highly doped n type GaAs subcollector layer . . . [and other layers] are made to grow above a semiinsulating GaAs substrate . . . by a metal organic vapor phase epitaxial growth method”); Ex. 1025, 4:40–45 (teaching “[f]orming two flat epitaxial layers of gallium arsenide to obtain [a] collector,” including “a layer . . . of the n⁺ conductivity type and a layer . . . of the n⁻ conductivity type” by “epitaxial growth . . . from the vapour phase or from the liquid phase”). The mere fact that Shim offers an alternative process does not, in the absence of a reason to adopt that alternative process, provide a reason for a person of ordinary skill in the art

to make Shirakawa's n-GaAs via Shim's method rather than via Shirakawa's own method. In addition, Patent Owner's declarant, Dr. Peter Elenius, testifies that the ion implantation involved in Shim's diffusion process would damage Shirakawa's gallium arsenide in a way that would dissuade a person of ordinary skill in the art from using that process to produce the HBT of Shirakawa. Ex. 2001 ¶¶ 52–57.

The other reason that Petitioner provides to combine the teachings of Shim and Shirakawa is that Shim's diffusion "method us[es] little energy and annealing treatment." Pet. 66 (quoting Ex. 1022, 1:34–40). Shim's method is described as "diffus[ion] by means of ion-implantation method using little energy and annealing treatment," which Shim distinguishes from earlier methods "widely used in the art," which involved "ion-implantation . . . using high energy." Ex. 1022, 1:12–40. Shim teaches that its lower-energy ion implantation does not suffer from the "problem" of the earlier method, "damaging of ohmic contacts of metal electrodes" due to the injection of "lots of impurity ions." *Id.* at 1:17–22; *see id.* at 3:37–40 ("the manufacturing method of the present invention can prevent damage to be generated in ohmic contacts of source/drain electrodes due to ion-injecting of high density"). Thus, the lower energy of Shim's process is a benefit of that process over earlier ion implantation processes, which use higher energy. Shim does not teach that its use of lower-energy ion implantation is an improvement over other processes, such as the epitaxial growth taught by Shirakawa and the other references cited by Petitioner. Thus, Petitioner does not explain sufficiently why lower energy would be a benefit of the Shim-Shirakawa combination over Shirakawa alone. Accordingly, we are not persuaded on the current record that Petitioner has shown sufficiently that a

person of ordinary skill in the art would have had a reason to combine the teachings of Shirakawa and Shim to arrive at a combination that teaches or suggests the “diffusion layer patterns” of the challenged claims.

c. Grounds based on additional references

As noted above, Petitioner challenges claims 6 and 7 based on Mitani and Tuinhout in addition to Shirakawa and Shim. Pet. 84–98. Petitioner does not allege that either Mitani or Tuinhout provides any reason to combine the teachings of Shirakawa and Shim other than those discussed above. *Id.* Accordingly, the addition of these references does not remedy the deficiency in Petitioner’s asserted ground.

CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we determine that Petitioner has not shown a reasonable likelihood that it will prevail in showing that at least one of the challenged claims is unpatentable. Accordingly, we do not institute an *inter partes* review of any challenged claim based on any ground asserted in the Petition.

ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition is denied, and no *inter partes* review is instituted.

IPR2022-01083
Patent 7,402,903 B2

For PETITIONER:

David L. McCombs
Gregory P. Huh
Alan Wang
HAYNES AND BOONE, LLP
david.mccombs.ipr@haynesboone.com
gregory.huh.ipr@haynesboone.com
alan.wang.ipr@haynesboone.com

For PATENT OWNER:

Seth A. Lindner
Michael Pomeroy
Scott Breedlove
Brad Liddle
Daniel L. Schmid
CARTER ARNETT PLLC
slindner@carterarnett.com
mpomeroy@carterarnett.com
sbreedlove@carterarnett.com
bliddle@carterarnett.com
dschmid@carterarnett.com