

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC., and
KIOXIA CORPORATION and KIOXIA AMERICA, INC.,
Petitioner,

v.

VIASAT, INC.,
Patent Owner.

IPR2022-01126¹
Patent 8,615,700 B2

Before THU A. DANG, KEVIN F. TURNER, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ Kioxia Corporation and Kioxia America, Inc. filed a petition and a motion for joinder in IPR2023-00408 and have been joined as petitioners to this proceeding.

I. INTRODUCTION

A. *Background and Summary*

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) seeking an *inter partes* review of claims 1, 2, 4, 8, 15, 17, and 19 (the “challenged claims”) of U.S. Patent No. 8,615,700 B2 (Ex. 1001, “the ’700 Patent”). Viasat, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 12 (“Prelim. Resp.”). We instituted an *inter partes* review. Paper 13 (“Institution Decision” or “Inst. Dec.”). Kioxia Corporation and Kioxia America, Inc. (collectively, “Kioxia”) filed a substantively identical petition, and we granted institution and joined Kioxia as a petitioner to this proceeding. Paper 25 (copy of Paper 9 from IPR2023-00408).

After institution in IPR2022-01126, Patent Owner filed a Patent Owner Response (Paper 15, “PO Resp.”), Petitioner filed a Reply (Paper 24, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 27, “PO Sur-reply”). We held an oral hearing on August 30, 2023, and a transcript is in the record. Paper 31 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that some of the challenged claims of the ’700 Patent are unpatentable. Briefly, in summary, Petitioner shows that claims 1, 4, 8, 15, 17, and 19 are anticipated by Wu, but does not show that claims 1, 2, 4, 8, 15, 17, and 19 would have been obvious in view of Jo in combination with either Wu or Wan, thus challenged claim 2 has not been shown to be unpatentable.

B. Related Matters

The parties identify the following district court cases as related matters: *Viasat, Inc. v. Western Digital Corp.*, No. 6:21-CV-01230-ADA (W.D. Tex.) (the “parallel district court litigation”) and *Viasat, Inc. v. Kioxia Corp.*, No. 6:21-CV-01231-ADA (W.D. Tex.). Paper 4, 1 (Patent Owner’s mandatory notices); Paper 23 (Petitioner’s updated mandatory notices).

The parties also identify IPR2022-01067, where the ’700 Patent is challenged by Kioxia, as a related matter. Papers 4, 23.

C. The ’700 Patent (Ex. 1001)

The ’700 Patent was issued from an application filed August 18, 2010. Ex. 1001, code (22). Patent Owner does not dispute Petitioner’s contention that the ’700 Patent claims are not entitled to the August 18, 2009 filing date of an earlier provisional application. *Id.* at code (60); Pet. 18; *see* PO Resp.

The ’700 Patent discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57), 1:30–31, 2:27–28. According to the ’700 Patent, “[e]ncoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded).” *Id.* at 1:31–33. The data streams are processed at a number of error detection sub-modules, which forward an error-containing portion of the data stream to an error correction module, which corrects the forwarded portion. *Id.* at 1:33–41.

An embodiment is shown in Figure 3, reproduced below.

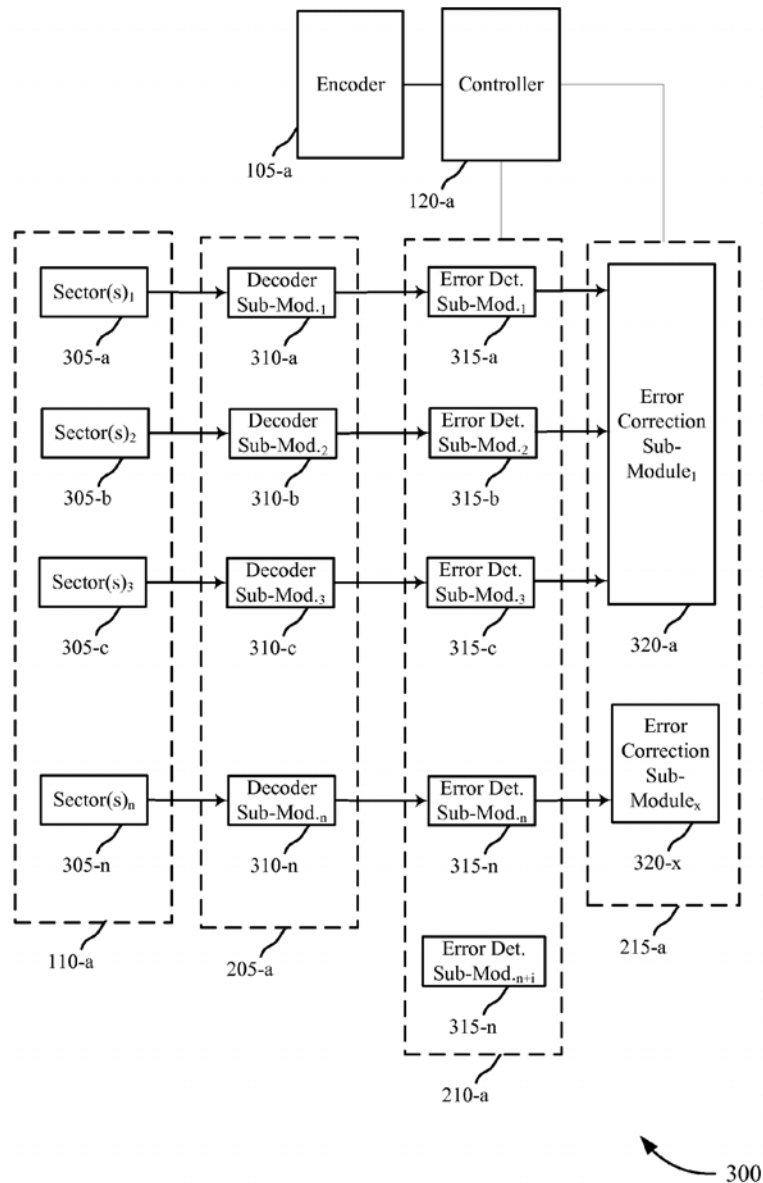


FIG. 3

Figure 3 “is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules.” Ex. 1001, 2:8–10, 6:29–32.

As shown in Figure 3, flash memory decoder system 300 includes flash memory 110-a, decoder module 205-a, error detection module 210-a, error correction module 215-a, controller 120-a, and encoder 105-a. Ex. 1001, 6:33–37. Flash memory 110-a includes a number of different sets of one or more active sectors 305. *Id.* at 6:39–40. Decoder module 205-a

includes a number of decoder sub-modules 310, each of which may be associated with a different set of sectors 305. *Id.* at 6:40–43. Error detection module 210-a includes a number of error detection sub-modules 315, each of which may be associated with a different set of sectors 305. *Id.* at 6:43–46. For example, encoded data may be read from a set of one or more of sectors 305-a by decoder sub-module 310-a, and processed (e.g., buffered, de-interleaved, and decoded to some extent) to generate a data stream, which may be forwarded to error detection sub-module 315-a. *Id.* at 6:46–52.

According to the '700 Patent, each error detection sub-module 315 evaluates a data stream to determine whether it contains an error and forwards the portion of the stream containing an error to error correction module 215-a. Ex. 1001, 6:61–67. Error correction module 215-a includes a number of error correction sub-modules 320, each of which handles errors from a number of error detection sub-modules 315 and corrects the portions of the data streams containing an error. *Id.* at 6:67–7:7.

D. Illustrative Claim

The Petition challenges claims 1, 2, 4, 8, 15, 17, and 19. Claims 2, 4, and 8 depend from claim 1, and claim 19 depends from claim 17. Claim 1 is illustrative and is reproduced below.

1. [preamble] A flash memory decoder comprising:

[1a] a decoding module configured to: receive encoded data from the flash memory; and decode the received encoded data to generate a plurality of partially decoded data streams;

[1b] an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel,

[1c] each error detection sub-module configured to: receive a different one of the plurality of partially decoded data

streams; detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module; and

[1d] the error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

Ex. 1001, 10:47–65 (bracketed text added; paragraphs adjusted); *see* Pet. 48–50 (claim chart identifying claim elements).

E. Asserted Challenges to Patentability and Evidence

Petitioner asserts the following challenges to patentability:

Claims Challenged	35 U.S.C. § ²	Reference(s)/Basis
1, 4, 8, 15, 17, 19	102(e)	Wu ³
1, 2, 4, 8, 15, 17, 19	103(a)	Jo, ⁴ Wu

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the ’700 Patent was issued on an application filed before that date, we refer to the pre-AIA versions of §§ 102 and 103. Ex. 1001, code (22).

³ Ex. 1004, US 2011/0126079 A1, filed November 24, 2009 and published May 26, 2011 (“Wu”). Petitioner asserts that Wu is prior art to the ’700 Patent under 35 U.S.C. § 102(e). Pet. 21.

⁴ Ex. 1005, US 2009/0063934 A1, filed August 27, 2008 and published March 5, 2009 (“Jo”). Petitioner asserts that Jo is prior art to the ’700 Patent under 35 U.S.C. § 102(b). Pet. 24.

Claims Challenged	35 U.S.C. § ²	Reference(s)/Basis
1, 2, 4, 8, 15, 17, 19	103(a)	Jo, Wan ⁵

Pet. 5.

F. Testimonial Evidence

The record includes a declaration of Lara Dolecek, Ph.D., submitted by Petitioner (Ex. 1003) and Dr. Dolecek’s deposition testimony submitted by Patent Owner (Ex. 2024). Also in the record is a declaration of Nader Bagherzadeh, Ph.D., submitted by Patent Owner (Ex. 2023) and Dr. Bagherzadeh’s deposition testimony submitted by Petitioner (Ex. 1021).

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is anticipated under 35 U.S.C. § 102 only if “each and every element as set forth in the claim is found, either expressly or inherently

⁵ Ex. 1006, US 2010/0070681 A1, filed September 12, 2008 and published March 18, 2010 (“Wan”). Petitioner asserts that Wan is prior art to the ’700 Patent under 35 U.S.C. §§ 102(a) and 102(e). Pet. 27.

described, in a single prior art reference.” *Verdegaal Bros. Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented,⁶ objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

⁶ Here, neither party submits evidence of secondary considerations.

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “at least a [bachelor of science degree] in electrical engineering or computer science or a related field, and four years’ experience designing, developing, or researching error correction coding (‘ECC’) systems (which include forward error correction or ‘FEC’ systems).” Pet. 19 (citing Ex. 1003 ¶¶ 23–25, 66). Petitioner states that “a higher education or skill level might make up for less experience, and vice-versa.” Pet. 19–20.

Patent Owner asserts that a POSITA would have had “at least a [bachelor of science degree] in electrical engineering, computer engineering, or computer science or a related field, and at least two years of experience in the design, development, or research of the hardware implementation of error correction systems.” PO Resp. 3 (citing Ex. 2023 ¶¶ 26–32, 67–92). In addition, Patent Owner asserts that “[a]dvanced education may substitute for experience and vice versa.” *Id.*

The parties’ articulations of the level of ordinary skill in the art are similar, and we adopt parts of each party’s description of a POSITA’s education and experience. We agree with Patent Owner that computer engineering is a relevant field of study. PO Resp. 3. Our finding is supported by the ’700 Patent, which describes systems, devices, methods, and software for forward error correction for a flash memory system, which may be integrated with a computer, server, or other computing device. Ex. 1001, 3:23–30. We adopt Patent Owner’s proposal regarding the length of a POSITA’s practical experience—two years—rather than four years, as proposed by Petitioner. Neither Petitioner nor Dr. Dolecek assert that two years of practical experience would have been insufficient to acquire

ordinary skill in the art. We disagree with Patent Owner’s assertion that a POSITA’s experience would have been limited to “hardware implementation.” PO Resp. 3. Our finding is supported by the ’700 Patent, which states that “embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof.” Ex. 1001, 10:26–28. Petitioner’s assertion that a POSITA needs to have experience in “error correction coding (‘ECC’) systems (which include forward error correction or ‘FEC’ systems)” (Pet. 19; Ex. 1003 ¶ 25) is consistent with the ’700 Patent, which discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57); *see also* Ex. 1003 ¶¶ 57, 66 (explaining that error correction coding (“ECC”) includes forward error correction (“FEC”)).

For these reasons, we find that a POSITA would have had a bachelor of science degree in electrical engineering, computer engineering, or computer science or a related field, and two years of experience designing, developing, or researching error correction coding systems, which include forward error correction systems.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner*

v. Sony Comput. Entm't Am. LLC, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012).

“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”

Realtime Data, LLC v. Iancu, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Neither party seeks express constructions of any claim terms. *See* Pet. 20; *see generally* PO Resp. We do not need to provide an express construction for any claim terms for purposes of resolving the controversy before us.

D. Petitioner's Wu Anticipation Challenge

Petitioner challenges claims 1, 4, 8, 15, 17, and 19 as anticipated by Wu. Pet. 31–52. Patent Owner opposes. PO Resp. 3–19. We provide an overview of Wu before turning to our analysis.

1. Wu (Ex. 1004)

Wu discloses multi-channel memory apparatus. Ex. 1004, codes (54), (57). Figure 8 is reproduced below.

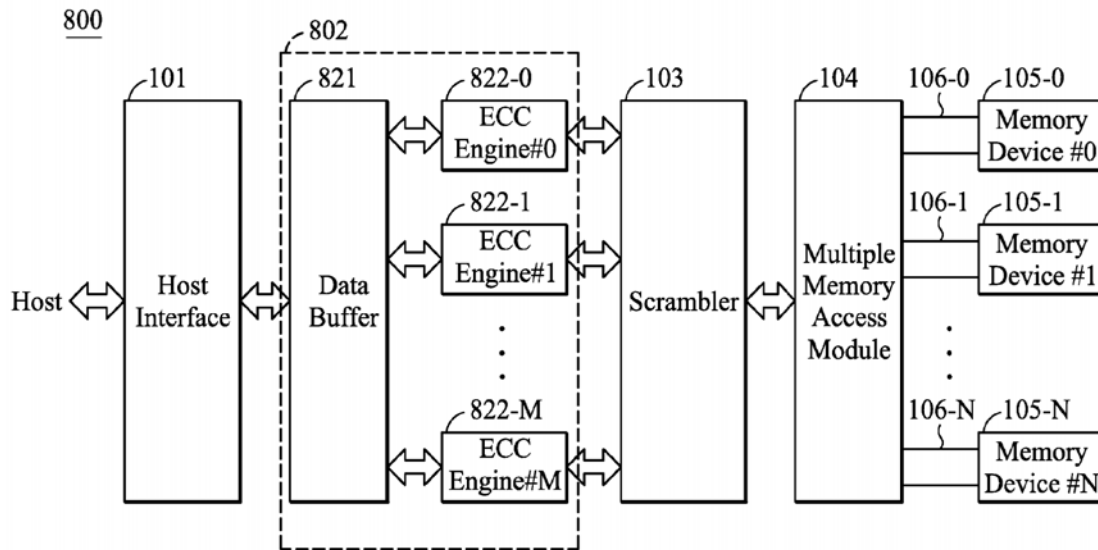


FIG. 8

Wu's Figure 8 shows multi-channel memory apparatus 800, including host interface 101, error correcting module 802, scramblers 103, multiple memory access module 104, memory devices 105-0 to 105-N, and storage channels 106-0 to 106-N. Ex. 1004 ¶¶ 22, 33. Error correcting module 802 includes ECC engine 822-0 and a plurality of sub-ECC engines 822-1 to 822-M coupled in parallel with the ECC engine 822-0. *Id.* ¶ 33.

Wu discloses that scrambler 103 performs intra-channel disarrangement for the data to be stored into the memory devices and rearranges the scrambled data read out from the memory devices in a reverse manner depending on the data transferring direction (e.g., write or read direction). Ex. 1004 ¶ 23. According to Wu, multiple memory access module 104 performs multiple access control of storage channels 106-0 to 106-N for error correcting module 802 and multiplexes the data received simultaneously from different memory devices 105-0 to 105-N to the error correcting module. *Id.* ¶ 24.

2. *Claim 1*

a) *Preamble*

The preamble of claim 1 recites “[a] flash memory decoder.”
Ex. 1001, 10:47.

Petitioner shows persuasively, and Patent Owner does not dispute, that Wu discloses the preamble of claim 1. Pet. 31–33 (citing Ex. 1003 ¶¶ 69–77; Ex. 1004 ¶¶ 22–24, 33, Fig. 8); see PO Resp. 3–19. Our finding is supported by Wu’s Figure 8, which shows a multi-channel memory apparatus. Ex. 1004 ¶¶ 22, 33, Fig. 8. Our finding is also supported by the testimony of Petitioner’s expert, Dr. Dolecek, that a POSITA would have understood that Wu discloses a “flash memory decoder,” as claimed, and her annotation of Wu’s Figure 8 identifying a flash memory and a decoder of the flash memory. Ex. 1003 ¶ 77.

b) *Claim Element [1a]*

Claim element [1a] recites “a decoding module configured to receive encoded data from the flash memory; and decode the received encoded data to generate a plurality of partially decoded data streams.” Ex. 1001, 10:4–51.

Petitioner contends that Wu discloses a “decoding module” corresponding to the combination of multiple memory access module 104 and scrambler 103. Pet. 33. Petitioner contends that, in Wu, the data retrieved from memory devices 105-0 to 105-N and provided to ECC Engines 822-0 to 822-M constitute disclosure of a “plurality of partially decoded data streams,” as recited in claim 1. Pet. 36.

Patent Owner argues that neither Wu's multiple memory access module nor Wu's scrambler is a "decoding module" that "generate[s] a plurality of partially decoded data streams," as claimed. PO Resp. 3–18.

We are persuaded by Petitioner's showing for claim element [1a] based on Wu. Pet. 33–37; Ex. 1003 ¶¶ 78–89. Petitioner shows that a "decoding module," as claimed, is disclosed by the combination of multiple memory access module 104 and scrambler 103 in Wu's Figure 8.

Pet. 33–34. Our finding is supported by Wu's Figure 8, which shows scrambler 103 coupled to multiple memory access module 104, which is in turn coupled to storage channels 106-0 to 106-N, with each storage channel being coupled to a memory device 105-0 to 105-N. Ex. 1004 ¶¶ 22–24 (describing Figure 1), ¶ 33 (describing Figure 8 with reference to Figure 1 and the corresponding description), Fig. 8.

Petitioner shows persuasively that the "decoding module," i.e., the combination of Wu's multiple memory access module 104 and Wu's scrambler 103, is "configured to: receive encoded data from the flash memory," as recited in claim element [1a]. Pet. 34. Our finding is supported by Wu, which discloses that the data stored on flash memory devices 105-0 to 105-N is encoded data. Ex. 1004 ¶¶ 22, 28, 29, Figs. 4, 5 (flow charts illustrating a write operation and a read operation, respectively). Wu further discloses that, during a read operation, the multiple memory access module reads data from the memory devices. *Id.* ¶ 29, Fig. 5; *see also id.* ¶ 24 (disclosing that multiple memory access module 104 receives data from memory devices 105-0 to 105-N).

Petitioner shows persuasively that the "decoding module," i.e., the combination of Wu's multiple memory access module 104 and Wu's scrambler 103, is "configured to: . . . decode the received encoded data to

generate a plurality of partially decoded data streams,” as recited in claim element [1a]. Pet. 34–37. Our finding is supported by Wu, which discloses that multiple memory access module 104 and scrambler 103 each rearrange data read out from memory devices through the storage channels, with multiple memory access module 104 performing inter-channel rearrangement and scrambler 103 performing intra-channel rearrangement. Ex. 1004 ¶¶ 23, 27; *see also* Ex. 1003 ¶¶ 84, 85 (Dr. Dolecek explaining the function of Wu’s multiple memory access module 104 and scrambler 103).

Petitioner and Dr. Dolecek assert that partial decoding is disclosed by the function of scrambler 103, or alternatively, by the function of multiple memory access module 104. Pet. 36–37; Ex. 1003 ¶¶ 86–88. On this record, the term “partially decoded” is broad enough to encompass both scrambler 103’s intra-channel rearrangement (descrambling) and multiple memory access module 104’s inter-channel rearrangement (de-interleaving).⁷ Ex. 1006 ¶ 52 (Wan disclosing that “scrambling is considered to be a form of encoding and descrambling is considered to be a form of decoding”); Pet. 36–37 (asserting that, according to Patent Owner’s confidential infringement contentions in the related litigation, de-

⁷ In our final written decision in the related *inter partes* review, we construe the phrase “decode the received encoded data” to mean “distinguish error correction bits from information bits in the received encoded data.” IPR2022-01067, Paper 34 at 17 & n.9. In IPR2022-01067, it was unnecessary to include intra-channel rearrangement (descrambling) or inter-channel rearrangement (de-interleaving) in the claim construction because the petitioner in that proceeding did not rely on these examples of “decoding” to prove its unpatentability challenges. *Id.* Similarly, in this proceeding, it is not necessary for us to include “distinguish error correction bits from information bits in the received encoded data” in the definition of “partially decoded” because Petitioner does not rely on that example to prove its unpatentability challenges.

interleaving can be partial decoding). Accordingly, the record supports both alternatives asserted by Petitioner and Dr. Dolecek.

Petitioner shows persuasively that the combination of Wu’s multiple memory access module 104 and Wu’s scrambler 103 “generate[s] a plurality of partially decoded data streams,” as recited in claim element [1a].

Pet. 36–37. Our finding is supported by Wu’s Figure 8, which shows a plurality of data streams flowing from scrambler 103 to ECC engines 822-0 to 822-M. Ex. 1004, Fig. 8; *see also* Pet. 37 (reproducing Wu’s Figure 8 with double-headed arrows between ECC engines 822-0 to 822-M and scrambler 103 shaded yellow to identify a “plurality of partially decoded data streams”); Ex. 1003 ¶ 86 (same).

Patent Owner disputes Petitioner’s contentions for claim element [1a] based on Wu. PO Resp. 3–18. Patent Owner begins by arguing that Wu’s multiple memory access module 104 (“MMAM”) multiplexes the data to output a single data stream, rather than generating a plurality of partially decoded data streams, as claimed. *Id.* at 5–8. Petitioner does not dispute Patent Owner’s assertion that the output of Wu’s MMAM 104 is “one long data stream.” *Id.* at 7; Pet. Reply 3. Instead, for this aspect of for claim element [1a], Petitioner points to the output of Wu’s scrambler, arguing that “Wu’s Fig. 8 . . . unambiguously discloses [M+1] double-sided arrows—i.e., multiple data streams—output from scrambler 103 to [M+1] ECC Engines.” Pet. Reply 2; *see also* Pet. 36–37 (same argument). We agree with Petitioner. Although Wu’s MMAM multiplexes the data to output a single data stream, that fact does not defeat Petitioner’s anticipation challenge. Petitioner shows persuasively that **the combination** of Wu’s MMAM 104 and Wu’s scrambler 103 “generate[s] a plurality of partially decoded data streams,” as claimed. Pet. 33, 36–37.

Next, Patent Owner argues that Wu’s scrambler does not generate multiple data streams. PO Resp. 8–15. According to Patent Owner, neither Wu nor Petitioner describes how the scrambler could generate multiple data streams from “one long data stream.” *Id.* Patent Owner acknowledges the multiple arrows in Wu’s Figure 8, but argues that Figure 8 is “akin to a non-anticipatory ‘accidental’ disclosure” and that “modifications,” including “additional, undisclosed components,” would be necessary to generate multiple data streams. *Id.* at 11–13 & n.1.

We agree with Petitioner that the depiction of multiple double-sided arrows between scrambler 103 and ECC Engines 822-0 to 822-M in Wu’s Figure 8 is sufficient to disclose the generation of a plurality of data streams, as claimed. Pet. 36–37; Pet. Reply 2–6. As between Petitioner’s position that the multiple arrows in Wu’s Figure 8 represent multiple data streams (Pet. 36–37; Pet. Reply 2–3), and Patent Owner’s position that “those arrows are not meant to be taken literally as literal data streams” (Tr. 35:16–17), we find that Petitioner’s position is more reasonable, consistent with the legal standard for anticipation, and amply supported in the record.

“In an anticipation analysis, the dispositive question is whether a skilled artisan would ‘reasonably understand or infer’ from a prior art reference that every claim limitation is disclosed in that single reference.” *Acoustic Tech., Inc. v. Itron Networked Sols., Inc.*, 949 F.3d 1366, 1373 (Fed. Cir. 2020) (citing *Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003)). “Expert testimony may shed light on what a skilled artisan would reasonably understand or infer from a prior art reference.” *Id.* (citing *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018)).

Petitioner’s contention is supported by Dr. Dolecek’s testimony that, “[a]s shown in Wu’s Figure 8, reproduced below, a POSITA would have understood that the data retrieved from memory devices 105-0 to 105-N and provided to ECC Engines 822-0 to 822-M corresponds to the claimed ‘plurality of partially decoded data streams’ (yellow in Figure 8).” Ex. 1003 ¶ 86 (reproducing Wu’s Figure 8 with double-headed arrows between ECC engines 822-0 to 822-M and scrambler 103 shaded yellow to identify a “plurality of partially decoded data streams”).

We find that Dr. Dolecek’s testimony about Wu’s Figure 8 and a “plurality of data streams” is more credible than Dr. Bagherzadeh’s testimony on this topic. Dr. Bagherzadeh testifies that Wu’s scrambler “does not split, copy, or otherwise ‘generate a plurality of partially decoded data streams.’” *Id.* ¶¶ 100, 108. But that testimony fails to take into account what the depiction of multiple double-sided arrows in Wu’s Figure 8 would have meant to a POSITA, as Dr. Dolecek testifies. Ex. 1003 ¶ 86 (reproducing Wu’s Figure 8 with double-headed arrows between ECC engines 822-0 to 822-M and scrambler 103 shaded yellow to identify a “plurality of partially decoded data streams”). The evidence does not support Dr. Bagherzadeh’s opinion that Wu’s Figure 8 is “incompatible” with Wu’s description and “there’s no way to generate a plurality of data streams from the Scrambler to the ECC Engines.” Ex. 2023 ¶ 109. As Dr. Dolecek explained below, when viewed through the eyes of a POSITA, Wu discloses that the scrambler can generate a plurality of data streams.

After quoting from Dr. Dolecek’s deposition testimony (Ex. 2023 ¶ 107 (quoting Ex. 2024, 32:15–22)), Dr. Bagherzadeh asserts that “Dr. Dolecek does not explain *how* she believes the intra-channel operation of the Scrambler on the ‘one long data stream’ it receives could generate a

plurality of data streams.” *Id.* ¶ 108. Dr. Bagherzadeh fails to take into account Dr. Dolecek’s testimony in response to follow-up questions from Patent Owner.

Q So you have found the plurality of data streams in the three arrows of Figure 8 going from the scrambler to the ECC engines?

A Yes. . . .

Q And how exactly, in your understanding as a person of skill, does the scrambler generate that plurality? . . .

THE WITNESS: . . . So the person of ordinary skill in the art would understand that these are multiple arrows here indicated explicitly to suggest parallel operations of the ECC engines.

And for them to have parallel operations, a person of ordinary skill in the art would assume that they are receiving inputs at the same time, and the scrambler would, for example, do that by sending descrambled data to different engines at a time, one at a time. . . .

Q So how does the scrambler’s function of intrachannel rearrangement generate multiple data streams? . . .

THE WITNESS: Once it’s descrambled on a per-block basis, it simply sends that block to a given engine, ECC engine. . . .

Q Can the scrambler send out multiple data streams in parallel at the same time?

A If it’s designed like that, yes.

Ex. 2024, 32:24–34:7 (objections and witness’s false start omitted).

Q So describe for me how in Figure 8 that would work for your analysis where the scrambler receiving the data from the multiplexer would then generate the plurality of partially decoded data streams.

A Right. Figure 8.

So if it receives a long string of data that has already been processed by the 104 unit, it would perform intra- -- intrachannel, if you will, intrablock disarrangement of data. And then it could

send each of these blocks or some multiples of these blocks to each of these ECC engines in order.

Id. at 36:5–15. Contrary to Dr. Bagherzadeh’s assertion, Dr. Dolecek does explain how Wu’s scrambler could generate a plurality of data streams. *Id.* Dr. Dolecek’s testimony persuasively refutes Dr. Bagherzadeh’s opinion that “there’s no way to generate a plurality of data streams from the Scrambler to the ECC Engines.” Ex. 2023 ¶ 109.

We disagree with Patent Owner’s argument that modifications would be needed to make Wu’s Figure 8 function as the “decoding module” of claim 1. PO Resp. 13–14. No modifications of Wu’s Figure 8 are needed. As demonstrated by Petitioner and Dr. Dolecek, the figure discloses claim element [1a] without the need for modification. Pet. 36–37; Ex. 1003 ¶ 86. Although Wu does not provide the details of the scrambler or other structures that would allow a single data stream to be partitioned into multiple data streams, the reference is presumed to be enabling. *Apple Inc. v. Corephotonics, Ltd.*, 861 F. App’x 443, 450 (Fed. Cir. 2021) (“[P]rior art patents and publications enjoy a presumption of enablement, and the patentee/applicant has the burden to prove nonenablement for such prior art.”).

Patent Owner does not meet its burden to prove that Wu is nonenabling. Wu provides at least as much information as the ’700 Patent about how to generate a plurality of partially decoded data streams. *See Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 781 (Fed. Cir. 1985) (answering the prior art enablement question by comparison with appellee’s own patent application). The ’700 Patent discloses that a decoder module receives encoded data from flash memory and processes the encoded data to generate a number of partially decoded data streams, but provides no

further detail about how to generate the data streams. Ex. 1001, 3:52–54, 6:9–14, 8:48–52, 9:10–12, Fig. 5 (block 510), Fig. 6 (block 625). When the level of detail supplied by the '700 Patent is used as a basis for comparison, Wu's Figure 8 provides sufficient information about how to generate a plurality of partially decoded data streams.

Patent Owner asserts that “modifications” would be needed to make Wu's Figure 8 work as the claimed “decoding module.” PO Resp. 13 (citing Ex. 2024, 34:8–35:1, 40:2–41:6). Dr. Dolecek's testimony does not, however, support Patent Owner's assertion and instead demonstrates that the asserted “modifications” are actually ways of implementing Wu's disclosure that would have been known to a POSITA. For example, Dr. Dolecek's testimony demonstrates that a POSITA would have known that one way to implement scrambler 103 would be to use multiple parallel scramblers, as illustrated in Wu's Figure 7 (Ex. 2024, 34:8–35:15, 37:19–38:3), or a demultiplexer or buffer to allow the partitioning of the data to be accessible in parallel to the multiple scramblers (*id.* at 40:2–22).

Next, Patent Owner argues that the intra-channel rearrangement performed by Wu's scrambler 103 is not the “partial decoding” of claim 1 because it does not occur “before, and in preparation for, error detection.” PO Resp. 15–18. Patent Owner's argument does not undermine the persuasiveness of Petitioner's showing for two reasons. First, it does not address Petitioner's alternative way of mapping claim 1 to Wu, which relies on the function of Wu's multiple memory access module 104 as disclosing the partial decoding of claim 1. Pet. 36 (“Alternatively, the partial decoding is disclosed by the inter-channel rearrangement performed by multiple memory access module 104”); Pet. 34–35 (addressing the partial decoding limitation and relying on Wu's disclosure that multiple memory

access module 104 “*rearrange[s] the data read out from memory devices through the storage channels*” (quoting Ex. 1004 ¶ 27)); *see also* Pet.

Reply 9 (asserting that Patent Owner “does not dispute that MMAM 104 ‘partially decodes’ data by performing inter-channel rearrangement”); PO Sur-reply 1–8 (contesting Wu anticipation challenge without revisiting Patent Owner’s argument about “partial decoding”).

Second, even if Patent Owner is correct that claim 1’s recitation of “partially decoded” refers to a step that “occurs before, and in preparation for, error detection” (PO Resp. 15), Petitioner shows that Patent Owner’s claim construction is met by Wu. Pet. Reply 8; Pet. 34–36. Petitioner shows persuasively that Wu discloses a decoding module that includes scrambler 103 and that Wu’s scrambler 103 performs intra-channel rearrangement (descrambling) before error detection and in preparation for error detection. Pet. Reply 8; Pet. 34–36. Our finding is supported by Wu’s Figure 8, which shows that, during a read operation, data flows from right to left, passing from memory devices 105 through storage channels 106, multiple memory access module 104, and scramblers 103, before reaching ECC engines 822, where error detection and correction takes place. Ex. 1004 ¶¶ 29, 33, Fig. 8; *see also id.* Fig. 5 (flow chart of a read operation). Although Wu discloses that “the scrambler (scrambler module) may be located anywhere in the data transferring paths (e.g. write or read paths)” (*id.* ¶¶ 23, 30), Wu’s Figure 8 shows scramblers 103 located *before* ECC engines 822 in the read path.

Wu discloses that, during a read operation, scramblers 103 “rearrange the scrambled data read out from the memory devices.” *Id.* ¶¶ 23, 30. In Wu’s Figure 8 embodiment, data rearrangement (descrambling) occurs before and in preparation for error detection. Our finding is supported by

the testimony of Dr. Bagherzadeh cited by Petitioner. Pet. Reply 8 (citing Ex. 1021, 36:10–14, 37:21–25). Dr. Bagherzadeh agreed that Wu’s Figure 8 embodiment “will not work” if the descrambling on a read operation were not performed and instead scrambled code words were sent to the error correcting module. Ex. 1021, 36:8–37:25. According to Dr. Bagherzadeh, “It will not work because . . . you’re twisting the bits as you’re writing it, but you’re not untwisting the bit[s]” during a read operation. *Id.* at 37:21–25.

c) Claim Element [1b]

Claim element [1b] recites “an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel.” Ex. 1001, 10:52–55.

Petitioner shows persuasively, and Patent Owner does not dispute, that Wu discloses claim element [1b]. Pet. 37–40 (citing Ex. 1003 ¶¶ 91–95; Ex. 1004 ¶¶ 33, 34, Figs. 8, 9); PO Resp. 3–19. More particularly, Petitioner demonstrates that Wu discloses “an error detection module” (Wu’s error detectors 902-0 to 902-K within ECC engines 822-0 to 822-M, collectively) “communicatively coupled with the decoding module” (Wu’s scrambler 103 and MMAM 104 in combination) “and comprising a plurality of error detection sub-modules” (Wu’s error detectors 902-0 to 902-K, individually) “operating in parallel,” as recited in claim element [1b]. Pet. 33, 37–40; Ex. 1003 ¶¶ 91–95; Ex. 1004 ¶¶ 33, 34, Figs. 8, 9.

Our finding is supported by Wu’s Figure 8, which shows “a plurality of ECC engines 822-0, 822-1 to 822-M” coupled to scramblers 103, which corresponds to part of the “decoding module.” Ex. 1004 ¶ 33, Fig. 8; *see* Pet. 33 (identifying scrambler 103 as part of the claimed “decoding

module”). Additional support is provided by Wu’s Figure 9, reproduced below.

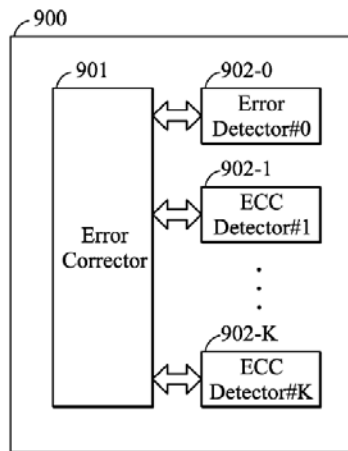


FIG. 9

Ex. 1004, Fig. 9. Wu’s Figure 9 shows ECC engine/sub-ECC engine 900, including ECC Detectors 902-0 to 902-K⁸ and Error Corrector 901. *Id.* ¶ 34.

As Dr. Dolecek explains, each of ECC Engines 822-0 to 822-M in Wu’s Figure 8 has the structure of ECC engine/sub-ECC engine 900 in Figure 9 and comprises ECC Detectors 902-0 to 902-K. Ex. 1003 ¶ 92; Ex. 1004 ¶ 34, Figs. 8, 9. Wu’s ECC Detectors 902-0 to 902-K (which reside within each ECC engine 822-0 to 822-M) collectively correspond to “an error detection module,” as recited in claim element [1b], with each detector individually corresponding to an error detection sub-module. Ex. 1003 ¶¶ 94, 98. Dr. Dolecek illustrates her testimony with the following annotated compilation of Wu’s Figures 8 and 9.

⁸ In the text, Wu refers to “error detectors 902-0 to 902-K” (Ex. 1004 ¶ 34), whereas, in Figure 9, each detector 902-0, 902-1, and 902-K is labeled “ECC Detector.” We understand that Wu uses the terms “error detector” and “ECC Detector” interchangeably to refer to the same structure, and we do the same.

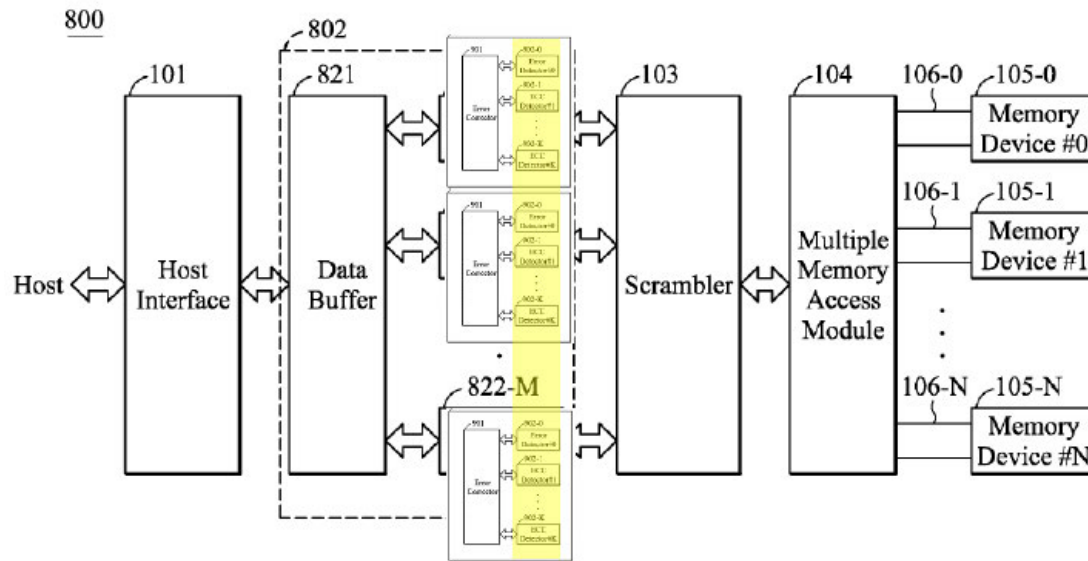


FIG. 8

Id.; see also Pet. 40 (same figure). Dr. Dolecek’s compilation shows multi-channel memory apparatus 800 from Wu’s Figure 8 with ECC engines 900 from Wu’s Figure 9. Consistent with Wu’s disclosure, Dr. Dolecek modifies Wu’s Figure 8 by replacing each of ECC Engines 822-0, 822-1, and 822-M with a copy of ECC engine 900 from Figure 9. Ex. 1003 ¶ 94; Ex. 1004 ¶ 34. In the annotated compilation, the three sets of ECC Detectors 902-0, 902-1, and 902-K are shaded yellow to identify “an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel,” as recited in claim element [1b]. Ex. 1003 ¶ 94. We credit Dr. Dolecek’s undisputed testimony that “a POSITA would have understood that Wu’s error detectors 902 operate in parallel.” *Id.* ¶ 95.

d) Claim Element [1c]

Claim element [1c] recites “each error detection sub-module configured to: [i] receive a different one of the plurality of partially decoded data streams; [ii] detect whether a portion of the respective received stream

contains an error; and [iii] forward the portion of the respective received stream containing an error to an error correction module.” Ex. 1001, 10:56–61 (bracketed text added).

Petitioner shows persuasively that Wu discloses claim element [1c]. Pet. 41–42 (citing Ex. 1003 ¶¶ 98–102; Ex. 1004 ¶ 34, Figs. 8, 9). As discussed above for claim element [1b], Wu discloses error detectors 902-0 to 902-K, which correspond to the recited “error detection sub-modules.” Ex. 1004 ¶ 34.

Our finding for clause [i] of claim element [1c] is supported by Dr. Dolecek’s testimony, as follows:

Each of the (K+1) error detectors within each ECC engine, (i.e., each “error detection sub-module”) receives (on a memory read operation) a portion of one of the (M+1) partially decoded data streams provided at the output of the “decoder module,” *i.e.*, at the output of scrambler 103. A POSITA would have understood that these portions of partially decoded data streams are themselves the claimed (K+1)×(M+1) “plurality of partially decoded data streams.”

Ex. 1003 ¶ 98 (cited at Pet. 41).

Regarding clause [ii] of claim element [1c], Wu discloses that “error detectors 902-0 to 902-K are arranged to . . . detect error(s) in the data read out from the memory devices.” Ex. 1004 ¶ 34; *see also* Pet. 31; Ex. 1003 ¶ 99 (Petitioner and Dr. Dolecek relying on this disclosure).

Regarding clause [iii] of claim element [1c], Wu’s Figure 9 shows double-sided arrows linking each of ECC Detectors 902-0 to 902-K to Error Corrector 901, which indicates that, during a read operation, data flows from the error detectors to the error corrector. Ex. 1004, Fig. 9. Referring to Figure 9, Wu discloses that “error corrector 901 is shared by the error

detectors 902-0 to 902-K and arranged to correct the error(s) of the data detected by the error detectors.” *Id.* ¶ 34.

Patent Owner argues that Wu does not disclose claim element [1c] “[f]or the same reasons” as Patent Owner presents for claim element [1a]. PO Resp. 18. According to Patent Owner, “Wu’s Figure 8 does not describe a scrambler that divides up the one long data stream it receives from the MMAM.” *Id.* at 18–19 (citing Ex. 1004 ¶ 23). We disagree for the same reasons discussed above in connection with claim element [1a]. *See* Section II.D.2.b, *supra*. Patent Owner’s argument is belied by Wu’s Figure 8, which shows that, during a read operation, a single data stream enters scrambler 103, and multiple data streams exit scrambler 103 and are received by ECC Engines 822-0 to 822-M.

e) Claim Element [1d]

Claim element [1d] recites “the error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.” Ex. 1001, 10:62–65.

Petitioner shows persuasively, and Patent Owner does not dispute, that Wu discloses claim element [1d]. Pet. 42–45 (citing Ex. 1003 ¶¶ 106–108; Ex. 1004 ¶¶ 22, 33, 34, Figs. 8, 9); PO Resp. 3–19. More particularly, Petitioner demonstrates that Wu discloses that “the error correction module” (Wu’s error correctors 901) is “communicatively coupled with and physically separate from the error detection module” (Wu’s error detectors 902-0 to 902-K) and “configured to correct the received portions of the respective received streams containing an error,” as recited in claim element [1d]. Pet. 43–45; Ex. 1003 ¶¶ 91–95; Ex. 1003

¶¶ 106–108; Ex. 1004 ¶¶ 22, 33, 34, Figs. 8, 9. Our finding is supported by Wu’s Figure 9, which shows Error Corrector 901 communicatively coupled with and physically separate from ECC Detectors 902-0 to 902-K. Ex. 1004, Fig. 9. Referring to Figure 9, Wu discloses that “error corrector 901 is shared by the error detectors 902-0 to 902-K and arranged to correct the error(s) of the data detected by the error detectors.” *Id.* ¶ 34.

3. *Claim 4*

Claim 4 depends from claim 1 and recites “wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.” Ex. 1001, 11:7–10.

Petitioner contends that Wu discloses the limitations of dependent claim 4. Pet. 45–46 (citing Ex. 1003 ¶¶ 112–114; Ex. 1004, Figs. 8, 9). Patent Owner does not dispute Petitioner’s contention (*see* PO Resp. 19), which we find persuasive and supported by the evidence. To illustrate her testimony for claim 4, Dr. Dolecek provides the following annotated compilation of Wu’s Figures 8 and 9.

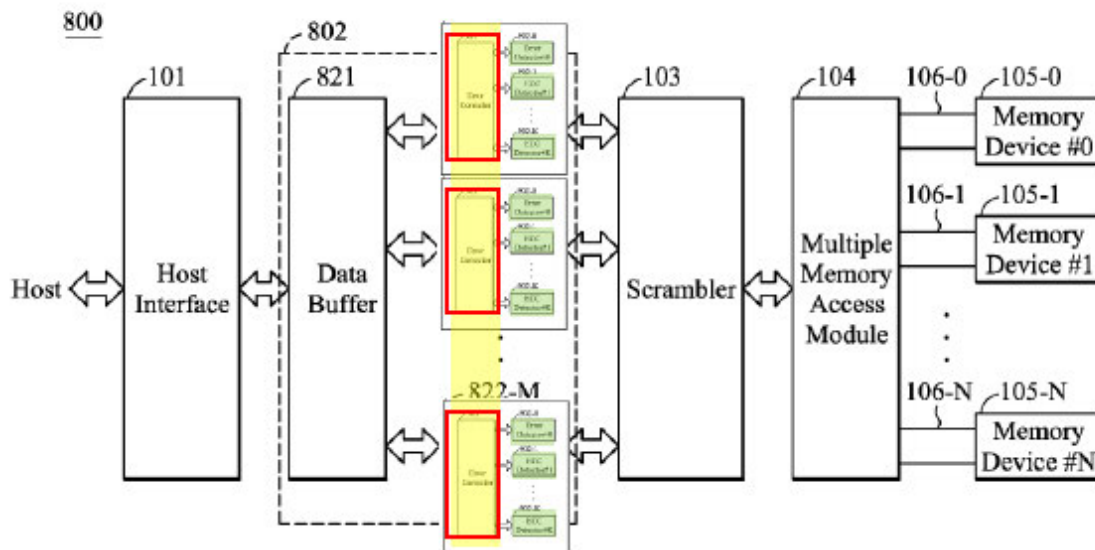


FIG. 8

Ex. 1004 ¶ 112; *see also* Pet. 45 (same figure). The annotated figure shows the multi-channel memory apparatus of Wu’s Figure 8 with each of ECC Engines 822-0, 822-1, and 822-M replaced by a copy of ECC engine 900 from Figure 9. As illustrated in the annotated figure, “the error correction module” (Wu’s Error Correctors 901, collectively, shaded yellow) “comprises a plurality of error correction sub-modules” (Wu’s Error Correctors 901, individually, outlined by red boxes) “operating in parallel and fewer in number than the error detection sub-modules” (Wu’s ECC Detectors 902, shaded green). Ex. 1003 ¶ 112; Ex. 1004 ¶ 34, Figs. 8, 9. Our finding is supported by Dr. Dolecek’s undisputed testimony that Wu’s “error correctors 901 operating in parallel are fewer in number than detectors 902.” Ex. 1003 ¶ 112.

4. Claim 8

Claim 8 recites

The flash memory decoder of claim 4, wherein, [8a] each error correction sub-module is assigned a set of two or more error

detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules; and [8b] each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module.

Ex. 1001, 11:36–46 (bracketed text added).

Petitioner shows persuasively that Wu discloses the limitations of dependent claim 8. Pet. 46–47 (citing Ex. 1003 ¶¶ 116–122; Ex. 1004 ¶¶ 33, 34, Figs. 8, 9). Patent Owner does not dispute Petitioner’s contention (*see* PO Resp. 19), which we find persuasive and supported by the evidence.

Our finding for claim element [8a] is supported by Dr. Dolecek’s testimony as follows.

Wu’s Figure 8, as described and annotated above in connection with claim 4 to include the exemplary ECC Engine 822 structure shown in Wu’s Figure 9, discloses “each error correction sub-module,” that is, error corrector modules 901 within ECC Engines 822-0- to 822-M, “is assigned a set of two or more error detection sub-modules,” that is, (k+1) error detector modules 902 within each ECC Engines 822-0- to 822-M “different from error detection sub-modules associated with other of the error correction sub-modules.”

Ex. 1003 ¶ 117 (referring to the annotated compilation of Wu’s Figures 8 and 9 reproduced above).

Our finding for claim element [8b] is supported by Wu’s Figure 8, which shows ECC engines 822-0 to 822-M “coupled in parallel” and Wu’s Figure 9, which shows that each ECC engine 822-0 to 822-M includes an ECC corrector connected to error detectors 902-0 to 902-K arranged in parallel. Ex. 1004 ¶¶ 33, 34, Figs. 8, 9. Further support is provided by Wu’s disclosure that “error corrector 901 is shared by the error detectors 902-0 to

902-K and arranged to correct the error(s) of the data detected by the error detectors.” *Id.* ¶ 34. We credit Dr. Dolecek’s undisputed testimony that Wu’s “error detector modules 902 operate so as to detect errors in parallel.” Ex. 1003 ¶ 122.

5. *Claim 15*

Claim 15 is similar to claim 1 and is reproduced below:

15. A system comprising:

[15a] an encoder configured to encode data for storage on a flash memory;

[15b] the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

[15c] a decoder, communicatively coupled with the flash memory, and configured to: retrieve the encoded data from flash memory to generate a plurality of data streams; and

[15d] process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams,

[15e] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[15f] forward the portion of the respective received stream containing an error to an error correction module of the decoder; and

[15g] correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:21–44 (bracketed text added; paragraphs adjusted).

Petitioner provides a table correlating the limitations of claim 15 with the equivalent limitations of claim 1. Pet. 48–50. Based on the correlation table, Petitioner asserts that “only limitations 15[a] and 15[b] are not

equivalently recited in claim 1.” Pet. 48. For the remaining limitations, Petitioner contends that claim 15 is anticipated by Wu “for the same reason[s]” as presented for claim 1. Pet. 47–48.

Patent Owner presents no arguments for claim 15 separate from its arguments for claim 1. *See* PO Resp. 19 (asserting that Petitioner’s challenge fails “for the same reasons.”).

Petitioner shows persuasively that Wu discloses claim elements [15a] and [15b]. More particularly, Petitioner shows that Wu discloses “an encoder,” ECC engine/sub-ECC engines 822-0 to 822-M, “configured to encode data for storage on a flash memory,” comprised of flash memory devices 105-0 to 105-N, and “the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data.” Pet. 51 (citing Ex. 1003 ¶ 132).

Our finding is supported, for example, by Wu’s disclosure that sub-ECC engines 822-0 to 822-M perform “error correction code encoding . . . on the data to be stored in the memory devices.” Ex. 1004 ¶ 33, Fig. 8; *see also id.* ¶ 33 (referring to Figure 1 and the corresponding description for a detailed description of ECC engine/sub-ECC engines 822-0 to 822-M and memory devices 105-0 to 105-N in Figure 8); *id.* ¶ 22 (describing Figure 1, stating “error correcting module 102 . . . is arranged to perform error correction code encoding on the data to be stored into the memory devices.”). Our finding is further supported by Wu’s disclosure that “memory device 105-0 to 105-N may be a NAND or NOR type flash.” *Id.* ¶ 24 (describing Figure 1).

We find that Petitioner shows that Wu discloses the remaining limitations of claim 15 for the same reasons as discussed above for claim 1.

6. *Claim 17*

Claim 17 is similar to claim 1 and is reproduced below.

17. A method comprising:

[17a] receiving encoded data from a flash memory comprising a plurality of data streams;

[17b] processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams,

[17c] wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and

[17e] forward the portion of the respective received stream containing an error to an error correction module; and

[17f] correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

Ex. 1001, 12:49–63 (bracketed text added; paragraphs adjusted).

Petitioner provides a table correlating the limitations of claim 17 with the equivalent limitations of claim 1. Pet. 48–50. Petitioner asserts that claim 17 recasts claim 1 in method format and that claim 17 is anticipated by Wu “for the same reason[s]” as presented for claim 1. Pet. 47–48.

Patent Owner presents no arguments for claim 17 separate from its arguments for claim 1. *See* PO Resp. 19 (asserting that Petitioner’s challenge fails “for the same reasons.”).

We find that Petitioner shows that Wu discloses each and every limitation of claim 17 for the same reasons as discussed above for claim 1.

7. *Claim 19*

Claim 19 depends from claim 17 and recites the same limitation as claim 4. Petitioner relies on the same arguments and evidence for claim 19 as it presents for claims 1, 4, and 17. Pet. 52. Patent Owner presents no arguments for claim 19 separate from its arguments for claim 1. *See* PO Resp. 19 (asserting that Petitioner’s challenge to the dependent claims fails “for the same reasons.”). We find that Petitioner shows that Wu discloses limitations of claim 19 for the same reasons as discussed above for claims 1 and 4.

8. *Conclusion*

Petitioner has shown by a preponderance of the evidence that claims 1, 4, 8, 15, 17, and 19 are anticipated by Wu.

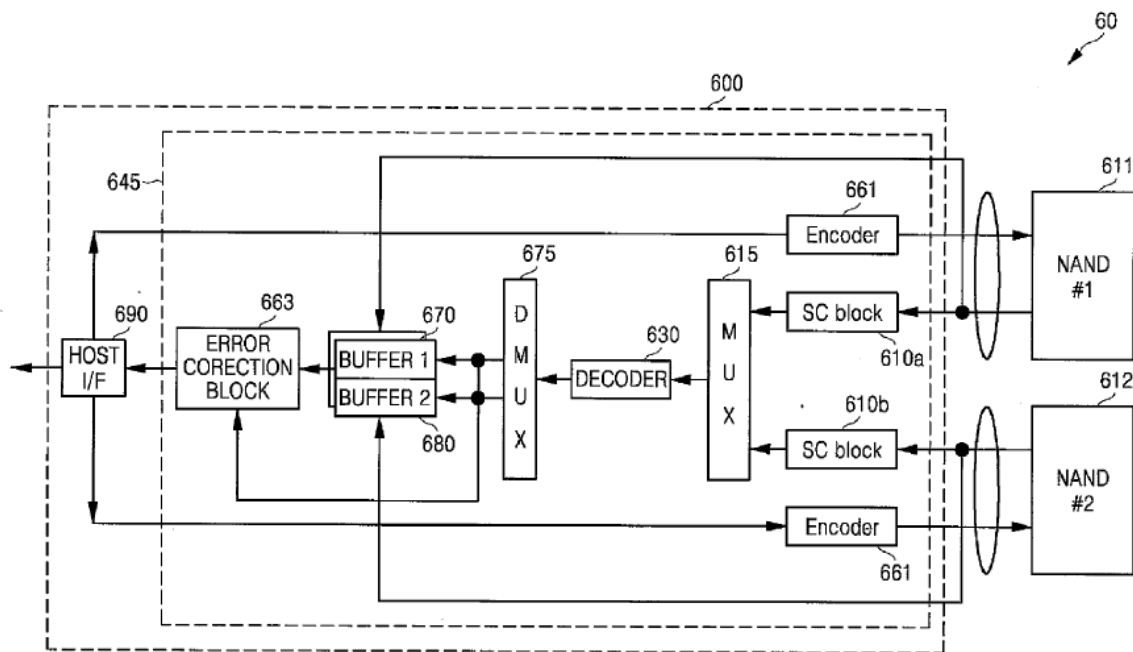
E. Petitioner’s Challenge based on Jo and Wu

Petitioner challenges claims 1, 2, 4, 8, 15, 17, and 19 as unpatentable and obvious based on Jo and Wu. Pet. 53–75. Patent Owner opposes. PO Resp. 20–44. We provide an overview of Jo before turning to our analysis, which focuses on particular disputed issues.

1. *Jo (Ex. 1005)*

Jo discloses a “multi-channel memory system including error correction decoder architecture.” Ex. 1005, code (54). Figure 6 is reproduced below.

FIG. 6



Jo's Figure 6 shows flash memory system 60 including flash memory controller 600 and ECC block 645, which communicates with NAND memory devices 611 and 612 over two communication channels operating in parallel. Ex. 1005 ¶¶ 21, 36, 38. ECC block 645 includes two data encoders 661, one each for communication channel, and two syndrome computation (SC) blocks 610a and 610b, one for each communication channel. *Id.* ¶ 37. SC blocks 610a and 610b each receive a set of data from a different sector of memory and detect whether or not the data set includes errors. *Id.* ¶¶ 39, 40.

ECC block 645 includes multiplexer 615, decoder block 630, demultiplexer 675, first and second memory buffers 670 and 680, third and fourth memory buffers (not labeled in Figure 6), and error correction block 663. Ex. 1005 ¶ 37. The two communication channels share the decoder block. *Id.* ¶ 41. According to Jo, "multiplexer 615 multiplexes between the first and second communication channels for locating errors that

occur in data sets received from the memory devices via the communication channels.” *Id.* ¶41. Jo further discloses that, “[o]nce the errors are identified in a data set, then the errors are corrected in error correction block 663 . . . and the decoded data set may then be sent to a host device.” *Id.*

2. Claims 1, 15, and 17—the Forward Limitation

Claims 1, 15, and 17 recite that “each error detection sub-module [is] configured to: [. . .] detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module.” Ex. 1001, 10:54–61 (claim 1, inserted text shown in brackets and omitted text replaced by ellipses); *id.* at 12:34–40 (claim 15, no text inserted or omitted); *id.* at 12:54–59 (claim 17, no text inserted or omitted). We refer to these limitations of claims 1, 15, and 17 as “the forward limitation.”

Petitioner contends that Jo discloses “each error detection sub-module configured to: . . . forward the portion of the respective received stream containing an error to an error correction module,” as recited in claim 1, and “the forwarded portion of the stream is received at buffers 670 and 680.” Pet. 64 (Petitioner’s annotation of Jo’s Figure 6 identifying SC blocks 610a and 610b and the nodes and channels leading to these blocks as the recited “error detection sub-module” (shaded green) and buffers 670 and 680 as part of the recited “error correction module” (shaded yellow)).

Patent Owner argues that Jo does not teach the forward limitation of claim 1 and that Petitioner’s challenges to claims 15 and 17 fail for the same reason. PO Resp. 41–44. According to Patent Owner, Jo “does not teach an error detection module in which each error detection sub-module ‘detect[s] whether a portion of the respective received stream contains an error’ and

then ‘forward[s] the portion of the respective received stream containing an error to an error correction module,’” as recited in claim 1. *Id.* at 41 (citing Ex. 1001, 10:58–61; emphasis added). In addition, Patent Owner argues there is no justification for including components outside Jo’s error detection/correction structures as part of the recited “error detection module.” PO Resp. 39.

We agree with Patent Owner that Petitioner does not show that Jo discloses the forward limitation of claims 1, 15, and 17. In our view, claim 1 requires that each error detection sub-module perform an ordered set of three steps: (1) receive a data stream; (2) detect whether a portion of the received stream contains an error; and (3) forward the portion of the received stream containing an error to an error correction module. Ex. 1001, 10:54–61. Claims 15 and 17 similarly require that steps (2) and (3) be performed in that order. *Id.* at 12:34–44 (claim 15); *id.* at 12:50–59 (claim 17). Patent Owner relies on this claim interpretation (PO Resp. 41–44; PO Sur-reply 18–19), and Petitioner does not show it is incorrect. *See* Pet. Reply 13 (asserting that Patent Owner’s argument “is based on the faulty premises that the claim requires forwarding only after error detection”). Petitioner argues, “Claim 1 does not require that errors be detected before data is forwarded” (*id.* at 14), but provides no support for that claim interpretation. Petitioner asserts that the “forward” step could happen “before . . . or simultaneously” with the “detect” step, but concedes that it has not cited any intrinsic evidence to support that reading of the claim. Tr. 25:7–14.

Patent Owner’s claim interpretation (which we adopt) is supported by the Specification of the ’700 Patent, which discloses, “Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and *then* forward the portion of the respective received

stream containing an error to the error correction module.” Ex. 1001, 3:57–60 (emphasis added). Patent Owner’s claim interpretation is further supported by Figure 3 of the ’700 Patent (reproduced above), which shows data flowing first to error detection sub-modules 315 and then to error correction submodules 320. *Id.* at 6:61–67 (describing Figure 3). Still further support is provided by the flow chart in Figure 6, which demonstrates that the error detection step and forwarding step occur in that sequence. *Id.* at 9:15–21 (blocks 635, 640).

For the first time at the hearing, Petitioner cited claim 13 as support for its claim interpretation. Tr. 25:12–24, 57:23–58:6. We agree with Patent Owner, however, that claim 13 demonstrates that the error detection step must be performed before the forwarding step in claim 1. Tr. 42:23–43:14; 62:13–16. Claim 13 depends from claim 1 and recites, “wherein each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module.” Ex. 1001, 12:12–15. Claim 13 recites an additional function that must be performed by the error detection sub-module. According to claim 1, the error detection sub-module forwards error-containing portions of the data stream to an error correction module, and according to claim 13, the error detection sub-module also directs error-free portions of the data stream to bypass the error correction module. Both of these functions require that the error detection sub-module first perform error detection. Patent Owner argues persuasively that it would be impossible to direct error-free portions to bypass the error correction module, if error detection had not already occurred. Tr. 43:3–14.

Petitioner asserts, “So maybe in Claim 13 the error detection does have to occur before forwarding, but in Claim 1, then you know from claim

differentiation that that's not required. You don't have to do error detection first." Tr. 58:1–4. We disagree. Claim 13 recites an additional function without modifying the order of the steps recited in claim 1. Claim differentiation does not apply because Patent Owner's interpretation does not involve reading a limitation from the dependent claim into the independent claim. *See Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) (explaining that "'claim differentiation' refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim").

Petitioner presents no argument in support of its Jo-led challenges that does not rely on its incorrect interpretation of the forward limitation of claims 1, 15, and 17. *See* Pet. Reply 13–15 (arguing, "Claim 1 does not require that errors be detected before data is forwarded . . ."). Petitioner asserts that the "forward" step is performed at "the branching dots" in Jo's Figure 6. *Id.* The parties agree that, at these dots, the data path branches in two directions: (1) to SC blocks 610a, b, which detect errors, and (2) to data buffers 670, 680, where the data is operated on by error correction block 663. Ex. 1007 ¶¶ 39–43, Fig. 6; PO Resp. 38–39; Pet. Reply 13–14. At best, Petitioner shows that data is forwarded at Jo's branching dots to an error correction module (Pet. 62–64; Pet. Reply 14–15), but Petitioner fails to show that any error detection occurs before the data is forwarded.

Furthermore, Petitioner does not show that Jo discloses the forward limitation, even if the claims were construed to encompass *simultaneous* performance of the "detect" and "forward" steps. *See* Tr. 62:7–13 (Patent Owner: "So simultaneity is not going to save them in this instance . . ."). Petitioner does not show that any error detection occurs simultaneous with data being forwarded from the branching dots to an error correction module.

Jo's Figure 6 demonstrates that the branching dots (where Petitioner alleges the "forward" step occurs) *precede* the SC blocks (where Petitioner asserts the "detect" step occurs) in the data path. Ex. 1005, Fig. 6; Pet. 62 (relying on the function of Jo's syndrome computation (SC) blocks as disclosing the "detect" step, quoting Ex. 1005 ¶ 40). Our understanding of Jo's Figure 6 is supported by Dr. Bagherzadeh's unrebutted testimony: "The data branches to the buffer elements *before* entering the controller and the error detecting of the SC Block." Ex. 2023 ¶ 136 (emphasis added; cited at PO Resp. 41–42).

Still further, Petitioner does not show persuasively that Jo discloses the forward limitation even under Petitioner's claim interpretation. Petitioner's contention for the forward limitation presumes that the "error detection sub-module," as claimed, includes not only SC blocks 610a and 610b in Jo's Figure 6, but also the "branching dots." Pet. 64; Pet. Reply 12–13. Petitioner presents no persuasive evidence that a POSITA would have considered the branching dots to be part of an "error detection sub-module," as recited in the claims. *See* PO Resp. 37–41; PO Sur-reply 18–20. Tellingly, when addressing the portion of claim element [1c] that recites "each error detection sub-module configured to: . . . detect whether a portion of the respective received stream contains an error," Petitioner and Dr. Dolecek identify syndrome computation blocks 610a and 610b, but *not* the branching dots. Pet. 62; Ex. 1003 ¶¶ 165–167; *see also* Ex. 1003 ¶ 164 (identifying "blocks 610a and 610b" in Jo's Figure 6 as "the error detection sub-modules").

Although Petitioner asserts that "[t]he black dots clearly are functionally integral with the rest of the controller 600 and ECC 645" (Pet. Reply 12), that assertion is mere attorney argument, with no support in the

expert testimony. Petitioner's unsupported assertion does not justify including the branching dots as part of an "error detection sub-module." The experts agree that the branching dots play no role in error detection.

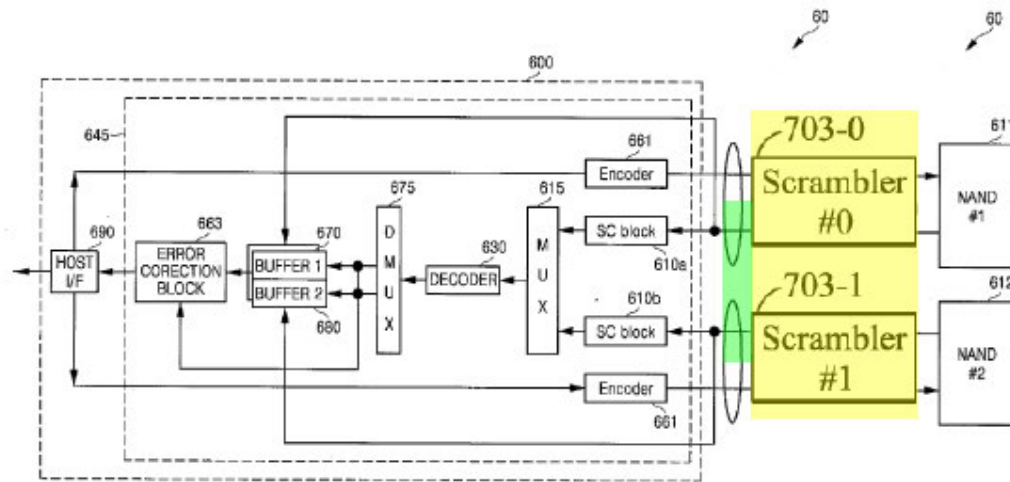
Dr. Dolecek concedes that the branching dot "does not perform [error] detection" and "the only thing it's doing is sending a copy of the data into the buffers." Ex. 2024, 70:8–24; *see also id.* at 71:20–23 ("[T]he dot indicates that the copy of the data is being sent into the buffers and that the same copy is being sent into the SC blocks."). Dr. Bagherzadeh explains the function of the branching dots and testifies that "a POSITA would not consider the communication channel and this branch located off the controller to be part of the 'error detection module' of claim 1." Ex. 2023 ¶¶ 60, 130–133. Accordingly, we are not persuaded by Petitioner's assertion that each of the branching dots are, respectively, part of an "error detection sub-module," as recited in the claims.

Petitioner's failure to show that Jo discloses the forward limitation is by itself a sufficient basis for our determination that Petitioner's Jo-led challenges do not succeed. Nevertheless, for completeness' sake, we also address Petitioner's rationale for combining Jo with Wu or Wan.

3. Rationale for Combining Jo and Wu

Petitioner acknowledges that Jo does not disclose a decoding module that partially decodes data before it is received by an error detection module. Pet. 56. For this aspect of claim element [1a], Petitioner combines Jo's Figure 6 with scramblers 703-0 and 703-1 from Wu's Figure 7. Pet. 56–59. Petitioner illustrates this combination with the following annotated figure:

FIG. 6



Pet. 59. Petitioner’s annotated figure shows a flash memory system of Jo’s Figure 6, which Petitioner modifies to include a scrambler in each of the memory channels. *Id.* Relying on teachings from Wu and Wan, Petitioner asserts that its proposed modification would provide several benefits, including reduced interference and improved reliability. Pet. 57–58.⁹ Petitioner contends that claims 15 and 17 recite limitations that are equivalent to claim element [1a] and relies on the same contentions for these limitations as it presents for claim element [1a]. Pet. 48–49, 73.

Patent Owner argues that a POSITA would not have combined Jo and Wu in the manner Petitioner proposes, with multiple scramblers, one for each memory device. PO Resp. 21–27, 31.

⁹ Petitioner also asserts that, “if located on Jo’s memory devices, [Wu’s scramblers] may promote portability of the memory die so that they can be used with different controllers.” Pet. 58 (citing Ex. 1006 ¶ 70). This asserted benefit does not support Petitioner’s proposed combination of Jo and Wu with scramblers located in the memory channels between the controller and NAND memory devices, as illustrated in Petitioner’s modification of Jo Figure 6 above.

We determine that Petitioner does not meet its burden to show a non-hindsight biased rationale for combining Jo and Wu in the manner it proposes. More particularly, Petitioner does not show a sufficient reason for modifying Jo's flash memory system to include multiple scramblers, with a scrambler in each memory channel. Petitioner's first two asserted benefits—reduced interference and improved reliability (Pet. 58)—are not dependent on the number of scramblers or where they are located in the data path. As Dr. Bagherzadeh testifies, “These are benefits that do not depend on having a Scrambler for each memory channel.” Ex. 2023 ¶ 125. Dr. Bagherzadeh's testimony is supported by Wu, which discloses that a scrambler reduces interference and “may be located anywhere in the data transferring paths (e.g. write or read paths).” Ex. 1004 ¶ 23.

Petitioner's third and fourth asserted benefits—helping to avoid header and ECC type data pattern failures and promoting portability of the memory die (Pet. 58)—are based on Wan's description of its Figure 8a, in which “scrambler/descrambler 812 is on the memory die 808 rather than in a controller 802 of the memory device 800.” Ex. 1006 ¶ 70, Fig. 8a. Petitioner does not explain how Wan would have led a POSITA to locate scramblers in each memory channel, rather than on the memory die, as taught by Wan's Figure 8a embodiment. *Id.* Petitioner's contention is credibly rebutted by Dr. Bagherzadeh's testimony that “Wan's teachings, specific to Wan, relate to location of a Scrambler on the flash memory chip itself, and do not tell a POSITA where a Wu-style Scrambler should be located or what advantages/disadvantages it would have in a location between the flash memory and the SC block of Jo, like Dr. Dolecek's combination contemplates.” Ex. 2023 ¶ 126.

Petitioner also does not persuade us that modifying Jo's Figure 6 embodiment to include a separate scrambler for each memory channel would have been consistent with Jo's teaching that "a more efficient utilization of area and circuitry in a memory controller" can be achieved by providing circuitry that is shared by multiple communication channels. Ex. 1005 ¶¶ 10, 28, 33, 41. In most of Wu's embodiments, a scrambler is shared by multiple memory channels. Ex. 1004, Figs. 1, 2, 6, 8. In view of these teachings, Petitioner's modification of Jo's flash memory device to include a separate scrambler in each memory channel deviates from the prior art, lacks a sufficient rational basis, and suffers from hindsight bias.

Petitioner argues that its proposed combination "provides more robust error detection and correction, because locating Wu's scramblers between Jo's NAND devices 611 and 612 and Jo's SC blocks 610 provides the unique benefit of reducing interference-based errors in not only the retrieved data, but also the data's associated ECC encoding data (e.g., parity bits)." Pet. Reply 15–16 (citing Ex. 1003 ¶¶ 156, 220; Ex. 1006 ¶ 70); *see also* Pet. Reply 19, 25 (similar argument, including for Jo plus Wan combination). We are not persuaded. Petitioner's argument addresses the location of the scramblers relative to the flash memory and error detectors, but does not address the number of scramblers per channel. As stated above, in most of Wu's embodiments, a scrambler is shared by multiple memory channels. Ex. 1004, Figs. 1, 2, 6, 8. Although Petitioner and Dr. Dolecek rely on Wan (Exhibit 1006), Wan teaches locating a scrambler/descrambler on a memory die, not between the memory device and the error detection module, as Petitioner proposes for its combination of Jo and Wu. Ex. 1003 ¶¶ 156, 220 (discussing Wan); Ex. 1006 ¶ 70, Fig. 8a.

Next, Petitioner argues that it “only has the burden to show that the proposed combination is desirable—not that it is the most desirable option.” Pet. Reply 17 (citing *Intel Corp. v. Qualcomm Inc.*, 2022 WL 880681, at *4 (Fed. Cir. Mar. 24, 2022)). In our view, however, Petitioner has not met its burden to show that it would have been desirable to modify Jo’s flash memory system to include multiple scramblers, with a scrambler in each memory channel. Petitioner’s evidence is not persuasive to show that multiple scramblers is a desirable option.

Next, Petitioner argues that its proposed combination of Jo and Wu “gains efficiency, because the combination would reduce the demands on Jo’s error correction circuitry.” Pet. Reply 17 (citing Ex. 2024, 111:25–112:14). In the cited excerpt, Dr. Dolecek testifies, “So while we are adding circuitry, what we are gaining is the avoidance of even bigger circuitry from the perspective of a more complex ECC engine.” Ex. 2024, 111:25–112:14. Although Dr. Dolecek pointed to Wan paragraph 49 as support for her opinion (Ex. 2024, 112:15–114:5), Wan says nothing about whether the addition of scramblers would reduce the size or complexity of the ECC engine. On this topic, we find Dr. Bagherzadeh’s testimony is well-reasoned and persuasive.

A POSITA reading Wan, including paragraph 49, would understand that Wan is simply noting the case for scrambling as a general proposition—to reduce interference-related program disturb caused by large blocks of adjacent identical cell values. But Wan does not teach that scrambling will allow for the use of smaller ECC circuitry nor that the result will be reduced area of circuitry overall. And a POSITA would not generally believe that adding scrambler circuitry necessarily reduces ECC circuitry or would reduce ECC circuitry so much so that the overall area and complexity of the circuitry would be reduced. Randomization operates independently of error detection and

correction. Scrambler functionality is not going to significantly change the underlying ECC circuitry required to do the error detection and correction. And whatever benefits it does bring to the reliability of the overall flash memory system, the addition of a Scrambler would not be expected to reduce the overall circuitry of the system.

Ex. 2023 ¶ 166. In any event, neither Petitioner’s argument (Pet. Reply 17) nor Dr. Dolecek’s testimony (Ex. 2024, 111:25–112:14) provides a reason for using multiple scramblers, one in each memory channel.

Next, Petitioner tries to circumvent Jo’s teaching about sharing error correction circuitry among multiple communication channels (Ex. 1005 ¶¶ 10, 28, 33, 41) by arguing that “Wu’s scrambling circuitry is . . . more analogous to Jo’s encoders 661 and SC blocks 610a/b, which are not shared by memory devices.” Pet. Reply 18; *see also id.* at 25 (repeating this argument for Jo plus Wan combination). We are not persuaded by Petitioner’s reasoning, which is based on the unsupported assumption that Jo’s error correctors—the shared circuitry—operates only on data that contains errors, not error-free data. *Id.* (arguing that “error corrector circuitry . . . may not be required for error-free data”). We agree with Patent Owner that, in Jo, “*all data* (error-containing and error-free) passes through the shared ECC circuitry” and Jo’s Figures 6 and 7 show no bypass capability for error-free data. PO Sur-reply 11; Ex. 1005 ¶¶ 42–50; Figs. 6, 7. Furthermore, Petitioner’s argument overlooks Wu’s teaching that scrambling circuitry may be shared by multiple memory channels. Ex. 1004, Figs. 1, 2, 6, 8.

Referring to Wu’s Figure 7, Petitioner asserts that the “use of sub-scramblers 703-1 to 703-N, one per channel, also reduces circuit size according to Wu.” Pet. Reply 19 (citing Ex. 1004 ¶ 26). Petitioner quotes

Wu's statement that "the cost and chip area required by the ECC engines may be greatly reduced." *Id.* This statement has nothing to do with using scramblers to reduce circuit size, as asserted by Petitioner. Pet. Reply 19. Instead, Wu teaches that a reduction in cost and chip area results from sharing an ECC engine among multiple storage channels, such that "an amount of ECC engines is less than an amount of the storage channels." Ex. 1004 ¶ 26. Sharing circuitry among multiple channels, as taught by Wu and Jo, is the opposite of what Petitioner proposes. Instead of allowing multiple memory channels to share a scrambler, Petitioner proposes to modify Jo to include a separate scrambler in each memory channel. Pet. 59. As discussed above, Petitioner's proposal is not consistent with Jo's teaching that "a more efficient utilization of area and circuitry in a memory controller" can be achieved by providing circuitry that is shared by multiple communication channels. Ex. 1005 ¶¶ 10, 28, 33, 41. Although Petitioner argues that "[t]his embodiment "eliminates otherwise required multiplexing and demultiplexing circuitry," that argument is plainly inconsistent with Wu's Figure 7, which shows multiple memory access module 104, which includes multiplexing unit 301. Ex. 1004 ¶¶ 27, 32, Figs. 3, 7.

Lastly, Petitioner asserts that scramblers are beneficial for "all manner of devices," including "sophisticated multi-level cell NAND memory," "smaller, low-cost memory devices like thumb drives," and "low-cost devices such as cell phones." Pet. Reply 20–21 (citing Ex. 1004 ¶¶ 22, 23; Ex. 1005 ¶¶ 8, 9; Ex. 1006 ¶ 49, Figs. 5a, 5b). Even assuming Petitioner's assertion is true, it does not address the deficiency in Petitioner's evidence concerning the manner in which Jo and Wu would have been combined. Petitioner does not show a sufficient reason for modifying Jo's flash

memory system to include multiple scramblers, with a scrambler in each memory channel.

4. Claims 2, 4, 8, and 19

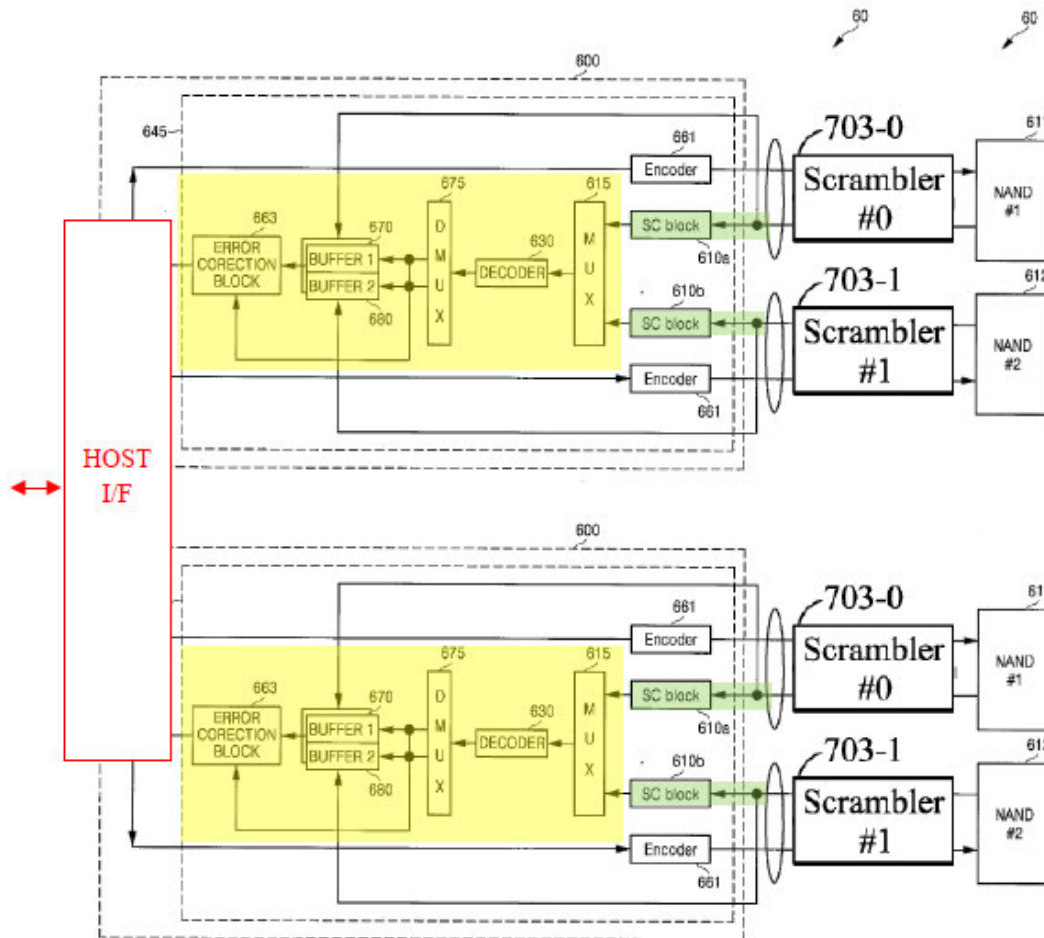
Petitioner's arguments and evidence for dependent claims 2, 4, 8, and 19 (Pet. 66–73, 75) do not remedy the deficiencies in Petitioner's challenge for independent claims 1 and 17, as discussed above (*see* Sections II.E.2 and II.E.3, *supra*), and Petitioner fails to show obviousness of the dependent claims for the same reasons.

5. Additional Reasoning for Claims 4, 8, and 19

Claim 4 depends from claim 1 and recites “wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.” Ex. 1001, 11:7–10. Claim 8 depends from claim 4. *Id.* at 11:37–41. Claim 19 depends from claim 17 and recites the same limitation as claim 4. *Id.* at 13:1–4.

Petitioner contends that a POSITA would have understood Jo as disclosing that its two-channel embodiments can be scaled to 2N channel embodiments, for example, by combining two-channel embodiments, and that “such replication would have been obvious to try” to provide larger memory capacity. Pet. 68, 71 (citing Ex. 1003 ¶¶ 187–191; Ex. 1005 ¶¶ 6, 9, 41). Petitioner contends that the following modification of Jo's Figure 6 is “disclosed and obvious.”

FIG. 6



Pet. 69–70; Ex. 1003 ¶ 189 (same figure in Dr. Dolecek’s testimony).
 Petitioner’s modification of Jo’s Figure 6 shows a flash memory system, which Petitioner modifies to include scramblers from Wu’s Figure 7 and reproduces twice to depict a four-channel memory device with an expanded host interface. Pet. 70. Petitioner’s modification includes four NAND memory devices, four encoders 661, and two error correction blocks 663.
Id.

Patent Owner argues that, consistent with Jo’s teachings, a POSITA interested in increasing the number of memory devices and channels would not have doubled the entire flash memory controller, as proposed by Petitioner, but instead would have added additional data buffers and

channels to the controller, while maintaining a single error corrector. PO Resp. 27–29; Ex. 2023 ¶¶ 144, 145.

We agree with Patent Owner. Petitioner does not show that Jo discloses “a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules,” as recited in claims 4 and 19, or that this feature would have been obvious. Petitioner does not point to any express disclosure in Jo of multiple error correction sub-modules that are fewer in number than the error detection sub-modules. Nor does Petitioner persuade us that a POSITA would have understood Jo as disclosing this feature or that it would have been obvious.

Petitioner contends that it would have been obvious to add more flash memory devices by replicating Figure 6 and doubling not only the number of memory devices but also the number of error correction blocks. Pet. 68–71. Petitioner does not explain why, when replicating Jo’s Figure 6, Petitioner expanded the host interface to communicate with four memory devices, but did not similarly expand the error corrector. Petitioner’s proposed modification is contrary to Jo’s teaching that “a more efficient utilization of area and circuitry in a memory controller” can be achieved by providing error correction circuitry that is shared by multiple communication channels. Ex. 1005 ¶¶ 10, 28, 33, 41. It is also contrary to Jo’s teaching that “an error corrector [is] adapted to correct errors detected by each of the *at least* first and second error detectors,” corresponding to at least first and second communication channels. *Id.* ¶ 12 (emphasis added).

Dr. Bagherzadeh testifies persuasively that “Dr. Dolecek’s modified Figure 6” as reproduced above, “unnecessarily adds a second error correction block in contradiction to the efficiency teachings of Jo.” Ex. 2023 ¶ 144. Instead of following Jo’s teaching that there can be “at least

two” memory devices and “at least” two error detectors per error corrector (Ex. 1005 ¶ 12), Petitioner and Dr. Dolecek duplicate the entire memory controller, doubling not only the number of memory devices and error detectors, but also the number of error correctors. Pet. 69–70; Ex. 1003 ¶ 189. Petitioner’s modification runs counter to Jo’s teachings about “efficient utilization of area and circuitry,” sharing error correction circuitry among multiple communication channels, and providing error correction circuitry that communicates with “at least” two memory devices. Ex. 1005 ¶¶ 10, 12, 14, 28, 33, 41, claim 1.

Petitioner argues that “the Petition’s design reduces circuitry over the prior art in essentially the same proportion as in Jo’s two-memory-device embodiments (e.g., Ex. 1005, Fig. 6) by maintaining a ratio of two error detection sub-modules per error correction module/sub-module.” Pet. Reply 21. Petitioner’s argument is not consistent with Jo, which teaches coupling not just two, but “at least” two, error detectors per error corrector. Ex. 1005 ¶ 12. In addition, Petitioner argues that “increasing the number of SC blocks beyond two without also adding error correction circuitry would create a bottleneck” that “would degrade performance and increase controller latency.” Pet. Reply 22–23 (citing Ex. 1005 ¶¶ 41, 45–50, Figs. 6, 7. Once again, Petitioner’s argument lacks supporting expert testimony. Patent Owner argues persuasively that “Petitioner’s conjecture ignores Jo’s teachings about the benefits of the pipelining functionality built into its error correction block, . . . which allows for shared error location and correction functions to be performed in parallel to improve latency.” PO Sur-reply 17 (citing Ex. 1005 ¶¶ 47–49, Fig. 7).

Judging between the parties’ competing proposals for modifying Jo to increase the number of memory devices and channels, we find that Patent

Owner's position more closely aligns with Jo's disclosure. PO Resp. 27–29; Ex. 2023 ¶¶ 144, 145. Jo repeatedly describes “at least” two memory devices, “at least” two communication channels, and “at least” two error detectors, but describes only a single corresponding error corrector. Ex. 1007 ¶¶ 12, 14, 15, 28, 37, 41, claim 1, Figs. 3, 6. Moreover, Petitioner bears the burden of proof, and Petitioner does not persuade us that its proposed modification is consistent with Jo's teachings.

6. Conclusion

Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 4, 8, 15, 17, and 19 are unpatentable based on Jo and Wu.

F. Petitioner's Challenge based on Jo and Wan

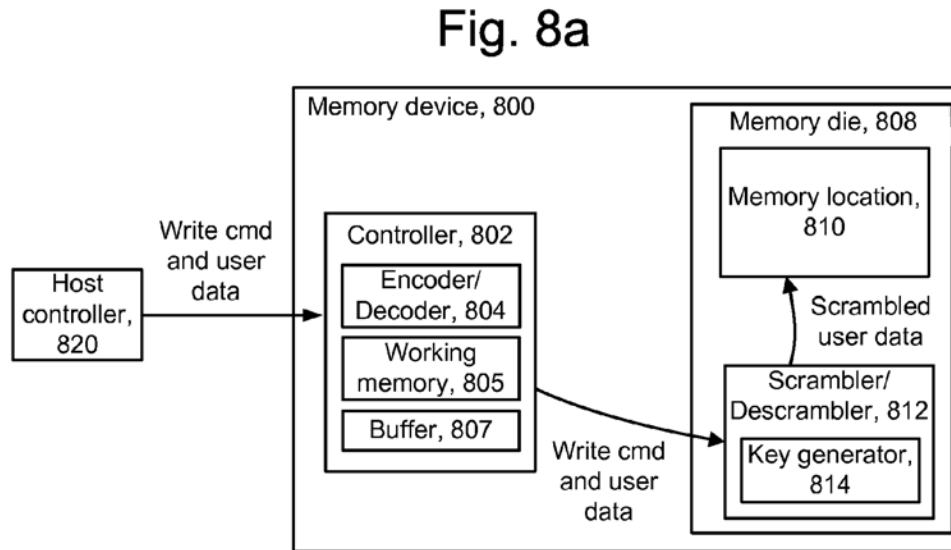
Petitioner challenges claims 1, 2, 4, 8, 15, 17, and 19 as unpatentable and obvious based on Jo and Wan. Pet. 76–89. Patent Owner opposes. PO Resp. 45–55. We provide an overview of Wan before turning to our analysis, which focuses on particular disputed issues.

1. Wan (Ex. 1006)

Wan discloses a method for scrambling and descrambling user data in a non-volatile storage system. Ex. 1006 ¶ 12. Wan teaches that “[d]ata scrambling for non-volatile memory such as NAND memories has become increasingly important in addressing system reliability issues that are inherently susceptible by design to worst-case data patterns which trigger memory program failures.” *Id.* ¶ 49. Wan discloses that “one approach involves performing scrambling and descrambling of data at an off-chip controller circuit, where non-user data is stored on-chip, and user data which is encoded using the non-user data is also stored on-chip.” *Id.* ¶ 50.

According to Wan, a “chip refers to a memory die on which a memory array is formed.” *Id.*

Figure 8a of Wan is reproduced below.



Wan’s Figure 8a depicts scrambling performed by on-chip circuitry using a key generator in a storage system. Ex. 1006 ¶ 28. Wan teaches that, “[i]n this approach, a scrambler/descrambler 812 is on the memory die 808 rather than in a controller 802 of the memory device 800.” *Id.* ¶ 70. Wan describes the Figure 8a embodiment as follows: “The controller 802 may process the user data such as by performing ECC coding and adding overhead data at an encoder/decoder 804. With this approach, the overhead data is also scrambled with the user data. This helps avoid header and ECC type data pattern failures.” *Id.*

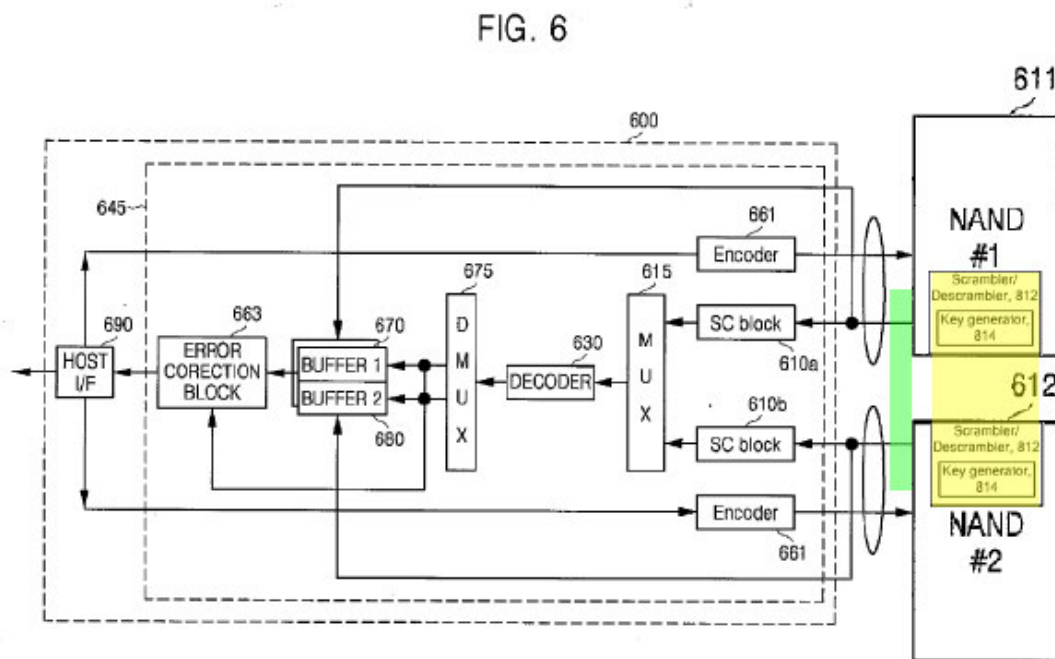
2. Claims 1, 15, and 17—the Forward Limitation

When addressing the forward limitation, the parties rely on the same arguments and evidence for Petitioner’s challenge based on Jo and Wan as they present for Petitioner’s challenge based on Jo and Wu. Pet. 62–64,

85–86; PO Resp. 54–55. For the reasons discussed in Section II.E.2 above, Petitioner does not show that Jo discloses the forward limitation of claims 1, 15, and 17. This deficiency is by itself a sufficient basis for our determination that Petitioner’s challenge based on Jo and Wan does not succeed.

3. *Petitioner’s Combination of Jo and Wan*

Petitioner acknowledges that Jo does not expressly disclose a decoding module that partially decodes data before it is received by an error detection module. Pet. 77. For this aspect of claim element [1a], Petitioner combines Jo’s Figure 6 with scrambler/descrambler 812 and key generator 814 of Wan’s Figure 8a. Pet. 77–85. Petitioner illustrates this combination as follows:



Pet. 85; Ex. 1003 ¶ 229 (same figure in Dr. Dolecek’s testimony).

Petitioner’s modification of Jo’s Figure 6 shows a flash memory system, which Petitioner modifies to include a scrambler in each of Jo’s NAND

memory devices 611 and 612. Relying on teachings from Wan, Petitioner asserts that its proposed modification would improve device reliability and allow memory die portability. Pet. 82–83. Petitioner also relies on the rationale discussed above for Petitioner’s combination of Jo and Wu. Pet. 82. Petitioner contends that claims 15 and 17 recite limitations that are equivalent to claim element [1a] and relies on the same contentions for these limitations as it presents for claim element [1a]. Pet. 48–49, 86–87.

Patent Owner argues that Petitioner’s combination of Jo and Wan would not result in the subject matter of the claims because, in Petitioner’s combination, the scrambler is located in the flash memory, not as part of the decoder. PO Resp. 51–54. In addition, Patent Owner argues that placing a scrambler on every memory device, as proposed by Petitioner, would be contrary to Jo’s aim of efficient use of area and circuitry and would not increase portability of the memory. *Id.* at 45–51.

a) Rationale for Combining Jo and Wan

Petitioner does not meet its burden to show a non-hindsight biased rationale for combining Jo and Wan in the manner it proposes. Neither of Petitioner’s rationales is sufficient to support modifying Jo by adding a scrambler to each memory device.

Petitioner’s first reason—improved device reliability—is not enough to support placing scramblers on the memory devices, as opposed to on the memory controller. Wan teaches both alternatives. According to Wan, scrambling and descrambling can be performed either by off-chip controller circuitry or by on-chip circuitry. Ex. 1006 ¶¶ 22, 23, 28, 29, Figs. 5a, 5b, 8a, 8b. Petitioner does not explain how locating a scrambler/descrambler in each memory chip would have been consistent with Jo’s teaching that “a

more efficient utilization of area and circuitry in a memory controller” can be achieved by providing circuitry that is shared by multiple communication channels. Ex. 1005 ¶¶ 10, 28, 33, 41. Dr. Bagherzadeh testifies persuasively that placing scramblers on the memory dies “does not allow for the flexibility . . . in placing fewer scramblers in more downstream locations.” Ex. 2023 ¶ 160. To the extent Petitioner’s Reply relies on the same arguments for the Jo and Wan combination as it presents for the Jo and Wu combination (Pet. Reply 24–25), we have addressed these arguments in Section II.E.3 above.

Turning to Petitioner’s second reason, Petitioner also does not show persuasively that its proposed modification of Jo would allow memory die portability. Petitioner relies on Wan’s teaching that the on-chip scrambling approach “provides portability of the memory die so that it can be used with different controllers, for instance, which are made by different manufacturers.” Pet. 83; Ex. 1006 ¶ 70. Petitioner does not explain why memory die portability would favor locating a scrambler on the memory device, as opposed to on the memory controller or elsewhere. Dr. Dolecek relies on memory die portability as a motivation for combining Jo and Wan (Ex. 1003 ¶¶ 217, 226), but not as a reason for choosing one scrambler location over another. Dr. Bagherzadeh provides unrebutted testimony that “a POSITA would recognize that the combination of Jo and Wan proposed by Dr. Dolecek would act to restrict portability and lock a user into a choice of controller technology that could support the specific division of the ECC system’s components.” Ex. 2023 ¶ 161. Dr. Bagherzadeh explains his reasoning as follows: “By putting the scrambler component outside the controller, and on the memory chip, Dr. Dolecek’s combination of Wan and Jo would require a controller that could account for this scrambling

functionality, limiting the ability to use the memory chips of the combination with some controllers.” *Id.* ¶ 162. We find that Dr. Bagherzadeh’s testimony provides a credible rebuttal to Petitioner’s evidence (Wan’s paragraph 70), and Petitioner provides no persuasive argument in reply. The weight of the evidence does not favor Petitioner on this issue.

b) Whether Petitioner’s Jo-Wan Combination Satisfies the Claims

The Petition does not show persuasively that incorporating Wan’s on-die scrambler/descrambler circuitry into Jo’s NAND flash memory chips 611 and 612, as proposed (Pet. 84–85), would result in the subject matter of claims 1, 15, and 17. Petitioner does not persuade us that scramblers located on Jo’s NAND memory devices would be part of a decoder, rather than part of the flash memory.

For both of its Jo-led challenges, the Petition maps a “decoder” (claim 1 preamble) to Jo’s ECC block 645. Pet. 54–55 (addressing Jo-Wu combination and providing color-coded version of Jo’s Figure 6); Pet. 76 (addressing Jo-Wan combination by cross-referencing prior Jo-Wu argument). For its Jo and Wan combination, the Petition maps a “decoding module” (claim element [1a]) to scramblers located on Jo’s NAND memory devices 611 and 612, which Petitioner identifies as a “flash memory.” Pet. 85, 88 (Petitioner’s modification of Jo’s Figure 6). Petitioner’s claim mapping does not satisfy claim 1, which recites, “A flash memory decoder comprising: a decoding module” Ex. 1001, 10:47–48. Although claims 15 and 17 do not recite a “decoding module,” Petitioner contends that claims 15 and 17 recite limitations that are equivalent to claim element [1a] and

relies on the same contentions for these limitations as it presents for claim element [1a]. Pet. 48–49, 86–87.

Petitioner argues for the first time in the Reply that the preamble of claim 1 is not limiting, that the Petition’s mapping for claim 15 does not rely on Wan’s scramblers for a “decoder,” and that the claim elements, “flash memory” and “decoder,” may be disclosed by a shared structure. Pet. Reply 10, 26–27. These arguments exceed the proper scope of a reply brief under 37 C.F.R. § 42.23(b) and need not be considered. In any event, Petitioner’s reply arguments do not cure the inconsistencies in the Petition, which maps a “decoder” to Jo’s ECC block 645, a “flash memory” to Jo’s NAND memory devices 611 and 612, and a “decoding module” to scramblers located on the flash memory. Pet. 54–55, 85, 88. At a minimum, these inconsistencies and Petitioner’s change of position in the reply brief undermine the persuasiveness of Petitioner’s challenge based on Jo and Wan.

4. Claims 2, 4, 8, and 19

Petitioner’s arguments and evidence for dependent claims 2, 4, 8, and 19 (Pet. 86, 89) do not remedy the deficiencies in Petitioner’s challenges for independent claims 1 and 17, as discussed above (*see* Sections III.F.2 and II.F.3, *supra*), and Petitioner fails to show obviousness of the dependent claims for the same reasons.

5. Additional Reasoning for Claims 4, 8, and 19

For claims 4, 8, and 19, Petitioner relies on the same arguments and evidence for its Jo and Wan combination as it presents for its Jo and Wu combination. Pet. 86, 89; Pet. Reply 27. Petitioner’s showing is deficient for the same reasons as discussed in Section II.E.5 above.

6. *Conclusion*

Petitioner has not shown by a preponderance of the evidence that claims 1, 2, 4, 8, 15, 17, and 19 are unpatentable based on Jo and Wan.

III. CONCLUSION¹⁰

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 4, 8, 15, 17, 19	102(e)	Wu	1, 4, 8, 15, 17, 19	
1, 2, 4, 8, 15, 17, 19	103(a)	Jo, Wu		1, 2, 4, 8, 15, 17, 19
1, 2, 4, 8, 15, 17, 19	103(a)	Jo, Wan		1, 2, 4, 8, 15, 17, 19
Overall Outcome			1, 4, 8, 15, 17, 19	2

¹⁰ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown that claims 1, 4, 8, 15, 17, and 19 of the '700 Patent are unpatentable;

FURTHER ORDERED that Petitioner has not shown that claim 2 of the '700 Patent is unpatentable; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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