

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANKER INNOVATIONS LTD.,
Petitioner

v.

MYPAQ HOLDINGS LTD.,
Patent Owner

Case IPR2022-01131
Patent 7,675,759

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,675,759

TABLE OF CONTENTS

I.	MANDATORY NOTICES.....	1
II.	STANDING AND FEES	2
III.	OVERVIEW OF THE '759 PATENT.....	2
	A. Subject Matter	2
	B. Prosecution History	4
IV.	SUMMARY OF PRIOR ART	4
V.	SUMMARY OF GROUNDS	9
VI.	LEVEL OF ORDINARY SKILL	9
VII.	CLAIM CONSTRUCTION.....	9
VIII.	INSTITUTION IS PROPER.....	10
	A. Institution is Proper Under 35 U.S.C. § 314(a).....	10
	B. Discretionary denial under General Plastic is not appropriate	12
	C. Institution is Proper Under 35 U.S.C. § 325(d).....	13
IX.	GROUND 1A: <i>Hirst</i> Anticipates Claims 1-3, 5-13, and 15-20	13
	A. Claim 1	13
	B. Claim 2	22
	C. Claim 3	23
	D. Claim 5	24

E.	Claim 6	25
F.	Claim 7	26
G.	Claim 8	29
H.	Claim 9	30
I.	Claim 10	31
J.	Claim 11	31
K.	Claim 12	31
L.	Claim 13	31
M.	Claim 15	32
N.	Claim 16	33
O.	Claim 17	35
P.	Claim 18	36
Q.	Claim 19	36
R.	Claim 20	36
X.	GROUND 1B: <i>Hirst</i> Renders Obvious 1-3, 5-13, and 15-20	36
A.	Claims 2 and 11	37
XI.	GROUND 2A: <i>Chagny</i> Anticipates Claims 1-2, 4-6, 11, 14-16, and 20	37
A.	Claim 1	38
B.	Claim 2	46
C.	Claim 4	47

D.	Claim 5	48
E.	Claim 6	48
F.	Claims 11, 14, 15.....	50
G.	Claim 16	50
H.	Claim 20	53
XIII. GROUND 2C: The Combination of <i>Chagny</i> and <i>Clark</i> Renders Obvious		
	Claims 3, 12-13, and 19.....	54
A.	Motivation to Combine	54
B.	Claim 3	57
C.	Claim 12	59
D.	Claim 13	59
E.	Claim 19	60
XIV. GROUND 3: <i>Hwang</i> in View of the Knowledge of a POSITA Renders		
	Obvious Claims 1-2, 4-6, 11, 14-16, and 20	60
A.	Claim 1	60
B.	Claim 2	70
C.	Claim 4	70
D.	Claim 5	71
E.	Claim 6	72
F.	Claims 11, 14, 15.....	74

G.	Claim 16	74
H.	Claim 20	76
XV.	CONCLUSION.....	76

LIST OF EXHIBITS

1001	U.S. Patent No. 7,675,759 by Artusi et al. (“the ’759 Patent”)
1002	Expert Declaration of Dr. Sayfe Kiaei
1003	U.S. Patent No. 6,294,904 to Hirst (“Hirst”)
1004	U.S. Patent No. 6,873,136 to Chagny (“Chagny”)
1005	U.S. Patent No. 6,664,775 to Clark et al. (“Clark”)
1006	U.S. Patent Application Publication No. 2004/0174152 to Hwang et al. (“Hwang”)
1007	Comparisons of Claim 6 to Claim 7 and Claim 16 to Claim 17 of the ’759 Patent
1008	Excerpts of the ’759 Patent File History
1009	Ned Mohan et al., <i>Power Electronics: Converters, Applications, and Design</i> (John Wiley & Sons, Inc., 2d Ed. 1995) (“Mohan”)
1010	U.S. Patent No. 5,747,976 to Wong (“Wong”)
1011	MyPAQ’s Preliminary Infringement Contentions, Exhibit 4, served in <i>MyPAQ Holdings, Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , 6:21-CV-398-ADA
1012	Alan Grebene, <i>Bipolar and MOS Analog Integrated Circuit Design</i> (John Wiley & Sons, Inc., 1984) (“Grebene”)
1013	MyPAQ’s Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , 6:21-CV-398-ADA
1014	<i>MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , No. 21-cv-00398, Dkt. 40 (W.D. Tex. Nov. 29, 2021) (“Scheduling Order”)

1015	S.A. Money, Microprocessor Data Book (Academic Press, Inc., 2 nd ed. 1990)
1016	MyPAQ's Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Dell Technologies Inc. et al.</i> , 6:21-CV-933-ADA
1017	MyPAQ's Preliminary Infringement Contentions, Exhibit 1, served in <i>MyPAQ Holdings, Ltd. v. Dell Technologies Inc. et al.</i> , 6:21-CV-933-ADA
1018	Reserved
1019	MyPAQ's Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Anker Innovations Ltd.</i> , 6:22-CV-150-ADA

Citations to exhibits including patents and patent applications reference original page, column, paragraph, or line numbers found in the underlying document.

Citations to other exhibits refer to exhibit page numbering.

LIST OF CLAIMS**Claim 1:**

1[Pre]	A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:
1[a]	a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and
1[b]	a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,
1[c]	said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,
1[d]	thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.

Claim 2:

2	The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.
----------	---

Claim 3:

3	The power converter as recited in claim 1 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.
----------	---

Claim 4:

4	The power converter as recited in claim 1 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.
----------	--

Claim 5:

5	The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter
----------	--

Claim 6:

6[Pre]	A power system coupled to a load, comprising:
6[a]	a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and
6[b]	a power converter, including:
6[c]	a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and
6[d]	a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,
6[e]	thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.

Claim 7:

7[Pre]	The power system as recited in claim 6 wherein said power system is coupled to another load and
7[a]	said power system controller is configured to receive another signal indicating another system operational state of said another load and to select another power converter operational state as a function thereof,
7[b]	said power system, further comprising: another power converter, including:
7[c]	another power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and
7[d]	another controller configured to receive another command from said power system controller to enter said another power converter operational state and to provide a signal to control said duty cycle of

	said another power switch as a function of said output characteristic and in accordance with said another command,
7[e]	thereby regulating an internal operating characteristic of said another power converter to improve an operating efficiency thereof as a function of said another system operational state.

Claim 8:

8	The power system as recited in claim 7 wherein at least one of said system operational state and said another system operational state, and said power converter operational state and said another power converter operational state, are different.
---	---

Claim 9:

9	The power system as recited in claim 7 wherein said power converter and said another power converter are configured to provide power to said load and said another load, respectively.
---	--

Claim 10:

10	The power system as recited in claim 7 wherein said power system controller is configured to sequentially operate said power converter and said another power converter.
----	--

Claim 11:

11	The power system as recited in claim 6 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.
----	--

Claim 12:

12	The power system as recited in claim 6 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.
----	--

Claim 13:

13	The power system as recited in claim 12 wherein said power converter status is selected from the group consisting of: a fully operational status, a failure likely status, a failed status, and an overloaded status.
-----------	---

Claim 14:

14	The power system as recited in claim 6 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.
-----------	---

Claim 15:

15	The power system as recited in claim 6 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.
-----------	---

Claim 16:

16[Pre]	A method of operating a power system coupled to a load, comprising:
16[a]	receiving a signal indicating a system operational state of said load;
16[b]	generating a power converter operational state as a function of said system operational state;
16[c]	inducing a power converter to enter said power converter operational state; and
16[d]	providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,
16[e]	thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.

Claim 17:

17[Pre]	The method as recited in claim 16 wherein said power system is coupled to another load and further comprising:
17[a]	receiving another signal indicating another system operational state of said another load;
17[b]	generating another power converter operational state as a function of said another system operational state;
17[c]	inducing another power converter to enter said another power converter operational state; and
17[d]	providing a signal to control a duty cycle of another power switch of said another power converter as a function of an output characteristic thereof and in accordance with said another power converter operational state,
17[e]	thereby regulating an internal operating characteristic of said another power converter to improve an operating efficiency thereof as a function of said another system operational state.

Claim 18:

18	The method as recited in claim 17 wherein said power converter and said another power converter are operated sequentially.
-----------	--

Claim 19:

19	The method as recited in claim 16 further comprising receiving a signal indicating a power converter status of said power converter and generating said power converter operational state as a function thereof.
-----------	--

Claim 20:

20	The method as recited in claim 16 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.
-----------	--

I. MANDATORY NOTICES

Real Party in Interest: The real party in interest include Anker Innovations Ltd. (“Anker”) (“Petitioner”).

Related Matters: The ’759 Patent is currently asserted by Patent Owner against Samsung in the case styled: *MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd.*, 6:21-CV-00398 (W.D. Tex.) (“Samsung Litigation”), which was originally filed on April 23, 2021. The ’759 Patent is also currently asserted by Patent Owner against Dell in the case styled: *MyPAQ Holdings Ltd. v. Dell Technologies Inc.*, 6:21-CV-00933 (W.D. Tex.) (“Dell Litigation”). The ’759 Patent is further currently asserted by Patent Owner against Anker in the case styled: *MyPAQ Holdings Ltd. v. Anker Innovations Ltd.*, 6:22-CV-00150 (W.D. Tex.) (“Anker Litigation”).

Petitioner is also concurrently filing a Petition for IPR against another patent held by PO, which is related to the ’759 Patent: IPR2022-01134 against U.S. Patent No. 7,675,759. The ’514 Patent is a continuation of an intervening continuation-in-part that claims priority to the ’759 Patent. *See* EX1001.

Lead Counsel and Back-Up Counsel: Petitioners designate lead and back-up counsel as noted below. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

Lead Counsel	Back-Up Counsel
Ping Wang Registration No. 48,328 RIMON PC 1990 K Street, N.W., Suite 420	Jason Xu <i>Pro hac vice forthcoming</i> RIMON PC 1990 K Street, N.W., Suite 420

Washington, DC 20006 202-519-2151 (phone)	Washington, DC 20006 202-470-2141 (phone) Eric Cohen Registration No. 27,429 RIMON PC 4208 Six Folks Road, Suite 1000 Raleigh, NC 27609 919-825-4877 (phone)
--	---

Service Information: Correspondence to lead and back-up counsel can be provided at the postal and electronic addresses above. Petitioners also consent to service by electronic mail at Anker759IPR@rimonlaw.com.

II. STANDING AND FEES

Standing: Petitioners certify under 37 C.F.R. § 42.104(a) that the '759 Patent is eligible for *inter partes* review and that Petitioners are not barred or estopped from requesting *inter partes* review on the grounds set forth herein.

Fees: The Office is authorized to charge the fee set forth in 37 C.F.R. § 42.15(a) to Deposit Account No. 50-5992 and any additional fees that might be due in connection with this Petition.

III. OVERVIEW OF THE '759 PATENT

A. Subject Matter

The '759 Patent involves power converters, which may convert an input voltage into an output voltage. EX1001, 1:21-24. Figure 2 illustrates an example “buck” power converter:

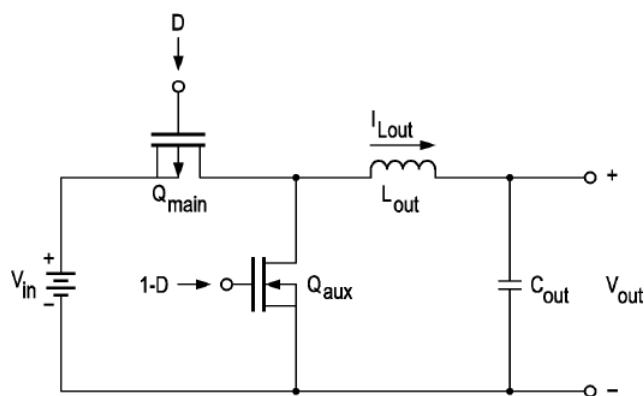


FIG. 2
(PRIOR ART)

EX1001, Fig. 2. The main power switch Q_{main} and auxiliary power switch Q_{aux} are turned on and off by drive signal D and complementary drive signal $1-D$. *Id.*, 8:57-9:15. When Q_{main} is turned on, Q_{aux} is turned off, and vice versa. As known in the art, and explained in the '759 Patent background, the duty cycle of the switches (i.e., ratio of on-time to the total switching period) in a power converter can be adjusted to regulate the output voltage V_{out} of the power converter. *Id.*, 1:36-55, 9:15-18; EX1002, ¶38.

The '759 Patent purports to improve power converters by using an “adaptive controller.” EX1001, Abstract. The '759 Patent describes adjusting an internal operating characteristic of the power converter based on a signal from an external source. *Id.*, 5:18-26. For example, when a load such as a microprocessor goes into a low-power system operational state (e.g., a standby mode), the microprocessor may signal the power converter to adjust its internal operating characteristics (e.g.,

switching frequency) to improve the efficiency of the power converter during such times of low demand from the load.

However, power converters capable of adjusting internal operating characteristics to improve efficiency based on an external signal indicating the state of the load were well known before the '759 Patent. EX1002, ¶¶39-40.

B. Prosecution History

U.S. Patent Application No. 11/710,276 was filed on February 23, 2007, as a continuation-in-part of application No. 11/607,325 filed on December 1, 2006. *See* EX1001. In a February 25, 2009 office action, the Examiner rejected claims 1-20, relying on, among other references, U.S. Publication 2008/0054874 ("Chandrasekaran"). Invoking the common ownership exception, Applicant argued that Chandrasekaran was not prior art. EX1008, 15-17. Thereafter, Examiner issued a Notice of Allowance. *Id.*, 4.

IV. SUMMARY OF PRIOR ART

The '759 Patent claims priority to December 1, 2006, and is subject to the pre-AIA provisions of 35 U.S.C. §§ 102-103.

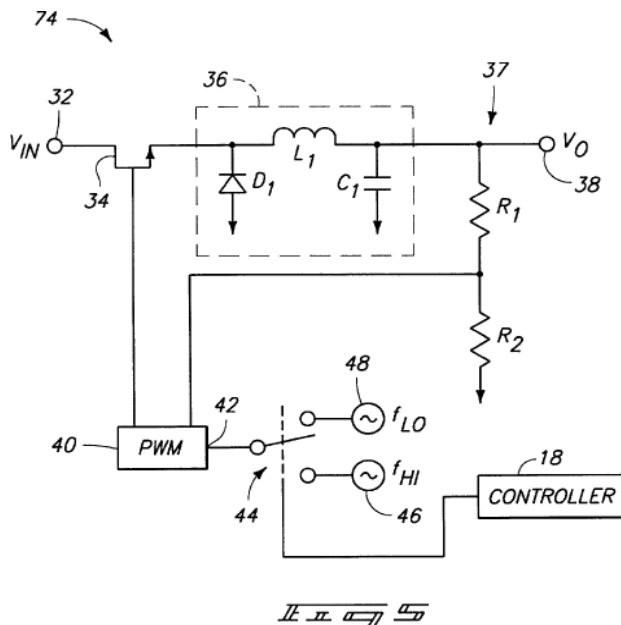
None of the *Hirst*, *Chagny*, *Clark*, or *Hwang* references described below were considered during examination of the '759 Patent.

A. Hirst (EX1003)

Hirst (U.S. Patent 6,294,904) issued on September 25, 2001. EX1003. *Hirst*

is prior art under 35 U.S.C. §§ 102(a) and (b).

Hirst describes “a multiple frequency switching power supply” that provides “a regulated output voltage.” EX1003, 2:44-54. Figure 5 of *Hirst* illustrates a power converter receiving signals from an external controller 18.



EX1003, Fig. 5. *Hirst* discloses that “in response to commands from the controller 18,” the power converter changes its switching frequency. *See id.*, 7:55- 8:5. By reducing switching frequency during standby mode, efficiency is improved “because switching losses are dramatically reduced.” *Id.*, 4:59-62; EX1002, ¶45.

B. Chagny (EX1004)

Chagny (U.S. Patent 6,873,136) issued on March 29, 2005. EX1004. *Chagny* is prior art under 35 U.S.C. §§ 102(a) and (b).

Chagny discloses a voltage regulator module (VRM) 200 (i.e., a power converter) that provides a “regulated DC voltage output 295” to processor 292. EX1004, 3:52-58.

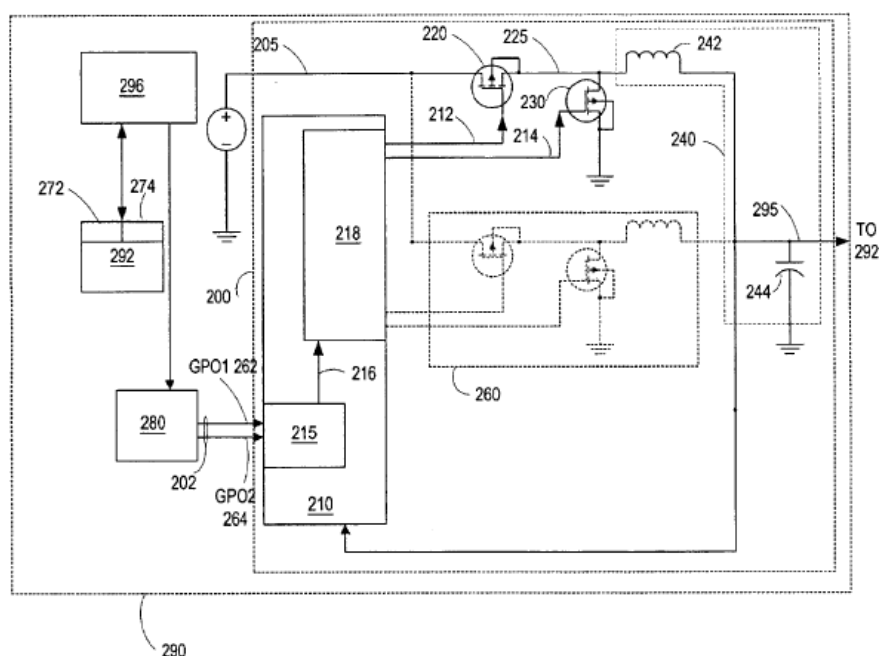


FIG. 2A

EX1004, Fig. 2A. *Changny*'s controller module 210 receives an activity input 202 indicative of the processor's activity level (*id.*, 3:60-65), and thereby changes the switching frequency of VRM 200 accordingly (*id.*, 5:9-12). By selecting a low switching frequency during periods of low processor activity, the efficiency of VRM 200 is improved. *Id.*, 5:20-23; EX1002, ¶47.

C. *Clark* (EX1005)

Clark (U.S. Patent 6,664,775) issued on December 16, 2003. EX1005. *Clark* is prior art under 35 U.S.C. §§ 102(a) and (b).

Clark describes “a portable device” that includes a voltage regulator 40 providing power to core logic 50 (e.g., a microprocessor). EX1005, 3:30-43.

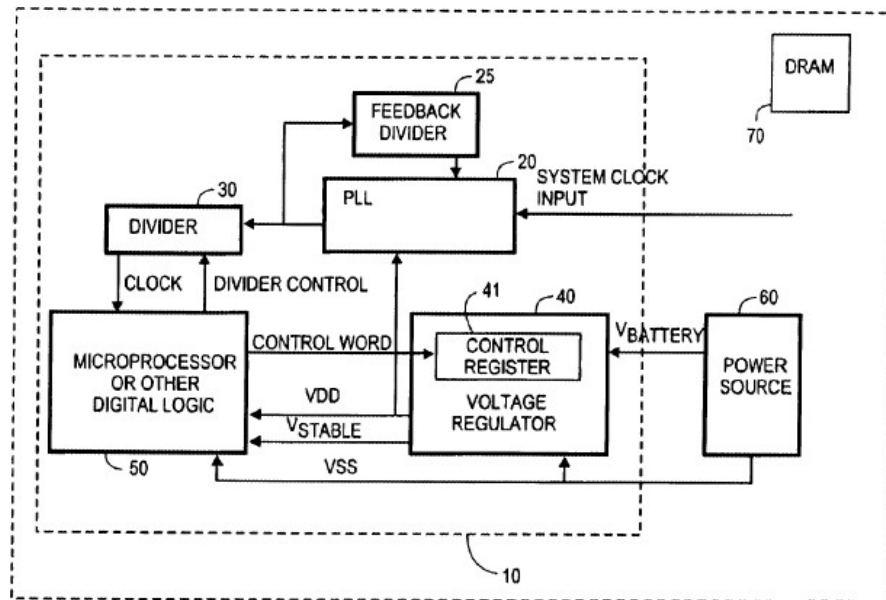


FIG. 1

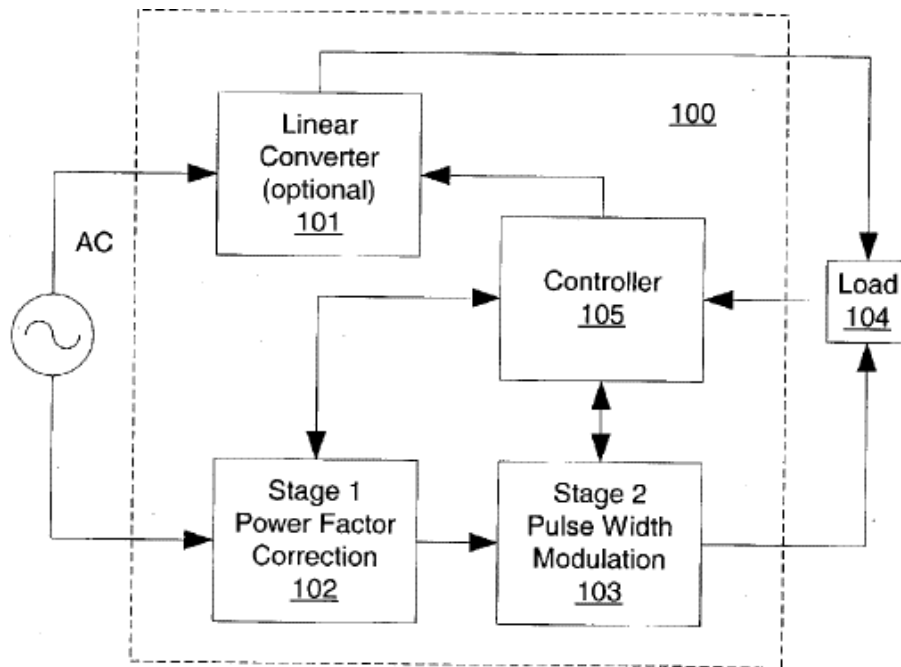
EX1005, Fig. 1. *Clark* teaches that “core logic 50 may send control signals to ... reduce the voltage potential range provided by voltage regulator 40,” thereby reducing “the amount of power consumed by integrated circuit 10.” *Id.*, 5:14-21.

Clark is analogous art because it is in the same field of endeavor— adaptable power systems—as the ’759 Patent. EX1002, ¶¶49-50.

D. Hwang (EX1006)

Hwang (U.S. Patent Application Publication 2004/0174152) published on September 9, 2004. EX1006. *Hwang* is prior art to the ’759 Patent under 35 U.S.C. §§ 102(a) and (b).

Hwang discloses a power converter 100 coupled to a smart load 104 (e.g., a microprocessor). EX1006, [0019], [0021].



EX1006, Fig. 1. *Hwang* discloses that load 104 sends a standby signal to controller 105 within power converter 100 indicating the level of power drawn by load 104, thereby causing “PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021]) to “improve efficiency” (*id.*, Abstract).

Hwang is analogous art because it is in the same field of endeavor— adaptable power systems—as the ’759 Patent. EX1002, ¶¶51-53.

V. SUMMARY OF GROUNDS

Ground	Claims	Statutory Basis (35 U.S.C. §)	Prior Art
1A	1-3, 5-13, 15-20	102	<i>Hirst</i>
1B	1-3, 5-13, 15-20	103	<i>Hirst</i>
2A	1-2, 4-6, 11, 14-16, 20	102	<i>Chagny</i>
2B	1-2, 4-6, 11, 14-16, 20	103	<i>Chagny</i>
2C	3, 12-13, 19	103	<i>Chagny, Clark</i>
3	1-2, 4-6, 11, 14-16, 20	103	<i>Hwang</i>

EX1002,¶54.

VI. LEVEL OF ORDINARY SKILL

A POSITA at the time of the '759 Patent would have had either (i) a Master of Science in Electrical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering or an equivalent field as well as at least two years of experience in the design of power electronics. EX1002,¶35.

VII. CLAIM CONSTRUCTION

Claim terms are construed according to their ordinary and customary meaning as understood by a POSITA and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). For purposes of this Petition, Petitioners interpret all claim terms in accordance with their ordinary and customary meaning.

VIII. INSTITUTION IS PROPER

A. Institution is Proper Under 35 U.S.C. § 314(a)

The six factors considered for § 314 denial strongly favor institution. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). The district court case is at an early stage and no trial date has been set. Petitioner has diligently prepared and filed this petition only about four months after Patent Owner filed its complaint against Anker.

1. No evidence regarding a stay. This petition precedes even the entry of any procedural schedule in the co-pending litigation, within which Anker intends to move for a stay after this petition is instituted, or earlier depending upon circumstances in the Western District of Texas. *Sand Revolution II LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative). Thus, Factor 1 does not support discretionary denial.
2. Parallel proceeding trial date. No schedule has been entered and no trial date set. Without a trial date, this factor weighs heavily against discretionary denial.
3. Investment in the parallel proceeding. Petitioner has filed this Petition at a very early stage of the litigation—a fact that “has weighed against exercising the authority to deny institution.” *Apple, Inc. v. Seven Networks*, IPR2020-00156, Paper 10 at 11-12 (June 15, 2020). Petitioner has not served its invalidity contentions. The parties have not exchanged preliminary positions on claim

construction or invalidity, and fact and expert discovery has not begun. Further, there is no evidence that the district court will conduct a *Markman* hearing or issue a *Markman* ruling before the prospective date for the Board's institution decision. Anker's promptness favors institution. *Fintiv*, Paper 11 at 11 ("If the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution under NHK.").

4. Overlapping issues with the parallel proceeding. The co-pending litigation is in its infancy. Petition challenges claims not asserted by the PO in district court. Compare EX1019 (asserting 5 claims against Anker) with Section V (challenging all 20 claims). Thus, "[i]nstituting trial here serves overall system efficiency and integrity goals ... by resolving materially different patentability issues." *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 at 19 (P.T.A.B. June 15, 2020) (finding the fourth factor "strongly" favored institution even though there was no stipulation). Nevertheless, to eliminate any doubt regarding overlap between the proceedings, Petitioner hereby stipulates that, if the Board institutes *inter partes* review of this Petition, then Petitioner, and the Real Parties in Interest listed herein, will not assert in the Anker Litigation that any of claims 1-20 of the '759 Patent is invalid on any ground involving the prior art relied upon in the grounds of invalidity herein. A lack of such overlap "has tended to weigh against exercising discretion to deny institution." *Fintiv*,

IPR2020-00019, Paper 11, 12-14.

5. Petitioner is a defendant. Anker is a defendant in the litigation. Because it is “far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same,” panels routinely grant institution when the parties are the same as in a district court proceeding. *See Sand Revolution II* at 12-13. Due to the exceedingly early stage of this litigation, Factor 5 is neutral and should not be a basis for denying institution.
6. Other circumstances. The prior art presented in this Petition renders the Challenged Claims unpatentable as obvious. The merits of Petitioner’s arguments are strong, especially given that the Board has already instituted IPR2022-00311 filed by Samsung/Dell against the same patent using the same grounds. Thus, this factor weighs against discretionary denial.

As such, because the *Fintiv* factors are either neutral or weigh against discretionary denial, and because this Petition was filed more than eight months before the statutory bar date, institution should not be denied on discretionary factors.

B. Discretionary denial under General Plastic is not appropriate

The ’759 patent is being challenged in case no. IPR2021-00312, but here, Anker is seeking to join that earlier case by filing this substantively identical Petition along with a motion for joinder. The present petition is permissible under 35 U.S.C. § 315(c), and is not a “follow-on” petition seeking to raise new issues. *Celltrion, Inc. v. Genentech, Inc.*, IPR2018-01019, Paper 11 at 9-11 (PTAB Oct. 30, 2018). As

explained by the Board in *Celltrion*, the *General Plastic* factors do not weigh in favor of discretionary denial where, as here, “a different petitioner files a ‘me-too’ or ‘copycat’ petition in conjunction with a timely motion to join.” *Id.* (the motion to join “obviates any concerns of serial harassment”).

C. Institution is Proper Under 35 U.S.C. § 325(d)

None of the *Becton, Dickinson* factors weigh in favor of discretionary denial under 35 U.S.C. § 325(d). *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential). None of the references relied upon by this Petition were before the Examiner, much less included in a rejection, during prosecution. Thus “the same or substantially the same prior art or arguments” were *not* previously presented to the Office.

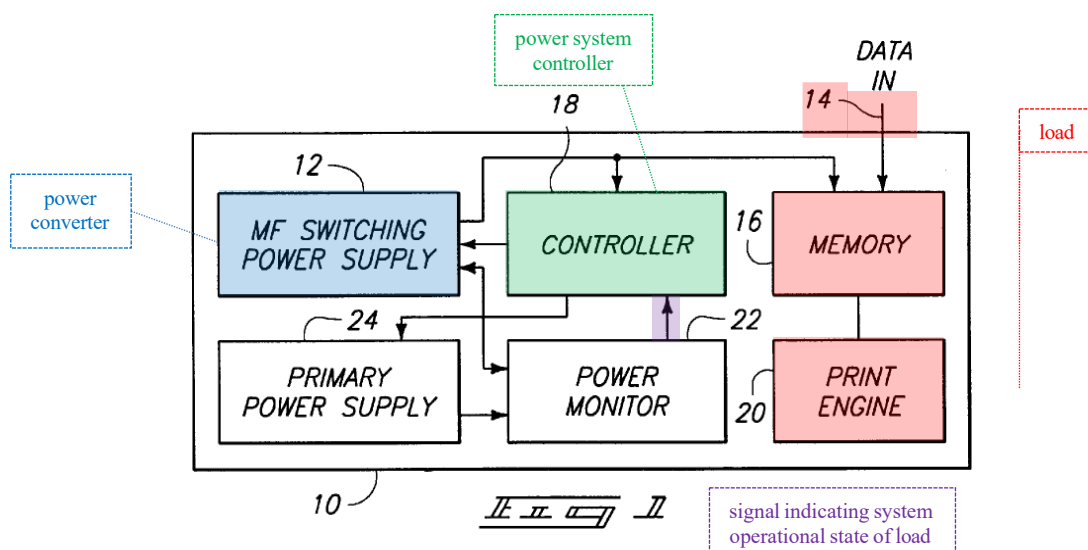
IX. GROUND 1A: Hirst Anticipates Claims 1-3, 5-13, and 15-20

A. Claim 1

- i. **1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

Hirst discloses a multiple-frequency (MF) “switching power supply” (i.e., power converter). EX1003, Abstract, 2:44-45. Figure 1 of *Hirst* provides a block diagram of a printer 10, including an MF switching power supply 12 and a print-engine controller 18 (i.e., power system controller). EX1003, 3:51-59. The MF switching power supply 12 may supply power to “data input port 14” and “data

memory 16” of printer 10 (collectively or individually¹, the load). *Id.*, 4:20-32.



EX1003, FIG. 1 (annotated); EX1002, ¶56.

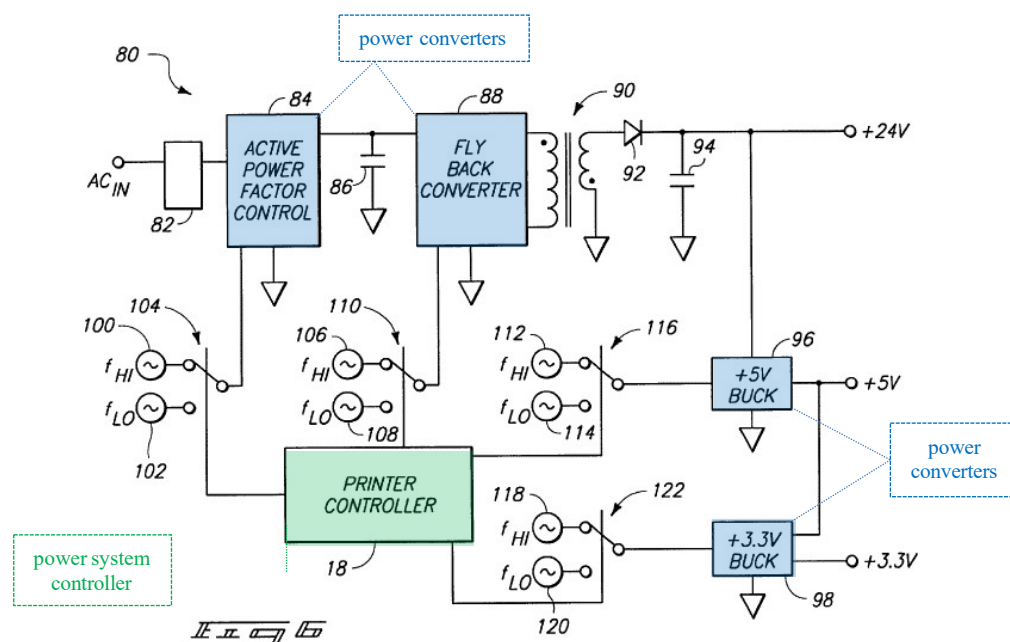
Hirst discloses that the printer may operate in a “normal mode of operation” or a “standby mode of operation” (i.e., different system operational states). EX1003, 3:17-23. The power consumption during these normal and standby modes is detected by “power consumption monitor 22.” *Id.*, 4:32-41.

In some embodiments, signals from power consumption monitor 22 directly control the switching frequency of an MF switching power supply. EX1003, 5:46-50. However, *Hirst* discloses that signals from the power consumption monitor 22 (i.e., signals indicating system operational state of the load) are also sent to and received by controller 18 (i.e., the power system controller). *See id.*, 8:27-33

¹ These individual components can also be separate loads supplied by multiple instances of *Hirst*’s multi-frequency power supply. EX1003, 4:27-32, FIG. 6.

(describing “controller 18” in Figure 6 as controlling the frequency of the switching power supply “in response to signals from the power monitor 22 of FIG. 1”), Fig. 1 (illustrating signal from power monitor 22 to controller 18); *see also id.*, 6:65-7:4 (describing “one embodiment of the power consumption monitor 22 of FIG. 1”), Fig. 3.

Hirst explains that by using controller 18 to control the frequency of the MF switching power supply, *Hirst* causes more than one instance of the MF switching power supply “to enter standby mode” (i.e., switch at a low frequency) “when the laser printer 10 of FIG. 1 enters the standby mode.” *Id.*, 8:5-8. This is shown in Figure 6 where controller 18 controls the frequency of multiple MF switching power supplies (i.e., power converters):



EX1003, Fig. 6 (annotated); EX1002, ¶59. *Hirst* explains that “controller 18” individually controls the frequency of each of the power supplies 84, 88, 96, and 98

shown in Figure 6 “in response to power levels being drawn from each of them.” EX1003, 8:27-49.

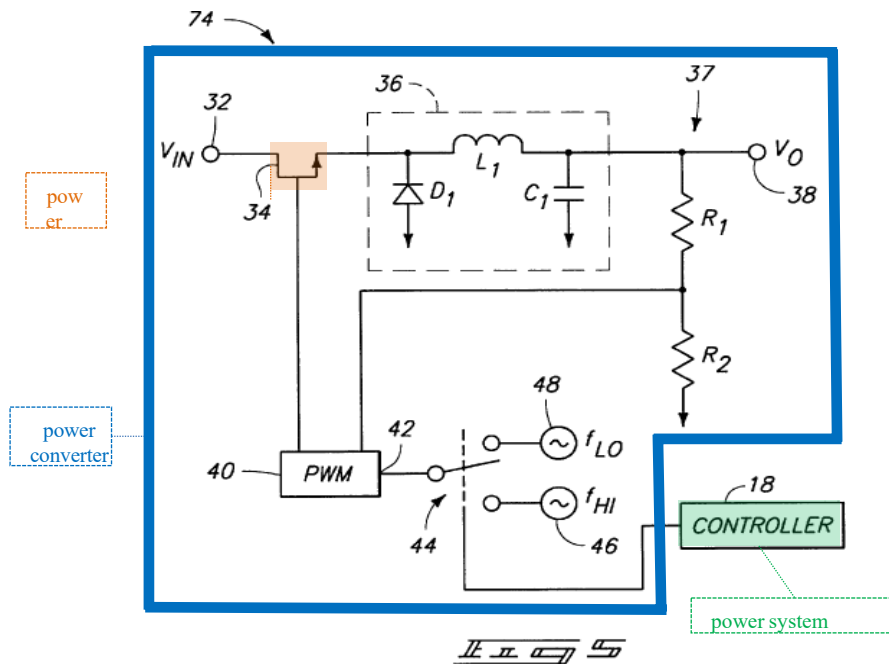
Accordingly, a POSITA would understand *Hirst* to disclose that controller 18 (i.e., the power system controller) is configured to receive a signal from a power system monitor 22 (i.e., a signal indicating the system operational state of a load coupled to the power converter), and thereby control the switching frequency of a power converter coupled to the load. EX1002, ¶60. Indeed, *Hirst*’s disclosure is similar to embodiments in the ’759 Patent whereby the switching frequency of a power converter is controlled based on a signal “from an external source” (like controller 18 of *Hirst*) based on the “actual load current” of the load coupled to the power converter. See EX1001, 12:18-30; EX1002, ¶60.

Hirst also discloses that controller 18 sets the frequency of the MF switching power supply “in response to other assessments of power need.” EX1003, 8:27-33. A POSITA would understand that such “other assessments” by controller 18 would include a signal based on, for example, the input data received at “data input port 14,” which operates “under the direction of controller 18.” See *id.*, 4:7-19 (describing processing of data received at data input port 14), 4:20-32 (describing “power consumption due to operation of the data input port, the data memory ... and the print engine 20”). Thus, a signal received by controller 18 representing the “other assessments of power need,” would *also* qualify as a signal indicating the system operational state of the load.

Hirst thus discloses claim 1[pre]. EX1002, ¶¶56-63.

- ii. 1[a]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and”

Figures 2-5 of *Hirst* share common reference numbers for common elements. EX1003, Figs. 2-5, 6:45-51. As shown in Figure 5, “switching transistor 34” serves as the power switch in a “buck” power converter. *Id.*, 6:1-5 (describing “turning the switching transistor 34 ON and OFF to supply electrical charge from the power input port 32 to the filtering circuit 36”), 5:18-20 (describing “buck” configuration); *see also id.*, Abstract, 2:45-49 (describing operation of “switching transistor”), 1:18-28.



EX1003, Fig. 5 (annotated); EX1002, ¶64.

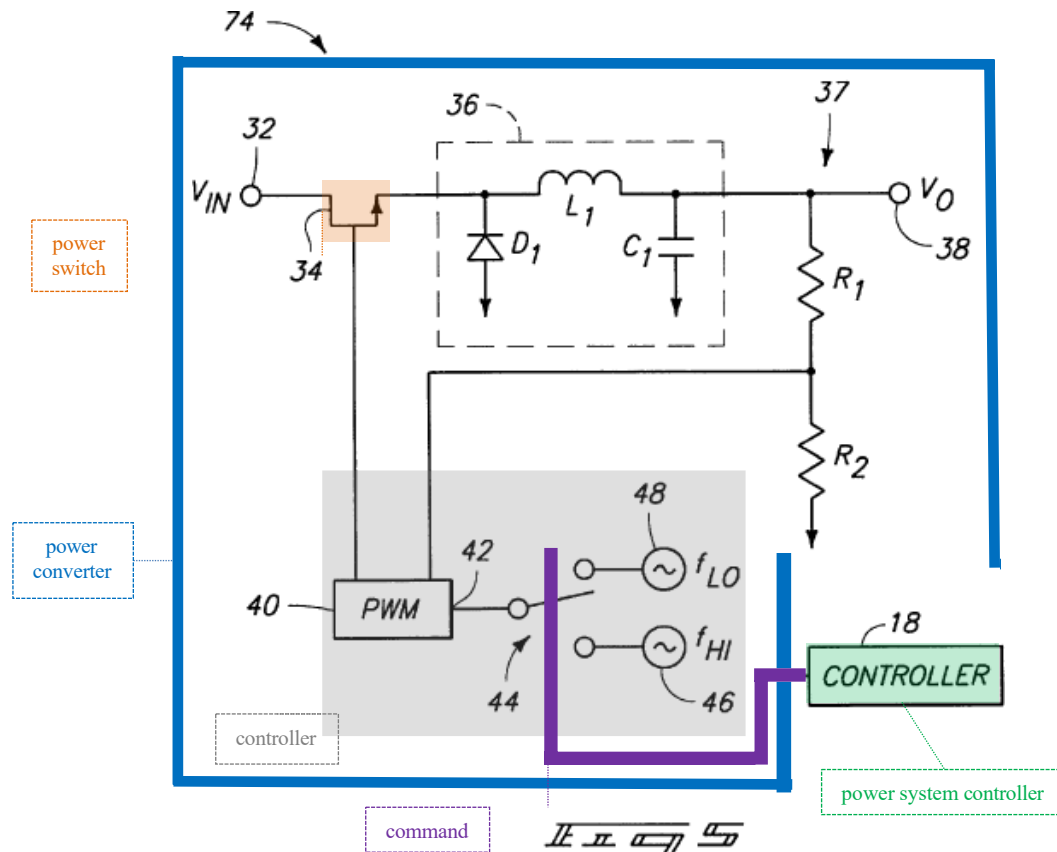
Hirst explains that the “duty cycle of the switching transistor 34 [i.e., the power switch] is varied in a conventional manner by the PWM circuit 40 in response

to voltages sensed by the voltage divider 37 to regulate the amount of charge that is transferred per cycle from the power input port 32 to the filtering circuit 36 and thus to maintain the desired output voltage V_{OUT} [i.e., regulated output characteristic] at the output 38.” EX1003, 6:8-14; *see also id.*, 6:1-20.

Hirst thus discloses claim 1[a]. EX1002, ¶¶64-66.

- iii. **1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”**

Figure 5 of *Hirst* illustrates a power converter “controller” including pulse-width modulation (PWM) circuit 40, first oscillator 46, second oscillator 48, and switch 44 (collectively, the power converter “controller” recited in claim 1[b], annotated in gray). EX1003, 5:24-31, 7:63-8:8. That claimed “controller” responds to a signal (annotated in purple) received from power system controller 18, as explained below.



EX1003, Fig. 5 (annotated); EX1002, ¶67.

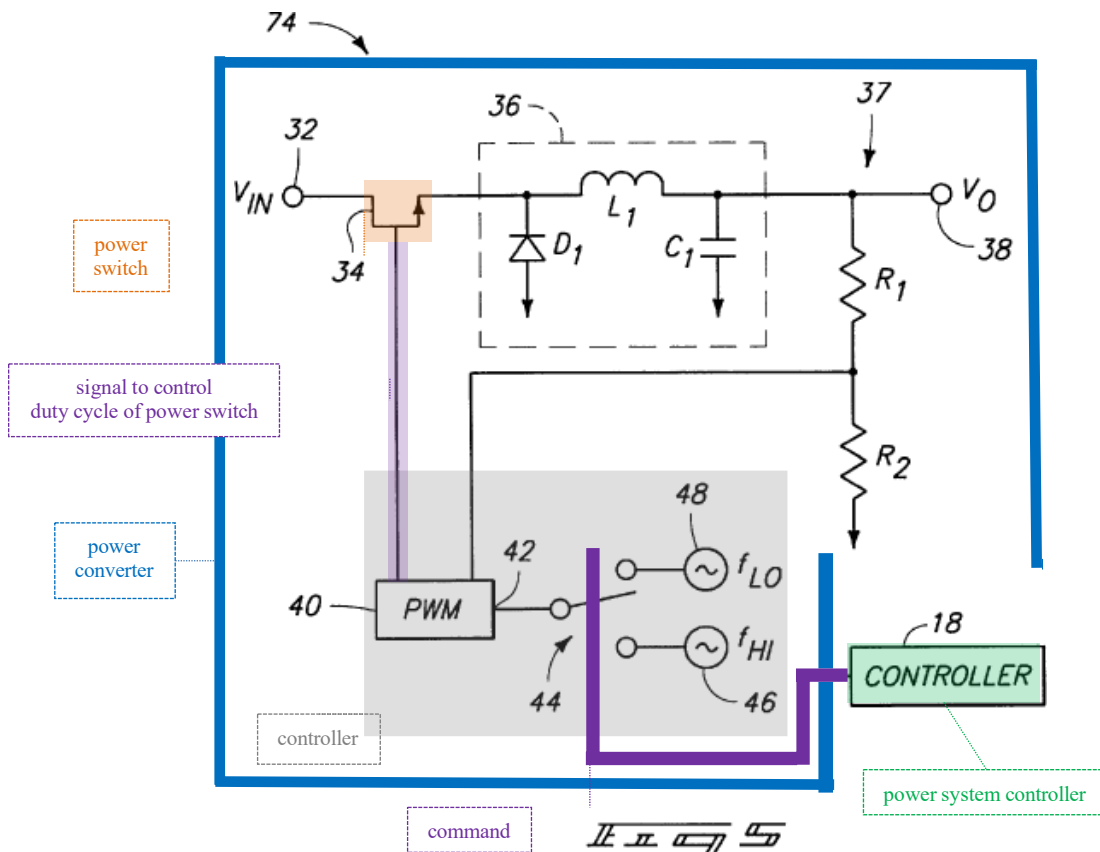
As described for claim 1[pre], controller 18 (i.e., the power system controller) receives a signal indicating the system operational state of the load. EX1003, 8:27-33 (describing “controller 18” acting “in response to signals from the power monitor 22 of FIG. 1”). As a function thereof, controller 18 (i.e., the power system controller) sends a command to the controller within the power converter to enter one of two power converter operational states: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. See EX1003, 7:66-8:5. This command “permits the controller 18 to cause ... the power supply 74, to enter the standby mode when the laser printer 10

of FIG. 1 enters the standby mode.” *Id.*, 8:5-8:8; *see also id.*, 3:17-23; EX1002, ¶68.

Hirst thus discloses claim 1[b]. EX1002, ¶¶67-69.

- iv. 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”

Figure 5 of *Hirst* shows the “gate of the switching transistor 34 is coupled to an output of the PWM circuit 40,” which is part of the power converter controller, as explained above. EX1003, 6:7-8.



EX1003, Fig. 5 (annotated); EX1002, ¶70. As described for claim 1[a], PWM circuit 40 controls the duty cycle of switching transistor 34 (i.e., the power switch) as a function of the feedback from the output voltage (i.e., as a function of said output

characteristic). EX1003, 6:8-14 (“[T]he duty cycle of the switching transistor 34 is varied in a conventional manner by the PWM circuit 40 in response to voltages sensed by the voltage divider 37 to regulate the amount of charge that is transferred per cycle ... and thus to maintain the desired output voltage V_{OUT} ”). Moreover, the switching transistor is also controlled in accordance with the command from the power system controller setting the frequency. EX1003, 6:15-18 (describing “limits over which the duty cycle may be varied” when PWM circuit 40 is “driven by” the first and second oscillators), 2:59-65 (describing provision of “first frequency” or “second frequency” to PWM circuit), 7:66-8:9, 6:34-37; *see also id.*, 5:32-35 (describing selective coupling of “oscillators 46 and 48 to the PWM circuit 40”).

Hirst thus discloses claim 1[c]. EX1002, ¶¶70-72.

- v. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

As described for claim 1[pre] and 1[b], the switching frequency (i.e., the internal operating characteristic) of the power converter in *Hirst* is selected as a function of the system operational state of the load. EX1003, 3:17-24 (“Commands from a print engine controller select a first switching frequency for the power supply when the printer is in a normal mode of operation and select a second switching frequency for the power supply when the printer is in a standby mode of operation.”), 7:66-8:8 (power converter placed in “standby mode” with low frequency f_{LO} “when the laser printer 10 of FIG. 1 enters the standby mode.”).

Hirst explains that switching losses in a switching power converter are proportional to switching speed. EX1003, 2:2-3. Efficiency can thus be “improved under light loading by lowering the switching speed [i.e., the switching frequency] of a switching element.” *Id.*, 1:46-48; *see also* EX1002, ¶¶74; EX1010, 2:15-34 (explaining switch loss). Consistent with this principle, *Hirst* explains that the reduction of its switching frequency when the load is in a standby mode “provides a sharp increase in switching power supply efficiency because switching losses are dramatically reduced.” EX1003, 4:59-62.

Hirst thus discloses claim 1[d]. EX1002, ¶¶73-75.

B. Claim 2

- i. **“2. The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

Claim 2 does not set an upper limit, or otherwise define, the recited “transition time.” PO’s infringement contentions in the Samsung Litigation merely point to a “fast and smooth voltage transition” without reference to any specific time that the transition must occur within. EX1011, 19; *see also* EX1017 (Dell Litigation), 18 (merely labeling a rise time of a voltage plot).

The MF switching power supply of *Hirst* (i.e., the power converter) is configured to transition between states “very rapidly.” EX1003, 2:37-41. As described for claim 1[b], the power converter operational states of *Hirst* include

(i) the “normal mode of operation” with a high switching frequency “ f_{HI} ,” and (ii) the “standby mode of operation” with a low switching frequency “ f_{LO} ,” EX1003, 7:63-8:8. A POSITA would appreciate that the transition from one switching-frequency state to the other would be completed within one switching cycle at the new frequency. EX1002, ¶77. Accordingly, *Hirst* transitions between power converter operational states within a transition time as recited by Claim 2. EX1002, ¶¶76-77.

C. Claim 3

- i. **“3. The power converter as recited in claim 1 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.”**

Hirst discloses that its MF switching power supply (i.e., the power converter) “includes a ripple monitor 49.” EX1003, 6:29-31, Fig. 2. *Hirst* explains that the “amount of ripple that is present in the output voltage V_O tends to increase as the amount of power being drawn from the MF switching power supply 30 increases.” *Id.*, 6:30-32. “When the ripple monitor 49 determines that the ripple in the output voltage V_O is too high, the ripple monitor 49 provides a signal to the controller 18 of FIG. 1 to increase the frequency of the MF switching power supply 30.” *Id.*, 6:32-37. For example, the frequency is increased by switching from the low-frequency oscillator to the high-frequency oscillator. *See id.*, 6:37-38 (“the frequency is increased by switching to the first oscillator 46”), 7:66-8:8 (describing “normal mode of operation” with a high frequency “ f_{HI} ” and a “standby mode of operation”

with the low frequency “ f_{LO} ”).

In sum, controller 18 (i.e., the power system controller) receives a signal from ripple monitor 49 indicating that the power supply ripple is too high (i.e., indicating a power converter status), and switches the power converter to a higher switching-frequency state (i.e., a different power converter operational state) as a function thereof. EX1002, ¶79; *see also* EX1001 (’759 Patent), 20:9-14 (associating “a high level of ripple voltage” with a “Failure Likely” power converter status).

Hirst thus discloses claim 3. EX1002, ¶¶78-81.

D. Claim 5

- i. **“5. The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of:
a fully operational power converter,
a reduced redundancy power converter, and
an idle power converter.”**

The ’759 Patent describes a “Fully Operational” power converter operational state as “[a]ll power converter components operational at full performance level,” as opposed to other states with “reduced switching frequency.” EX1001, Table I, 19:20-36.

As described for claim 1[b], *Hirst* discloses power converter operational states including a “normal mode of operation” with a high switching frequency “ f_{HI} .” EX1003, 7:63-8:8; *see also id.*, 2:59-65 (describing “first frequency” during “normal mode” and “second frequency” during “standby mode”). *Hirst*’s power converter in

the normal mode of operation with high switching frequency “ f_{HI} ” discloses a fully operational power converter. *Hirst* thus discloses claim 5. EX1002,¶¶82-83.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

Later elements of claim 6 require the “power system” of claim 6[pre] to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Hirst* discloses claim 6[pre] in the same manner described for claim 1[pre]. See Section IX.A.i; EX1002,¶84.

ii. 6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”

As described for claim 1[pre], *Hirst* discloses a power system controller configured to receive a signal indicating a system operational state of a load. See Section IX.A.i. As described for 1[b], the power system controller of *Hirst* sends a command to the power converter to enter a power converter operational state as a function of said signal. See Section IX.A.iii. *Hirst* thus discloses a power system controller configured to “select” a power converter operational state as a function of the signal indicating the system operational state. *Hirst* thus discloses claim 6[a]. EX1002,¶85.

iii. 6[b]: “a power converter, including:”

As described for claim 1[pre], *Hirst* discloses a power converter. See Section

IX.A.i; EX1002,¶86.

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”**

Claim 6[c] is identical to claim 1[a] and is disclosed in the manner described for claim 1[a]. *See* Section IX.A.ii; EX1002,¶87.

- v. **6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

Claim 6[d] restates limitations of claim 1[b]-[c] and is disclosed in the manner described for claim 1[b]-[c]. *See* Sections IX.A.iii-iv; EX1002,¶88.

- vi. **6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

Claim 6[e] is identical to claim 1[d] and is disclosed in the manner described for claim 1[d]. *See* Section IX.A.v; EX1002,¶89.

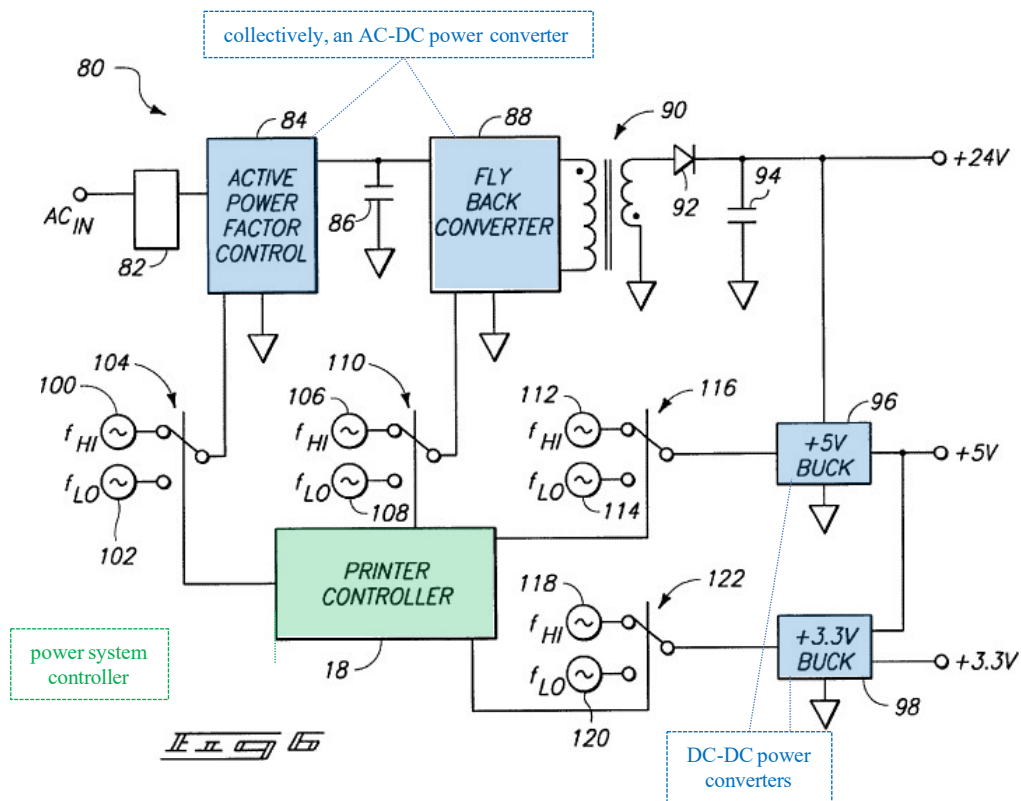
F. Claim 7

Claim 7, which is dependent on claim 6, repeats each limitation of claim 6, but for “*another* load” and “*another* power converter” (and the associated states, signals, and command) under the control of the same “power system controller.” *See* EX1007, 1 (side-by-side comparison); EX1002,¶90.

The power system of *Hirst* is coupled to multiple loads, including the “data input port 14,” “data memory 16,” and “print engine 20.” EX1003, 4:20-24, Fig. 1.

These multiple loads require different “voltages or currents in order to operate properly.” *Id.*, 4:24-27. Accordingly, an “AC-to-DC power supply 24 is often used to provide a primary power supply, with *one or more efficient DC-to-DC switching power supplies 12* to provide the data-handling circuits 14, 16 ... with electrical power.” *Id.*, 4:27-31; EX1002, ¶91.

Figure 6 of *Hirst* illustrates a power system including multiple MF switching power supplies for providing different output voltages to the multiple loads (e.g., the “data-handling circuits 14, 16” illustrated in Fig. 1 and described at 4:27-31).



EX1003, Fig. 6 (annotated); see also *id.*, 5:18-23, EX1002, ¶92.

Hirst explains: “FIG. 6 is a simplified block diagram of a group of power supplies 80 for the laser printer 10 of FIG. 1. Modern laser printers 10 include a number of power supplies 80, many or all of which may be switching power supplies.” EX1003, 8:9-12. As shown in Figure 6, active power factor control power supply 84 and fly back converter 88 collectively form an AC-DC power converter with a 24 V output suited for the “higher voltage[]” required by “print engine 20.” See EX1003, 4:24-27; *see also id.*, 8:17-23; EX1002, ¶93. As also shown in Figure 6, buck converters 96 and 98 provide lower voltages suited for lower-voltage components such as data input port 14 and data memory 16.² See EX1003, 4:20-31; *see also id.*, 8:17-23; EX1002, ¶94.

Hirst further discloses that the frequency for each of the MF switching power supplies in Figure 6 is under the control of the same “controller 18” (i.e., the power system controller). *Id.*, 8:27-49. Moreover, *Hirst* discloses that controller 18 “individually” selects the frequency for each of the multiple power supplies 84, 88, 96, and 98 “in response to power levels being drawn from each of them” (i.e., in response to the system operational state of their respective loads). *Id.*, 8:42-49; *see also id.*, 7:63-8:8 (disclosing “the controller 18 cause[s] more than one MF switching

² As shown in Figure 6, the +3.3 volt buck converter 98 is a load to the +5 buck converter 96, which in turn is a load to the + 24 volt output. EX1002, ¶94.

power supply” “to enter the standby mode”); EX1002,¶95. Based on this disclosure, a POSITA would understand that, for *each* of the respective power supplies and loads, controller 18 receives a signal indicating the system operational state of the load in the same manner described above for claim 1[pre] and 6[a]. EX1002,¶95.

Accordingly, a POSITA would understand that each power converter illustrated in Figure 6 of *Hirst*, and each of their respective loads, disclose the requirements of claim 6 (and the similar requirements of claim 1) in the same manner described for claims 1 and 6 in Sections IX.A and IX.E. EX1002,¶96. Thus, *Hirst* also discloses claim 7 including the requirements of “*another* power converter” and “*another* load” (and associated states, signals, and command) under the control of the same “power system controller.” *Id.*

G. Claim 8

- i. “8. The power system as recited in claim 7 wherein at least one of said system operational state and said another system operational state, and said power converter operational state and said another power converter operational state, are different.”**

Although claim 8 only requires one of the respective system operational states or respective power converter operational states be different from each other, *Hirst* discloses both.

As described for claim 1[b] and claim 6[a], *Hirst* discloses multiple power converter operational states: (i) a “normal mode of operation” with a high switching

frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. EX1003, 7:66-8:8. As described for claim 7, the multiple power converters of *Hirst*’s power system each can have a different power converter operational state. *Id.*, 8:42-49 (“The first frequency f_{HI} and the second frequency f_{LO} ***need not be the same*** for each of the power supplies 84, 88, 96 and 98. The controller 18 may switch all of the power supplies 84, 88, 96 and 98 together or ... ***may set them individually in response to power levels being drawn from each of them.***”). Accordingly, *Hirst* discloses that “said power converter operational state” and “said another power converter operational state” are different.

Moreover, *Hirst* discloses the system operational state of multiple loads can also differ. *See id.*, 8:44-49 (“The controller 18 may switch all of the power supplies 84, 88, 96 and 98 ... individually in response to ***power levels being drawn from each of them.***”); *see also id.*, 4:27-31 (disclosing multiple different loads).

Hirst thus discloses claim 8. EX1002, ¶¶97-100.

H. Claim 9

- i. **“9. The power system as recited in claim 7 wherein said power converter and said another power converter are configured to provide power to said load and said another load, respectively.”**

For the reasons described for claims 6 and 7, *Hirst* discloses claim 9. *See* Sections IX.E and IX.F; EX1002, ¶101.

I. Claim 10

- i. “10. The power system as recited in claim 7 wherein said power system controller is configured to sequentially operate said power converter and said another power converter.”**

As described for claim 7, *Hirst*’s multiple power converters can have different power converter operational states. *See* Section IX.F. Moreover, *Hirst* discloses that controller 18 (i.e., the power system controller) controls the operational states of the multiple power converters “in a preferred order” (i.e., sequentially). EX1003, 8:42-49 (“The first frequency f_{HI} and the second frequency f_{LO} need not be the same for each of the power supplies 84, 88, 96 and 98. The *controller 18 may switch all of the power supplies 84, 88, 96 and 98* together or may switch them *in a preferred order*, or may set them individually in response to power levels being drawn from each of them.”). *Hirst* thus discloses claim 10. EX1002, ¶¶102.

J. Claim 11

Hirst discloses the additional elements of claim 11 in the same manner described for similar claim 2. *See* Section IX.B; EX1002, ¶103.

K. Claim 12

Hirst discloses the additional elements of claim 12 in the same manner described for similar claim 3. *See* Section IX.C; EX1002, ¶104.

L. Claim 13

- i. “13. The power system as recited in claim 12 wherein said power converter status is selected from the group consisting of: a fully operational status, a failure likely status, a failed**

status, and an overloaded status.”

As described for claim 3 (and claim 12), *Hirst* explains that the “amount of ripple that is present in the output voltage V_O tends to increase as the amount of power being drawn from the MF switching power supply 30 increases.” EX1003, 6:30-32. “When the ripple monitor 49 determines that the ripple in the output voltage V_O is too high, the ripple monitor 49 *provides a signal to the controller 18* of FIG. 1 to increase the frequency of the MF switching power supply 30.” *Id.*, 6:32- 37.

Thus, the status signal from the ripple monitor is an indication that the “power being drawn” from the power supply is too high (i.e., the power converter is overloaded) for the given switching frequency. *See id.*, 6:30-37; EX1002, ¶¶105-106. The power converter status signal from ripple monitor 49 therefore indicates an “overload status” at the given frequency. EX1002, ¶106.

In addition, the '759 Patent describes a “Failure Likely” status as “Power converter operating with reduced operational capability,” and further associating “Failure Likely” with “a high level of ripple voltage.” EX1001, Table II, 20:9-14. Thus, the power converter status signal from *Hirst*’s ripple monitor indicating that the “ripple in the output voltage V_O is too high” (EX1003, 6:32-37) also serves as a failure likely status as recited in claim 13. EX1002, ¶107.

Accordingly, *Hirst* discloses claim 13 in multiple ways. EX1002, ¶¶105-108.

M. Claim 15

Hirst discloses the additional elements of claim 15 in the same manner

described for similar claim 5. *See* Section IX.D; EX1002, ¶109.

N. Claim 16

i. 16[pre]: “A method of operating a power system coupled to a load, comprising:”

Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Hirst* thus discloses claim 16[pre] in the same manner described for claim 6 (and similar elements of claim 1). *See* Sections IX.A.i and IX.E.i; EX1002, ¶110; EX1003, 1:13-15 (“The invention relates to multiple frequency switching power supplies and *methods to operate* a switching power supply.”).

ii. 16[a]: “receiving a signal indicating a system operational state of said load;”

As described for claims 1[pre] and 6[a], *Hirst* discloses a power system controller that receives a signal indicating a system operational state of a load. For the same reasons described in Sections IX.A.i (1[pre]) and IX.E.ii (6[a]), *Hirst* discloses method step 16[a]. EX1002, ¶111.

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

As described for claim 1[pre] and 1[b], *Hirst* describes a controller 18 that receives a signal indicating the system operational state of the load. *See* Sections IX.A.i and IX.A.iii; *see also* EX1003, 8:27-33 (describing “controller 18” acting “in response to signals from the power monitor 22 of FIG. 1”). As a function thereof, controller 18 sends a command to the power converter to enter one of two power

converter operational states: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. See EX1003, 7:66-8:5; see also *id.*, 8:5-9 (describing power supply entering “standby mode” when “laser printer 10 of FIG. 1 enters the standby mode), EX1003, 3:17-24 (“Commands from a print engine controller *select a first switching frequency* for the power supply when the printer is in *a normal mode* of operation and *select a second switching frequency* for the power supply when the printer is in *a standby mode* of operation.”).

Thus, *Hirst* discloses that a power converter operational state is generated, by the power converter for example, as a function of the system operational state of the load. EX1002, ¶¶112-113.

iv. 16[c]: “inducing a power converter to enter said power converter operational state; and”

As described for claims 1[b] and 6[a], *Hirst* discloses that the power converter receives a command from controller 18 to enter one of two power converter operational states: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. See EX1003, 7:66-8:5; see also *id.*, 3:17-24 (“Commands from a print engine controller *select a first switching frequency* for the power supply when the printer is in *a normal mode* of operation and *select a second switching frequency* for the power supply when the printer is in *a standby mode* of operation.”); see also Sections

IX.A.iii and IX.E.ii. *Hirst* thus discloses that controller 18, for example, induces a power converter to enter said power converter operational state. EX1002,¶114.

- v. **16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”**

The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Hirst* discloses claim 16[d] in the same manner described for claims 1[b]-[c]. *See* Sections IX.A.iii-iv; EX1002,¶115.

- vi. **16[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

Claim 16[e] is identical to claim 1[d] and is disclosed in the same manner described for claim 1[d]. *See* Section IX.A.v; EX1002,¶116.

O. Claim 17

Similar to the way claim 7 repeats the limitations of claim 6 but for “*another* load” and “*another* power converter” (and the associated states, signals, and command), claim 17 repeats the limitations of claim 16 but for “*another* load” and “*another* power converter” performing the same steps recited in claim 16. *See* EX1007, 2 (side-by-side comparison).

Thus, for the same reasons described for claims 7 and 16, the power system of *Hirst* including multiple power converters and loads respectively coupled thereto discloses each step recited in claim 17. *See* Sections IX.F and IX.N; EX1002,¶¶117-118.

P. Claim 18

Hirst discloses the additional elements of claim 18 in the same manner described for similar claim 10. *See* Section IX.I; EX1002,¶119.

Q. Claim 19

Hirst discloses the additional elements of claim 19 in the same manner described for similar claim 3. *See* Sections IX.C (claim 3), IX.N (claim 16); EX1002,¶120.

R. Claim 20

Hirst discloses the additional limitations of claim 20 in the same manner described for similar claim 5. *See* Section IX.D; EX1002,¶121.

X. GROUND 1B: *Hirst* Renders Obvious 1-3, 5-13, and 15-20

As described for Ground 1A, *Hirst* discloses each element of claims 1-3, 5-13, and 15-20. To the extent that PO argues that the disclosures of *Hirst* relied upon in Ground 1A represent separate embodiments, a POSITA would nonetheless have viewed them together as predictable variations of each other when considering the disclosure of *Hirst*. EX1002,¶¶122-123. For example, the disclosures of *Hirst* with reference to Figures 1, 2, 5, and 6, are all aspects of *Hirst*'s inventive concept. *See*

EX1003, 6:29-37 (describing ripple monitor 49 of Figure 2 as providing signal to controller 18 of Figure 1), 7:63-8:8 (relating “controller 18” in Figure 5 to Figure 1), 8:27-33 (relating “controller 18” in Figure 6 to Figure 1).

Accordingly, to the extent that PO argues Ground 1A relies upon separate embodiments of *Hirst*, a POSITA would have been capable and motivated to combine those embodiments. EX1002, ¶124. Therefore, the challenged claims would nonetheless be rendered obvious. *See Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) (holding that “[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness”). Indeed, as described in Ground 1A, *Hirst* discloses (and thus at least also suggests to a POSITA) each element recited in claims 1-3, 5-13, and 15-20. EX1002, ¶124.

A. Claims 2 and 11

As described in Section IX.B, *Hirst* discloses a power converter configured to transition between different switching-frequency states (i.e., power converter operational states). EX1003, 7:63-8:8. A POSITA would have found it obvious that the transition from one switching-frequency state to the other could be completed within a transition time, for example a time bound by the period of one cycle at the new switching frequency. EX1002, ¶125. Thus *Hirst* in view of the knowledge of a POSITA renders obvious claims 2 and 11.

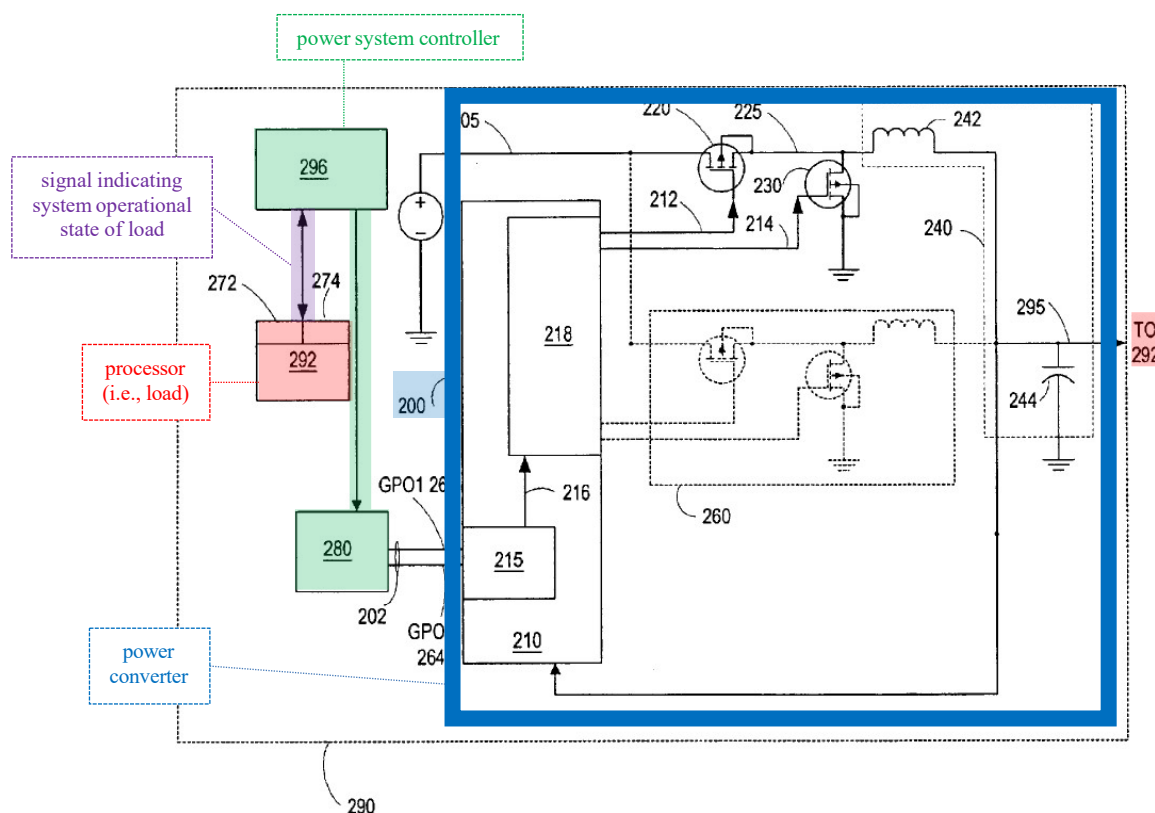
XI. GROUND 2A: Chagny Anticipates Claims 1-2, 4-6, 11, 14-16, and 20

A. Claim 1

- i. **1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

Chagny discloses a voltage regulator module (“VRM”) (i.e., a power converter). EX1004, Abstract; 3:54-56. As shown in Figure 2A, “the regulated DC voltage output 295 provides power to a processor 292.” EX1004, 3:56-58.

Processor 292 is thus a load coupled to VRM 200.



EX1004, Fig. 2A (annotated); EX1002, ¶127.

Chagny explains that the “loading, usage or activity level” of “processor 292” (i.e., the system operational state of the load) will “vary depending on the number of

instructions executed within a predefined time interval.” *Id.*, 4:18-20; *see also* 4:20-34 (describing activity levels). And as shown in Figure 2A, software program 296 receives a signal from processor 292 indicating the activity level (i.e., indicating the system operational state of the load). EX1004, 4:35-37 (“In one embodiment, a software program 296, which may be included in the operating system (not shown) of the device 290, monitors the processor 292 loading.”); EX1002, ¶128.

Based on the detected activity level, software program 296 generates and sends an “activity input 202” signal to controller 210 of VRM 200. EX1004, 4:40-43 (“Based on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292.”). And as shown in Figure 2A, the “activity input 202” signal may be sent to VRM 200 via I/O controller hub (ICH) 280. *Id.*, Fig. 2A, 4:46-61 (describing bits stored in I/O controller hub 280). Accordingly, *Chagny*’s software program 296,² either alone or collectively with I/O controller hub (ICH) 280, serves as the power system controller³⁴ recited in claim 1[pre].

² The ’759 Patent includes embodiments where “the power system controller” is constructed as an element of a server (i.e., the load). EX1001, 20:58-61, 18:24-33, Fig. 11.

³ As an alternative mapping, the I/O controller hub (ICH) 280 alone may also serve as the “power system controller” of claim 1[pre]. In this mapping, the signal shown in

Thus, *Chagny* discloses claim 1[pre]. EX1002, ¶¶127-130.

- ii. **1[a]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and”**

The switches 220 and 230, inductance 242, and capacitor 244, are configured in what is known as a “buck” topology. *See* EX1004 (*Chagny*), 1:51-59 (describing “buck” DC-DC converter); EX1001 (’759 Patent), Fig. 2, 8:57-9:18 (describing “buck” converter); EX1002, ¶131. *Chagny*’s charge switch 220 serves as the “power switch” recited in claim 1[a]. EX1002, ¶131.

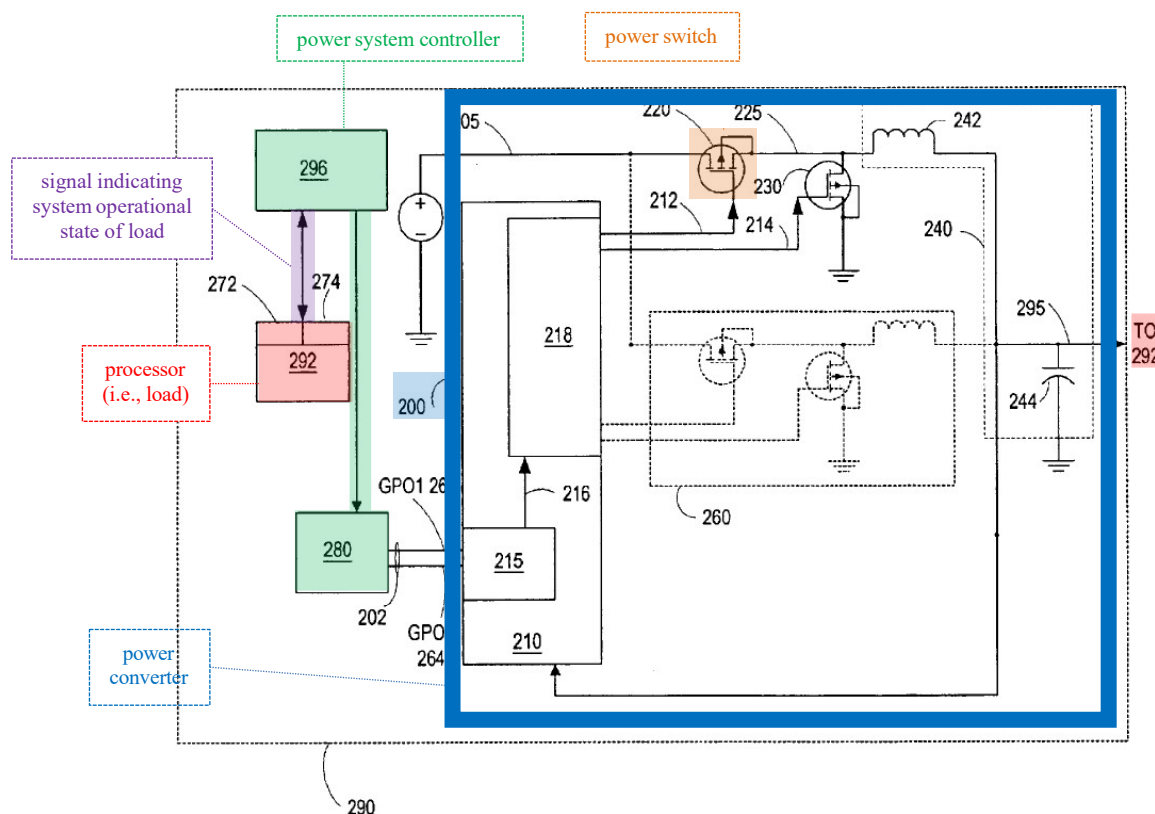


Figure 2A from software program 296 to I/O controller hub (ICH) 280 serves as the signal indicating a system operational state of the load. EX1002, ¶129.

EX1004, Fig. 2A (annotated); EX1002, ¶132.

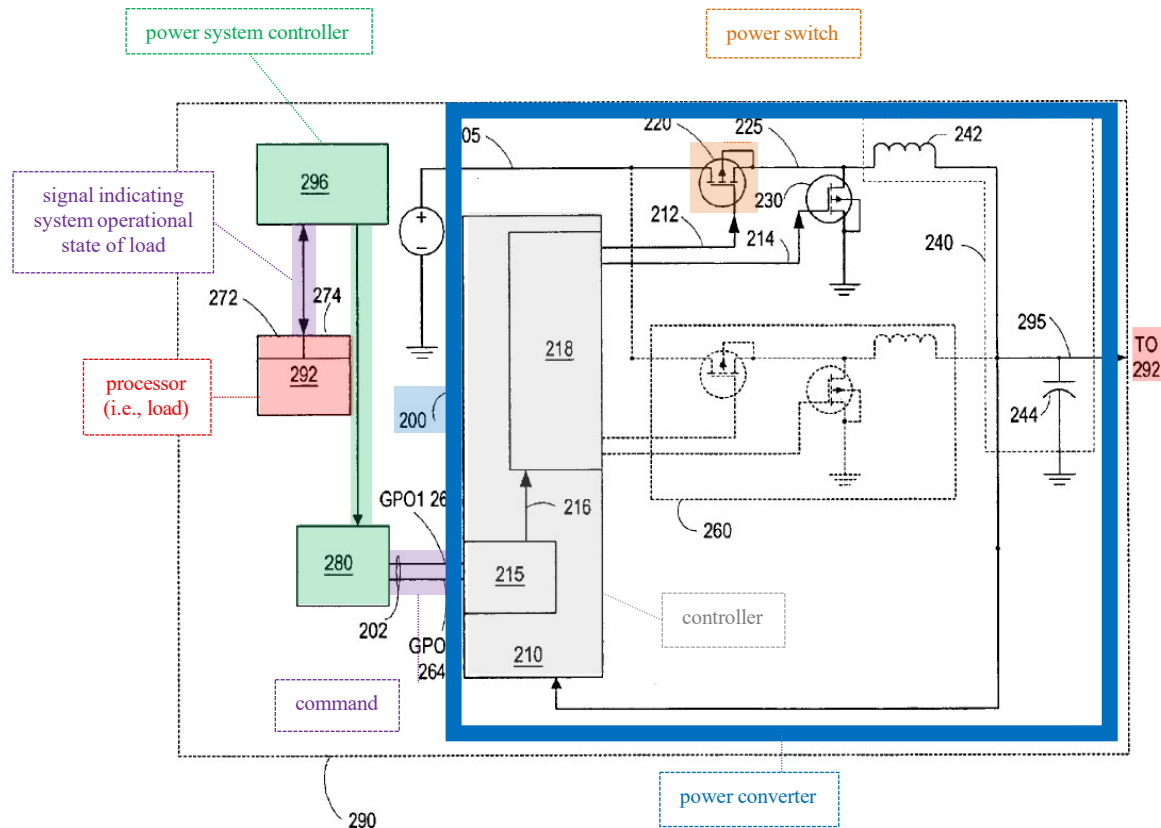
It was well-known that, in the baseline equation for a buck power converter, the output voltage is equal to the input voltage times the duty cycle of the high-side switch (referred to as charge switch 200 in *Chagny*), where the duty cycle is the ratio of the on-time (i.e., conduction-time) of the high-side switch to the overall switching period. EX1002, ¶¶133-134; EX1009, 19 (deriving equation for buck). Consistent with this understanding, *Chagny* describes how charge switch 220 (i.e., the power switch) and discharge switch 230 turn on and off in an alternating fashion from each other. EX1004, 5:34-40, 6:45-49; EX1002, ¶135. A square wave that alternates between the DC voltage input 205 and ground is generated at node 225. EX1004, 5:40-42 (“The DC voltage input 225 is ‘chopped’ by the charge switch 220 to generate the switched DC voltage output 225.”); EX1002, ¶135. The square wave at node 225 therefore has an average voltage over time that is equal to the input voltage 205 times the duty cycle of the charge switch 220. EX1002, ¶135. The square wave at node 225 is filtered by inductance 242 and capacitor 244 to provide a regulated output voltage based on the average value of the square wave (i.e., based on the duty cycle of charge switch 220). See EX1004, Fig. 2A, 5:44-46 (“The square wave ... has an average voltage equal to the required output voltage.”); 5:47-51, (“The filter module 240 filters the switching frequency 216 from the switched DC voltage output 225 and generates the regulated DC voltage output 295.”); 4:63-65 (“The controller

module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200.”); EX1002,¶136.

Accordingly, based on *Chagny*’s disclosure, a POSITA would understand that “charge switch 220” (i.e., the power switch) is configured to conduct for a duty cycle to provide “regulated DC voltage output 295” (i.e., a regulated output characteristic) at the output of VRM 200 (i.e., at the output of the power converter). *Chagny* thus discloses claim 1[a]. EX1002,¶¶131-137.

- iii. **1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”**

Chagny’s VRM 200 includes a “controller module 210” (i.e., a controller), configured to receive “activity input 202” (i.e., a command) from the power system controller identified in Section XI.A.i for claim 1[pre]. EX1004, 4:62-67 (“The controller module 210 includes a frequency selector module 215,” which “is operable to receive the activity input 202 ...”).



EX1004, Fig. 2A (annotated); EX1002, ¶138.

As described for claim 1[pre], activity input 202 is generated by *Chagny*'s power system controller as a function of the signal indicating the “activity level” (i.e., the system operational state) of processor 292. *See* Section XI.A.i. In turn, *Chagny*'s controller 210 selects different switching frequency states (i.e., power converter operational states)⁵ based on activity input 202. EX1004, 5:9-12 (“[T]he controller module 210 dynamically changes the switching frequency 216 of the

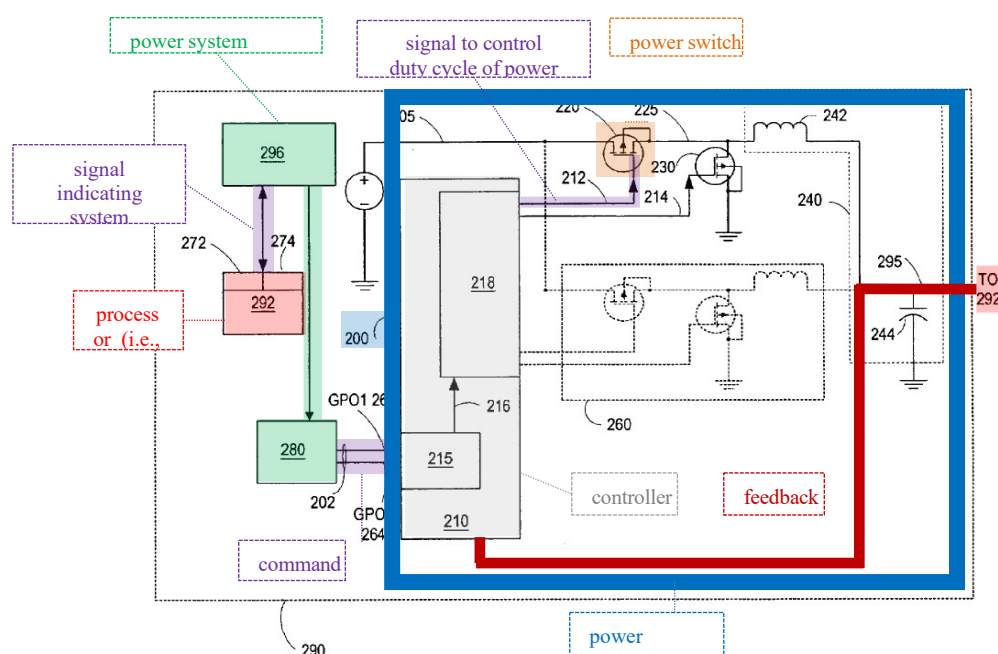
⁵ The '759 Patent lists “reduced switching frequency” as an example among “power converter operational state” descriptions. *See* EX1001, Col. 19, Table I.

VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.”); *see also id.*, 4:66-5:3 (selecting switching frequency based on processor activity level), 5:3-8 and 5:12-18 (listing example processor activity levels and corresponding VRM switching frequencies), 4:46-49.

Chagny thus discloses claim 1[b]. EX1002, ¶¶138-140.

- iv. 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”

Chagny’s controller module 210 (i.e., said controller) includes “FET driver module 218.” EX1004, 4:62-63; *see also id.*, 3:60-4:7. As shown in Figure 2A, FET driver module 218 provides “charge control signal 212” to control charge switch 220 (i.e., said power switch). *Id.*, 5:38-40.



EX1004, Fig. 2A (annotated); EX1002, ¶142.

As described for claim 1[a], the duty cycle of charge switch 220 (i.e., the power switch) determines the voltage level of *Chagny*'s "regulated DC voltage output 295." *See* Section XI.A.ii. And as shown in Figure 2A, "controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200." EX1004, 4:63-65; *see also id.*, 9:5-7, 10:14-16. Because it is the duty cycle of charge switch 220 that determines the output voltage, and because *Chagny* explicitly states that controller module 210 regulates the DC output voltage as a function of the feedback, a POSITA would have understood *Chagny* to disclose that controller module 210 is configured to control the duty cycle of charge switch 220 as a function of the feedback from the regulated DC voltage output 295 (i.e., as function of said output characteristic). EX1002, ¶143; EX1009, 17-18 (describing known duty cycle control as function of feedback from the output voltage).

In addition, "FET drive module 218" controls charge switch 220 in accordance with "activity input 202 (i.e., the command). *See* EX1004, 5:28-31 ("The FET driver module 218 is operable to receive the selected value of the switching frequency 216 and generate the charge and discharge control signals 212 and 214, each having the switching frequency 216."); *see also id.*, 4:66-5:2, 5:34-46.

Chagny thus discloses claim 1[c]. EX1002, ¶¶141-145.

- v. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

Chagny’s controller module 210 “dynamically changes the switching frequency 216” (i.e., regulates an internal operating characteristic) of VRM 200 in response to the activity input 202 indicative of the activity level of processor 292. EX1004, 5:9-12; *see also id.*, 4:41-43, 5:3-8, 5:12-18. *Chagny* expressly describes how the switching frequency of the VRM (i.e., the internal operating characteristic of said power converter) is varied to “improve efficiency” as a function of the processor activity level (i.e., said system operational state). EX1004, 2:59-61 (“To improve efficiency, the VRM advantageously changes the switching frequency of the VRM in accordance with the activity of the processor.”); *see also id.*, 5:16-23 (describing selection of low switching frequency when “activity of processor is low” to “save power” and improve “VRM 200 efficiency”); 3:9-10.

Chagny thus discloses claim 1[d]. EX1002, ¶¶146-148.

B. Claim 2

- i. **“2. The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

As described for claim 1[b] in Section XI.A.iii, *Chagny*’s power converter is configured to dynamically change between different switching-frequency states (i.e., power converter operational states) as a function of the activity level of the

processor. EX1004, 4:66-5:18. *Chagny* discloses that in some embodiments, the “the demand for power required by the processor 292 is advantageously controlled by limiting the number of instructions executed for *a predefined time period*. This control mechanism ensures that the VRM 200 *reacts responsively and on time according to the processor 292 demand*.” *Id.*, 5:62-66 (emphasis added). In other words, *Chagny* sets a “predefined period of time,” within which VRM 200 transitions from one switching-frequency state to another, before changing the activity level of processor 292. *Id.* *Chagny* thus discloses claim 2. EX1002, ¶¶150-153.

C. Claim 4

- i. **“4. The power converter as recited in claim 1 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

The '759 Patent background explains that a “core state” is “under software operating system control” and relates to “various levels of a processor sleep state,” achieved by “halting instruction execution” among other items. EX1001, 4:23-39; EX1002, ¶154.

Chagny discloses that “software program 296 generates the activity input 202 indicative of levels of activity of the processor 292,” (i.e., the load) which “includes 2 bits ... GPO1 262 and GPO2 264 . . . used to define up to 4 activity levels of the processor 292.” EX1004, 4:43-49; *see also id.*, 4:23-30 (defining high, medium, and

low activity level based on the processing loading). Moreover, “software program 296 defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clock cycle.” *Id.*, 5:57-61; *see also id.*, 6:3-4. Accordingly, the activity level of processor 292 (i.e., system operational state of the load) at any of *Chagny*’s activity levels (e.g., low, medium, high) is dependent on at least a core state of processor 292. *Chagny* thus discloses claim 4. EX1002, ¶¶155-157.

D. Claim 5

The ’759 Patent describes a “Fully Operational” power converter operational state as “[a]ll power converter components operational at full performance level,” as opposed to other states with “reduced switching frequency.” EX1001, Table I, 19:20-36.

Chagny discloses a power converter operational state wherein “the switching frequency 216 is selected to be high 150 to advantageously limit the voltage ripples” EX1004, 5:9-18; *see also id.*, 5:5-8 and 5:23-26 (describing low, medium, and high switching frequency states). The highest switching-frequency state of *Chagny*’s VRM 200 represents a power converter state where all power converter components operate at full performance level (i.e., a fully operational power converter). EX1002, ¶¶159-160.

Chagny thus discloses claim 5. EX1002, ¶¶158-161.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

Later elements of claim 6 require the “power system” of claim 6[pre] to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Chagny* discloses claim 6[pre] in the same manner described for claim 1[pre]. See Section XI.A.i; EX1002, ¶162.

ii. 6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”

As described for claim 1[pre], *Chagny* discloses a power system controller configured to receive a signal indicating a system operational state of a load. See Section XI.A.i. And as described for 1[b], the power system controller of *Chagny* sends a command to the power converter controller to enter a power converter operational state as a function of said signal. *Chagny* thus discloses a power system controller configured to “select” a power converter operational state as a function of the signal in the same manner described for claim 1[b]. See Section XI.A.iii. *Chagny* thus discloses claim 6[a]. EX1002, ¶163.

iii. 6[b]: “a power converter, including:”

As described for claim 1[pre], *Chagny* discloses a power converter. See Section XI.A.i; EX1002, ¶164.

iv. 6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”

Claim 6[c] is identical to claim 1[a] and is disclosed in the manner described for claim 1[a]. *See* Section XI.A.ii; EX1002,¶165.

- v. **6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

Claim 6[d] restates limitations of claim 1[b]-[c] and is disclosed in the manner described for claim 1[b]-[c]. *See* Sections XI.A.iii-iv; EX1002,¶¶166-167.

- vi. **6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

Claim 6[e] is identical to claim 1[d] and is disclosed in the manner described for claim 1[d]. *See* Section XI.A.v; EX1002,¶168.

F. Claims 11, 14, 15

Claims 11, 14, and 15 mirror claims 2, 4, and 5 respectively and are thus disclosed in same manner described in Sections XI.B (claim 2), XI.C (claim 4), and XI.D (claim 5). EX1002,¶¶169-171.

G. Claim 16

- i. **16[pre]: “A method of operating a power system coupled to a load, comprising:”**

Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Chagny* thus discloses claim 16[pre] in the same manner described for claim 6 (and similar elements of claim 1). *See* Sections XI.A.i and XI.E.i;

EX1002,¶172; *see also* EX1004, 2:40-43 (“the present disclosure [] relates to a system and method for improving the efficiency of a VRM”).

ii. 16[a]: “receiving a signal indicating a system operational state of said load;”

As described for claims 1[pre] and 6[a], *Chagny* discloses a power system controller that receives a signal indicating a system operational state of a load. Thus, for the same reasons described in Sections XI.A.i (1[pre]) and XI.E.ii (6[a]), *Chagny* discloses method step 16[a]. EX1002,¶173.

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

As described for claims 1[pre] and 1[b], *Chagny* discloses that a switching-frequency state (i.e., a power converter operational state) is generated as a function of the activity level of the processor (i.e., as a function of the system operational state). *See* Sections XI.A.i and XI.A.iii; *see also* EX1004, 4:40-43 (“Based on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292.”), 4:66-5:3 (“The frequency selector module 215 is operable to ... select a switching frequency 216 ... which dynamically matches the level of activity of the processor 292.”), 5:5-12 (disclosing switching frequencies states selected as function of the processor activity level).

Thus, *Chagny* discloses claim 16[b]. EX1002,¶¶174-175.

iv. 16[c]: “inducing a power converter to enter said power

converter operational state; and”

As described for claim 1[b], *Chagny* discloses that VRM 200 enters different switching-frequency states (i.e., power converter operational states) based on activity input 202. *See* Section XI.A.iii. The activity input 202 therefore induces VRM 200 to enter the power converter operational state. EX1004, 5:9-12 (the controller “dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292.”), 5:12-18, 4:46-49. *Chagny* thus discloses claim 16[c]. EX1002, ¶176.

- v. **16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”**

The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Chagny* discloses claim 16[d] in the same manner described for claims 1[b]-[c]. *See* Sections XI.A.iii-iv; EX1002, ¶177.

- vi. **16[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

Claim 16[e] is identical to claim 1[d], and is thus disclosed by *Chagny* in the same manner described for claim 1[d]. *See* Section XI.A.v; EX1002,¶178.

H. Claim 20

Chagny discloses the additional elements of claim 20 in the same manner described for claim 5. *See* Section XI.D; EX1002,¶179.

XII. GROUND 2B: *Chagny* in View of the Knowledge of a POSITA Renders Obvious Claims 1-2, 4-6, 11, 14-16, and 20

As described in Ground 2A, *Chagny* discloses a software program 296 that serves (alone or collectively with I/O controller hub (ICH) 280) as the “power system controller” recited in the claims. *See, e.g.*, Section XI.A.i (1[pre]), XI.A.iii (1[b]). To the extent PO argues that the power system controller must be implemented in hardware, a POSITA would have found it obvious to execute *Chagny*’s “software program 296,” which may be “included in the operating system” of the device (EX1004, 4:35-40), on hardware such as processor 292⁶ or alternatively a separate hardware controller. EX1002,¶180. For example, “software program 296” analyzes

⁶ The ’759 Patent includes embodiments where “the power system controller” is constructed as an element of a server (i.e., the load). EX1001, 20:58-61, 18:24-33, Fig. 11.

“the processor instruction pipeline stack” (EX1004, 4:30-35), and sets “bits in a register of processor 292” to control the number of instructions executed per cycle by the processor (*id.*, 5:57-61). Moreover, *Chagny* describes that a “processor” is “operable to execute the computing instructions,” which are “also known as a ‘software program,’” stored in memory. *Id.*, 7:36-41; *see also* EX1002, ¶180-182; EX1015, 5, 10-11.

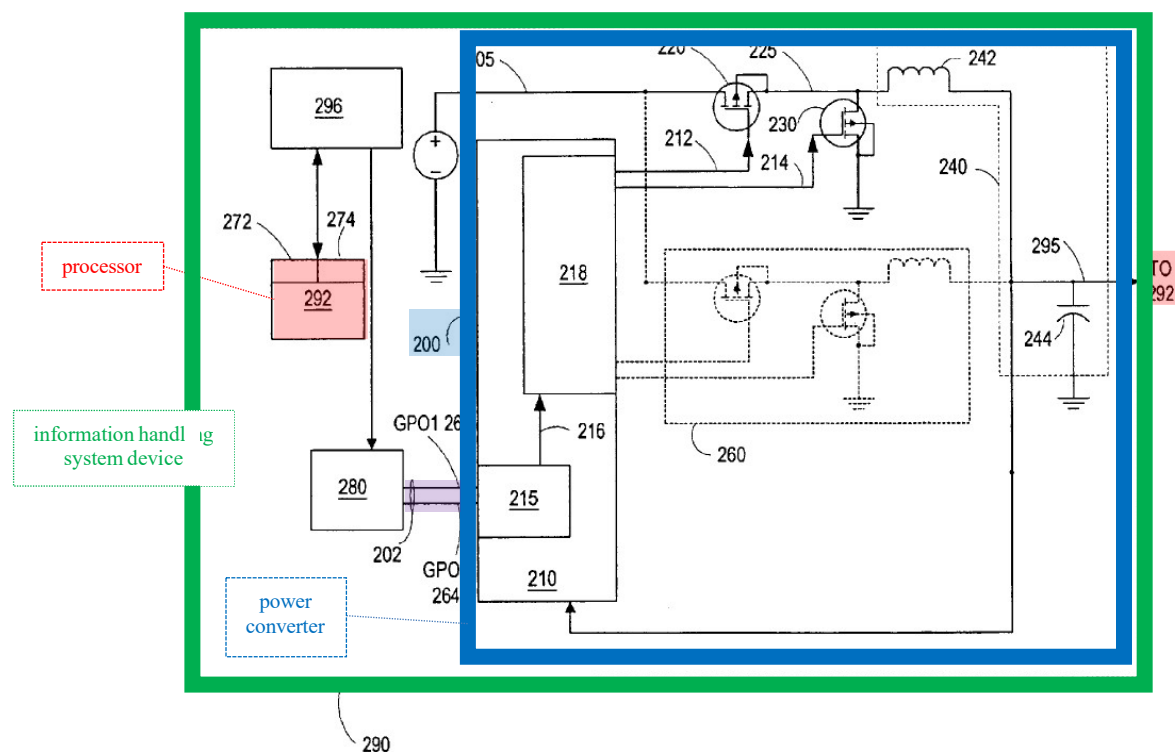
Accordingly, claims 1-2, 4-6, 11, 14-16, and 20 are also rendered obvious by *Chagny* in view of the knowledge of a POSITA. EX1002, ¶183.

XIII. GROUND 2C: The Combination of *Chagny* and *Clark* Renders Obvious Claims 3, 12-13, and 19

As described above in Ground 2A, *Chagny* discloses each element of independent claims 1, 6, and 16. *See* Sections XI.A (claim 1), XI.E (claim 6), XI.G (claim 16). When further combined with *Clark*, the resulting combination further discloses and/or suggests to a POSITA each element of dependent claims 3, 12-13, and 19, and therefore renders those claims obvious. EX1002, ¶184.

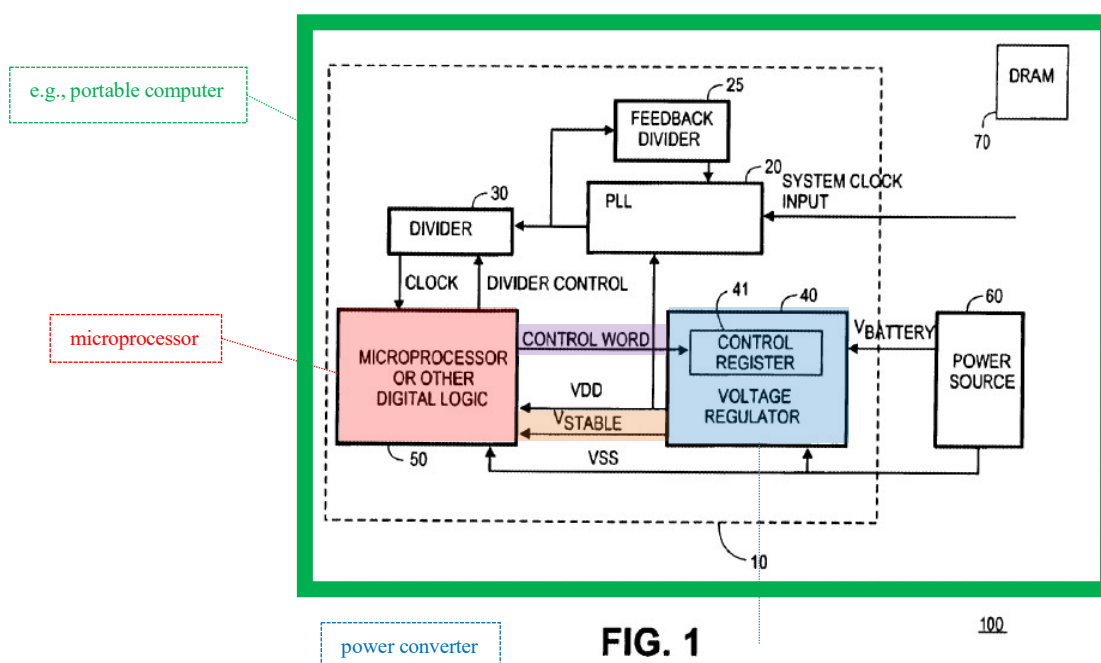
A. Motivation to Combine

Chagny discloses an “information handling system device 290” that includes a processor 292 and a voltage regulator module (VRM) 200 for providing a regulated voltage to the processor 292.



EX1004, Fig. 2A (annotated); EX1002, ¶185. As described above for Ground 2A, *Chagny* describes changing the frequency of VRM 200 (i.e., power converter) to “improve efficiency” of the power converter when the activity of the processor is low. EX1004, 2:59-61; *see also id.*, 5:16-23.

Like *Chagny*, *Clark* discloses a device (e.g., portable computer) that includes both a microprocessor (also referred to as “core logic 50”) and a voltage regulator 40 (i.e., a power converter) for providing a regulated voltage to the microprocessor. EX1005, 3:9-20, 3:31-33.



EX1005, Fig. 1 (annotated); EX1002, ¶186. *Clark* discloses that by reducing the clock frequency of the microprocessor, as well as reducing the voltage provided by the voltage regulator to the microprocessor, the power consumed by the microprocessor during light processing loads is “dramatically reduced.” *See id.*, 5:14-23; *see also id.*, 4:54-67, 3:44-60, Figs. 5 (illustrating different processing levels), Fig. 6 (illustrating power savings); EX1002, ¶187.

A POSITA would have been motivated to combine the information handling system device 290 of *Chagny* with the teachings of *Clark*. The underlying goal behind *Chagny*’s efficient power converter is to “extend the battery life” of the system. EX1004, Title. *Clark* furthers that goal by also improving the efficiency of the microprocessor. EX1005, 4:54-67, 5:14-23; EX1002, ¶188.

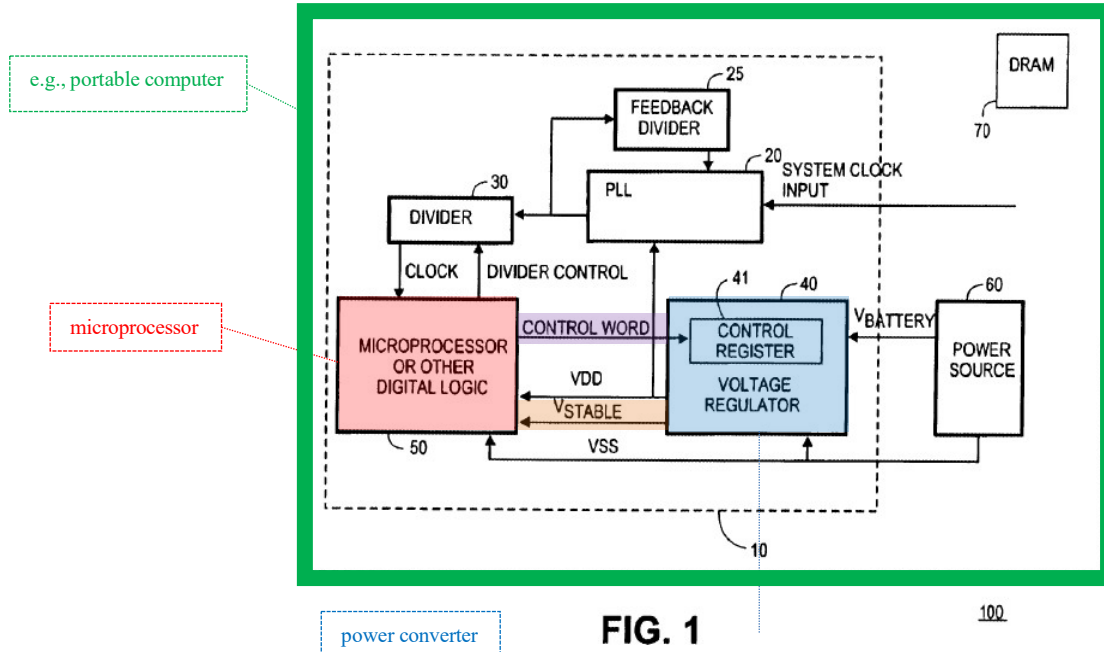
Therefore, with respect to *Chagny*'s power converter, a POSITA would have been motivated to incorporate *Clark*'s control of the power converter output voltage based on the processor activity level with *Chagny*'s control over the power converter switching frequency based on the processor activity level. For example, a POSITA would have been motivated to modify *Chagny*'s system to further include the control functions of *Clark* along with the "control word" and "Vstable" signals that *Clark* uses to communicate between the microprocessor and the power converter. *See* EX1005, 3:44-60, 5:24-36; EX1002, ¶189. Such a combination represents the use of a known technique (i.e., *Clark*'s dynamic control of the power converter output voltage) to improve a similar device (i.e., *Chagny*'s information handling system and voltage regulator module) in the same way. *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1740 (2007); EX1002, ¶190. Moreover, a POSITA would have a reasonable expectation of success because like the "control word" sent from *Clark*'s microprocessor to its power converter to control the output voltage based on processor loading (EX1005, 3:44-60, Fig. 1), *Chagny* is already configured to send control signals to its power converter based on the activity level of its processor (EX1004, 4:40-43, 5:9-12, Fig. 2A); EX1002, ¶190.

B. Claim 3

As described in Section XIII.A, a POSITA would have been motivated to incorporate *Clark*'s control over the power converter output voltage based on the

processor activity level with *Chagny*'s VRM 200, which already includes control over the power converter switching frequency based on the processor activity level. EX1002, ¶191. Given that both types of control are based on the processor activity level, a POSITA would understand that, in the combination of *Chagny* and *Clark*, the commands to *Chagny*'s VRM 200 for updating the switching frequency would coincide with the commands to update the output voltage. *Id.*

Clark discloses that a “Vstable” signal (i.e., a status signal) is sent from its power converter (referred to in *Clark* as a voltage regulator) back to the microprocessor to indicate whether a transition from one voltage to another has been completed. EX1005, 5:24-36.



EX1005, Fig. 1 (annotated); EX1002, ¶192. According to *Clark*, the microprocessor (also referred to as “core logic”) “may wait until the Vstable signal is asserted”

before instructing the power converter to further increase the output voltage to a new value. EX1005, 5:24-36, Fig. 2. In other words, *Clark* teaches waiting for the Vstable signal (i.e., the status signal) from the power converter to indicate that one transition is complete before making another transition. EX1002,¶193. And because the commands to *Chagny*'s VRM 200 for updating the switching frequency would coincide with the commands for updating the output voltage, a POSITA would understand that the commands to update the switching frequency state (i.e., the power converter operational state) would also be held until the Vstable signal (i.e., the status signal) indicated that prior transitions were complete. EX1002,¶194.

The combination of *Chagny* and *Clark* thus renders obvious the additional limitations of dependent claim 3. EX1002,¶¶191-195.

C. Claim 12

The combination of *Chagny* and *Clark* renders obvious the additional elements of claim 12 in the same manner described for similar claim 3. *See* Section XIII.B; EX1002,¶196.

D. Claim 13

- i. **“13. The power system as recited in claim 12 wherein said power converter status is selected from the group consisting of: a fully operational status, a failure likely status, a failed status, and an overloaded status.”**

As described above for claim 3, *Clark* discloses that the Vstable signal (i.e., the status signal) is used to determine whether the power converter (referred to as a

“voltage regulator” in *Clark*) is “changing,” or is instead “stable” (i.e., fully operational). EX1005, 5:27-36; *see also* Section XIII.B. The combination of *Chagny* and *Clark* thus renders obvious claim 13. EX1002, ¶197.

E. Claim 19

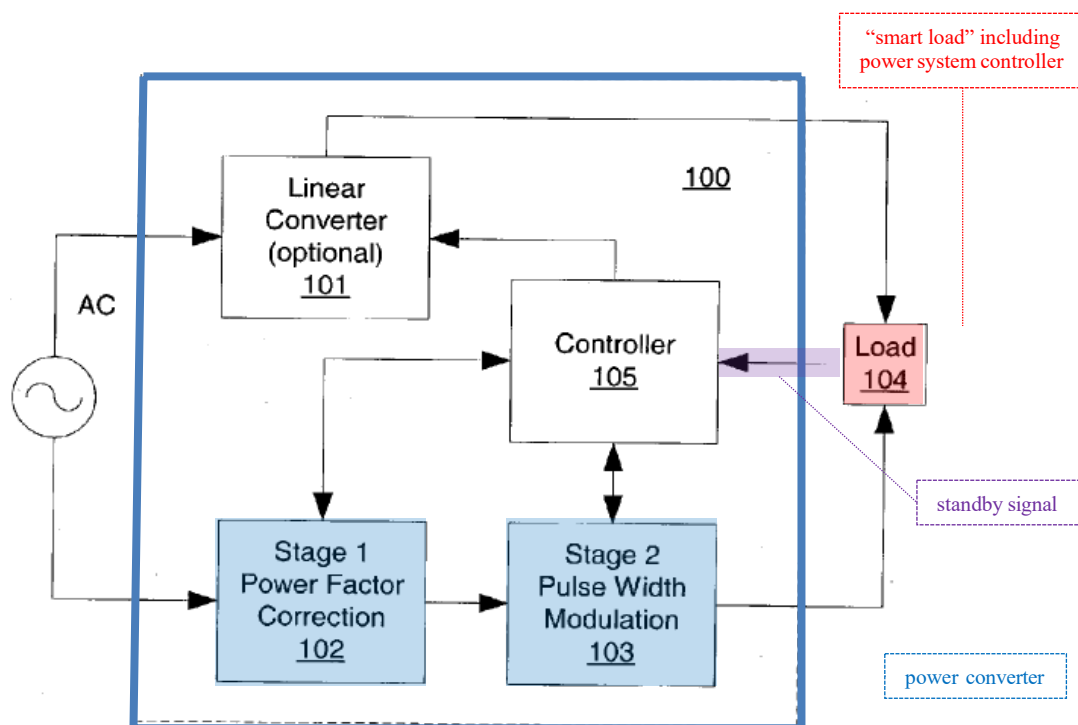
The combination of *Chagny* and *Clark* renders obvious the additional elements of claim 19 in the same manner described for similar claim 3. *See* Section XIII.B; EX1002, ¶198.

XIV. GROUND 3: Hwang in View of the Knowledge of a POSITA Renders Obvious Claims 1-2, 4-6, 11, 14-16, and 20

A. Claim 1

- i. **1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

Hwang discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006]. Like Figure 3 of the ’759 Patent (EX1001, Fig. 3), *Hwang*’s power converter is a “two-stage power converter” with a “power factor correction (PFC) stage 102” and a “PWM stage 103” (EX1006, [0019]).



EX1006, Fig 1 (annotated); EX1002, ¶200.

As shown in Figure 1, *Hwang's* power converter 100 is coupled to a smart load 104. EX1006, Fig. 1, [0031] (describing load 104 as “smart load”), [0038]. *Hwang* discloses that smart load 104 “may include a microprocessor that may enter a standby mode during periods of low activity or non-use.” *Id.*, [0031]; *see also id.*, [0021] (“where the load 104 is a microprocessor or controller, it may enter a standby or ‘sleep’ mode during periods of low activity”); EX1002, ¶201. *Hwang* also discloses that smart load 104 sends a “standby signal” to controller 105 within power converter 100. *Id.*, [0021], [0031].

Based on *Hwang's* disclosure of a smart load 104 including a “microprocessor” that enters standby mode during periods of low activity (*id.*,

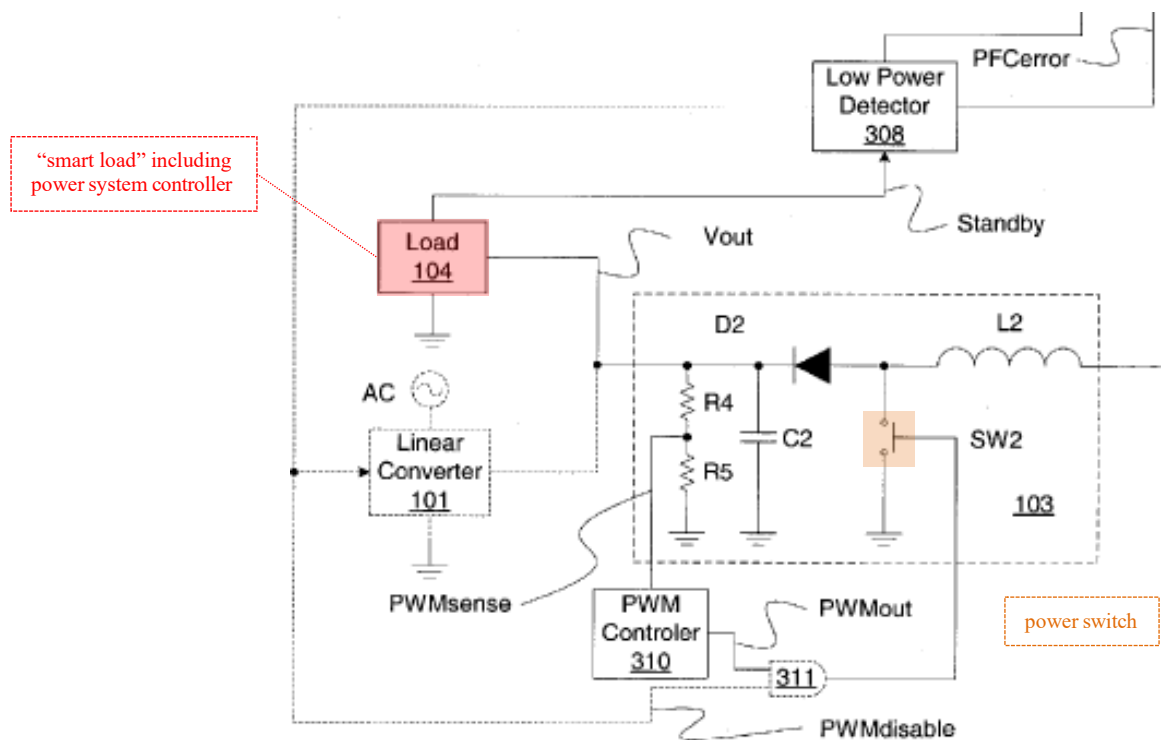
[0031], [0021]), and based on a POSITA's understanding of well-established principles of microprocessor operation, a POSITA would have understood, or at least found it obvious, that the microprocessor within smart load 104 could include an internal control unit that controls the internal operations of the microprocessor. EX1002, ¶202. A POSITA would have further understood that such an internal control unit would serve as the "power system controller" recited in claim 1[pre] by receiving a signal indicative of the microprocessor's activity level (i.e., indicative of the system operational state of the microprocessor load).⁴ EX1002, ¶¶202-203; EX1015, 5-6. Indeed, a POSITA would have found it obvious that such an internal control unit (i.e., the power system controller) would be included to in turn send a "standby signal" to the power converter as expressly disclosed by *Hwang*. EX1006, [0021], [0031]; EX1002, ¶202-203.

Accordingly, *Hwang* in view of the knowledge of a POSITA discloses and suggests claim 1[pre]. EX1002, ¶¶200-204.

- ii. **1[a]: "a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and"**

⁴ An architecture with a power system controller built into a microprocessor load is similar to those described in the '759 Patent where the "power system controller" may be included as "an element" of a "server" (i.e., the load) EX1001, 20:58-61, 18:24-33, Fig. 11; EX1002, ¶202.

As shown in Figure 3, the PWM stage 103 from Figure 1 includes “switch SW2” (i.e., the power switch). EX1006, [0029].



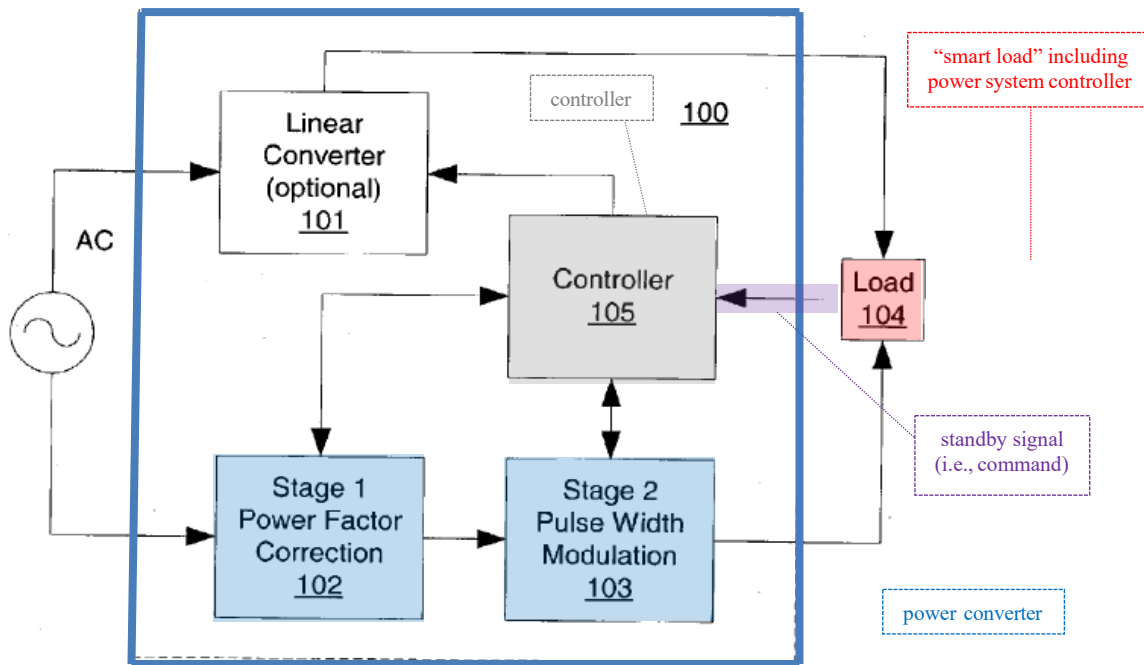
EX1006, Fig. 3 (excerpt) (annotated); EX1002, ¶205. As *Hwang* describes, a PWM controller in a switching power converter adjusts the “duty cycle” of the PWM signal controlling the switch “to regulate the output voltage” (i.e., to provide a regulated output characteristic). EX1006, [0003]. And with respect to Figure 3, *Hwang* states: “The PWM controller 310 may cause the switch SW2 [i.e., the power switch] to be switched on and off in an attempt to cause the output voltage Vout to remain substantially constant.” *Id.*, [0030]; *see also id.*, [0034] and [0036] (both referencing duty cycle), Figs. 7A-7D.

Hwang thus discloses claim 1[a]. EX1002, ¶¶205-208.

- iii. 1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”

Hwang's power converter 100 includes “controller 105” (i.e., a controller).

EX1006, [0019].



EX1006, Fig 1 (annotated); EX1002, ¶209.

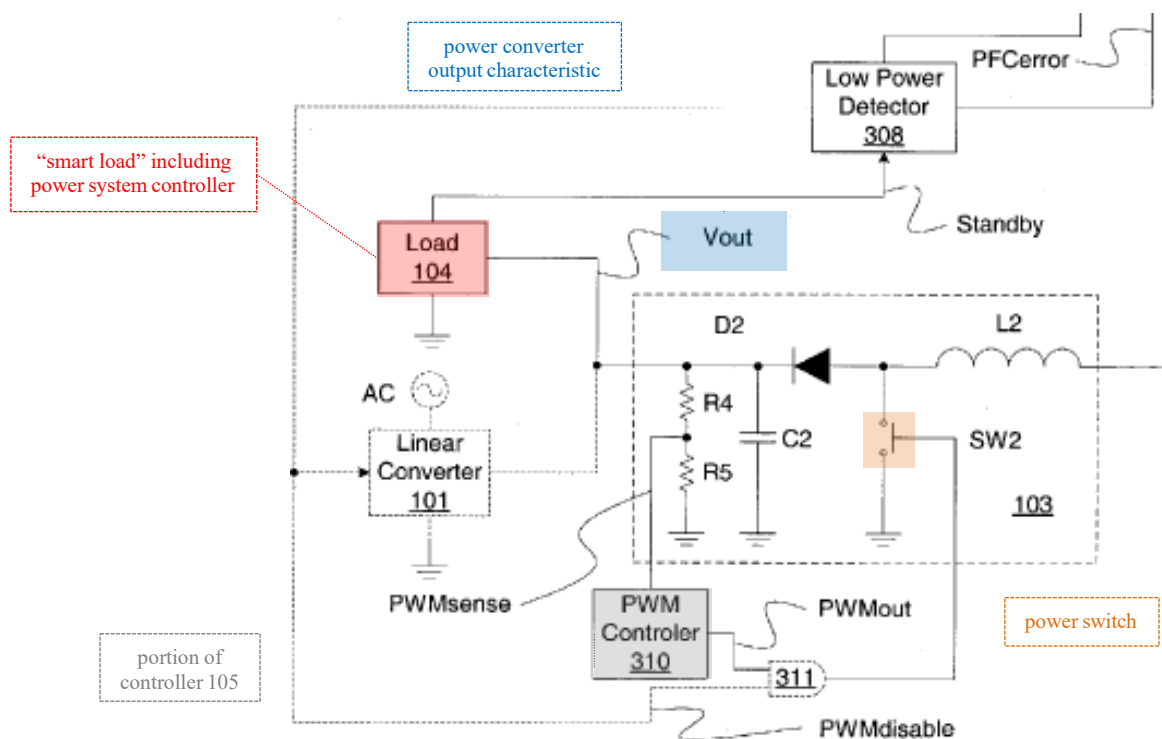
As described for claim 1[pre], controller 105 receives a “standby signal” (i.e., a command) from a power system controller within smart load 104 that is a function of the signal within smart load 104 indicating the activity level (i.e., the system operational state) of the microprocessor within smart load 104. *See* Section XIV.A.i; EX1006, [0021], [0031]. *Hwang* then explains that the “standby signal” instructs controller 105 to enter a “standby mode” (i.e., a power converter operational state)

and thereby “disable the PFC stage 102” and “cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]; *see also* [0031], Fig. 2.

Hwang thus discloses claim 1[b]. EX1002, ¶¶209-212.

- iv. 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”

Controller 105 shown in Figure 1 of *Hwang* includes PWM controller 310 shown in Figure 3. EX1006, [0026].

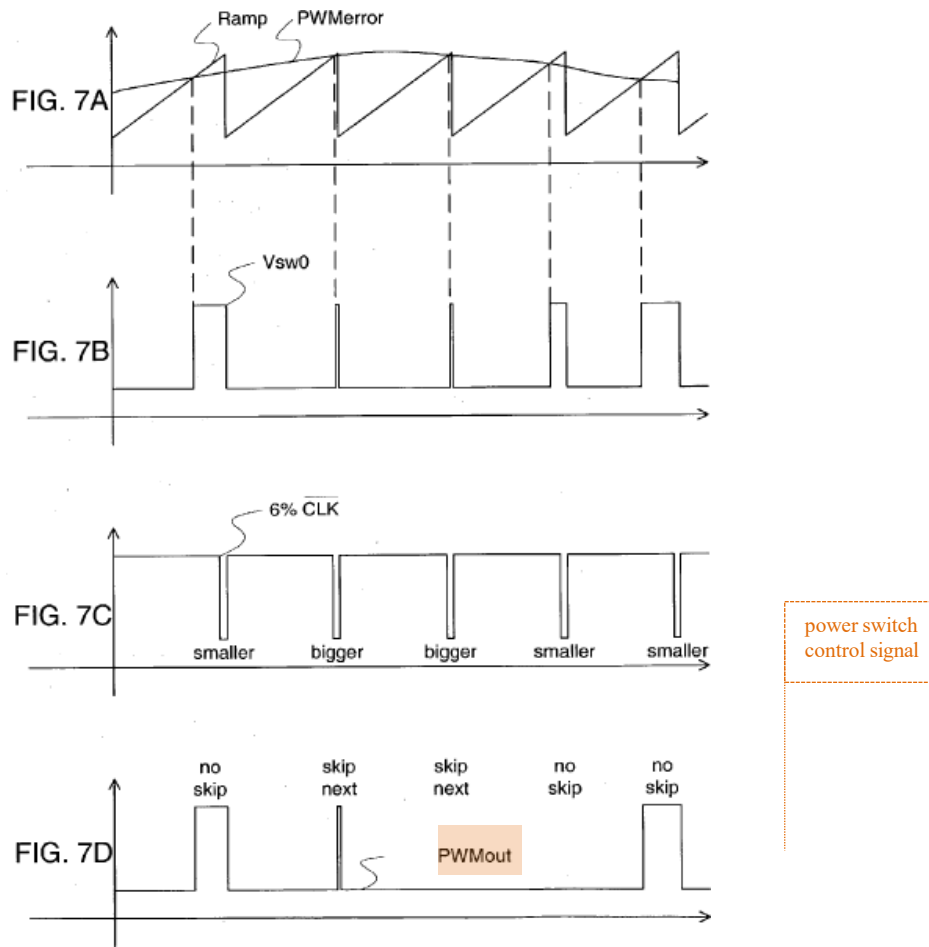


EX1006, Fig. 3 (excerpt) (annotated); EX1002, ¶213.

As shown in Figure 3, PWM controller 310 receives a feedback signal representative of the output voltage (i.e., an output characteristic) of the converter.

Id., Fig. 3, [0030] (“signal PWMsense, representative of the output voltage Vout ... may be coupled into the PWM controller 310”). As described for claim 1[a], the PWM controller controls the duty cycle of switch SW2 (i.e., the power switch) to regulate the output voltage as a function of the feedback to regulate the output voltage. EX1006, [0003] (describing “adjusting the duty cycle” as a function of “measured output voltage”), [0030]; *see also* Section XIV.A.ii; EX1002, ¶¶214-215. *Hwang* thus discloses controlling the duty cycle as a function of Vout (i.e., the output characteristic).

Hwang also discloses that the duty cycle of the power switch is controlled in accordance with the “standby signal” (i.e., the command) from the power system controller. Although Figure 3 shows that PWM stage 103 may be disabled by a PWMdisable signal feeding AND gate 311 (EX1006, Fig. 3), *Hwang* explicitly discloses that, during standby mode, controller 105 may either (i) “disable the PWM stage,” or (ii) “cause PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021]). And as shown in Figures 7A-7D, during pulse-skipping mode, a switching cycle of the PWM stage is skipped (i.e., the duty cycle forced to zero) if the duty cycle of the previous switching cycle was less than a given threshold. *Id.*, [0036], [0041]-[0042] (describing pulse-skipping operation).



EX1006, FIG. 7A-D (annotated); EX1002, ¶¶216-217. Thus, the power switch is also controlled in accordance with the standby signal (i.e., the command) placing PWM stage 103 into pulse-skipping mode.

Hwang thus discloses claim 1[c]. EX1002, ¶¶213-218.

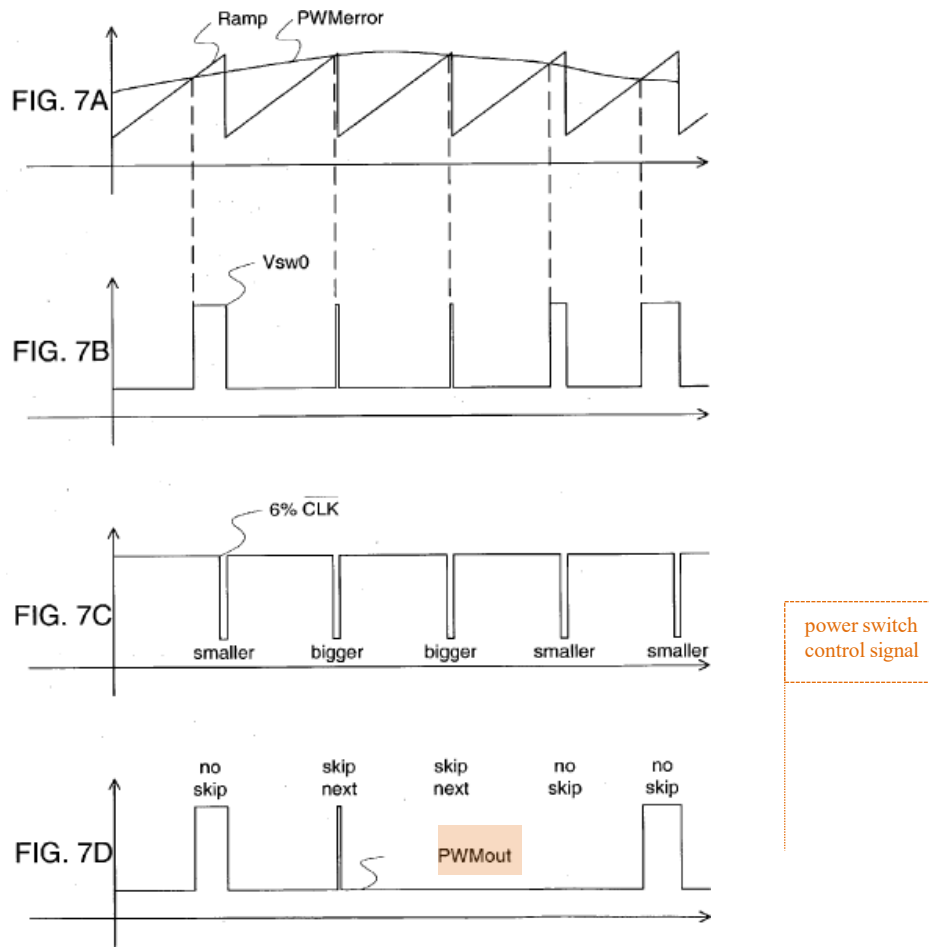
- v. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

As described for claim 1[pre] and 1[b], controller 105 places the power converter in standby mode as a function of a standby signal (i.e., the command) from

a power system controller within smart load 104 that is a function of activity level (i.e., the system operational state) of the microprocessor within smart load 104. *See* Sections XIV.A.i and XIV.A.iii; EX1006, [0021], [0031].

“While in standby mode, the controller 105 may disable the PFC stage 102” and “may cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]. The ’759 Patent lists the “disabling of ... power factor correction,” as well as “switching frequency,” among example internal operating characteristics. EX1001, 18:64-19:5. Thus, the disabling of *Hwang*’s power factor correction (PFC) stage 102 serves as a first internal operating characteristic. *See* EX1006, [0016], [0021]. Likewise, the reduction of the PWM stage’s average switching frequency during pulse-skipping mode serves as another internal operating characteristic.

Figures 7A-7D provide an example where two cycles are skipped over the period of five cycles. *Id.*, Figs. 7A-7D, [0036] and [0041]-[0042] (describing pulse skipping operation). During this period, the average switching frequency is reduced to 60% of the nominal switching frequency. EX1002, ¶222; EX1012, 37 (Fig. 10.38) (illustrating skipped pulses), 34 (describing pulse skipping as “modified version” of “variable-frequency” operation).



EX1006, FIG. 7A-D (annotated); EX1002, ¶222.

Hwang also explains how this regulating of internal operating characteristics improves efficiency. EX1006, [0006] (describing the entry of “pulse-skipping mode” and/or the disabling of one or more stages “to improve efficiency of the power converter”), Abstract (describing “pulse-skipping mode to improve efficiency”), [0004].

Hwang thus discloses claim 1[d]. EX1002, ¶¶219-224.

B. Claim 2

- i. **“2. The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

In response to a standby signal from the smart load 104, controller 105 “may enter standby mode” (i.e., a power converter operational state) and thereby “disable the PFC stage 102” and “cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]; *see also* Section XIV.A.iii. It would have been obvious to a POSITA that this entry into standby mode—i.e., a transition from one power converter operational state (i.e., non-standby mode) to another (i.e., standby mode)—would occur within a transition time. EX1002, ¶226.

Hwang, alone or in view of the knowledge of a POSITA, discloses and/or suggests claim 2. EX1002, ¶¶225-227.

C. Claim 4

- i. **“4. The power converter as recited in claim 1 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

The '759 Patent background explains that a “core state” relates to “levels of a processor sleep state,” achieved by “halting instruction execution” among other items. EX1001, 4:23-39; EX1002, ¶228.

As described in Section XIV.A.i for claim 1[pre], *Hwang* discloses that smart load 104 includes a microprocessor that enters a “standby mode” (i.e., the system

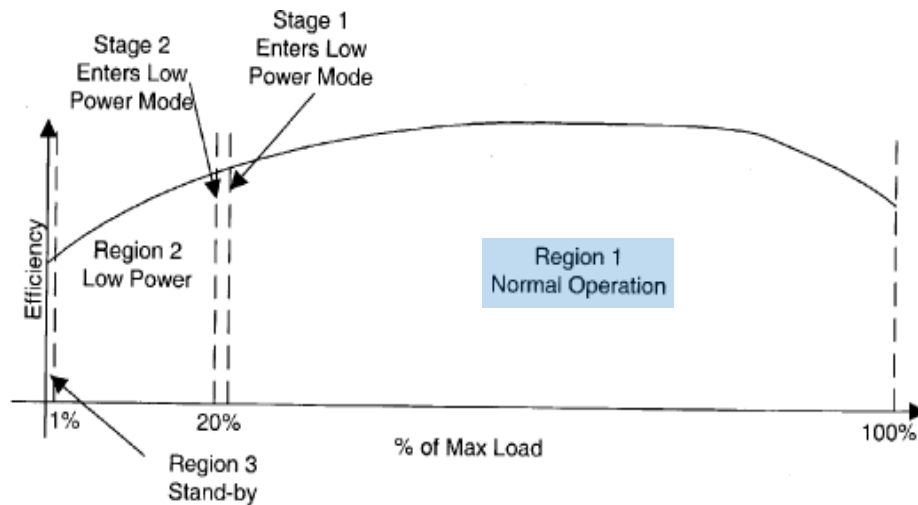
operational state) “during periods of low activity or non-use.” EX1006, [0031]; *see also id.*, [0021] (describing “a standby or ‘sleep’ mode during periods of low activity”). Thus, a POSITA would have understood that the standby mode of *Hwang*’s smart load depends on a core state of its microprocessor. *Hwang* thus discloses and renders obvious claim 4. EX1002, ¶¶229-230.

D. Claim 5

- i. **“5. The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of:
a fully operational power converter,
a reduced redundancy power converter, and
an idle power converter.”**

The ’759 Patent describes a “Fully Operational” power converter operational state as “[a]ll power converter components operational at full performance level,” as opposed to other states with “reduced switching frequency.” EX1001, Table I, 19:20-36.

Hwang discloses various power converter operational states including Normal Operation, Low Power, and Stand-by. EX1006, [0024], Fig. 2; *see also* Section XIV.A.iii (claim 1[b]). Under the “Normal Operation” state, *Hwang*’s power converter is fully operational—without any stage disabled and without pulse-skipping reducing the average switching frequency. EX1006, [0024], Table 1.



EX1006, Fig. 2 (annotated); EX1002, ¶232. The “Normal Operation” of *Hwang* discloses “a fully operational power converter.” EX1002, ¶¶231.

Hwang thus discloses and renders obvious claim 5. EX1002, ¶¶231-233.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

Later elements of claim 6 require the “power system” of claim 6[pre] to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Hwang* discloses and/or renders obvious claim 6[pre] in the same manner described for claim 1[pre]. See Section XIV.A.i; EX1002, ¶234.

ii. 6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”

For the reasons described for 1[pre], *Hwang* in view of the knowledge of a POSITA discloses and suggests a power system controller configured to receive a

signal indicating a system operational state of a load. *See* Section XIV.A.i. As described for 1[b], the power system controller of *Hwang* commands the power converter to enter a power converter operational state as a function of said signal. *Hwang* thus discloses a power system controller configured to “select” a power converter operational state as a function of the signal in the same manner described for 1[b]. *See* Section XIV.A.iii. *Hwang* thus discloses claim 6[a]. EX1002,¶235.

iii. 6[b]: “a power converter, including:”

As described for claim 1[pre], *Hwang* discloses a power converter. *See* Section XIV.A.i; EX1002,¶236.

iv. 6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”

Claim 6[c] is identical to claim 1[a] and is disclosed in the manner described for claim 1[a]. *See* Section XIV.A.ii; EX1002,¶237.

v. 6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”

Claim 6[d] restates limitations of claim 1[b]-[c] and is disclosed in the manner described for claim 1[b]-[c]. *See* Sections XIV.A.iii-iv; EX1002,¶238.

vi. 6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”

Claim 6[e] is identical to claim 1[d] and is disclosed in the manner described

for claim 1[d]. *See* Section XIV.A.v; EX1002,¶239.

F. Claims 11, 14, 15

Claims 11, 14, and 15 mirror claims 2, 4, and 5 respectively and are thus disclosed in same manner described in Sections XIV.B (claim 2), XIV.C (claim 4), and XIV.D (claim 5). EX1002,¶¶240-242.

G. Claim 16

i. 16[pre]: “A method of operating a power system coupled to a load, comprising:”

Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Hwang* thus discloses claim 16[pre] in the same manner described for claim 6 (and similar elements of claim 1). *See* Sections XIV.A.i and XIV.E.i; EX1002,¶243.

ii. 16[a]: “receiving a signal indicating a system operational state of said load;”

As described for claims 1[pre] and 6[a], *Hwang* in view of the knowledge of a POSITA discloses and suggests a power system controller that receives a signal indicating a system operational state of a load. Thus, for the same reasons described in Sections XIV.A.i (1[pre]) and XIV.E.ii (6[a]), *Hwang* discloses method step 16[a]. EX1002,¶244.

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

As described for claim 1[pre] and 1[b], *Hwang* discloses that power converter normal operation and/or standby modes (i.e., power converter operational states) are

generated as a function of the activity level of the microprocessor in smart load 104 (i.e., as a function of the system operational state). *See* Sections XIV.A.i and XIV.A.iii; *see also* EX1006, [0021], [0024], [0031], Fig. 2. *Hwang* thus discloses claim 16[b]. EX1002, ¶245.

iv. 16[c]: “inducing a power converter to enter said power converter operational state; and”

Smart load 104 sends a standby signal to controller 105 to place the power converter in “standby mode” (i.e., a power converter operational state) and thereby “disable the PFC stage 102” and “cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]; Section XIV.A.iii (claim 1[b]). The standby signal from smart load 104 thereby induces the power converter to enter said power converter operational state. *Hwang* thus discloses claim 16[c]. EX1002, ¶246.

v. 16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”

The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Hwang* discloses claim 16[d] in the same manner described for claims 1[b]-[c]. *See* Sections XIV.A.iii-iv; EX1002, ¶247.

vi. 16[e]: “thereby regulating an internal operating

characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”

Claim 16[e] is identical to claim 1[d], and is thus disclosed by *Hwang* in the same manner described for claim 1[d]. *See* Section XIV.A.v; EX1002,¶248.

H. Claim 20

Hwang thus discloses the additional elements of claim 20 in the same manner described for similar claim 5. *See* Section XIV.D; EX1002,¶249.

XV. CONCLUSION

Petitioners respectfully request that IPR be instituted and the challenged claims be cancelled.

DATE: June 15, 2022

Respectfully Submitted,

/s/ Ping Wang
Ping Wang
Registration No. 48,328

CERTIFICATE OF COMPLIANCE

1. Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. §42.24(a), contains 13988 words which is no more than 14,000 words and therefore complies with the type-volume limitations of 37 C.F.R. §42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, Claims List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

DATE: June 15, 2022

Respectfully Submitted,

/s/ Ping Wang
Ping Wang
Registration No. 48,328

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§42.6(e) and 42.105, the undersigned certifies that on June 15, 2022, a complete and entire copy of the PETITION FOR *INTER PARTES* REVIEW (“petition”), Petitioners’ power of attorney, and related Exhibits were served on Patent Owner via Express Mail or by means at least as fast and reliable as Express Mail at the correspondence address of record for the subject patent,

SHERIDAN ROSS P.C.
1560 Broadway
Suite 1200
Denver, CO 80202

And a courtesy copy is also being forwarded to Patent Owner’s Litigation Counsel via electronic mail to:

Charles Ainsworth (charley@pbatyler.com)

Robert Christopher Bunt (rcbunt@pbatyler.com)

Alfonso G. Chan (achan@shorechan.com)

Michael W. Shore (mshore@shorechan.com)

Samuel E. Joyner (sjoyner@shorechan.com)

Halima Shukri Ndai (hndai@shorechan.com)

Brian D. Melton (bmelton@susmangodfrey.com)

Krisina J. Zuñiga (kzuniga@susmangodfrey.com)

Steven M. Shepard (sshepard@susmangodfrey.com)

DATE: June 15, 2022

Respectfully Submitted,

/s/ Ping Wang
Ping Wang
Registration No. 48,328