

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANKER INNOVATIONS LTD.,
Petitioner

v.

MYPAQ HOLDINGS LTD.,
Patent Owner

Case IPR2022-01131
Patent 7,675,759

DECLARATION OF DR. SAYFE KIAEI

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I. INTRODUCTION

1. I have been retained by Anker Innovations Ltd. (“Anker” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I submitted a substantially identical declaration at the request of Samsung/Dell in IPR2022-00312.

2. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

3. I have been asked to consider whether certain references disclose or suggest the features recited in the claims of U.S. Patent No. EX1001 – US7675759B2 (“the ’759 patent”) (EX1001).¹ My opinions are set forth below.

II. EXPERIENCE AND QUALIFICATIONS

4. I am a professor at Arizona State university and am an independent consultant for this IPR. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment.

5. In forming my opinions, I have relied on my education, experience, and knowledge regarding electrical engineering, computer science, and consumer electronics product design. A copy of my current curriculum vitae, which details

¹ Where appropriate, I refer to exhibits I understand will be attached to the petition for *inter partes* review of the ’759 patent (the “Petition”).

my education and professional and academic experience, is included as Appendix A to this declaration.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

7. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

8. I received my Ph.D. in Electrical and Computer Engineering from Washington State University in 1987. I have several patents and over 100 journal and international conference publications. I have graduated over 70 MS and PhD students working under my supervision on their thesis, and many of them are professors in academia or have senior positions in industry. My research is funded by various sources, including industry and federal agencies, such as NSF, USAID, DARPA, JPL, and NASA.

9. Since 2001, I have held the position of Motorola Endowed Chair Professor in Analog and Radio Frequency Integrated Circuitry at the School of Electrical, Computer, and Energy Engineering at Arizona State University (“Arizona State”) in Tempe, Arizona.

10. I am also the Director of the National Science Foundation Center, Connection One. Connection One is a research center focused on developing wireless communication system and networking technologies.

11. From 1987 to 1993, I was an assistant/associate professor at Oregon State University (“Oregon State”).

12. From 1997 to 2002, I was also an adjunct professor at the University of Texas (“UT”) at Austin, while I worked full time at Motorola in Austin.

13. At Oregon State, UT, and Arizona State, I taught courses in the areas of analog and digital integrated circuits, power management circuits, communication systems; radio frequency (“RF”) systems and circuits; radio-frequency identification (“RFID”); magnetic and electronic sensors; analog circuits; digital integrated circuits, including HDL, Verilog, and VHDL; digital signal processing; and related areas.

14. At Arizona State, I developed a new course content and labs on analog integrated circuit, power management, and RF systems.

15. I have been involved in research, teaching, and developing products in the areas of analog and digital circuits, linear and switching power management integrated circuits (PMIC), sensors, electronics, communications, and related areas for the last 30 years.

16. I have worked in industry and academia on the systems and circuits for portable systems, including linear and switching PMIC, analog circuits and RFIC. The analog, RF and power management circuits were integrated in the mobile Bluetooth, the Global Positioning System (GPS), RFID, magnetic and

electronic sensors, wireless local area networks (LAN) (or WiFi), and related areas.

17. From 1993 to 2001, I worked at Motorola Wireless Integrated Technology Center and Motorola Analog/Digital Design groups. This group was responsible for the design and development of analog, digital, Power Management IC, DC-DC power converter, RFIC, Analog and digital baseband IC and circuits.

18. During my work in industry, I have designed and contributed to the design of many analog, RF, and power management IC's for radio transceivers for commercial products, including designs for radio transceiver integrated circuits. Many of my designs are still in use today in products manufactured by the companies I have worked for, including Motorola, Intel, and Sony.

19. I have over 200 journal and conference publications, 9 patents (and applications), and standards contributions. Several of these patents and publications are in the areas of power management, switching DC-DC converters, linear regulators, and related areas. The list of my publications is included in my resume.

20. I am an active member of IEEE Circuits and system power management technical program committee and have served in that group for over 15 years. I am an IEEE Fellow, which is the highest level of IEEE membership awarded by the IEEE directors to recognize a high level of demonstrated

extraordinary accomplishments. The IEEE Fellow Award is a special recognition for members with extraordinary accomplishments in the IEEE technical fields. To ensure that the recognition is extraordinary, the total number of recipients each year cannot exceed 0.1% of the total higher grade membership. The IEEE is the Institute of Electrical and Electronics Engineers, the world's largest association of technical professionals whose objectives include the educational and technical advancement of electrical and electronic engineering, telecommunications, computer engineering, and related disciplines.

21. I am a member of the IEEE Circuits and Systems Society, IEEE Solid State Circuits Society, IEEE Signal Processing Society, and IEEE Communication Society. I am also a member of the IEEE RF and Microwave committees, IEEE Low Power Symposium Committee, and IEEE Fellow Selection Committee. I was one of the key organizers establishing the IEEE Radio Frequency Integrated Circuits (RFIC) symposium in 1995, and I have been on the executive and technical committees of RFIC for the last 16 years. The RFIC Symposium is now the premier international symposium in the world where the latest RF circuits and components are presented. I have been involved in several international conferences in the areas of RF, Communication, Signal Processing, and IC design.

22. I have received several awards including the Carter Best Teacher Award, the IEEE Darlington Award (which is given for the best technical paper on

circuits and systems in the IEEE Circuits and Systems Society), and the Motorola 10X Rapid Design Cycle Reduction Award.

23. My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including. Based on my above-described experience, I am an expert in the field relevant to the '759 Patent at issue here and have been an expert in the relevant field since before the claimed priority date of the '759 Patent. I am familiar with how a person having ordinary skill in the art ("POSITA") would have understood and used the terminology found in the '759 Patent before and at the time of its filing.

III. LEGAL STANDARDS

24. My opinions are also informed by my understanding of the relevant law. I understand that the patentability analysis is conducted on a claim-by-claim and element-by-element basis, and that there are several possible reasons that a patent claim may be found to be unpatentable.

25. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation and (2) obviousness.

A. Anticipation

26. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference or system. I understand that inherency

requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would have been so recognized by a person of ordinary skill in the art (“POSITA”). In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

B. Obviousness

27. I understand that the prior art may render a patent claim “obvious.” I understand that two or more prior art references (e.g., prior art articles, patents, or publications) that each disclose fewer than all elements of a patent claim may nevertheless be combined to render a patent claim obvious if the combination of the prior art collectively discloses all elements of the claim and one of ordinary skill in the art at the time would have been motivated to combine the prior art in such a way. I understand that this motivation to combine need not be explicit in any of the prior art, but may be inferred from the knowledge of one of ordinary skill in the art at the time the patent was filed. I also understand that one of

ordinary skill in the art is not an automaton, but is a person having ordinary creativity. I further understand that one or more prior art references, articles, patents or publications that disclose fewer than all of the elements of a patent claim may render a patent claim obvious if including the missing element would have been obvious to one of skill in the art (e.g., the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system).

28. Under the doctrine of obviousness, a claim may be invalid if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains.

29. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

30. I understand that any evidence of secondary indicia of non-obviousness should be considered when evaluating whether a claimed invention would have been obvious to one of ordinary skill at the time of invention. These secondary indicia of non-obviousness may include, for example:

- a long felt but unmet need in the prior art that was satisfied by the claimed invention;

- commercial success of processes claimed by the patent;
- unexpected results achieved by the invention;
- praise of the invention by others skilled in the art;
 - the taking of licenses under the patent by others; and
 - deliberate copying of the invention.

31. I understand that there must be a nexus between any such secondary indicia and the claimed invention.

32. It is also my understanding that there are additional considerations that may be used as further guidance as to when the above factors will result in a finding that a claim is obvious, including the following:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of conception and reduction to practice a known problem for which there was an obvious solution encompassed by the patent's claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

33. Finally, I understand that a claim may be deemed invalid for obviousness in light of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art.

IV. LEVEL OF ORDINARY SKILL IN THE ART

34. I am informed and understand that the person having ordinary skill in the art ("POSITA") is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor's skill is not determinative of the level of ordinary skill. I further understand that factors that may be considered in determining level of skill include: (i) type of problems encountered in art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv)

sophistication of the technology; and (v) educational level of active workers in the field. I understand that not all such factors may be present in every case, and one or more of them may predominate. In a given case, every factor may not be present, and one or more factors may predominate.

35. In my opinion, a POSITA at the time of invention of the '759 Patent would have had either (i) a Masters of Science in Electrical Engineering or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering or an equivalent field as well as at least two years of experience in the design of power electronics.

36. Around the time of invention, I was familiar with this level of skill because I managed engineers at Motorola, and graduate students at ASU, working in this area including those with this level of skill.

V. OVERVIEW OF THE '759 PATENT

37. I have reviewed the '759 Patent, which is entitled "Power System with Power Converters Having an Adaptive Controller." EX1001. I understand that this patent was filed on February 23, 2007 and issued on March 9, 2010. *Id.* I also understand that this patent claims priority as a continuation-in-part of application No. 11/607,325 filed on December 1, 2006.

A. Subject Matter of the '759 Patent

38. The '759 Patent involves a switch-mode power converter, referred to

as a “power converter,” which may convert an input voltage into an output voltage. EX1001, 1:21-24. Figure 2 illustrates an example “buck” power converter that converts a DC input voltage to a DC output voltage:

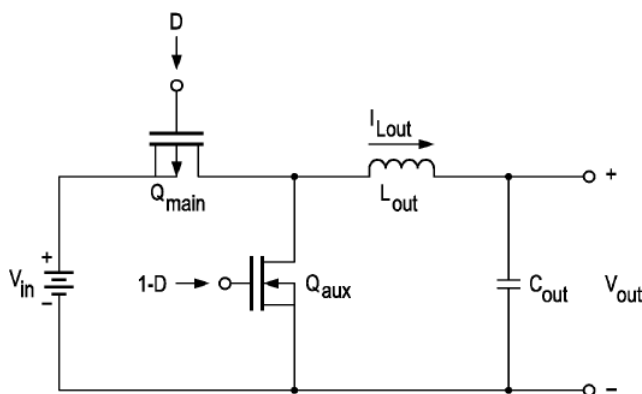


FIG. 2
(PRIOR ART)

EX1001, Fig. 2. The main power switch Q_{main} and auxiliary power switch Q_{aux} are turned on and off by drive signal D and complementary drive signal $1-D$ respectively. *Id.*, 8:57-9:15. When Q_{main} is turned on, Q_{aux} is turned off, and vice versa. As known in the art, and explained in the '759 Patent background, the duty cycle of the switches (i.e., ratio of on-time to the total switching period) in a power converter can be adjusted to regulate the output voltage V_{out} of the power converter. *Id.*, 1:36-55, 9:15-18. The “buck” converter, also known as step down converter, is a well-known power converter, which produces a lower DC output voltage than the input DC voltage, EX1009 (Mohan), 19 (Section 7-3, p.164).

39. The '759 Patent purports to improve power converters by using an “adaptive controller.” EX1001, Abstract. The '759 Patent acknowledges that it

was “well known” to control output characteristics (e.g., the output voltage) of a converter based on the needs of a microprocessor coupled to the output. *Id.*, 3:43-51. But, the ’759 Patent purports to improve upon the prior art by adjusting an internal operating characteristic (e.g., switching frequency) to improve efficiency based on a signal from an external source representing the state of the load. *Id.*, 5:18-26. For example, when a load such as a microprocessor goes into a low-power system operational state (e.g., a standby mode), the microprocessor may signal the power converter to adjust its internal operating characteristics (e.g., switching frequency) to improve the efficiency of the power converter during such times of low demand from the load.

40. However, as I describe in this declaration, power converters capable of adjusting internal operating characteristics (e.g., switching frequency) to improve efficiency based on the state of the load were well known prior to the ’759 Patent.

B. Prosecution History of the ’759 Patent

41. I have reviewed the prosecution history of the ’759 Patent. I understand that U.S. Patent Application No. 11/710,276 was filed on February 23, 2007, as a continuation-in-part of application No. 11/607,325 filed on December 1, 2006. *See* EX1001. I understand that in an Office Action dated February 25, 2009, the Examiner rejected claims 1-20, relying on, among other references, U.S.

Publication 2008/0054874 (“Chandrasekaran”). I understand that the Applicant argued that Chandrasekaran was not prior art. EX1008, 15-17. Subsequently, the Examiner issued a Notice of Allowance. *Id.*, 4. However, I understand that the Examiner did not consider the prior art that I analyze in this declaration. *See* EX1001 (listing references before the Examiner).

VI. CLAIM CONSTRUCTION

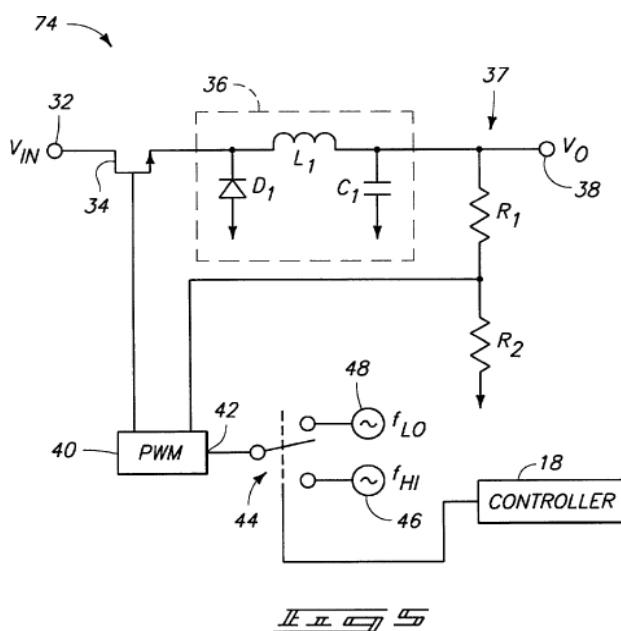
42. I understand that “claim construction” is the process of determining a patent claim’s meaning. I also understand that, during an *inter partes* review, a claim construction analysis begins with the plain meaning of the claim term, which is the ordinary and customary meaning given to the term by those of ordinary skill in the art at the time of the invention. I also understand that the claims of a patent must be interpreted in light of the specification—that is, the claim language itself, the written description, and the figures in the patent—as well as the patent’s prosecution history and/or any reexamination history.

43. In my opinion, and for the purposes of this declaration, the claim terms of the ’759 Patent do not require a construction. For purposes of this declaration, I interpret all claim terms in accordance with their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention, having taken into consideration the language of the claims, the specification, and the prosecution

VII. SUMMARY OF PRIOR ART

44. *Hirst* (U.S. Patent 6,294,904) issued on September 25, 2001.

45. *Hirst* describes “a multiple frequency switching power supply” that provides “a regulated output voltage.” EX1003, 2:44-54. Figure 5 of *Hirst* illustrates a power converter receiving signals from an external controller 18.



Anker, EX1002, p. 19

improved “because switching losses are dramatically reduced.” *Id.*, 4:59-62.

B. Chagny (EX1004)

46. *Chagny* (U.S. Patent 6,873,136) issued on March 29, 2005. EX1004.

The '759 Patent was filed on February 23, 2007 and claims priority to December 1, 2006. *Chagny* thus predates the '759 Patent by over a year.

47. *Chagny* discloses a voltage regulator module (VRM) 200 (i.e., a power converter) that provides a “regulated DC voltage output 295” to processor 292. EX1004, 3:52-58.

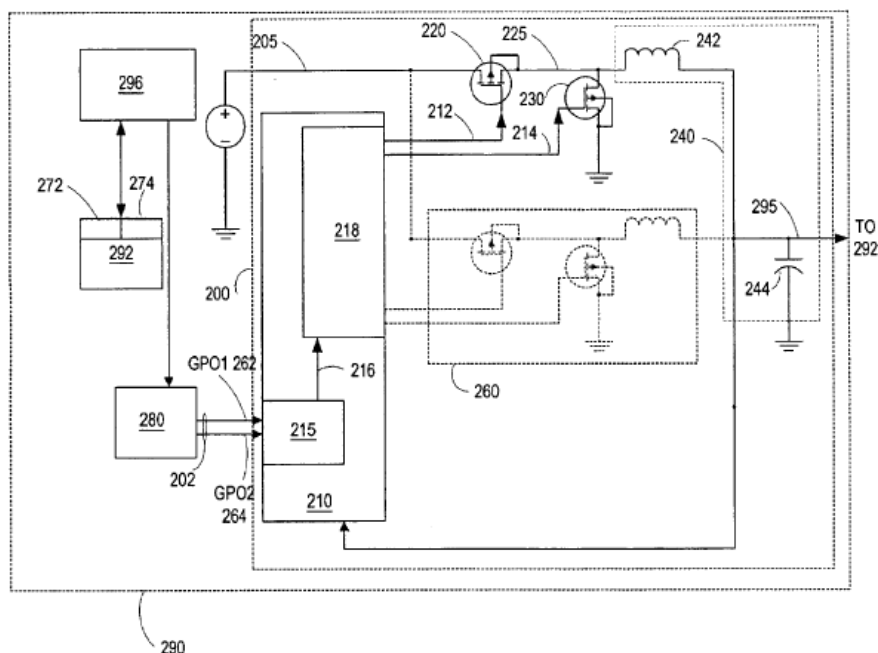


FIG. 2A

EX1004, Fig. 2A. *Changny*'s controller module 210 receives an activity input 202 indicative of the processor's activity level (*id.*, 3:60-65), and thereby changes the switching frequency of VRM 200 accordingly (*id.*, 5:9-12). By selecting a low

switching frequency during periods of low processor activity, the efficiency of VRM 200 is improved. *Id.*, 5:20-23.

C. Clark (EX1005)

48. *Clark* (U.S. Patent 6,664,775) issued on December 16, 2003. EX1005. The '759 Patent was filed on February 23, 2007 and claims priority to December 1, 2006. *Clark* thus predates the '759 Patent by over 2 years.

49. *Clark* describes “a portable device” that includes a voltage regulator 40 providing power to core logic 50 (e.g., a microprocessor). EX1005, 3:30-43.

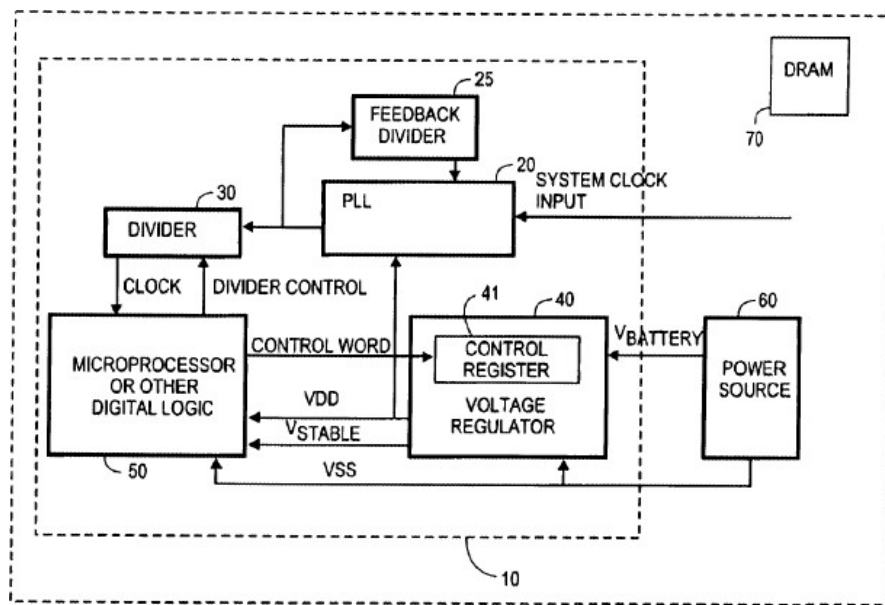


FIG. 1

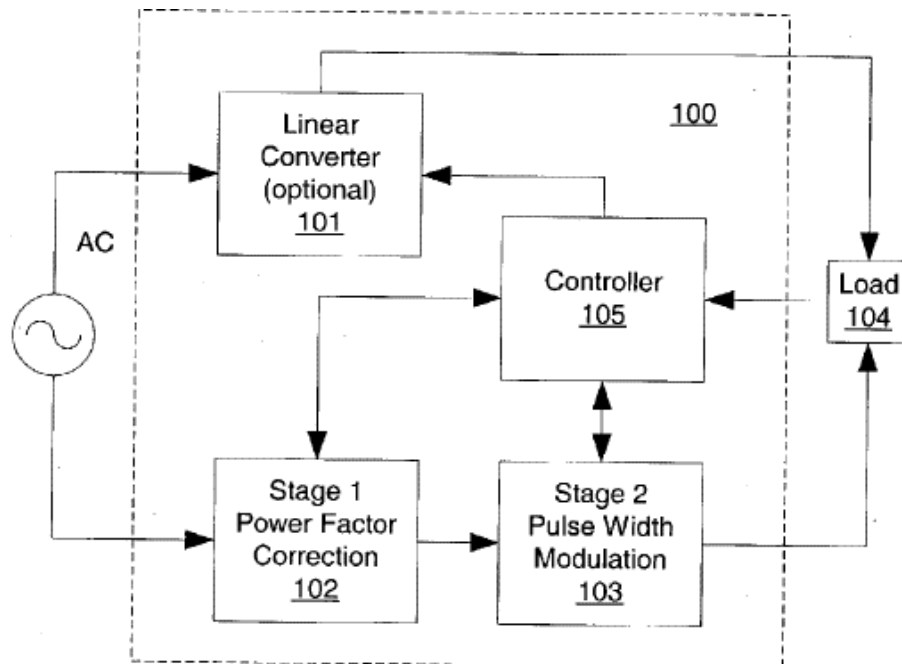
EX1005, Fig. 1. *Clark* teaches that “core logic 50 may send control signals to ... reduce the voltage potential range provided by voltage regulator 40,” thereby reducing “the amount of power consumed by integrated circuit 10.” *Id.*, 5:14-21.

50. *Clark* is in the same field of endeavor—adaptable power systems—as the '759 Patent and, in my opinion, a POSITA would have understood that *Clark* is very pertinent to potential problems identified in the '759 Patent such as improving efficiency.

D. *Hwang* (EX1006)

51. *Hwang* (U.S. Patent Application Publication 2004/0174152) published on September 9, 2004. EX1006. The '759 Patent was filed on February 23, 2007 and claims priority to December 1, 2006. *Hwang* thus predates the '759 Patent by over 2 years.

52. *Hwang* discloses a power converter 100 coupled to a smart load 104 (e.g., a microprocessor). EX1006, [0019], [0021].



EX1006, Fig. 1. *Hwang* discloses that the load 104 sends a standby signal to the controller 105 within power converter 100 indicating the level of power drawn by load 104, thereby causing “PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021]) in order to “improve efficiency” (*id.*, Abstract).

53. *Hwang* is in the same field of endeavor—adaptable power systems—as the ’759 Patent and, in my opinion, a POSITA would have understood that *Hwang* is very pertinent to potential problems identified in the ’759 Patent such as improving efficiency.

VIII. SUMMARY OF PRIOR ART GROUNDS

54. A summary of the invalidity grounds considered herein is below.

Ground	Claims	Basis	Prior Art
1A	1-3, 5-13, 15-20	Anticipation	Hirst
1B	1-3, 5-13, 15-20	Obviousness	Hirst
2A	1-2, 4-6, 11, 14-16, 20	Anticipation	Chagny
2B	1-2, 4-6, 11, 14-16, 20	Obviousness	Chagny
2C	3, 12-13, 19	Obviousness	Chagny and Clark
3	1-2, 4-6, 11, 14-16, 20	Obviousness	Hwang

IX. GROUND 1A: HIRST ANTICIPATES CLAIMS 1-3, 5-13, and 15-20

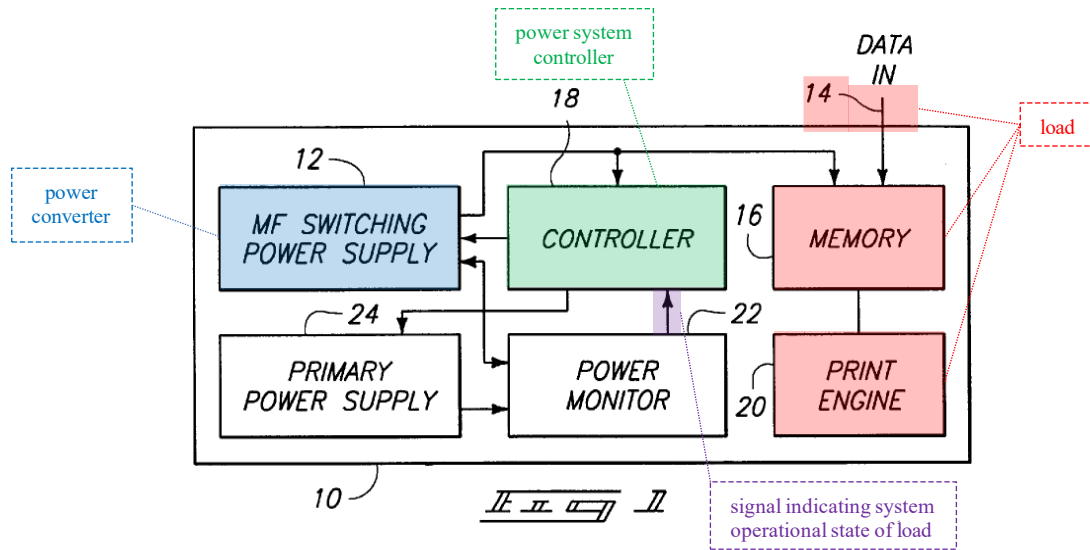
55. In my opinion, *Hirst* discloses each element of Claims 1-3, 5-13, and 15-20, and thus anticipates those claims.

A. **Claim 1**

- i. **1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

56. *Hirst* discloses a multiple-frequency (MF) “switching power supply” (i.e., power converter). EX1003, Abstract, 2:44-45. Figure 1 of *Hirst* provides a block diagram of a printer 10, including a multi-function switching power supply 12 and a print-engine controller 18 (i.e., power system controller). EX1003, 3:51-59. A multi-frequency power supply 12 may supply power to “data input port 14” and “data memory 16” of printer 10 (collectively or individually², the load). *Id.*, 4:20-32.

² These individual components can also be separate loads supplied by multiple instances of *Hirst*’s multi-frequency power supply. EX1003, 4:27-32 (“one or more efficient DC-to-DC switching power supplies 12” used to “provide the data-handling circuits 14, 16 and 18 with electrical power”), FIG. 6 (showing multiple switching power supplies providing multiple output voltages).



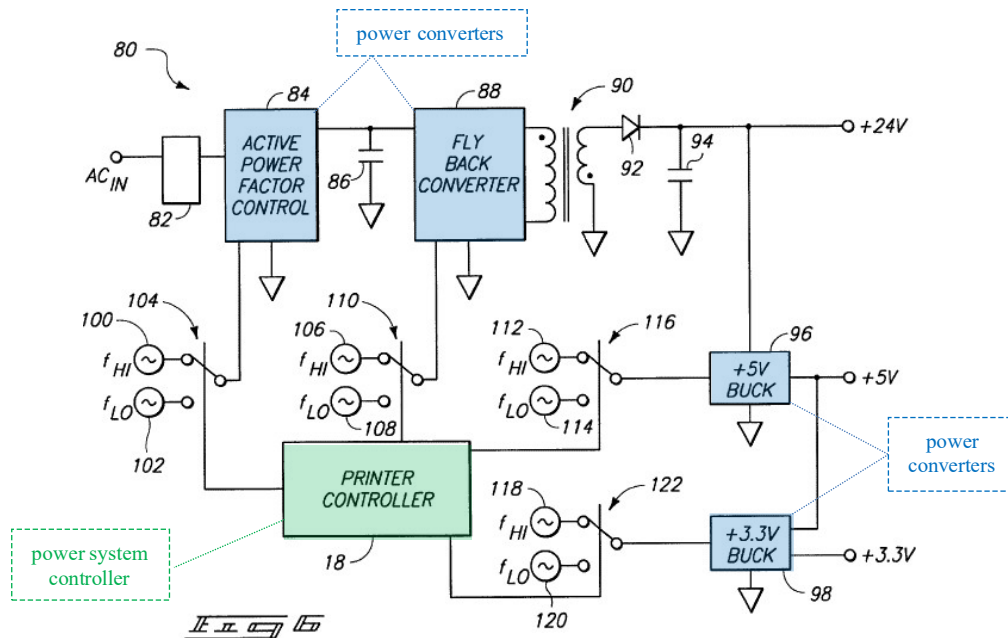
EX1003, FIG. 1 (annotated).

57. *Hirst* discloses that the printer may operate in either a “normal mode of operation” or a “standby mode of operation” (i.e., different system operational states). EX1003, 3:17-23. The consumption during these normal and standby modes is detected by “power consumption monitor 22.” *Id.*, 4:32-41.

58. *Hirst* discloses that, in some embodiments, signals from power consumption monitor 22 directly control the switching frequency of an MF switching power supply. EX1003, 5:46-51. However, *Hirst* also discloses that signals from the power consumption monitor 22 (i.e., signals indicating system operational state of the load) are also sent to and received by the print-engine controller 18 (i.e., the power system controller). *See id.*, 8:27-33 (describing “controller 18” in Figure 6 as controlling the frequency of the switching power supply “in response to signals from the power monitor 22 of FIG. 1”), Fig. 1

(illustrating signal from power monitor 22 to controller 18), 4:7-13 (disclosing “the data input port 14 and the data memory 16 ... operate together under the direction of the controller 18”); 3:19 (referring to “print engine controller”); *see also id.*, 6:65-7:4 (describing “one embodiment of the power consumption monitor 22 of FIG. 1” as shown in Figure 3), Fig. 3.

59. *Hirst* explains that by using controller 18 (i.e., the power system controller recited in claim 1 of the ’759 Patent) to control the frequency of the MF switching power supply, *Hirst* causes more than one instance of the MF switching power supply “to enter standby mode” (i.e., switch at a low frequency) “when the laser printer 10 of FIG. 1 enters the standby mode.” *Id.*, 8:5-8. This is shown, for example, in Figure 6, where controller 18 is configured to control the frequency of multiple multi-frequency switching power supplies 84, 88, 96, and 98 (i.e., multiple power converters):



EX1003, Fig. 6 (annotated). Notably, *Hirst* explains that “controller 18” individually controls the frequency of each of the power supplies 84, 88, 96, and 98 shown in Figure 6 “in response to power levels being drawn from each of them.” EX1003, 8:27-49.

60. In my opinion, a POSITA would understand *Hirst* to disclose that controller 18 (i.e., the power system controller) is configured to receive a signal from a power system monitor 22 (i.e., a signal indicating the system operational state of a load coupled to the power converter), and thereby control the switching frequency of a power converter coupled to the load. For example, *Hirst*’s disclosure is similar to embodiments in the ’759 Patent whereby the switching frequency of a power converter is controlled based on a signal “from an external source” (like controller 18 of *Hirst*) based on the “actual load current” of the load

coupled to the power converter. *See* EX1001, 12:18-30.

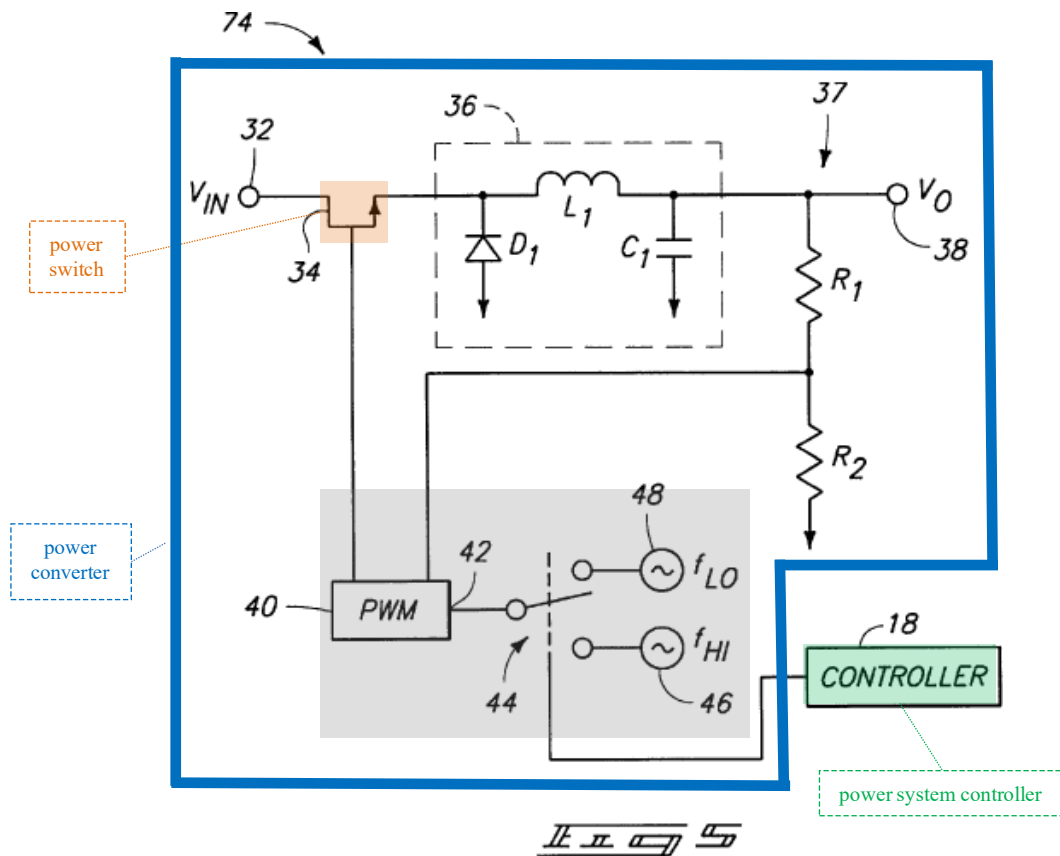
61. In addition, *Hirst* discloses that controller 18 sets the frequency of the multi-frequency switching power supply “in response to other assessments of power need.” EX1003, 8:27-33 (“The controller 18 is able to couple either a first oscillator 100 having a first frequency f_{HI} or a second oscillator 102 having a second frequency f_{LO} to the active power factor power supply 84 via a switch 104 in response to signals from the power monitor 22 of FIG. 1 or in response to other assessments of power need.”).

62. In my opinion, based on the disclosure in *Hirst*, a POSITA would understand that such “other assessments” by controller 18 (i.e., the **power system controller**) would include a signal (i.e., a **signal indicating the system operational state of the load**) based on, for example, the input data received at “data input port 14,” which operates “under the direction of controller 18.” *See id.*, 4:7-19 (describing processing of data received at data input port 14), 4:20-32 (describing “power consumption due to operation of the data input port, the data memory, the controller 18, and the print engine 20” and provision of one or more DC-to-DC switching power supplies 12 to provide power for those circuits). Thus, in addition to the signal from power consumption monitor 22, a signal received by controller 18 representing the “other assessments of power need,” would also qualify as a “**signal indicating the system operational state of the load.**”

63. Thus, in my opinion, *Hirst* discloses each element of claim 1[pre].

- i. **1[a]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and”**

64. Figures 2-5 of *Hirst* illustrate embodiments of the multi-frequency power supply in further detail and share common reference numbers for common elements. *See* EX1003, Figs. 2-5, 6:45-51. As shown in Figure 5, for example, “switching transistor 34” serves as the power switch in a “buck” type power converter. *See id.*, 6:1-5 (describing “turning the switching transistor 34 ON and OFF to supply electrical charge from the power input port 32 to the filtering circuit 36”), 5:18-20 (describing “buck” configuration); *see also id.*, Abstract, 2:45-49 (describing operation of “switching transistor”), 1:18-28 (describing “buck” switching power supply).



EX1003, Fig. 5 (annotated).

65. *Hirst* explains that the “pulse width of the ON portion of the duty cycle of the switching transistor 34 [i.e., the power switch] is varied in a conventional manner by the PWM circuit 40 in response to voltages sensed by the voltage divider 37 to regulate the amount of charge that is transferred per cycle from the power input port 32 to the filtering circuit 36 and thus to maintain the desired output voltage V_{OUT} [i.e., regulated output characteristic] at the output 38.”

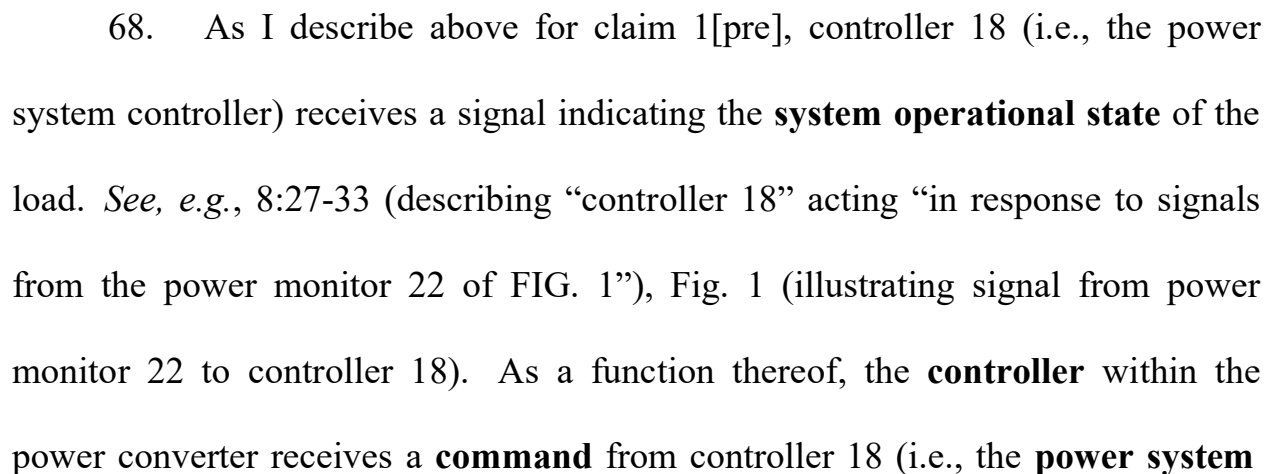
EX1003, 6:8-14; *see also id.*, 6:1-20.

66. Thus, in my opinion, *Hirst* discloses each limitation of claim 1[a].

- i. **1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”**

67. Figure 5 of *Hirst* illustrates a power converter “controller” including pulse-width modulation (PWM) circuit 40, first oscillator 46, second oscillator 48, and switch 44 (collectively, the power converter “controller” recited in claim 1[b], annotated in gray). EX1003, 5:24-31 (“The MF switching power supply 30 includes a power input port 32 to accept an input voltage VIN, a switching transistor 34, a filtering circuit 36, a voltage divider 37, a power output port 38 to provide an output voltage VOUT and a pulse width modulation (PWM) circuit 40 having an input 42. The MF switching power supply 30 also includes a switch 44 and multiple clock signal sources or oscillators 46 and 48.”), 7:63-8:8 (“FIG. 5 is a simplified schematic diagram of a multiple frequency (MF) switching power supply 74, in accordance with an embodiment of the present invention. In the embodiment shown in FIG. 5, the MF switching power supply 74 switches from the normal mode of operation using the first oscillator 46 having the first clock frequency fHI to the standby mode of operation using the second clock signal from the second oscillator 48 having the second clock frequency fLO in response to commands from the controller 18 of FIG. 1. This permits the controller 18 to cause more than one MF switching power supply, such as the power supply 74, to enter the standby mode when the laser printer 10 of FIG. 1 enters the standby mode.”).

EX1003, Fig. 5 (annotated).



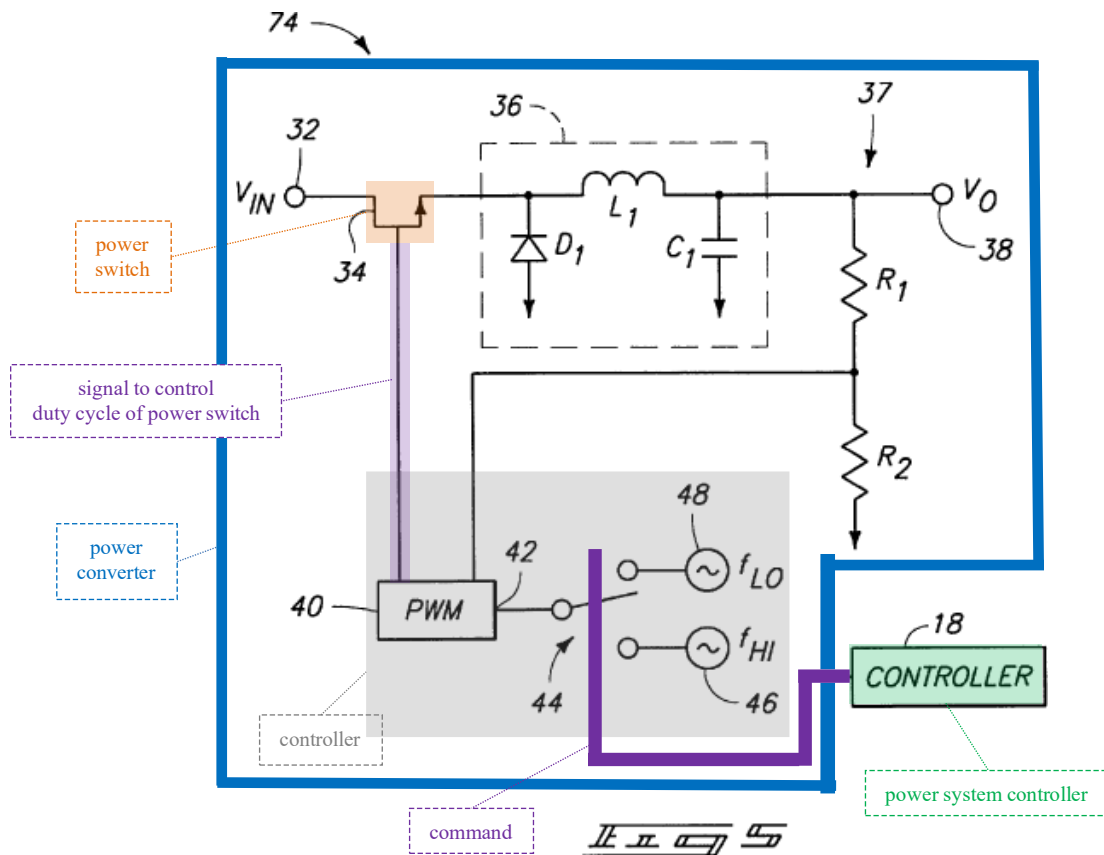
controller) to enter one of two **power converter operational states**: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. *See* EX1003, 7:66-8:5 (“[T]he MF switching power supply 74 switches from the normal mode of operation using the first oscillator 46 having the first clock frequency f_{HI} to the standby mode of operation using the second clock signal from the second oscillator 48 having the second clock frequency f_{LO} in response to commands from the controller 18 of FIG. 1.”). This command “permits the controller 18 to cause more than one MF switching power supply, such as the power supply 74, to enter the standby mode when the laser printer 10 of FIG. 1 enters the standby mode.” *Id.*, 7:66-8:8 (“In the embodiment shown in FIG. 5, the MF switching power supply 74 switches from the normal mode of operation using the first oscillator 46 having the first clock frequency f_{HI} to the standby mode of operation using the second clock signal from the second oscillator 48 having the second clock frequency f_{LO} in response to commands from the controller 18 of FIG. 1. This permits the controller 18 to cause more than one MF switching power supply, such as the power supply 74, to enter the standby mode when the laser printer 10 of FIG. 1 enters the standby mode.”); *see also id.*, 3:17-23 (“In another aspect, the invention includes provision of a control input on a multiple frequency switching power supply. Commands from a print engine controller select a first switching frequency for the power

supply when the printer is in a normal mode of operation and select a second switching frequency for the power supply when the printer is in a standby mode of operation.”).

69. Thus, in my opinion, *Hirst* discloses each limitation of claim 1[b].

- i. **1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

70. As shown in Figure 5 of *Hirst*, the “gate of the switching transistor 34 is coupled to an output of the PWM circuit 40,” which is part of the power converter controller, as explained above. EX1003, 6:7-8.



EX1003, Fig. 5 (annotated). As I describe above for claim 1[a], PWM circuit 40 (which is part of the power-converter “controller” recited in claim 1[b]) controls the duty cycle of switching transistor 34 (i.e., the power switch) as a function of the feedback from the output voltage (i.e., as a function of said output characteristic). EX1003, 6:8-14 (“A pulse width of the ON portion of the duty cycle of the switching transistor 34 is varied in a conventional manner by the PWM circuit 40 in response to voltages sensed by the voltage divider 37 to regulate the amount of charge that is transferred per cycle from the power input port 32 to the filtering circuit 36 and thus to maintain the desired output voltage

V_{OUT} at the output 38.”).

71. The switching transistor 34 is also controlled in accordance with the command from the power system controller setting the frequency. EX1003, 6:15-18 (describing “limits over which the duty cycle may be varied” when PWM circuit 40 is “driven by” the first oscillator 46 and the second oscillator 48), 2:59-65 (describing provision of “first frequency” or “second frequency” to pulse width modulation circuit), 7:65-8:8 (describing selection of frequency from first or second oscillator), 6:34-37; *see also id.*, 5:32-35 (describing how switch 44 can “selectively couple one of several oscillators 46 and 48 to the PWM circuit 40”).

72. Thus, in my opinion, *Hirst* discloses each limitation of claim 1[c].

- i. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

73. As I describe above for claim 1[pre] and 1[b], the switching frequency of the power converter (i.e., the **internal operating characteristic of said power converter**) in *Hirst* is selected as a function of the **system operational state** of the load. *See, e.g.*, EX1003, 3:17-24 (“Commands from a print engine controller select a first switching frequency for the power supply when the printer is in a normal mode of operation and select a second switching frequency for the power supply when the printer is in a standby mode of operation.”), 7:66-8:8 (power converter placed in “standby mode” with low frequency f_{LO} “when the laser printer

10 of FIG. 1 enters the standby mode.”).

74. And as explained in *Hirst*’s background, and well known by the POSITA, the switching losses in a switching power converter are proportional to switching speed. EX1003, 2:2-3; *see also* EX1010, 2:15-34 (explaining how switch loss can predominate at light loads and is proportional to frequency). Thus, as explained by *Hirst*, efficiency can be “improved under light loading by lowering the switching speed [i.e., the switching frequency] of a switching element.” EX1003, 1:46-48. Consistent with this principle, *Hirst* explains that the reduction of its switching frequency when the load is in a standby mode “provides a sharp increase in switching power supply efficiency because switching losses are dramatically reduced.” EX1003, 4:59-62.

75. Thus, in my opinion, *Hirst* discloses each limitation of claim 1[d].

B. Claim 2

- i. **2: “The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

76. I understand that although claim 2 recites “within a transition time,” Claim 2 does not set an upper limit, or otherwise define the “transition time” recited therein.

77. The multi-frequency power supply of *Hirst* (i.e., the power converter) is configured to transition between states “very rapidly.” EX1003, 2:37-41. As I

describe above for claim 1[b], the power converter operational states of *Hirst* include (i) the “normal mode of operation” with a high switching frequency “ f_{HI} ,” and (ii) the “standby mode of operation” with a low switching frequency “ f_{LO} ,” EX1003, 7:63-8:8. In my opinion, a POSITA would appreciate that the transition from one switching-frequency state to a new switching-frequency state would be completed within one switching cycle at the new frequency. Thus, in my opinion, *Hirst* transitions between power converter operational states within a transition time as recited by Claim 2.

C. **Claim 3**

- i. **3: “The power converter as recited in claim 1 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.”**

78. *Hirst* discloses that its multi-frequency switching power supply (i.e., the power converter) “includes a ripple monitor 49.” EX1003, 6:29-31, Fig. 2. *Hirst* explains that the “amount of ripple that is present in the output voltage V_O tends to increase as the amount of power being drawn from the MF switching power supply 30 increases.” *Id.*, 6:30-32. “When the ripple monitor 49 determines that the ripple in the output voltage V_O is too high, the ripple monitor 49 ***provides a signal to the controller 18*** of FIG. 1 to increase the frequency of the MF switching power supply 30.” *Id.*, 6:32-37. For example, the frequency is increased by

switching from the low-frequency oscillator to the high-frequency oscillator. *See id.*, 6:37-38 (“the frequency is increased by switching to the first oscillator 46”), 7:66-8:8 (describing “normal mode of operation” with a high frequency “ f_{HI} ” of first oscillator 46, and a “standby mode of operation” with the low frequency “ f_{LO} ” of second oscillator 48).

79. In sum, controller 18 (i.e., the **power system controller**) receives a signal from ripple monitor 49 indicating that the power supply ripple is too high (i.e., **indicating a power converter status**), and switches the power converter to a higher switching-frequency state (i.e., a different **power converter operational state**) as a function thereof.

80. Notably, the '759 Patent specification itself describes a “Failure Likely” status as “Power converter operating with reduced operational capability,” and further associates “Failure Likely” with “a high level of ripple voltage.” EX1001, Table II, 20:9-14. Thus, the power converter status signal from *Hirst*’s ripple monitor indicating that the “ripple in the output voltage V_O is too high” (EX1003, 6:32-37) serves as a failure-likely status. Indeed, one of the goals of the power converters is to minimize the output voltage ripple, typically to below 1-2% of the maximum output voltage. *See, e.g.*, EX1009, 25-27. Ripple has many drawbacks including wasting power, lowering efficiency, impacting the load circuits, heating components, increasing noise, and other undesirable impacts.

Furthermore, excess ripple may increase the supply, ground, and load current, severely impacting and damaging the circuits, input/output pins, and the load circuits. Accordingly, the status signal from the ripple monitor of *Hirst* serves a role to protect the associated circuitry and load from overly high ripple voltages.

81. Thus, in my opinion, *Hirst* thus discloses each element of claim 3.

D. Claim 5

- i. **5: “The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

82. As I describe above for claim 1[b], *Hirst* discloses power converter operational states including a “normal mode of operation” with a high switching frequency “ f_{HI} .” *See, e.g.*, EX1003, 7:63-8:8; *see also id.*, 2:59-65 (describing “first frequency” during “normal mode” and “second frequency” during “standby mode”). Table 1 of the ’759 Patent describes various power converter operational states, including a “fully operational” state, which is characterized as “[a]ll power converter components operational at full performance level,” whereas “reduced switching frequency” is an attribute of “very light load.” EX1001, Table 1. Consistent with descriptions in the ’759 Patent itself, *Hirst*’s power converter at the normal mode of operation with the high switching frequency “ f_{HI} ” discloses a fully operational power converter as recited in the claims.

83. Thus, in my opinion, *Hirst* thus discloses each limitation of claim 5.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

84. Later elements of claim 6 require the “power system” of claim 6[pre] to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Hirst* discloses claim 6[pre] in the same manner that I describe above for claim 1[pre]. See Section IX.A.i.

ii. 6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”

85. As I describe above for claim 1[pre], *Hirst* discloses a power system controller configured to receive a signal indicating a system operational state of a load. See Section IX.A.i. And as I describe above for claim 1[b], the power system controller of *Hirst* sends a command to the power converter controller to enter a power converter operational state as a function of said signal. Thus, in my opinion, *Hirst* discloses a power system controller configured to “select” a power converter operational state as a function of the signal in the same manner as I describe above for claim 1[b]. See Section IX.A.iii. Therefore, *Hirst* discloses in my opinion each limitation of claim 6[a].

iii. 6[b]: “a power converter, including:”

86. As I describe above for claim 1[pre], *Hirst* discloses a power system that includes a power converter. See Section IX.A.i. For example, *Hirst* discloses

a multiple-frequency “switching power supply” (i.e., power converter). EX1003, Abstract, 2:44-45, Fig. 1, Fig. 5.

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”**

87. Claim 6[c] is identical to claim 1[a]. Thus, claim 6[c] is disclosed by *Hirst* in the same manner as I describe above for claim 1[a] in Section IX.A.ii.

- v. **6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

88. Claim 6[d] restates limitations recited in claims 1[b]-[c].

1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state” 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”	6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”
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Thus, *Hirst* discloses claim 6[d] in the same manner as I describe above for claim

1[b]-[c] in Sections IX.A.iii and IX.A.iv.

- vi. **6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

89. Claim 6[e] is identical to claim 1[d]. Thus, claim 6[e] is disclosed by *Hirst* in the same manner as I describe above for claim 1[d] in Section IX.A.v.

F. Claim 7

- i. **7[pre]: “The power system as recited in claim 6 wherein said power system is coupled to another load and”**

7[a]: “said power system controller is configured to receive another signal indicating another system operational state of said another load and to select another power converter operational state as a function thereof”

7[b]: “said power system, further comprising: another power converter, including:”

7[c]: “another power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”

7[f]: “another controller configured to receive another command from said power system controller to enter said another power converter operational state and to provide a signal to control said duty cycle of said another power switch as a function of said output characteristic and in accordance with said another command,”

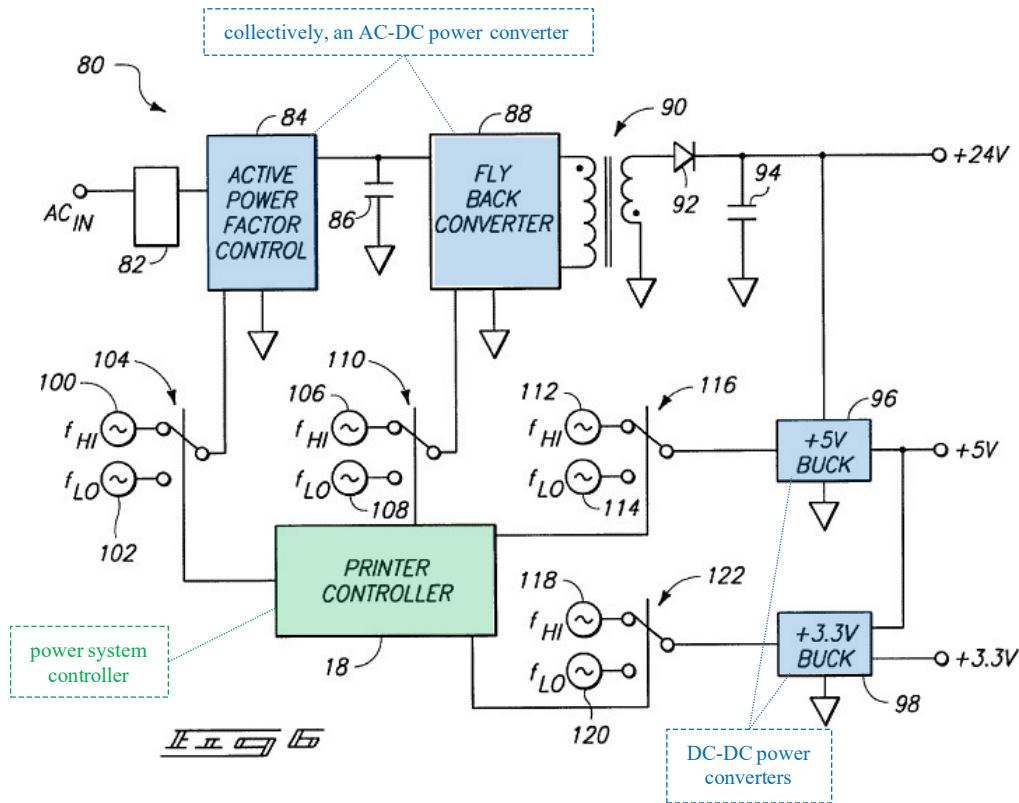
7[e]: “thereby regulating an internal operating characteristic of said another power converter to improve an operating efficiency thereof as a function of said another system operational state.”

90. Claim 7, which is dependent on claim 6, repeats each limitation of

claim 6, but for “another load” and “another power converter” as underlined above (and the associated states, signals, and command) under the control of the same “power system controller.” Compare claim 7[pre]-[e] and claim 6[pre]-[e]; see also EX1007, 1 (side-by-side comparison of claims 6 and 7).

91. The power system of *Hirst* is coupled to multiple loads, including the “data input port 14,” “data memory 16,” and “print engine 20.” EX1003, 4:20-24, Fig. 1. *Hirst* teaches how these different multiple loads require different “voltages or currents in order to operate properly.” *Id.*, 4:24-27. Accordingly, an “AC-to-DC power supply 24 is often used to provide a primary power supply, with ***one or more efficient DC-to-DC switching power supplies 12*** to provide the data-handling circuits 14, 16 ... with electrical power.” *Id.*, 4:27-31.

92. Figure 6 of *Hirst* illustrates an example power system including the numerous multi-frequency switching power supplies contemplated at column 4, lines 27-31 of *Hirst* for providing different output voltages to the different loads (e.g., data-handling circuits 14, 16 illustrated in Fig. 1 and described at 4:27-31 of *Hirst*).



EX1003, Fig. 6 (annotated).

93. *Hirst* explains: “FIG. 6 is a simplified block diagram of a group of power supplies 80 for the laser printer 10 of FIG. 1. Modern laser printers 10 include a number of power supplies 80, many or all of which may be switching power supplies.” EX1003, 8:9-12. As shown in Figure 6, active power factor control power supply 84 and fly back converter 88 collectively form an AC-DC power converter with a 24 V output suited for the “higher voltage[]” required by “print engine 20.” See EX1003, 4:24-27; see also *id.*, 8:17-23 (“An output from the active power factor control power supply 84 is coupled to a capacitor 86 and to an input to a fly back converter 88. An output from the fly back converter 88 is

coupled to a primary winding of a transformer 90. A secondary winding of the transformer 90 is coupled through a diode 92 to a capacitor 94 to provide a +24 volt power source. A +5 volt buck converter 96 is coupled to the +24 volt power source to provide a +5 volt output, and a +3.3 volt buck converter 98 is coupled to the +5 volt output to provide a +3.3 volt output.”).

94. As also shown in Figure 6, buck converters 96 and 98 provide lower voltages suited for lower-voltage components such as data input port 14 and data memory 16.³ *See* EX1003, 4:20-31 (“In order to reduce power consumption due to operation of the data input port 14, the data memory 16, ... and the print engine 20, these components have been designed to operate with progressively lower power supply voltages over the last several years. However, other kinds of functions, such as an electromechanical drive for feeding paper through the print engine 20, require higher voltages or currents in order to operate properly. As a result, the AC-to-DC power supply 24 is often used to provide a primary power supply, with one or more efficient DC-to-DC switching power supplies 12 to provide the data-handling circuits 14, 16 ... with electrical power.”); *see also id.*, 8:17-23. Indeed, a POSITA would have understood the various different circuit blocks in the printer

³ As shown in Figure 6, the +3.3 volt buck converter 98 is powered by the +5V buck converter and is thus a load to the +5V buck converter 96, which in turn is powered by the +24 volt output and is thus a load to the + 24 volt output.

may require different supply voltages tailored towards those block. For example, the digital circuit technology maybe fabricated in lower supply voltage whereas the analog blocks, ADC (analog to digital converters) and other sensitive blocks may requires higher supply voltages with increased dynamic range, noise, efficiency, and other requirements.

95. *Hirst* further discloses that the frequency for each of the multi-frequency switching power supplies in Figure 6 is under the control of the same “controller 18” (i.e., the power system controller). *Id.*, 8:27-49. Moreover, *Hirst* discloses that controller 18 “individually” selects the frequency for each of the power supplies 84, 88, 96, and 98 “in response to power levels being drawn from each of them” (i.e., in response to the system operational state of their respective loads). *Id.*, 8:42-49; *see also id.*, 7:63-8:8 (disclosing “the controller 18 cause[s] more than one MF switching power supply” “to enter the standby mode”), 5:18-23 (“While the MF switching power supplies shown in FIGS. 2-5 are shown as being buck power supplies, it will be appreciated that other kinds of switching power supplies may use the inventive concepts illustrated.”). Accordingly, a POSITA would understand that, for each of the respective power supplies and loads, controller 18 receives a signal indicating the system operational state of the load in the same manner described above for claim 1[pre] and 6[a]. *Id.*, 8:42-49 (“The controller 18 may switch all of the power supplies 84, 88, 96 and 98 together or

may switch them in a preferred order, or may set them individually *in response to power levels being drawn from each of them.*”).

96. Thus in my opinion, based on *Hirst*’s disclosures, a POSITA would understand that each of the multiple power converters illustrated in Figure 6 and each of their respective loads disclose the requirements of claim 6 (and the similar requirements of claim 1) in the same manner as I describe above for claims 1 and 6 in Sections IX.A and IX.E. In my opinion, *Hirst* therefore also discloses each element of claim 7 including the requirements of “*another* power converter” and “*another* load” (and the associated states, signals, and command) under the control of the same “power system controller.”

G. Claim 8

- i. 8: “The power system as recited in claim 7 wherein at least one of said system operational state and said another system operational state, and said power converter operational state and said another power converter operational state, are different.”**

97. I note that, based on the language of claim 8, only one of the respective **system operational states** or respective **power converter operational states** need to be different from each other. In my opinion, *Hirst* discloses both options for meeting claim 8.

98. As I describe above for claim 1[b] and claim 6[a], *Hirst* discloses multiple power converter operational states: (i) a “normal mode of operation” with

a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. EX1003, 7:66-8:8. And as I describe above for claim 7, the multiple power converters of *Hirst*’s power system each can have a different **power converter operational state**. EX1003, 8:42-49 (“The first frequency f_{HI} and the second frequency f_{LO} *need not be the same* for each of the power supplies 84, 88, 96 and 98. The controller 18 may switch all of the power supplies 84, 88, 96 and 98 together or ... *may set them individually in response to power levels being drawn from each of them.*”). Thus, in my opinion, *Hirst* discloses that “said power converter operational state” and “said another power converter operational state” are different.

99. Moreover, *Hirst* also discloses the system operational state of multiple loads can also differ. *See id.*, 8:44-49 (“The controller 18 may switch all of the power supplies 84, 88, 96 and 98 together or may switch them in a preferred order, or may set them individually in response to *power levels being drawn from each of them.*”); *see also id.*, 4:27-31 (disclosing multiple different loads).

100. *Hirst* thus discloses each limitation of claim 8.

H. Claim 9

- i. **9: “The power system as recited in claim 7 wherein said power converter and said another power converter are configured to provide power to said load and said another load, respectively.”**

101. As I describe above for claims 6 and 7, *Hirst* discloses a power system

including “*another load*” and “*another power converter*” (and the associated states, signals, and command) under the control of the same “power system controller.” And as I also describe above for claims 6 and 7, the “power converter” and “another power converter” are configured to provide power to “said load” and “said another load” respectively. *See* Sections IX.E (claim 6) and IX.F (claim 7).

I. Claim 10

- i. 10: “The power system as recited in claim 7 wherein said power system controller is configured to sequentially operate said power converter and said another power converter.”**

102. As I describe above for claim 7, the multiple power converters of *Hirst*’s power system each can have a different requirement and power converter operational state. Moreover, *Hirst* discloses that controller 18 (i.e., the power system controller) controls the operational states of the multiple power converters “in a preferred order” (i.e., sequentially). EX1003, 8:42-49 (“The first frequency f_{HI} and the second frequency f_{LO} need not be the same for each of the power supplies 84, 88, 96 and 98. The *controller 18 may switch all of the power supplies 84, 88, 96 and 98* together or may switch them *in a preferred order*, or may set them individually in response to power levels being drawn from each of them.”), Fig. 6; *see also* Section IX.F (claim 7). Thus, in my opinion, *Hirst* discloses each limitation of claim 10.

J. Claim 11

- i. 11: “The power system as recited in claim 6 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

103. Claim 11 mirrors the language of claim 2, but depends from claim 6 instead of claim 1. Thus, *Hirst* discloses the additional elements of dependent claim 11 in the same manner as I describe above for claim 2. *See* Section IX.B.

K. Claim 12

- i. 12: “The power system as recited in claim 6 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.”**

104. Claim 12 mirrors the language of claim 3, but depends from claim 6 instead of claim 1. Thus, *Hirst* discloses the additional elements of dependent claim 12 in the same manner as I describe above for claim 3. *See* Section IX.C.

L. Claim 13

- i. 13: “The power system as recited in claim 12 wherein said power converter status is selected from the group consisting of: a fully operational status, a failure likely status, a failed status, and an overloaded status.”**

105. As I describe above for claim 3 (which is mirrored by claim 12), *Hirst* explains that the “amount of ripple that is present in the output voltage V_O tends to increase as the amount of power being drawn from the MF switching power supply 30 increases.” *Id.*, 6:30-32. “When the ripple monitor 49 determines that the

ripple in the output voltage V_O is too high, the ripple monitor 49 *provides a signal to the controller 18* of FIG. 1 to increase the frequency of the MF switching power supply 30.” *Id.*, 6:32-37.

106. Thus, the status signal from the ripple monitor is an indication that the “power being drawn” from the power supply is too high (i.e., the power converter is overloaded) for the given switching frequency. *See id.*, 6:30-37. The power converter status signal from ripple monitor 42 therefore indicates an “overload status” at the given frequency.

107. In addition, the ’759 Patent describes a “Failure Likely” status as “Power converter operating with reduced operational capability,” and further associating “Failure Likely” with “a high level of ripple voltage.” EX1001, Table II, 20:9-14. Thus, the power converter status signal from *Hirst’s* ripple monitor indicating that the “ripple in the output voltage V_O is too high” (EX1003, 6:32-37) also serves as a failure likely status as recited in claim 13. One of the key requirements of a power converter is to control and minimize the output voltage ripple. EX1009, 25-27. Large output voltage ripple can, for example, cause a short in the circuit or severely impact the load. Furthermore, ripple has many drawbacks including wasting power, lowering efficiency, impacting the load circuits, heating components, increasing noise, and other undesirable impacts. Excess ripple may also increase noise, increase ground bounce and ground noise,

and potentially damage the power-converter circuit and/or the load circuit.

108. Accordingly, *Hirst* discloses claim 13 in multiple ways.

M. Claim 15

- i. **15: “The power system as recited in claim 6 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

109. Claim 15 mirrors the language of claim 5, but depends from claim 6 instead of claim 1. Thus, *Hirst* discloses the additional elements of dependent claim 15 in the same manner as I describe above for claim 5. *See* Section IX.D.

N. Claim 16

- i. **16[pre]: “A method of operating a power system coupled to a load, comprising:”**

110. Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Hirst* thus discloses claim 16[pre] in the same manner as described above for claim 6 (and similar elements of claim 1). *See* Sections IX.A.i (claim 1[pre]) and IX.E.i (claim 6[pre]); *See also* EX1003 (*Hirst*), 1:13-15 (“The invention relates to multiple frequency switching power supplies and *methods to operate* a switching power supply.”).

- ii. **16[a]: “receiving a signal indicating a system operational state of said load;”**

111. As I describe above for claims 1[pre] and 6[a], *Hirst* discloses a power system controller that receives a signal indicating a system operational state

of a load. Thus, for the same reasons I describe in Sections IX.A.i (1[pre]) and IX.E.ii (6[a]), *Hirst* discloses method step 16[a].

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

112. As I describe above for claims 1[pre] and 1[b], *Hirst* describes a controller 18 that receives a signal indicating the system operational state of the load. *See* Sections XI.A.i (1[pre]) and XI.A.iii (1[b]); *see also* EX1003, 8:27-33 (describing “controller 18” acting “in response to signals from the power monitor 22 of FIG. 1”). As a function thereof, a controller within the power converter receives a command from controller 18 to enter one of two power converter operational states: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. *See* EX1003, 7:66-8:5; *see also id.*, 8:5-8 (describing power supply entering “standby mode” when “laser printer 10 of FIG. 1 enters the standby mode), EX1003, 3:17-24 (“Commands from a print engine controller *select a first switching frequency* for the power supply when the printer is in *a normal mode* of operation and *select a second switching frequency* for the power supply when the printer is in *a standby mode* of operation.”).

113. In my opinion, *Hirst* thus discloses that a power converter operational state is generated, by the power converter for example, as a function of the system operational state of the load.

iv. 16[c]: “inducing a power converter to enter said power converter operational state; and”

114. As described for claim 1[b] and claim 6[a], *Hirst* discloses that the power converter receives a command from controller 18 to enter one of two power converter operational states: (i) a “normal mode of operation” with a high switching frequency “ f_{HI} ”, or (ii) a “standby mode of operation” with a low switching frequency “ f_{LO} ”. See EX1003, 7:66-8:5; see also *id.*, 3:17-24 (“Commands from a print engine controller *select a first switching frequency* for the power supply when the printer is in *a normal mode* of operation and *select a second switching frequency* for the power supply when the printer is in *a standby mode* of operation.”); see also Sections IX.A.iii (1[b]) and IX.E.ii (6[a]). Thus, in my opinion, *Hirst* thus discloses that controller 18, for example, induces a power converter to enter said power converter operational state.

v. 16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”

115. The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Hirst* discloses claim 16[d] in the same manner as I describe

above for claims 1[b]-[c]. *See* Sections IX.A.iii-iv.

- vi. **16[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

116. Claim 16[e] is identical to claim 1[d]. Thus, claim 16[e] is disclosed by *Hirst* in the same manner as I describe above for claim 1[d]. *See* Section IX.A.v.

O. Claim 17

- i. **17[pre]: “The method as recited in claim 16: wherein said power system is coupled to another load and further comprising:”**

17[a]: “receiving another signal indicating another system operational state of said another load;”

17[b]: “generating another power converter operational state as a function of said another system operational state;”

17[c]: “inducing another power converter to enter said another power converter operational state; and”

17[d]: “providing a signal to control a duty cycle of another power switch of said another power converter as a function of an output characteristic thereof and in accordance with said another power converter operational state,”

17[e]: “thereby regulating an internal operating characteristic of said another power converter to improve an operating efficiency thereof as a function of said another system operational state.

117. Similar to the way claim 7 substantively mirrors the language of claim 6 with the addition of “*another* load” and “*another* power converter” (and the

associated states, signals, and command), claim 17 substantively mirrors the language of claim 16 with the addition of “*another* load” and “*another* power converter” performing the same steps recited in claim 16. *Compare* claim 17 [pre]-17[e] and claim 16[pre]-16[e]; *see also* EX1007, 2 (side-by-side comparison of claims 16 and 17).

118. Thus, for the same reasons I describe above for claim 7 and claim 16, the power system of *Hirst* including multiple power converters and loads respectively coupled thereto discloses each step recited in claim 17. *See* Sections IX.F (claim 7) and IX.N (claim 16).

P. Claim 18

- i. 18: “The method as recited in claim 17 wherein said power converter and said another power converter are operated sequentially.”**

119. Claim 18 is similar to claim 10, but depends from claim 17 instead of claim 7, and is in the form of a method claim. As I describe above for claim 10 in Section IX.I (which in turn references claim 7), the multiple power converters of *Hirst*’s power system each can have a different power converter operational state. Moreover, *Hirst* discloses that controller 18 (i.e., the power system controller) controls the operational states of the multiple power converters “in a preferred order” (i.e., sequentially). EX1003, 8:42-49 (“The first frequency f_{HI} and the second frequency f_{LO} need not be the same for each of the power supplies 84, 88,

96 and 98. The *controller 18 may switch all of the power supplies 84, 88, 96 and 98* together or may switch them *in a preferred order*, or may set them individually in response to power levels being drawn from each of them.”), Fig. 6; *see also* Section IX.F (claim 7). Thus, in my opinion, *Hirst* discloses each limitation of claim 18.

Q. Claim 19

- i. 19: “The method as recited in claim 16 further comprising receiving a signal indicating a power converter status of said power converter and generating said power converter operational state as a function thereof.”**

120. Claim 19 is similar to claim 3, but depends from claim 16 instead of claim 1, and is in the form of a method claim. *Hirst* discloses the additional elements of dependent claim 19 in the same manner as I describe above for claim 3. *See* Section IX.C.

R. Claim 20

- i. 20: “The method as recited in claim 16 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

121. Claim 20 is similar to claim 5, but depends from claim 16 instead of claim 1. *Hirst* discloses the additional elements of dependent claim 20 in the same manner as I describe above for claim 5. *See* Section IX.D.

X. GROUND 1B: HIRST RENDERS OBVIOUSNESS CLAIMS 1-3, 5-13, and 15-20

122. As I describe above for Ground 1A, *Hirst* discloses each element of claims 1-3, 5-13, and 15-20, and therefore anticipates those claims.

123. To the extent that one considers the disclosures of *Hirst* that I rely upon in Ground 1A to represent separate embodiments within *Hirst*, a POSITA in my opinion would have nonetheless viewed them together as predictable variations of each other when considering the disclosure of *Hirst*. For example, I note that the disclosures of *Hirst* with reference to, for example, Figures 1, 2, 5, and 6, are all aspects of *Hirst*'s inventive concept relating back to the system-level block diagram shown in Figure 1. *See* EX1003, 6:29-37 (describing ripple monitor 49 of Figure 2 as providing signal to controller 18 of Figure 1), 7:63-8:8 (relating "controller 18" in Figure 5 to Figure 1), 8:27-33 (relating "controller 18" in Figure 6 to Figure 1). Indeed, the disclosures with respect to each of these figures are complementary to each other and compatible with each other.

124. Given the advantages described in *Hirst*, it is my opinion that a POSITA would have been motivated, and capable, to combine those embodiments. Therefore, claims 1-3, 5-13, and 15-20 are also rendered obvious by *Hirst*. For example, as I describe above in Ground 1A (*see* Section IX), *Hirst* discloses, and therefore also at least suggests to a POSITA, each element recited of claims 1-3, 5-13, and 15-20.

A. Claims 2 and 11

125. As I describe in Section IX.B, *Hirst* discloses a power converter configured to transition between different switching-frequency states (i.e., power converter operational states). EX1003, 7:63-8:8. A POSITA would have found it obvious that the transition from one switching-frequency state to the other could be completed within a transition time, for example a time bound by the period of one cycle at the new switching frequency. Thus, *Hirst* in view of the knowledge of a POSITA renders obvious claims 2 and 11.

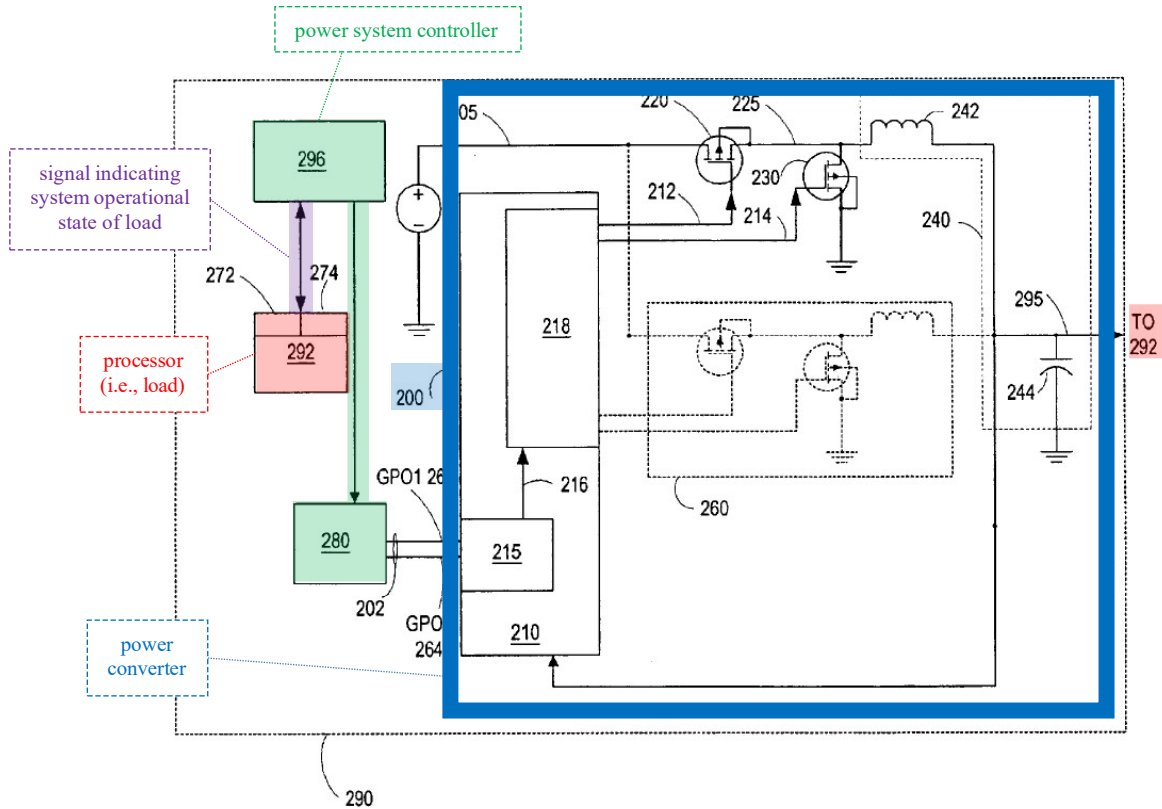
XI. GROUND 2A: CHAGNY ANTICIPATES CLAIMS 1-2, 4-6, 11, 14-16, and 20

126. In my opinion, *Chagny* discloses each element of Claims 1-2, 4-6, 11, 14-16, and 20, and thus anticipates those claims.

A. Claim 1

- i. 1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

127. *Chagny* discloses a voltage regulator module (“VRM”) (i.e., a power converter). EX1004, Abstract. “The VRM 200” shown in Figure 2A, “is operable to receive a direct current (DC) voltage input 205 and generate a regulated DC voltage output 295.” EX1004, 3:54-56.



EX1004, Fig. 2A (annotated). As shown in Figure 2A, “the regulated DC voltage output 295 provides power to a processor 292.” EX1004, 3:56-58. Processor 292 is thus a load coupled to VRM 200.

128. *Chagny* explains that the “loading, usage or activity level” of “processor 292” (i.e., the system operational state of the load) will “vary depending on the number of instructions executed within a predefined time interval.” *Id.*, 4:18-20; *see also* 4:20-34 (describing exemplary “high,” “medium,” and “low” activity levels). And as shown in Figure 2A, software program 296 receives a signal from processor 292 (i.e., the load) indicating the activity level of the load (i.e., indicating the system operational state of the load). EX1004, 4:35-43 (“In

one embodiment, a software program 296, which may be included in the operating system (not shown) of the device 290, monitors the processor 292 loading. The software program 296 may utilize predictive techniques to forecast the processor 292 loading by analyzing the processor instruction pipeline stack.”).

129. Based on the detected activity level, software program 296 generates and sends an “activity input 202” signal to controller 210 of VRM 200 (i.e., the power converter). EX1004, 4:40-43 (“Based on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292.”). And as shown in Figure 2A, the “activity input 202” signal may be sent to VRM 200 via I/O controller hub (ICH) 280. *Id.*, Fig. 2A (illustrating I/O controller hub (ICH) 280), 4:46-61 (describing bits stored in I/O controller hub 280). Accordingly, *Chagny*’s software program 296,⁴ either alone or collectively with I/O controller hub (ICH) 280, may

⁴ The controller is capable of monitoring the processor activity and loading and provides certain control functions via software or hardware means, as understood by a POSITA. Here, the power system controller of *Chagny* monitors the processor loading by examining the instructions being executed via “a software program” “included in the operating system” of the device to “monitor[] the processor 292 loading.” EX1004, 4:35-37. Similarly, the ’759 Patent states “the power system controller PSC” can be “separate from the servers SVR” or may be

serve as the power system controller⁵ recited in claim 1[pre].

130. In my opinion, *Chagny* thus discloses each element of claim 1[pre].

- i. **1[a]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and”**

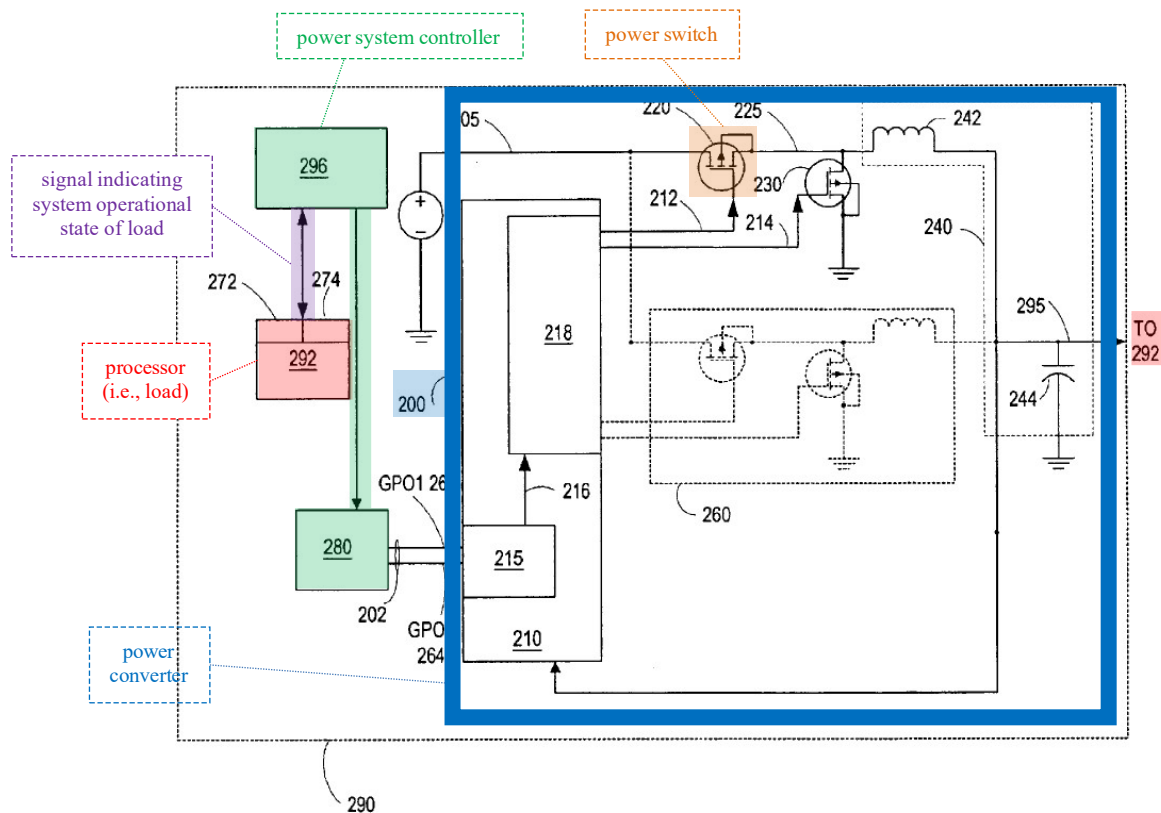
131. The switches 220 and 230, inductance L 242, and capacitor C 244, are configured in what is known in the art as a “buck” topology. *See* EX1004 (*Chagny*), 1:51-59 (describing “buck” DC-DC converter); *see also* EX1001 (’759 Patent), Fig. 2, 8:57-9:18 (describing similar configuration in Figure 2 as a “buck power converter”). *Chagny*’s charge switch 220 serves as a “power switch” configured to conduct for a duty cycle to provide a regulated output as recited in claim 1[a].

132. I note that *Chagny*’s switches 220 and 230 as shown in Fig. 2A are similarly configured to alternate between opposing on and off states, similar to

“an element of one or more servers SVR.” EX1001, 20:58-61. A POSITA would have understood the load (processor or server SVR) power consumption is related to the number of processor instructions being executed per second, commonly referred to MIPS (Millions of instructions per second).

⁵ Furthermore, the I/O controller hub (ICH) 280 alone may also serve as the “power system controller” of claim 1[pre]. The signal shown in Figure 2A from software program 296 to I/O controller hub (ICH) 280 serves as the signal indicating a system operational state of the load.

those of the buck converter shown in Fig. 2 of '759 patent. *See* EX1004 (*Chagny*), 5:32-40 (“During a charge cycle the charge switch 220 is closed and the discharge switch 230 is open. During a discharge cycle the charge switch 220 is open and the discharge switch 230 is closed. The opening and closing of the charge and discharge switches 220 and 230 is controlled by the charge and discharge control signals 212 and 214 respectively.”); EX1001 ('759 Patent), 8:67-9:27 (describing “main power switch Q_{main} is enabled to conduct by a gate drive signal D for a primary interval” and how during a “complementary interval” the “switch Q_{main} is transitioned to a non-conducting state and an auxiliary power switch Q_{aux} is enabled to conduct by a complementary gate drive signal $1-D$ ”).



EX1004, Fig. 2A (annotated).

133. A “buck” converter, also known as step down converter, is and was a well-known power converter topology, which produces a lower DC output voltage than the input DC voltage. EX1009 (Mohan), 19.

134. It was well-known in the art that, in the baseline equation for a buck power converter, the output voltage is equal to the input voltage times the duty cycle of the high-side switch (referred to as charge switch 200 in *Chagny*), where the duty cycle is the ratio of the on-time (i.e., conduction-time) of the high-side switch to the overall switching period. EX1009 (Mohan), 19 (p.164) (deriving equation for buck in continuous conduction mode). Consistent with this understanding, *Chagny* describes how charge switch 220 (i.e., the power switch) and discharge switch 230 turn on and off in an alternating fashion from each other. EX1004, 5:34-40, 6:45-49.

135. The output of the switches 220 and 230 at node 225 is a pulse-width modulated (PWM) signal. The voltage at node 225 is a square wave that alternates between the DC voltage input 205 and ground. EX1004, 5:40-42 (“The DC voltage input 225 is ‘chopped’ by the charge switch 220 to generate the switched DC voltage output 225.”). The square wave at node 225 therefore has an average voltage over time that is equal to the input voltage 205 times the duty cycle of the charge switch 220.

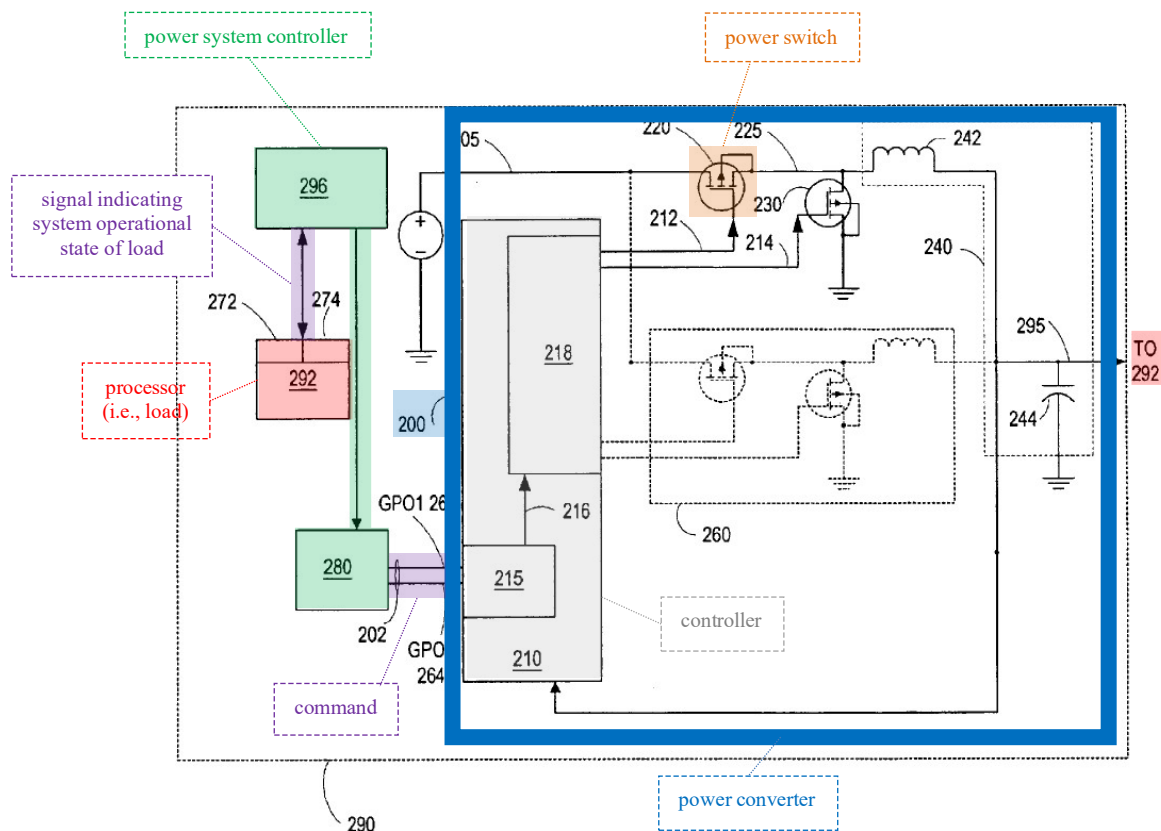
136. The pulse-width modulated square wave at node 225 is then filtered by inductance 242 and capacitor 244 to provide a regulated output voltage based on the average value of the square wave (i.e., based on the duty cycle of charge switch 220). *See* EX1004, Fig. 2A, 5:44-46 (“The square wave ... has an average voltage equal to the required output voltage.”); 5:47-51, (“[T]he filter module 240 includes an inductance L 242 and a capacitor C 244. The filter module 240 filters the switching frequency 216 from the switched DC voltage output 225 and generates the regulated DC voltage output 295.”); 4:63-65 (“The controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200.”).

137. Thus, in my opinion, based on *Chagny*’s disclosure, a POSITA would understand that “charge switch 220” (i.e., the power switch) is configured to conduct for a duty cycle to provide “regulated DC voltage output 295” (i.e., a regulated output characteristic) at the output of VRM 200 (i.e., at the output of the power converter). *Chagny* therefore discloses each limitation of claim 1[a].

- i. **1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”**

138. *Chagny*’s VRM 200 includes a “controller module 210” (i.e., the power-converter **controller**), configured to receive “activity input 202” (i.e., the command) from the **power system controller** identified above in Section XI.A.i

for claim 1[pre]. EX1004, 4:62-67 (“The controller module 210 includes a frequency selector module 215,” which “is operable to receive the activity input 202”); *see also id.*, 2:62-67 (“In one embodiment, a method for generating the regulated DC voltage output of the VRM receiving the activity input 202 indicative of levels of activity of the processor. A first switching frequency is selected from a plurality of switching frequencies of the VRM.”), 4:46-51 (“In one embodiment, the activity input 202 includes 2 bits, defined as General Purpose Output bits GPO1 262 and GPO2 264. The 2 bits are used to define up to 4 activity levels of the processor 292. In alternative embodiments, additional bits may be used to defined more than 4 activity levels of the processor 292.”).



EX1004, Fig. 2A (annotated).

139. As I describe above for claim 1[pre], activity input 202 (i.e., the **command**) to the controller 210 is generated by *Chagny*'s power system controller as a function of the signal indicating the "activity level" (i.e., the system operational state) of processor 292. *See* Section XI.A.i. In turn, *Chagny*'s controller 210 selects different switching frequency states (i.e., power converter operational states)⁶ based on activity input 202 (i.e., the command). EX1004, 4:66-5:3 ("The frequency selector module 215 is operable to receive the activity input 202 ... and select a switching frequency 216 from a plurality of switching frequencies as an output, which dynamically matches the level of activity of the processor 292."), 5:9-12 ("[T]he controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292."); *see also id.*, 5:3-8 ("In one embodiment, the plurality of switching frequencies exactly corresponds to the levels of activity of the processor 292. For example, in the embodiment having low, medium and high activity levels there are 3 corresponding low 130, medium 140 and high 150 switching frequencies."), 5:12-18 ("When the activity of the processor 292 is high, the switching frequency 216 is selected to be high 150 to

⁶ The '759 Patent lists "reduced switching frequency" as an example among "power converter operational state" descriptions. *See* EX1001, Col. 19, Table I.

advantageously limit the voltage ripples and maintain the regulated DC voltage output 295 above its specified minimum value. When the activity of the processor 292 is low, the switching frequency 216 is selected to be low 130 to save power.”), 4:46-49 (“In one embodiment, the activity input 202 includes 2 bits, defined as General Purpose Output bits GPO1 262 and GPO2 264. The 2 bits are used to define up to 4 activity levels of the processor 292.”).

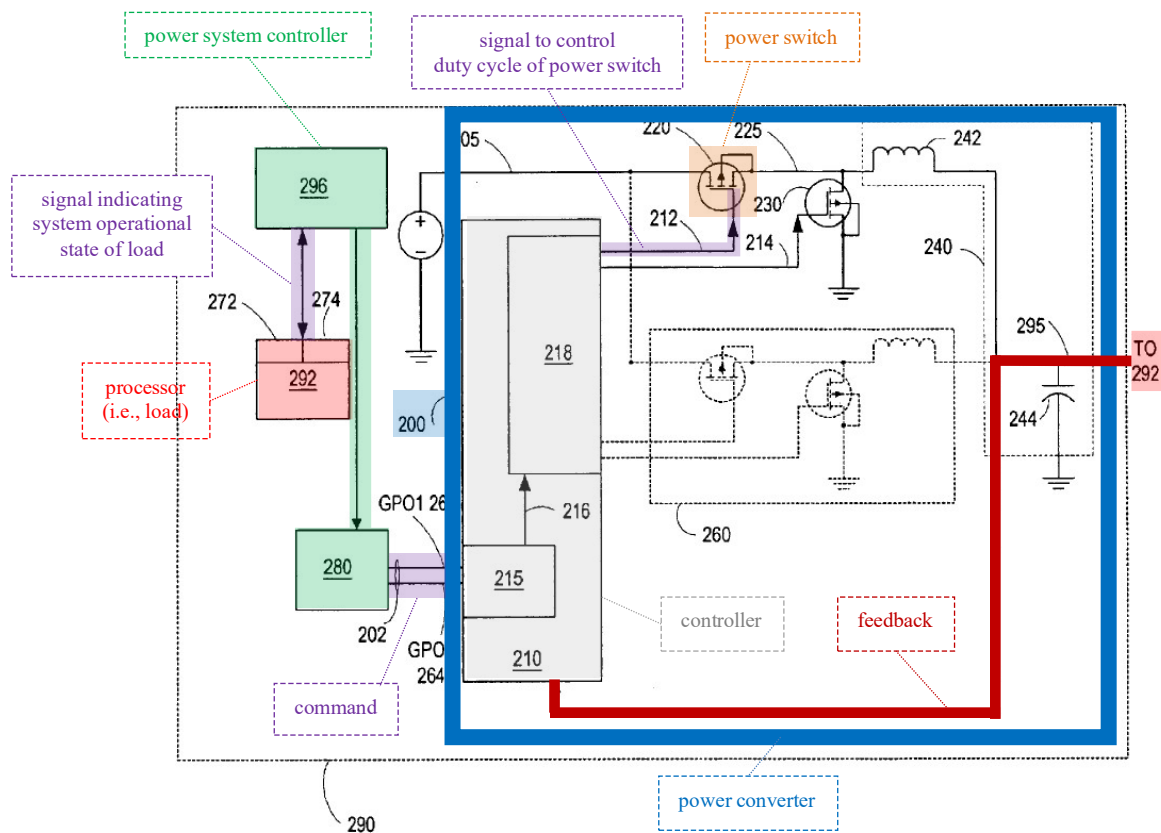
140. Thus, in my opinion, *Chagny* discloses each limitation of claim 1[b].

- i. **1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

141. *Chagny*’s controller module 210 (i.e., **said controller**) includes “FET driver module 218” for generating signals 212 and 214 to control switches 220 and 230 respectively. EX1004, 4:62-63; *see also id.*, 3:60-4:7 (“The VRM 200 for generating the regulated DC voltage output 295 includes: a) a controller module 210 operable to receive an activity input 202 indicative of levels of activity of the processor 292, b) a charge switch 220 operable to receive the DC voltage input 205 and generate a switched DC voltage output 225 in response to receiving a charge control signal 212 from the controller module 210, c) a discharge switch 230 electrically coupled to the controller module 210 and the charge switch 220, the controller module 210 generating a discharge control signal 214 to provide a discharge path for the switched DC voltage 225 while the charge switch 220 is

open ...”).

142. As shown in Figure 2A, FET driver module 218 provides “charge control signal 212” to control the turning on and off of charge switch 220 (i.e., said power switch). *Id.*, 5:38-40 (“The opening and closing of the charge and discharge switches 220 and 230 is controlled by the charge and discharge control signals 212 and 214 respectively.”).



EX1004, Fig. 2A (annotated).

143. As I describe above for claim 1[a], the duty cycle of charge switch 220 (i.e., the power switch) determines the voltage level of *Chagny*’s “regulated DC voltage output 295.” *See* Section XI.A.ii. And as shown in Figure 2A above,

“controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200.” EX1004, 4:63-65; *see also id.*, 9:5-7, 10:14-16. Because it is the duty cycle of charge switch 220 that determines the output voltage (*see, e.g.*, EX1009, 19), and because *Chagny* explicitly states that controller module 210 regulates the DC output voltage as a function of the feedback (EX1004, 4:63-65), a POSITA in my opinion would have understood from *Chagny*’s disclosures that controller module 210 is configured to control the duty cycle of charge switch 220 as a function of the feedback from the regulated DC voltage output 295 (i.e., as function of said output characteristic).

144. In addition, “FET drive module 218” within controller 210 sets the switching frequency of charge switch 220 in accordance with “activity input 202 (i.e., the command). *See* EX1004, 5:28-31 (“The FET driver module 218 is operable to receive the selected value of the switching frequency 216 and generate the charge and discharge control signals 212 and 214, each having the switching frequency 216.”); *see also id.*, 4:66-5:2, 5:34-46.

145. Thus, in my opinion, *Chagny* discloses each limitation of claim 1[c].

- i. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

146. *Chagny*’s controller module 210 “dynamically changes the switching frequency 216” (i.e., regulates an internal operating characteristic) of VRM 200 in

response to the activity input 202 indicative of the activity level of the processor 292. EX1004, 5:9-12 (“Thus the controller module 210 dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292. When the activity of the processor 292 is high, the switching frequency 216 is selected to be high 150 to advantageously limit the voltage ripples and maintain the regulated DC voltage output 295 above its specified minimum value. When the activity of the processor 292 is low, the switching frequency 216 is selected to be low 130 to save power.”); *see also id.*, 4:40-45 (“Based on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292. The activity input 202 may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis.”), 5:3-8, 5:12-18.

147. *Chagny* expressly describes how the switching frequency of the VRM (i.e., the internal operating characteristic of said power converter) is varied to “improve efficiency” as a function of the processor activity level (i.e., said system operational state). EX1004, 2:59-61 (“To improve efficiency, the VRM advantageously changes the switching frequency of the VRM in accordance with the activity of the processor.”); *see also id.*, 5:16-23 (describing selection of low switching frequency when “activity of processor is low” to “save power” and

improve “VRM 200 efficiency”); 3:9-10.

148. Thus, in my opinion, *Chagny* discloses each limitation of claim 1[d].

B. Claim 2

- i. **2: “The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

149. I understand that although claim 2 recites “within a transition time,” Claim 2 does not set an upper limit, or otherwise define the “transition time” recited therein.

150. As I describe above in Section XI.A.iii for claim 1[b], *Chagny*’s power converter is configured to dynamically change between different switching-frequency states (i.e., power converter operational states) as a function of the activity level of the processor. EX1004, 4:66-5:3 (“The frequency selector module 215 is operable to receive the activity input 202. e.g., GPO1 262 and GPO2 264, and select a switching frequency 216 from a plurality of switching frequencies as an output, which dynamically matches the level of activity of the processor 292.”); *see also id.*, 5:3-18.

151. *Chagny* determines the number of instructions executed in a given predefined time to assess the processor activity level. EX1004, 4:18-23 (“The processor 292 loading, usage or activity level will vary depending on the number of instructions executed within a predefined time interval. The processor 292 is

described to be 100% or fully loaded if it is executing the maximum number of instructions per specification within the predefined time interval.”).

152. *Chagny* also discloses: “The demand for power required by the processor 292 is advantageously controlled by limiting the number of instructions executed for *a predefined time period*. This control mechanism ensures that the VRM 200 *reacts responsively and on time according to the processor 292 demand*.” *Id.*, 5:62-66. In other words, *Chagny* sets a “predefined period of time,” within which VRM 200 transitions from one switching-frequency state to another, before changing the activity level of processor 292. *Id.* Here, the “predefined period” that the processor sets is the transition time within which the VRM changes power converter operational states in order to be “on time.”

153. In my opinion, *Chagny* thus discloses each limitation of claim 2.

C. **Claim 4**

- i. **4: “The power converter as recited in claim 1 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

154. The ’759 Patent background explains that a “core state” of a processor is “under software operating system control” and affects the “level of power consumption” of the processor. EX1001, 4:23-26. According to the ’759 Patent, the highest core state is where the processor executes instructions “at its full operational level.” *See id.*, 4:26-37. On the other hand, various core-state “sleep

levels” are “achieved by halting instruction execution.” *Id.*, 4:28-37. In other words, the “core state” as described in the ’759 Patent background specifies the activity level (e.g., the rate at which instructions are executed) of the processor.

155. *Chagny* discloses that the processor 292 (i.e., the load) activity level is determined based on the number of instructions executed within a time interval. EX1004, 4:18-23 (“The processor 292 loading, usage or activity level will vary depending on the number of instructions executed within a predefined time interval. The processor 292 is described to be 100% or fully loaded if it is executing the maximum number of is instructions per specification within the predefined time interval.”).

156. *Chagny* discloses that “the software program 296 generates the activity input 202 indicative of levels of activity of the **processor 292**,” (i.e., the load) which “includes 2 bits, defined as General Purpose Output bits GPO1 262 and GPO2 264. . . used to define up to 4 activity levels of the processor 292.” *Id.*, 4:43-49; *see also id.*, 4:23-30 (defining high, medium, and low activity level based on the processing loading). Moreover, “the software program 296 defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clock cycle.” *Id.*, 5:57-61; *see also id.*, 6:3-4. Accordingly, the activity level of processor 292 (i.e., system operational state of the load) depends on at least a core state of the

processor 292.

157. Thus, in my opinion, *Chagny* discloses each limitation of claim 4.

D. Claim 5

- i. **5: “The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

158. The '759 Patent describes a “Fully Operational” power converter operational state as “[a]ll power converter components operational at full performance level,” as opposed to other states with “reduced switching frequency.” EX1001, Table I.

159. *Chagny* discloses assessing the load processor activity level and selecting the power converter operational state based on the load activity level. *See* EX1004, 4:23-35 (“[T]he activity level (not shown) of the processor 292 may be grouped into 3 levels as follows: a) a high activity level ..., b) a medium activity level ..., and c) a low activity level Thus any loading value for the processor 292 may be grouped under the high, the medium or the low activity level. In alternative embodiments, the number of groups and the range definition criteria within each group may vary.”).

160. *Chagny* discloses a power converter operational state wherein “the switching frequency 216 is selected to be high 150 to advantageously limit the voltage ripples” EX1004, 5:9-23 (“Thus the controller module 210

dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the processor 292. When the activity of the processor 292 is high, the switching frequency 216 is selected to be high 150 to advantageously limit the voltage ripples and maintain the regulated DC voltage output 295 above its specified minimum value. When the activity of the processor 292 is low, the switching frequency 216 is selected to be low 130 to save power. In this case, the voltage ripples may be higher as the voltage required by the processor 292 tends to stay in the middle of its operating range. The selection of the low 130 frequency value for the switching frequency 216 advantageously improves the VRM 200 efficiency, as shown in FIG. 1.”). The highest switching-frequency state of *Chagny*’s VRM 200 represents a power converter state where all power converter components operate at full performance level (i.e., a fully operational power converter).

161. Thus, in my opinion, *Chagny* discloses each limitation of claim 5.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

162. Later elements of claim 6 require the “power system” of claim 6[pre] to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Chagny* discloses claim 6[pre] in the same manner that I describe above for claim 1[pre]. See Section XI.A.i.

- ii. **6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”**

163. As I describe above for claim 1[pre], *Chagny* discloses a power system controller configured to receive a signal indicating a system operational state of a load. *See* Section XI.A.i. And as I describe above for claim 1[b], the power system controller of *Chagny* sends a command to the power converter controller to enter a power converter operational state as a function of said signal. Thus, in my opinion, *Chagny* discloses a power system controller configured to “select” a power converter operational state as a function of the signal in the same manner as I describe above for claim 1[b]. *See* Section XI.A.iii. Therefore, *Chagny* discloses in my opinion each limitation of claim 6[a].

- iii. **6[b]: “a power converter, including:”**

164. As I describe above for claim 1[pre], *Chagny* discloses a power system that includes a power converter. *See* Section XI.A.i. For example, *Chagny* discloses voltage regulator module (VRM) 200 (i.e., power converter). EX1004, Abstract. The VRM 200 is “operable to receive a direct current (DC) voltage input 205 and generate a regulated DC voltage output 295.” *Id.*, 3:54-56. Therefore, *Chagny* discloses in my opinion each limitation of claim 6[b].

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”**

165. Claim 6[c] is identical to claim 1[a]. Thus, claim 6[c] is disclosed by

Chagny in the same manner as I describe above for claim 1[a] in Section XI.A.ii.

- v. **6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

166. Claim 6[d] restates limitations recited in claims 1[b]-[c].

1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state” 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”	6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”
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167. Thus, *Chagny* discloses claim 6[d] in the same manner as I describe above for claim 1[b]-[c] in Sections XI.A.iii and XI.A.iv.

- vi. **6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

168. Claim 6[e] is identical to claim 1[d]. Thus, claim 6[e] is disclosed by *Chagny* in the same manner as I describe above for claim 1[d] in Section XI.A.v.

F. Claim 11

- i. **11: “The power system as recited in claim 6 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

169. Claim 11 mirrors the language of claim 2, but depends from claim 6 instead of claim 1. Thus, *Chagny* discloses the additional elements of dependent claim 11 in the same manner as I describe above for claim 2. *See* Section XI.B.

G. Claim 14

- i. **14: “The power converter as recited in claim 6 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

170. Claim 14 mirrors the language of claim 4, but depends from claim 6 instead of claim 1. Thus, *Chagny* discloses the additional elements of dependent claim 14 in the same manner as I describe above for claim 4. *See* Section XI.C.

H. Claim 15

- i. **15: “The power system as recited in claim 6 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

171. Claim 15 mirrors the language of claim 5, but depends from claim 6 instead of claim 1. Thus, *Chagny* discloses the additional elements of dependent claim 15 in the same manner as I describe above for claim 5. *See* Section XI.D.

I. Claim 16

- i. **16[pre]: “A method of operating a power system coupled to a load, comprising:”**

172. Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Chagny* thus discloses claim 16[pre] in the same manner as described above for claim 6 (and similar elements of claim 1). *See* Sections XI.A.i (claim 1[pre]) and XI.E.i (claim 6[pre]); *See also* EX1004 (*Chagny*), 2:40-43 (“the present disclosure [] relates to a system and method for improving the efficiency of a VRM”).

- ii. **16[a]: “receiving a signal indicating a system operational state of said load;”**

173. As I describe above for claims 1[pre] and 6[a], *Chagny* discloses a power system controller that receives a signal indicating a system operational state of a load. Thus, for the same reasons I describe in Sections XI.A.i (1[pre]) and XI.E.ii (6[a]), *Chagny* discloses method step 16[a].

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

174. As I describe above for claims 1[pre] and 1[b], *Chagny* discloses that a switching-frequency state (i.e., a power converter operational state) is generated as a function of the activity level of the processor (i.e., as a function of the system operational state). *See* Sections XI.A.i and XI.A.iii; *see also* EX1004, 4:40-43 (“Based on the processor 292 loading and/or the forecasted values, the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292.”), 4:66-5:3 (“The frequency selector module 215 is operable to ... select a switching frequency 216 ... which dynamically matches the level of activity of the processor 292.”), 5:5-12 (disclosing switching frequencies states selected as function of the processor activity level).

175. Thus, in my opinion, *Chagny* discloses each limitation of claim 16[b].

iv. 16[c]: “inducing a power converter to enter said power converter operational state; and”

176. As I describe above for claim 1[b], *Chagny* discloses that VRM 200 enters different switching-frequency states (i.e., power converter operational states) based on activity input 202. *See* Section XI.A.iii. The activity input 202 therefore induces the VRM 200 to enter the power converter operational state. EX1004, 5:9-12 (the controller “dynamically changes the switching frequency 216 of the VRM 200 responsive to the activity input 202 indicative of the activity level of the

processor 292.”), 5:12-18, 4:46-49. Thus, in my opinion, *Chagny* discloses each limitation of claim 16[c].

- v. **16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”**

177. The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Chagny* discloses claim 16[d] in the same manner as I describe above for claims 1[b]-[c]. See Sections XI.A.iii-iv.

- vi. **16[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

178. Claim 16[e] is identical to claim 1[d]. Thus, claim 16[e] is disclosed by *Chagny* in the same manner as I describe above for claim 1[d]. See Section XI.A.v.

J. Claim 20

- i. **20: “The method as recited in claim 16 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

179. Claim 20 is similar to claim 5, but depends from claim 16 instead of

claim 1. *Chagny* thus discloses the additional elements of dependent claim 20 in the same manner as I describe above for claim 5. *See* Section XI.D.

XII. GROUND 2B: CHAGNY IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-2, 4-6, 11, 14-16, and 20

180. As I describe in Ground 2A, *Chagny* discloses a software program 296 that serves as the “power system controller” recited in the claims. *See, e.g.*, Section XI.A.i (1[pre]), XI.A.iii (1[b]). To the extent that one argues that the “power system controller” recited in the claims must be implemented in hardware, a POSITA would have found it obvious that *Chagny*’s “software program 296,” which may be “included in the operating system” of the device (EX1004, 4:35-37), could be executed on hardware such as processor 292 itself⁷ or a separate hardware controller.

181. In my opinion, a POSITA would have found it obvious to execute *Chagny*’s “software program 296,” which may be “included in the operating system” of the device (EX1004, 4:35-37), on processor 292 itself. *Chagny* explains that the “software program 296” monitors the processor loading by “analyzing the processor instruction pipeline stack” (EX1004, 4:37-40), and also sets “bits in a register of processor 292” to control the number or instructions

⁷ The ’759 Patent itself includes embodiments where “the power system controller PSC” is constructed as an element of the server (i.e., the load). EX1001, 18:24-33 and 20:58-61.

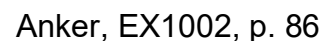
executed per cycle by the processor (*id.*, 5:57-61). Moreover, *Chagny* describes that a “processor” is “operable to execute the computing instructions,” which are “also known as a ‘software program,’” stored in memory. *Id.*, 7:36-41. Further, the Microprocessor Data Book by S.A. Money describes the basic architecture for well-known processor-based systems. *See* EX1015, 5 (describing processor-based systems with central processing unit (CPU), memory to store the instructions to be executed, and input/output ports); *see also id.*, 5 (Fig. 1.1). The Money book goes on to describe various types of processor-based devices, including those where the CPU and the memory are included together on a single chip. *Id.*, 10-11.

182. A POSITA would have also found it obvious that the software program 296 could be executed in a separate microcontroller, controller, or processor. Furthermore, the software program 296 could have been implemented in a FPGA (field programmable gate array), specific custom ASIC (application specific integrated circuits), or other hardware. A POSITA would have understood that the specific implementation would depend on the overall system configuration and would not change the functionality of the software program 296.

183. Accordingly, claims 1-2, 4-6, 11, 14-16, and 20 are also rendered obvious by *Chagny* in view of the knowledge of a POSITA.

184. As I describe above in Ground 2A, *Chagny* discloses each element of independent claims 1, 6, and 16. See Sections XI.A (claim 1), XI.E (claim 6), XI.I (claim 16). When further combined with *Clark*, the resulting combination further discloses and/or suggests to a POSITA in my opinion each element of dependent claims 3, 12-13, and 19, and therefore renders those claims obvious.

185. *Chagny* discloses an “information handling system device 290” that includes a processor 292 and a voltage regulator module (VRM) 200 for providing a regulated voltage to the processor 292.



EX1004, Fig. 2A (annotated). As I describe above for Ground 2A, *Chagny* describes changing the frequency of VRM 200 (i.e., power converter) to improve efficiency of the power converter when the activity of the processor is low. EX1004, 2:59-61 (“To improve efficiency, the VRM advantageously changes the switching frequency of the VRM in accordance with the activity of the processor.”); *see also id.*, 5:16-23 (describing selection of low switching frequency when “activity of processor is low” to “save power” and improve “VRM 200 efficiency”).

186. Like *Chagny*, *Clark* discloses a device (e.g., portable computer) that includes both a microprocessor (also referred to as “core logic 50”) and a voltage regulator 40 (i.e., a power converter) for providing a regulated voltage to the microprocessor. EX1005, 3:9-20, 3:31-33.

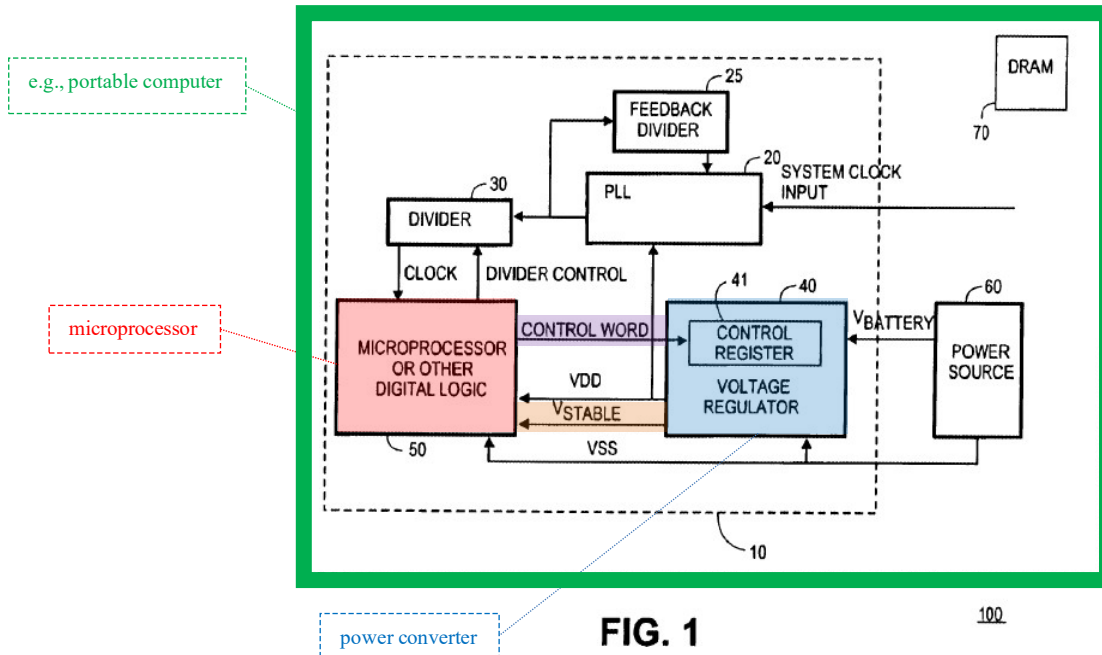


FIG. 1

EX1005, Fig. 1 (annotated).

187. *Clark* discloses that by reducing the clock frequency of the microprocessor, as well as reducing the voltage provided by the voltage regulator to the microprocessor, the power consumed by the microprocessor during light processing loads is “dramatically reduced.” *See id.*, 5:14-23; *see also id.*, Abstract (“[A]n integrated circuit has a voltage regulator and a clock divider that may be used to adjust the operational frequency and/or voltage potential of the integrated circuit to reduce the power consumption of the integrated circuit while in operation.”), 4:54-67, 3:44-60, Figs. 5 (illustrating different processing levels), Fig. 6 (illustrating power savings).

188. In my opinion, a POSITA would have been motivated to combine the information handling system device 290 of *Chagny* with the teachings of *Clark* to

improve the operating efficiency of the system. The underlying goal behind *Chagny*'s efficient power converter is to "extend the battery life" of the system. EX1004, Title. *Clark* furthers that goal by also improving the efficiency of the microprocessor system by changing the supply voltage and operating frequency of the microprocessor. EX1005, 4:54-67 ("Particular embodiments of the present invention may be used to reduce the power consumption of an integrated circuit while the integrated circuit is in operation. For example, if a user is executing an application that may be executed using a lower frequency without an appreciable degradation in performance experienced by the user, the frequency may be reduced to conserve power."), 5:14-23.

189. Therefore, with respect to *Chagny*'s power converter, a POSITA would have been motivated to incorporate *Clark*'s control of the power converter output voltage (reducing or increasing the processor supply voltage) based on the processor activity level with *Chagny*'s control over the power converter switching frequency based on the processor activity level resulting in higher system power consumption efficiency. For example, a POSITA would have been motivated to modify *Chagny*'s system to further include the control functions of *Clark* along with the "control word" and "Vstable" signals that *Clark* uses to communicate between the microprocessor and the power converter. See EX1005, 3:44-60 ("During the operation of integrated circuit 10, voltage regulator may provide core

logic 50 with an operational voltage range (e.g., $V_{dd}-V_{ss}$). In an alternative embodiment, voltage regulator 40 may comprise a control register 41 that may be set or programmed to indicate the voltage potentials to be provided. For example, core logic 50 may write a control word to control register 41 to indicate the voltage potentials to be provided by voltage regulator 40. As explained in more detail below, the voltage potential range provided to core logic 50 by voltage regulator 40 may be adjusted depending, at least on part, on the desired frequency at which core logic 50 is to operate.”), 5:24-36.

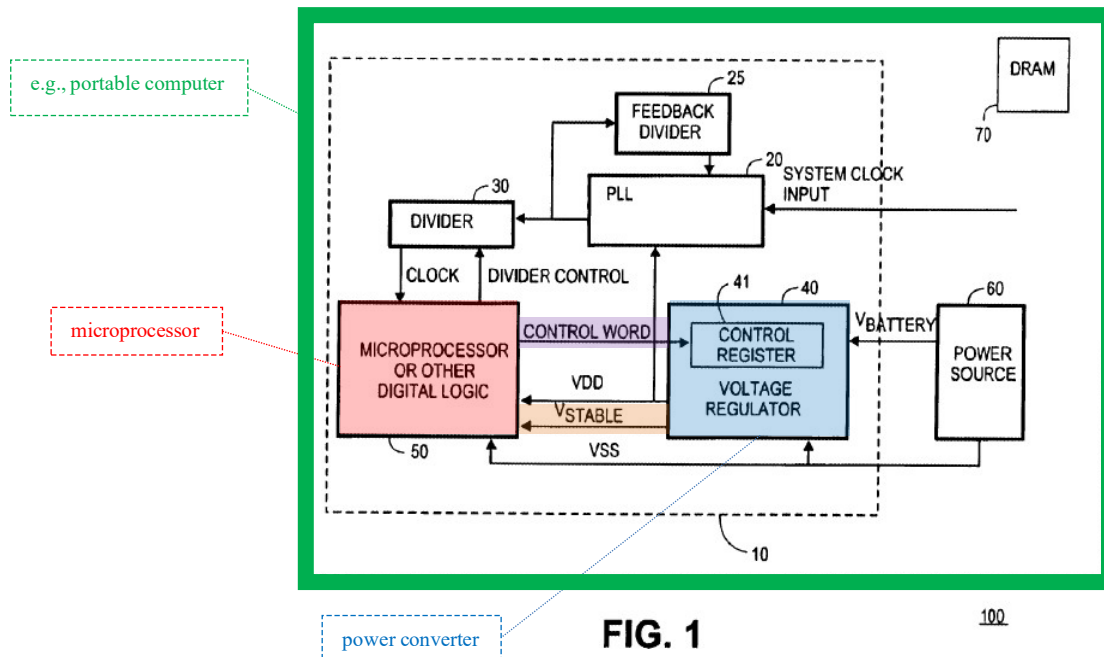
190. This combination represents the use of a known technique (i.e., *Clark*’s dynamic control of the power converter output voltage) to improve a similar device (i.e., *Chagny*’s system and voltage regulator module) in the same way. Moreover, a POSITA in my opinion would have a reasonable expectation of success because like the “control word” sent from *Clark*’s microprocessor to its power converter to control the output voltage based on processor loading (EX1005, 3:44-60, Fig. 1), *Chagny* is already configured to send control signals to its power converter based on the activity level of its processor (EX1004, 4:40-43, 5:9-12, Fig. 2A).

B. Claim 3

- i. **3: “The power converter as recited in claim 1 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.”**

191. As I describe above in Section XIII.A, a POSITA would have been motivated to incorporate *Clark*’s control over the power converter output voltage based on the processor activity level with *Chagny*’s VRM 200, which already includes control over the power converter switching frequency based on the processor activity level. Given that both types of control are based on the processor activity level, a POSITA would understand that, in the combination of *Chagny* and *Clark*, the commands to *Chagny*’s VRM 200 for updating the switching frequency would coincide with the commands to update the output voltage.

192. *Clark* discloses that a “Vstable” signal (i.e., a status signal) is sent from its power converter (referred to in *Clark* as a voltage regulator) back to the microprocessor to indicate whether a transition from one voltage to another has been completed. EX1005, 5:24-36.



EX1005, Fig. 1 (annotated).

193. According to *Clark*, the microprocessor (also referred to as “core logic”) “may wait until the *Vstable* signal is asserted” before instructing the power converter to further increase the output voltage to a new value. EX1005, 5:24-36, Fig. 2. In other words, *Clark* teaches waiting for the *Vstable* signal (i.e., the status signal) from the power converter to indicate that the converter output voltage transition is complete before making another transition.

194. Because the commands to *Chagny*’s VRM 200 for updating the switching frequency would coincide with the commands for updating the output voltage, a POSITA would understand that the commands to update the switching frequency state (i.e., the power converter operational state) would also be held until the *Vstable* signal (i.e., the status signal) is asserted and is valid, thus indicating

that prior transitions were complete.

195. The combination of *Chagny* and *Clark* thus renders obvious the additional limitations of dependent claim 3.

C. Claim 12

- i. 12: “The power system as recited in claim 6 wherein said power system controller is configured to receive a signal indicating a power converter status of said power converter, said power converter operational state being a function of said power converter status.”**

196. Claim 12 mirrors the language of claim 3, but depends from claim 6 instead of claim 1. Thus, the combination of *Chagny* and *Clark* discloses the additional elements of dependent claim 12 in the same manner as I describe above for claim 3. *See* Section XIII.B.

D. Claim 13

- i. 13: “The power system as recited in claim 12 wherein said power converter status is selected from the group consisting of: a fully operational status, a failure likely status, a failed status, and an overloaded status.”**

197. As I describe above for claim 3, *Clark* discloses that the *V*_{stable} signal (i.e., the status signal) is used to determine whether the power converter (referred to as a “voltage regulator” in *Clark*) is “changing,” or is instead “stable” (i.e., fully operational). EX1005, 5:27-36; *see also* Section XIII.B. The combination of *Chagny* and *Clark* thus renders obvious each limitation of claim 13.

E. Claim 19

- i. 19: “The method as recited in claim 16 further comprising receiving a signal indicating a power converter status of said power converter and generating said power converter operational state as a function thereof.”**

198. Claim 19 is similar to claim 3, but depends from claim 16 instead of claim 1, and is in the form of a method claim. The combination of *Chagny* and *Clark* thus discloses the additional elements of dependent claim 19 in the same manner as I describe above for claim 3. *See* Section XIII.B.

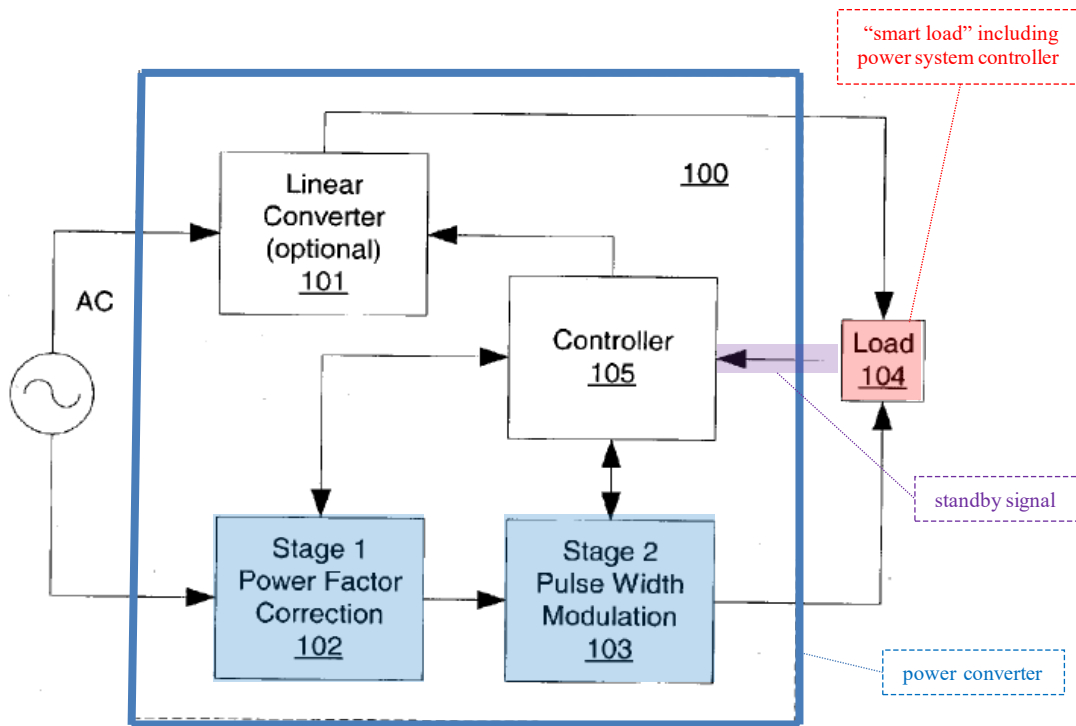
XIV. GROUND 3: HWANG IN VIEW OF THE KNOWLEDGE OF A POSITA RENDERS OBVIOUS CLAIMS 1-2, 4-6, 11, 14-16, and 20

199. In my opinion, *Hwang* in view of the knowledge of a POSITA discloses and/or suggests each element of Claims 1-2, 4-6, 11, 14-16, 20, and thus renders obvious those claims.

A. Claim 1

- i. 1[pre]: “A power converter coupled to a power system controller configured to receive a signal indicating a system operational state of a load coupled thereto, comprising:”**

200. *Hwang* discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006]. Like the power converter in Figure 3 of the ’759 Patent (EX1001, Fig. 3), *Hwang*’s power converter is a “two-stage power converter” with a “power factor correction (PFC) stage 102” and a “PWM stage 103” (EX1006, [0019]).



EX1006, Fig 1 (annotated).

201. As shown in Figure 1, the output of *Hwang*'s power converter 100 is coupled to a smart load 104. *See* EX1006, Fig. 1; *see also id.*, [0031] (describing load 104 as "smart load"), [0038]. *Hwang* discloses that smart load 104 "may include a microprocessor that may enter a standby mode during periods of low activity or non-use." *Id.*, [0031]; *see also id.*, [0021] ("where the load 104 is a microprocessor or controller, it may enter a standby or 'sleep' mode during periods of low activity for power conservation"). *Hwang* also discloses that smart load 104 sends a standby signal to the controller 105 within power converter 100. *Id.*, [0021] ("The controller 105 may sense a signal from the load 104 that indicates the level of the power drawn by the load 104. A standby signal from the load 104

may instruct the controller 105 to enter standby mode. For example, where the load 104 is a microprocessor or controller, it may enter a standby or “sleep” mode during periods of low activity for power conservation. While in standby mode, the controller 105 may disable the PFC stage 102. Also, while in standby mode, the controller 105 may cause PWM stage 103 to enter pulse-skipping mode or alternatively may disable the PWM stage 103 and enable the optional linear converter 101.”), [0031].

202. Based on *Hwang*’s disclosure of a smart load 104 that includes a “microprocessor” that enters a standby mode during periods of low activity (*id.*, [0031], [0021]), and based on a POSITA’s understanding of well-established principles of microprocessor operation, a POSITA in my opinion would have understood, or at least found it obvious, that the microprocessor within smart load 104 could include an internal control unit that controls the internal operations of the microprocessor, and that serves as a “power system controller” as recited in claim 1[pre] by receiving a signal indicative of the microprocessor’s activity level (i.e., indicative of the system operational state of the microprocessor load).⁸

⁸ An architecture with a power system controller built into a microprocessor load is similar to those described in the ’759 Patent itself where the “power system controller PSC” may be included as “an element of one or more servers SVR.” EX1001, 20:58-61.

Indeed, a POSITA would have found it obvious that such an internal control unit (i.e., the power system controller) would be included to in turn send a standby signal to the power converter as expressly disclosed by *Hwang*. EX1006, [0021], [0031].

203. As an example of well-known principles of microprocessor operation, the Money textbook published in 1990 illustrates and describes the general architecture known in the art for devices (e.g., the smart load 104 in *Hwang*) including microprocessors. EX1015, 5 (Fig. 1.1); *see also id.*, 10-11 (describing types of microprocessor based devices). Major blocks include, among others, memory, Input/Output (I/O) ports, and the central processing unit (CPU). *Id.*, 5 (Fig. 1.1).

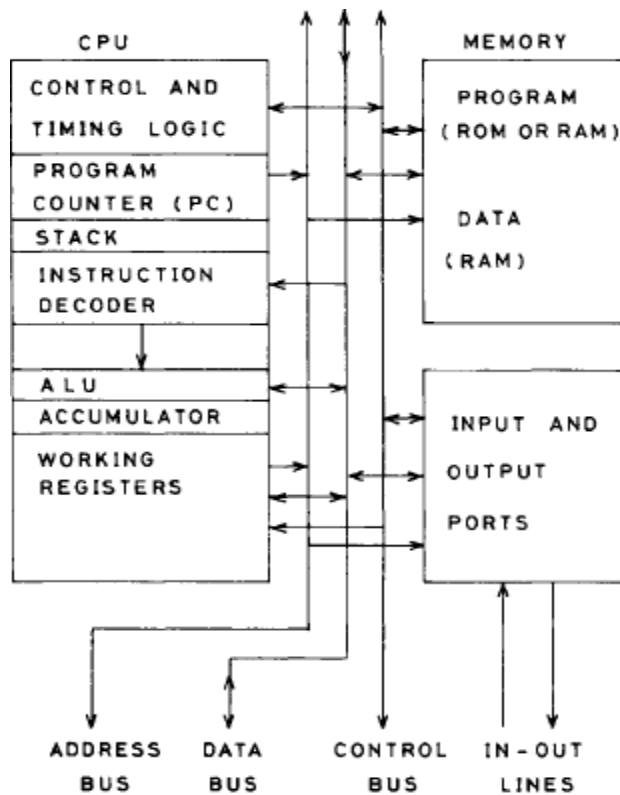


Fig. 1.1

EX1015, 5 (Fig. 1.1). As described in Money, the CPU of a microprocessor includes both control and execution units. *Id.*, 6-7. The control unit “is used to control the timing and sequence of operations in the system.” *Id.*, 5. Thus, in my opinion, a POSITA would have understood, or at least found obvious, that the microprocessor within *Hwang*’s smart load 104 includes a control unit that serves as the “power system controller” as recited by claim 1[pre] that receives a signal of the microprocessor’s activity level (i.e., indicative of the system operational of the microprocessor load). Indeed, a POSITA would have found it obvious that such a control unit (i.e., the power system controller) would be included to in turn send, via an I/O port, a standby signal to the power converter as disclosed by *Hwang*.

EX1006, [0021], [0031].

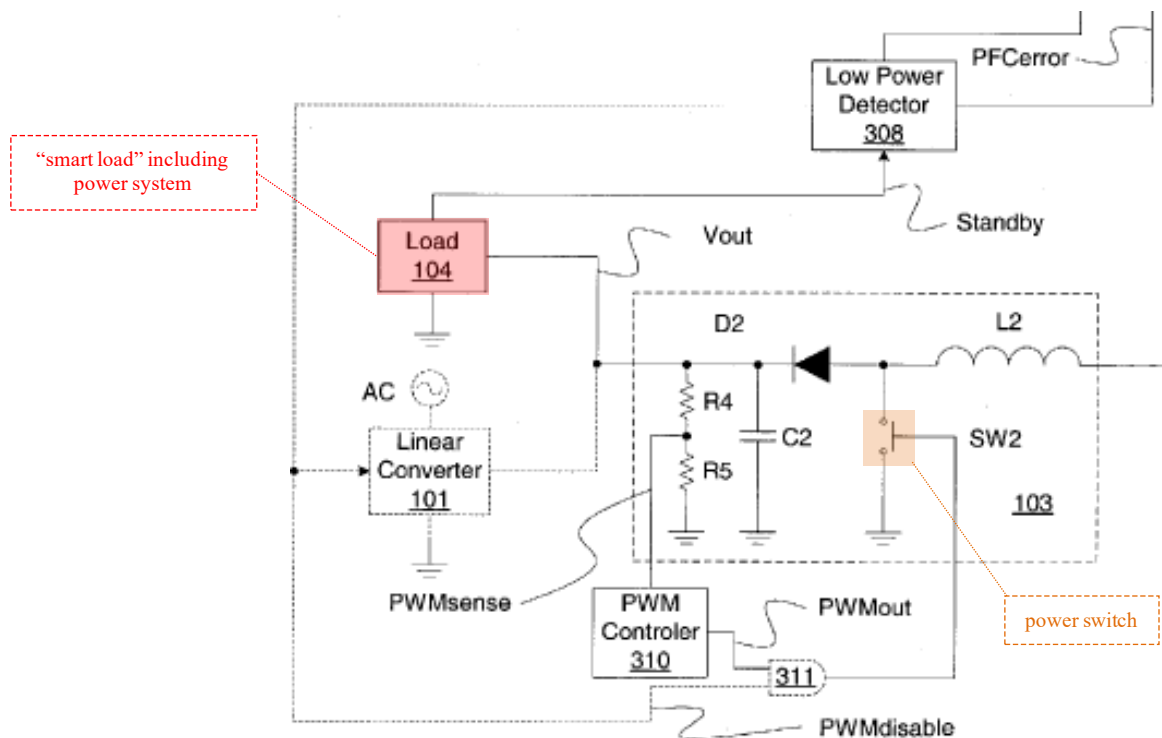
204. Accordingly, *Hwang* in view of the knowledge of a POSITA discloses and suggests each element of claim 1

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[pre]
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- i. **1[a]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof; and”**

205. Figure 3 of *Hwang* shows an embodiment of the power converter from Figure 1. EX1006, [0026]. As shown in Figure 3, PWM stage 103 includes “switch SW2” (i.e., the power switch). EX1006, [0029].



EX1006, Fig. 3 (excerpt) (annotated).

206. As described in *Hwang*’s background, a Pulse Width Modulation (PWM) controller in a switching power converter adjusts the “duty cycle” of the

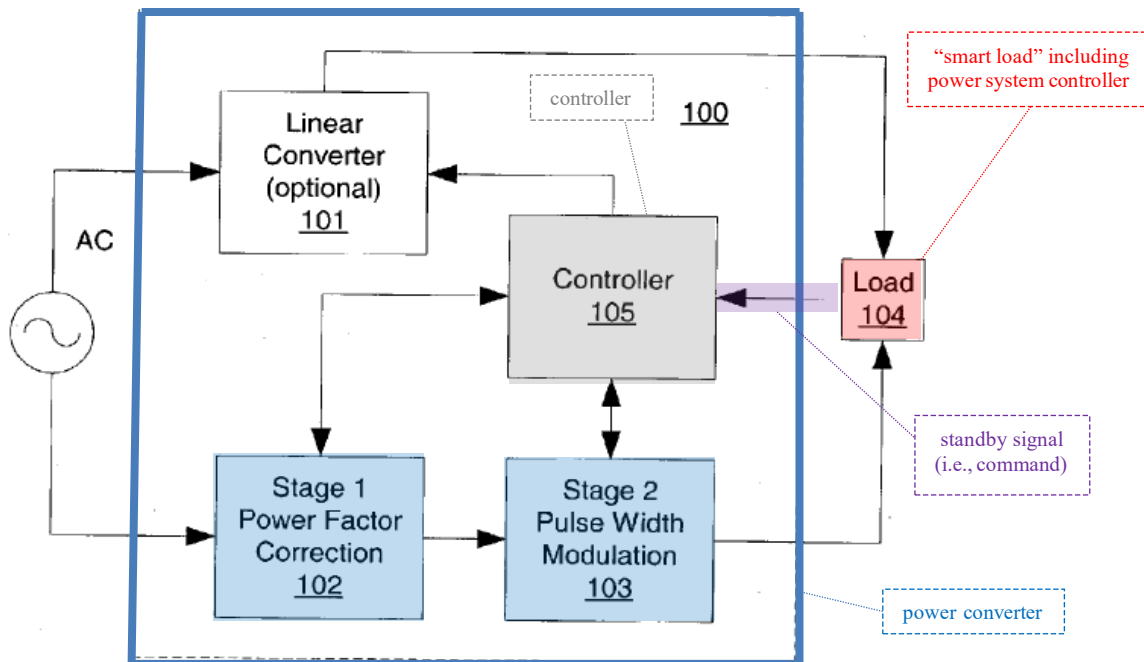
PWM signal controlling the switch “to regulate the output voltage” (i.e., to provide a regulated output characteristic). EX1006, [0003].

207. With respect to Figure 3, *Hwang* states: “The PWM controller 310 may cause the switch SW2 [i.e., the power switch] to be switched on and off in an attempt to cause the output voltage V_{out} to remain substantially constant.” *Id.*, [0030]; *see also id.*, [0034] (“The **duty cycle** of the switch SW2 is controlled in response to the signal V_{sw0} .”), [0036] (disclosing pulse skipping based on “the duty of cycle of the PWM signal”), [0007], Figs. 7A-7D (showing variable duty cycle of PWMout as a function of V_{sw0}).

208. Thus, in my opinion, *Hwang* discloses each limitation of claim 1[a].

- i. **1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state,”**

209. As shown in Figure 1, *Hwang*’s power converter 100 includes “controller 105” (i.e., a controller). EX1006, [0019].



EX1006, Fig 1 (annotated).

210. As I describe above for claim 1[pre], controller 105 receives a standby signal (i.e., a command) from the power system controller within smart load 104 (microprocessor) that is a function of the signal within smart load 104 indicating the activity level (i.e., the system operational state) of the microprocessor within smart load 104. *See* Section XIV.A.i; EX1006, [0021], [0031].

211. As I describe above, *Hwang* explains that the standby signal (i.e., the command) instructs controller 105 to enter a “standby mode” (i.e., a power converter operational state). EX1006, [0021] (“A standby signal from the load 104 may instruct the controller 105 to enter standby mode.”), [0031], Fig. 2. “While in standby mode, the controller 105 may disable the PFC stage 102” and “may cause PWM stage 103 to enter pulse-skipping mode.” *Id.*, [0021].

212. Thus, in my opinion, *Hwang* thus discloses each limitation of claim 1[b].

213. The controller 105 shown in Figure 1 of *Hwang* includes PWM controller 310 shown in Figure 3. EX1006, [0026].

EX1006, Fig. 3 (excerpt) (annotated).

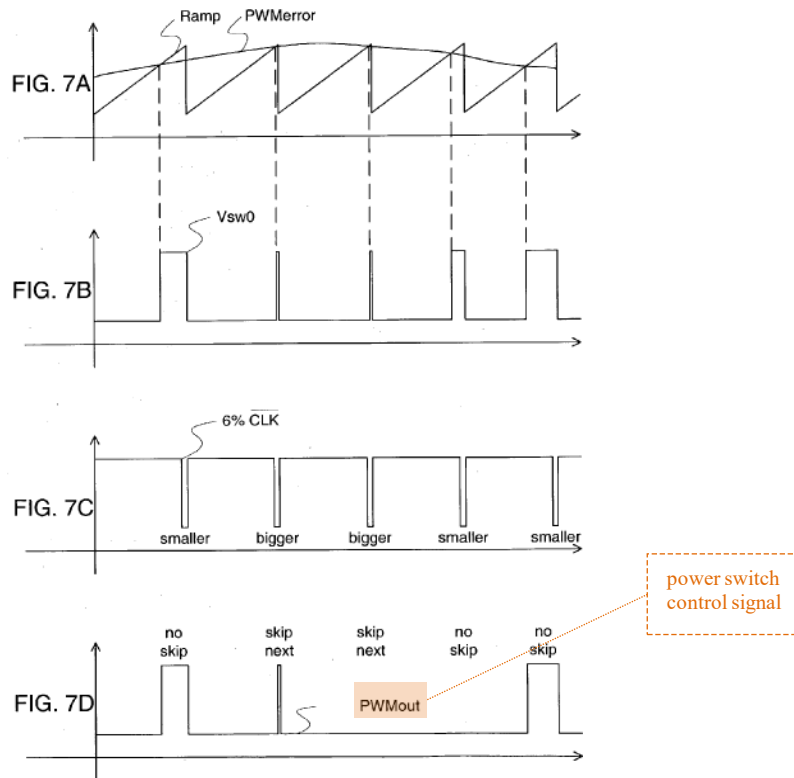
voltage V_{out} obtained by the voltage divider by the resistors R4 and R5. *Id.*, Fig. 3, [0030] (“signal PWMsense, representative of the output voltage V_{out} ... may be coupled into the PWM controller 310”).

215. As I describe above for claim 1[a], the PWM controller controls the duty cycle of switch SW2 (i.e., the power switch) to regulate the output voltage as a function of the feedback to regulate the output voltage. EX1006, [0003] (“A typical switch in a switching power converter may be modulated by a Pulse Width Modulation (PWM) signal A PWM signal has a constant frequency and an adjustable duty cycle. ... A typical goal for a power converter is to regulate the output voltage independent of changes in the load or the input voltage. A power converter may do this by measuring an output voltage of the power converter, comparing the output voltage to a reference voltage, and adjusting the duty cycle of the PWM signal ... to compensate for any discrepancy between the desired output voltage and the measured output voltage.”), [0030]; *see also* Section XIV.A.ii. *Hwang* thus discloses controlling the duty cycle as a function of the output voltage V_{out} (i.e., the output characteristic).

216. *Hwang* also discloses that the duty cycle of the power switch is controlled in accordance with the “standby signal” (i.e., the command) from the power system controller. For example, although Figure 3 shows that PWM stage 103 may be disabled by a PWMdisable signal feeding AND gate 311 (EX1006,

Fig. 3), *Hwang* explicitly discloses that, during standby mode, controller 105 may either (i) “disable the PWM stage,” or (ii) “cause PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021]).

217. Figures 7A-7D shows the pulse-skipping mode described by *Hwang*. By skipping the PWM pulses, the output voltage V_{out} can be regulated under light load conditions. During pulse-skipping mode, a switching cycle of the PWM stage is skipped (i.e., the duty cycle forced to zero for that switching cycle) if the duty cycle of the previous switching cycle was less than a given threshold. *Id.*, Abstract (“A pulse-width modulation (PWM) signal including a series of pulses is produced by comparing the error signal to a ramp signal. The duty cycle of the PWM signal is compared to a reference duty cycle. If the duty cycle of the PWM signal is less than the reference duty cycle then the next pulse in the PWM signal is skipped.”), [0036], [0041]-[0042] (describing pulse-skipping operation).



EX1006, FIG. 7A-D (annotated). Accordingly, the duty cycle of the power switch is also controlled in accordance with the standby signal (i.e., the command) placing the PWM stage 103 in pulse-skipping mode.

218. Thus, in my opinion, *Hwang* discloses each limitation of claim 1[c].

- i. **1[d]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

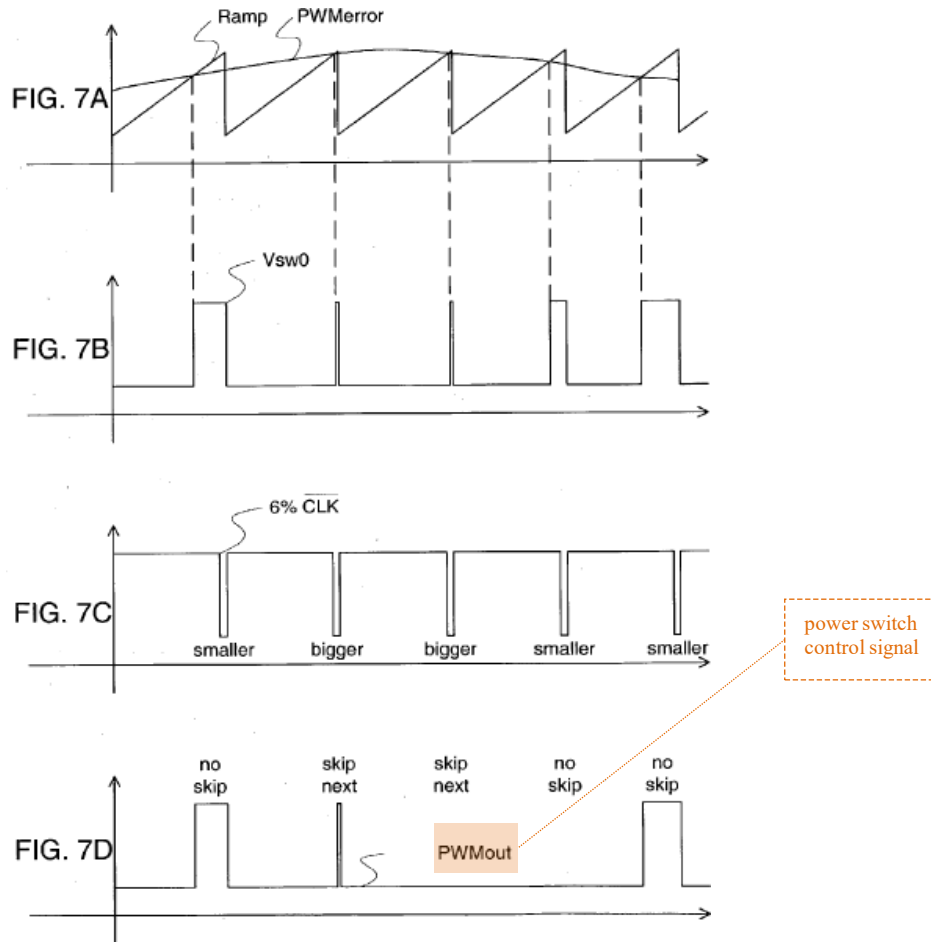
219. As I describe above for claim 1[pre] and 1[b], controller 105 places the power converter in standby mode as a function of a standby signal (i.e., the command) from a power system controller within smart load 104 that itself is a function of activity level (i.e., the system operational state) of the microprocessor

within smart load 104. *See* Sections XIV.A.i and XIV.A.iii; EX1006, [0021], [0031].

220. “While in standby mode, the controller 105 may disable the PFC stage 102” and “may cause PWM stage 103 to enter pulse-skipping mode.” *Id.*, [0021]. Accordingly to the ’759 Patent specification, both of these actions represent regulating an internal operating characteristic to improve operating efficiency.

221. The ’759 Patent lists the “disabling of ... power factor correction,” as well as “switching frequency,” among example internal operating characteristics. EX1001, 18:64-19:5. Thus, the disabling of *Hwang*’s power factor correction (PFC) stage 102 serves as a first internal operating characteristic. *See* EX1006, [0016], [0021]. Likewise, the reduction of the PWM stage’s average switching frequency during pulse-skipping mode serves as another internal operating characteristic.

222. Figures 7A-7D provide an example where two cycles are skipped over the period of five cycles. *Id.*, Figs. 7A-7D, [0036] and [0041]-[0042] (describing pulse skipping operation). Thus, during this period, the average switching frequency is reduced to 60% of the nominal switching frequency. EX1012, 37 (Fig. 10.38) (illustrating skipped pulses), 34 (describing pulse skipping as “modified version” of “variable-frequency” operation).



EX1006, FIG. 7A-D (annotated).

223. *Hwang* also explains how this regulating of internal operating characteristics improves efficiency. EX1006, [0006] (describing the entry of “pulse-skipping mode” and/or the disabling of one or more stages “to improve efficiency of the power converter”), Abstract (describing “pulse-skipping mode to improve efficiency”), [0004] (“One way to increase the efficiency of the power converter is to minimize the use of the switch.”).

224. Thus, in my opinion, *Hwang* discloses each element of claim 1[d].

B. Claim 2

- i. **2: “The power converter as recited in claim 1 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

225. I understand that although claim 2 recites “within a transition time,” Claim 2 does not set an upper limit, or otherwise define the “transition time” recited therein.

226. In response to a standby signal from the load 104, controller 105 “may enter standby mode” (i.e., a power converter operational state) and thereby “disable the PFC stage 102” and “cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]; *see also* Section XIV.A.iii. In my opinion, a POSITA would have found it obvious that this entry into standby mode to represent a transition from one power converter operational state (i.e., non-standby mode) to another (i.e., standby mode) within a transition time.

227. In my opinion, *Hwang* alone or in view of the knowledge of a POSITA thus discloses and/or suggests each element of claim 2.

C. Claim 4

- i. **4: “The power converter as recited in claim 1 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

228. The ’759 Patent background explains that a “core state” of a processor

is “under software operating system control” and affects the “level of power consumption” of the processor. EX1001, 4:23-26. According to the ’759 Patent, the highest core state is where the processor executes instructions “at its full operational level.” *See id.*, 4:26-37. On the other hand, various core-state “sleep levels” are “achieved by halting instruction execution.” *Id.*, 4:28-37. In other words, the “core state” as described in the ’759 Patent background specifies the activity level (e.g., the rate at which instructions are executed) of the processor.

229. As I describe above for claim 1[pre] in Section XIV.A.i, *Hwang* discloses that smart load 104 includes a microprocessor that enters a “standby mode” (i.e., the system operational state) “during periods of low activity or non-use.” EX1006, [0031]; *see also id.*, [0021] (describing “a standby or ‘sleep’ mode during periods of low activity”).

230. A POSITA would have understood in my opinion that the standby mode of *Hwang*’s smart load depends on a core state of its microprocessor. Thus, in my opinion, *Hwang* discloses and also renders obvious claim 4.

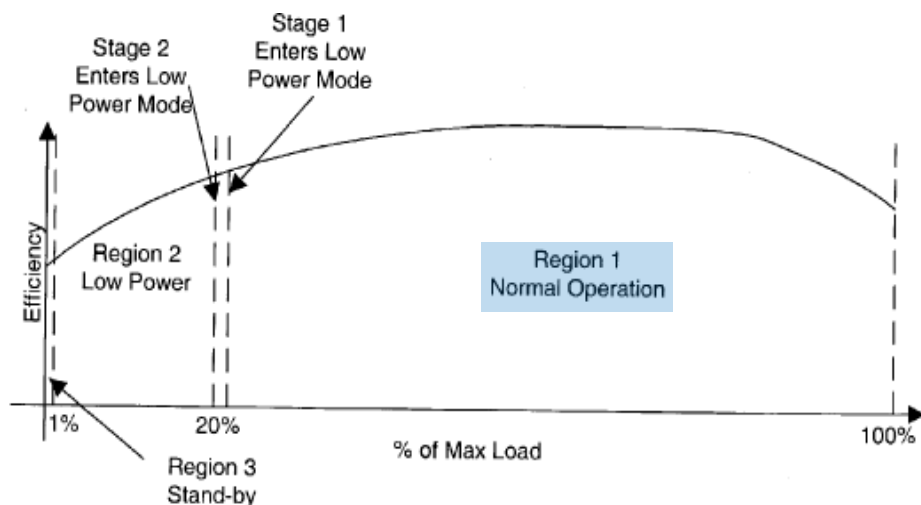
D. Claim 5

- i. 5: “The power converter as recited in claim 1 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

231. The ’759 Patent describes a “Fully Operational” power converter operational state as “[a]ll power converter components operational at full

performance level,” as opposed to a “Very Light Load” state with “reduced switching frequency.” EX1001, Table I.

232. *Hwang* discloses various power converter operational states including Normal Operation, Low Power, and Stand-by. EX1006, [0024], Fig. 2; *see also* Section XIV.A.iii (claim 1[b]). Under the “Normal Operation” state, *Hwang*’s power converter is fully operational—without any stage disabled and without pulse-skipping reducing the average switching frequency. EX1006, [0024], Table 1.



EX1006, Fig. 2 (annotated). The “Normal Operation” of *Hwang* thus discloses “a fully operational power converter.”

233. Thus, in my opinion, *Hwang* discloses and renders obvious claim 5.

E. Claim 6

i. 6[pre]: “A power system coupled to a load, comprising:”

234. Later elements of claim 6 require the “power system” of claim 6[pre]

to include a “power system controller” and a “power converter,” both of which are recited in claim 1[pre]. Thus, *Hwang* discloses and renders obvious claim 6[pre] in the same manner that I describe above for claim 1[pre]. See Section XIV.A.i.

ii. 6[a]: “a power system controller configured to receive a signal indicating a system operational state of said load and to select a power converter operational state as a function thereof; and”

235. As I describe above for claim 1[pre], *Hwang* in view of the knowledge of a POSITA discloses and suggests a power system controller configured to receive a signal indicating a system operational state of a load. See Section XIV.A.i. And as I describe above for claim 1[b], the power system controller of *Hwang* sends a command to the power converter controller to enter a power converter operational state as a function of said signal. Thus, in my opinion, *Hwang* discloses a power system controller configured to “select” a power converter operational state as a function of the signal in the same manner as I describe above for claim 1[b]. See Section XIV.A.iii. Therefore, *Hwang* discloses in my opinion each limitation of claim 6[a].

iii. 6[b]: “a power converter, including:”

236. As I describe above for claim 1[pre], *Hwang* discloses a power system that includes a power converter. See Section XIV.A.i. For example, *Hwang* discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006]. Like the power converter in Figure 3 of the ’759 Patent (EX1001, Fig. 3), *Hwang*’s power

converter is a “two-stage power converter” with a “power factor correction (PFC) stage 102” and a “PWM stage 103” (EX1006, [0019], Figs. 1 and 3). Therefore, *Hwang* discloses in my opinion each limitation of claim 6[b].

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide a regulated output characteristic at an output thereof, and”**

237. Claim 6[c] is identical to claim 1[a]. Thus, claim 6[c] is disclosed by *Hwang* in the same manner as I describe above for claim 1[a] in Section XIV.A.ii.

- v. **6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command,”**

238. Claim 6[d] restates limitations recited in claims 1[b]-[c].

1[b]: “a controller configured to receive a command from said power system controller to enter a power converter operational state as a function of said signal indicating said system operational state” 1[c]: “said controller further configured to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”	6[d]: “a controller configured to receive a command from said power system controller to enter said power converter operational state and to provide a signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said command”
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Thus, *Hwang* discloses claim 6[d] in the same manner as I describe above for claims 1[b]-[c] in Sections XIV.A.iii and XIV.A.iv.

- vii. **6[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

239. Claim 6[e] is identical to claim 1[d]. Thus, claim 6[e] is disclosed by *Hwang* in the same manner as I describe above for claim 1[d] in Section XIV.A.v.

F. Claim 11

- i. **11: “The power system as recited in claim 6 wherein said power converter is configured to enter said power converter operational state within a transition time from another power converter operational state.”**

240. Claim 11 mirrors the language of claim 2, but depends from claim 6 instead of claim 1. Thus, *Hwang* discloses the additional elements of dependent claim 11 in the same manner as I describe above for claim 2. *See* Section XIV.B.

G. Claim 14

- i. **14: “The power converter as recited in claim 6 wherein said load includes a processor and said system operational state depends on one of a core state and a performance state of said processor.”**

241. Claim 14 mirrors the language of claim 4, but depends from claim 6 instead of claim 1. Thus, *Hwang* discloses the additional elements of dependent claim 14 in the same manner as I describe above for claim 4. *See* Section XIV.C.

H. Claim 15

- i. **15: “The power system as recited in claim 6 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

242. Claim 15 mirrors the language of claim 5, but depends from claim 6 instead of claim 1. Thus, *Hwang* discloses the additional elements of dependent claim 15 in the same manner as I describe above for claim 5. *See* Section XIV.D.

I. Claim 16

- i. **16[pre]: “A method of operating a power system coupled to a load, comprising:”**

243. Claim 16 recites substantially similar elements as claim 6, but in the form of a method claim. *Hwang* thus discloses claim 16[pre] in the same manner as described above for claim 6 (and similar elements of claim 1). *See* Sections XIV.A.i (claim 1[pre]) and XIV.E.i (claim 6[pre]).

- ii. **16[a]: “receiving a signal indicating a system operational state of said load;”**

244. As I describe above for claims 1[pre] and 6[a], *Hwang* in view of the knowledge of a POSITA discloses and suggests a power system controller that receives a signal indicating a system operational state of a load. Thus, for the same reasons I describe in Sections XIV.A.i (1[pre]) and XIV.E.ii (6[a]), *Hwang* discloses method step 16[a].

iii. 16[b]: “generating a power converter operational state as a function of said system operational state;”

245. As I describe above for claim 1[pre] and 1[b], *Hwang* discloses that power converter normal operation and/or standby modes (i.e., power converter operational states) are generated as a function of the activity level of the microprocessor in smart load 104 (i.e., as a function of the system operational state). *See* Sections XIV.A.i and XIV.A.iii; *see also* EX1006, [0021], [0024], [0031], Fig. 2. Thus, in my opinion, *Hwang* discloses each element of claim 16[b].

iv. 16[c]: “inducing a power converter to enter said power converter operational state; and”

246. As I describe above in Section XIV.A.iii for claim 1[b], smart load 104 sends a standby signal to controller 105 to place the power converter in “standby mode” (i.e., a power converter operational state) and thereby “disable the PFC stage 102” and “cause PWM stage 103 to enter pulse-skipping mode.” EX1006, [0021]. The standby signal from smart load 104 thereby induces the power converter operational state. Thus, in my opinion, *Hwang* thus discloses claim 16[c].

v. 16[d]: “providing a signal to control a duty cycle of a power switch of said power converter as a function of an output characteristic thereof and in accordance with said power converter operational state,”

247. The “providing ...” step in claim 16[d] mirrors the “to provide ...” language in claim 1[c], but recites “in accordance with said power converter

operational state” as opposed to “in accordance with said command.” However, in claim 1[b], the “power converter operational state” is entered based on the “command.” Thus, *Hwang* discloses claim 16[d] in the same manner as I describe above for claims 1[b]-[c]. *See* Sections XIV.A.iii-iv.

- vi. **16[e]: “thereby regulating an internal operating characteristic of said power converter to improve an operating efficiency thereof as a function of said system operational state.”**

248. Claim 16[e] is identical to claim 1[d]. Thus, claim 16[e] is disclosed by *Hwang* in the same manner as I describe above for claim 1[d]. *See* Section XIV.A.v.

J. Claim 20

- i. **20: “The method as recited in claim 16 wherein said power converter operational state is selected from the group consisting of: a fully operational power converter, a reduced redundancy power converter, and an idle power converter.”**

249. Claim 20 is similar to claim 5, but depends from claim 16 instead of claim 1. *Hwang* thus discloses the additional elements of dependent claim 20 in the same manner as I describe above for claim 5. *See* Section XIV.D.

XV. CONCLUSION

250. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. I further understand that willful false statements and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Executed on June 9, 2022.

A handwritten signature in cursive script, reading "Sayfe Kiaei".

Dr. Sayfe Kiaei

Appendix A

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

Sayfe Kiaei

Professor, Motorola Endowed Chair Professor

School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

FIELDS OF SPECIALIZATION

- Analog, Digital, RF, Power Management Integrated Circuits
- Power Management IC, Battery Management, Energy System, Energy Management
- Sensors, Bio-electronics, Bio-sensors, Hearing Aid Electronics, Implanted devices electronics
- Communication Systems, Wireless Communications, Wireline Communication System, Audio/Video and signal processing

DEGREES

- **Ph.D.**, Electrical and Computer Engineering, Washington State University, 1987
- **M.S.**, Electrical and Computer Engineering, Washington State University, 1984
- **B.S.E.E.**, Electrical Engineering, Northeastern University/WSU, 1982

ACADEMIC POSITIONS

Fall 2001-Present: Professor, Motorola Endowed Chair Professor in Analog and RFIC School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

- **Professor:** Research and teaching in integrated circuits, RF circuits and systems, mixed-signal and Analog IC, Sensors, Power management IC, Bio-electronics
- **Research Projects:**
 - Analog and digital IC, RFIC, Power Management IC transceiver
 - VLSI, Processor System Architecture, ASIC
 - PMIC, Battery Management & Sensing, Integrated Power Electronics
 - Wireless communication system, wireless modems, wireless mobile system, WiFi, Bluetooth, Wireline Communication system and transceivers, MODEM standards, CABLE MODEM, DOCIS, DSL, Signal Processing, Digital Signal Processing, Adaptive Signal Processing
 - Sensors, Bio-electronics, Bio-sensors, Hearing Aid Electronics, Implanted devices electronics
- Research Funded by NSF, USAID, DARPA, JPL, NASA, Motorola Inc., Intel Inc., Broadcom, Qualcomm, Raytheon, General Dynamics, Texas Instruments, and over 10 other industries. List of Current significant research awards:
 - Partnership Center for Energy systems, USAID, 2015-2020, \$18M. Principle Investigator
 - QESST NSF ERC Center on Solar Energy, Battery Management, PMIC, DC-DC, AC-DC, NSF, 2010-2020, \$36M, Co-PI, Test-bed Director
 - Solar Energy Development in ME, Private funds and World Bank, \$2M
 - Connection One NSF Center, Director, 2004-Present, Total funding \$5M, average annual funding over \$750K.

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2004-Present, Director and founder of NSF IUCRC Center Connection One, School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ; <https://connectionone.org>

- The NSF Connection One Industry/University Cooperative Research Center was established the center in 2002 with focus on communication system, integrated Circuits and Systems, wireless system, PMIC, RF, sensors, and related areas. The center has five university member with over 30 industrial members. Total funding over \$10M, annually over \$500K. www.connectionone.org

2014-2020, Director, USAID, US-PCASE: Center for Advance Studies in Energy, Funding \$18M.
<https://uspcase.asu.edu/>

- **Director and PI:** PCASE - Partnership Center for Energy systems, Energy Center funded by the USAID.
- USIAD Centers for Advanced Studies in Energy program (USPCAS-E) is a partnership between Arizona State University and two leading Pakistani universities: the National University of Science and Technology (NUST) Islamabad and the University of Engineering and Technology in Peshawar (UET).
- PCASE has developed two new Graduate schools of Energy. Within 5 years, the center has over 1000 MS and PHD Students, with 14 new energy degrees in MS and PhD, two new building with 20+ energy labs in the power system, grid, power electronics, renewable energy, PV, Wind, Hydro, bio-fuel, fuel cell, batteries and storage, and thermal areas.

2008-2012: Associate Dean of Research, Ira A. Fulton Schools of Engineering, Arizona State University

Responsible for leading the research infrastructure, promoting and developing research programs with industry and federal agencies, leading large multi-university proposals, investing and providing seed funding to foster new research areas, and promoting graduate program in the college of engineering. Research Enterprise support included:

- Increase College of Engineering research funding from \$50M to over \$80M.
- Working with Vice President for Research, Dean's, and directors on University-wide research initiatives.
- Established the first NSF Engineering Research Center (ERC) at the ASU on Solar Energy QESST. Managed, organized and planned the ERC proposal process. ASU is the lead school partnering with MIT, Georgia Tech, U of Delaware, Cal-Tech, U of New Mexico, and UA.
- Lead several trans-disciplinary 4M research projects (4M: multi-million, multi-investigator, multi-disciplinary, multi-university grants) in energy, security, and related initiatives.
- Oversight of over 20 existing research centers in the college of Engineering.
- Engage with industry and federal government to establish new research collaborations.
- Organized workshops and supported proposals for NSF, NIH, DOE, DOD, DARPA, etc.
- Organized workshops for new assistant professors to apply for NSF CAREER Awards. ASU CAREER awards grew from 3 annual awards in 2008 to over 15 CAREER awards by 2012.
- Research Administration and pre-award proposal administration for the schools. Developed a decentralized research administration and advancement team for the Schools supporting 5 schools, 12 departments, over 220 engineering faculty, with funding over \$70M.
- Annual budget over \$7M for supporting research centers, seed funding for new center, cost sharing, proposal support, equipment and infrastructure support, graduate scholarships, and research administration.
- ADR Staffs included, Director of industrial and government liaison, Director of research administration, and 14 research advancement staff.
- Graduate Programs: Recruiting, Fellowships, marketing, outreach, coordination with departments

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1997-2001, Adjunct Professor, Electrical and Computer Engineering Dept., The University of Texas, Austin, Texas, Taught graduate courses at UT Austin on Introduction to Telecommunication System and Digital Communications. Co-advised two Ph.D. program committees in IC design and Telecomm (while at Motorola)

1987-1993, NSF Center For Digital / Analog IC (CDADIC) Co-Director, NSF IUCRC Center director at Oregon State University. The CDADIC was established the center in 1987 with focus on integrated circuits at WSU, UW, and OSU with over 20 industrial members - <https://cdadic.oregonstate.edu/>

1987-1993, Assistant / Associate Professor (Tenured) Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR

- Research and classes in Electronics, DSP, Communication system and networks, Wireless systems, MODEMS. Graduated 30 MS and Ph.D. students.
- Faculty Chair, Computer Engineering Program, Developed a new Computer Engineering Program at OSU in 1987

INDUSTRIAL POSITIONS

1993-2001: Motorola Inc., Senior Member of Technical Staff, Personal Communication Sector, Austin, Texas - Worked projects related to wireless communications, two way radios, wireless networks, ADSL and MODEM, RF, and related areas.

- **Motorola Cellular Division, Wireless Technology Center (WITC), 1997-2002.** Responsible for development of analog, RF, and PMIC integrated circuits and systems for wireless handset. Lead number of projects including cellular, wireless connectivity (Bluetooth and WIFI transceiver), GPS and location Receiver, wireless networks, 2-way radios and related areas. Worked on the development of various subcomponents including system design, link budget, RF front-end, filtering, analog front-end, power management, battery management, and baseband circuits and systems.
- **Motorola Semi-conductor products sector (SPS), Broadband Products Operations, 1995-1997,** Worked on the development of XDSL (ADSL, VDSL, G.lite) systems including OFDM, modulation, synchronization, equalization and the development of a single chip ADSL transceiver (*CopperGold[™]*). The transceiver contained Analog Front End (A/D, D/A, Hybrid), DMT, modulation/demodulation, FFT, IFFT, echo canceler, time domain equalizer, front-end constellation mapping, Trellis code modulation, Viterbi decoder) and an on-chip DSP core.
- **Land Mobile Products Sector LMPS 1993-1995,** Responsible for Wireless digital two-way radios, hot spot wireless network, next generation of digital two-way radios, "*Talk about Radios*", Japanese cellular systems (PHS).
- **Standards,** Represented Motorola in various standards including 2G-4G, GPS, Bluetooth working group, WiFi, 802.11, and DSL standards including T1E1, International Telecommunication Unit (ITU), T1E1, ETSI, 3GPPP, Universal ADSL Working Group (UAWG), Bluetooth working group, G.Lite working group, etc.

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- **University relations**, Responsible for the development of collaborative research programs with several universities. Responsible for funding research in the areas of Wireless Transceiver IC Design, RF, and mixed-signal and baseband system architecture.

1985-87: Member of Research Staff, Boeing Co., Bellevue, Wa, Flight Systems Research and Technology Center, summer. Design Engineer, Hardware and CAD tool development for system control.

AWARDS

- IEEE Fellow 2004-Present
- IEEE Fellows CAS Committee Chair, 2009-2012
- Global Standards Award, For contributions in the International Telecommunication Unit (ITU) for Asymmetric Digital Subscriber Line (ADSL) G.Lite Standards. Motorola Inc., 1999.
- 10X Cycle Reduction Award, for development of new IC design process from DSP algorithm to IC layout, Motorola Inc., 1995.
- IEEE Darlington best paper Award, IEEE Circuits and Systems Society Best Paper Award, 1995. For “Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS for mixed-signal ICs,” Published at: *IEEE Trans. on Circuits and Systems II*, Sept. 93.
- Carter Best Teaching Award, College of Engineering Best Teacher Award, Oregon State University, 1992. For “*outstanding and inspirational teaching in the College of Engineering*”. Award is selected by the confidential vote of all of the undergraduate students in the College of Engineering among over 125 professors in the College.
- Industrial University Fellowship (IUF) Award, *National Science Foundation*, 1993.
- Research Initiation Award, *National Science Foundation*, 1990-93.
- Outstanding Graduate Student Scholarship, *Azur-Data Inc.* WSU, 1984

RESEARCH PROJECTS

Partial list of Research Awards:

- USAID, PCASE – Center for Energy systems, 2015-2020, \$18M. PI and Director
- NSF, QESST NSF ERC Center on Solar Energy, 2010-2020, \$36M, Kiaei, Co-PI, Testbed Director,
- Private Donors, \$1.5M, 2012-2015, Solar Energy Development
- NSF IUCRC Center, Connection One 2002-present, Over \$10M as PI, over \$0.5M annual center awards
- NSF, Micro-Power Multi-Phase MEMS Hearing Aid, 2007-2011, \$500K
- NSF - Design for Implantable Bio-Sensors, 2007-2009, \$480K
- Science Foundation of AZ, PEPER- Photovoltaic Environmental Performance and Reliability for the Arizona-Wide Electric Grid, 2009-2013, \$1.2M
- SRC –Self Characterization for Calibration and Process Feedback of MEMS Devices, 2011-2014, \$300K

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- NSF- Cognitive MIMO Communications for Dynamic-Spectrum Wireless Networks – 2012-2014, \$150K
- NSF, Autonomous Self-Healing Sensor Network Radio, 2010-2014, \$250K
- DARPA, Neural-Enabled Prostheses with Sensorimotor Integration, \$500K
- NSF, Microwave Sensors for Vital Signs Monitoring Device Design, 2011-2013, \$250K
- NSF, Various REU funds, 8/31/12-8/31/13, \$400K
- DARPA, Nano-Mechanical RF Band pass resonator for 2GHz RF Applications, with JPL, \$2.2 M, 2002-2005,
- Qualcomm, Connection One Center, Various projects in 3G-5G, WiFi (802.11), GPS, and Bluetooth , 2005-Present, \$1.2M
- Texas Instruments, Various projects in Battery & Power management, and RFIC, 2005-20012, \$1.5M
- *Motorola Inc.*, Various projects in Battery & Power management, and RFIC, 2002-2010, \$1.2M.
- *SIRF Technologies*, GPS Transceiver, 2005, \$300K.
- *Ridgetop Inc.*, RF Harsh Environment, \$200K
- Freescale Semiconductor, PWM, Battery & Power management, 2006, \$150K
- State of Arizona, *WINTech- Wireless Integrated Nano Technology Center Support* (2005-2009), Ranging from 450K annually from 2005-2009.
- BAE Systems; “New Techniques for Time Measurement Circuits LiDAR; 2005-2008; \$650K
- SRC (Semi-conductors research Corp), Ultra-Wideband Transceivers for cellular and WiFi 802.11, \$225K, 2001-2003
- Intel Corporation, Design of Multi-Standard RF Front-End Circuits for Cellular and WiFi, \$300K, 2002-2005
- *National Science Foundation*, Adaptive Compensation of Analog circuits imperfections using DSP methods, \$150K, 1996 (tie project with UC San Diego NSF center), 2010-2011
- Center for the Design of Analog/Digital IC’s (CDADIC) 1987-1995, At Oregon State, \$1.5M
- Low Power IF processing for Direct Digital Transceivers, *Motorola Inc*, \$100K, 93.
- Hewlett-Packard Faculty Chair position in Mixed-Signal IC, HP, 1995-97, \$500K
- *National Science Foundation*, *Motorola Inc.* Faculty Industry Fellowship, \$250K, 93-94.
- *National Science Foundation*, *Research Initiation Award (RIA)* (same as current *CAREER Award*), Synthesis and Automatic Derivation of Multi-Rate VLSI Arrays for DSP Algorithms, , 90-93. \$320K.
- CDADIC, various projects on Low-Noise Source Coupled Logic (SCL), Mixed-Mode IC's, *CDACIC* \$350K, 1988-1992.
- Decimation Filters for A/D Noise Enhancements, Tektronix, Inc., \$100K, 1988.
- Various grants for IC Fabrication (DARPA/MOSIS, VLSI), testing equipment (Tek, HP), DSP system development (TI, Motorola), ranging in various amounts up to \$200K/year. At Oregon State, 1988-1997.

PROFESSIONAL RECOGNITION

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- IEEE Fellow, 2004-Present
- IEEE Fellow Committee Chair, CAS, 2008-2010
- IEEE Fellow Committee member, 2007-2010.
- IEEE Senior Member, 1993-Present, IEEE Member 1987-1992.
- IEEE Faculty Advisor, Oregon State University, 1987-1990

IEEE Editorials

- IEEE Microwave Magazine, Editor,
- IEEE System Journal, Associate Editor, 2010-2011.
- IEEE Transactions on VLSI, Associate Editor, Jan 2001-2008.
- IEEE Communication Magazine, Editor, Feature Issues on “Circuits for Wireless and Wireline Communications,” April 1999.
- IEEE Transactions on Microwave Theory and Techniques , editor, Special Issue on: "Radio Frequency IC Design,” Dec. 1998.
- IEEE Transactions on Circuits and Systems-II, editor, Special Issue on: “Low-Power Wireless Communication Systems,” June 1997.
- Associate Editor, IEEE Transactions on Circuits and Systems-II, 1993-1996.
- *Editor and Reviewer for many IEEE journals and conferences*
- *Founding member of IEEE RF Integrated Circuits Symposium*
- *Associate Editor, IEEE Communications, Tutorial & Surveys Magazine, 2006-2009.*

Conference Organizations

- RFIC Executive Committee members, 2000-2017
- RFIC Steering Committee Member, RFIC symposium, 1996-2017.
- RFIC Founding member, 1995-96.
- Technical Program Chair, IEEE International Sym. on Circuits and Systems, Phoenix, AZ, 2002.
- ISSCC Admin Council, Conferences Committee 2000-2005.
- General Chair, Radio Frequency IC (RFIC) Symposium, Seattle, WA, 2002.
- Technical Program Chair, RFIC Symposium, Phoenix, AZ, 2001.
- Finance Chair, RFIC symposium, Boston, MA, 2000.
- Publicity Chair, RFIC symposium, Los Angeles, CA, 1999.
- Transactions Chair, RFIC symposium, Baltimore, MD, 1998.
- General Chair, Int. Sym. on Low-Power Electronics and Design (ISLPED), Monterey, CA, 97.
- Executive Committee Member, Int. Symp. On Low-Power Electronics and Design, 96-2000.
- Technical Program Committee Member of the following conferences:

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- International Conference on Circuits and Systems: 1996, 2000, 2001, 2004-2008
- RFIC Symposium, 1996-2018
- Application Specific Array Processing (ASAP): 2000-2002
- Technical Program Chair, Int. Sym. on Low-Power Electronics and Design, Monterey, CA, 96.
- Arizona Telecom Comm (ATIC)
- GLS VLSI 1998, Lafayette, Louisiana, 1998
- VLSI Design 98, Chennai, India, Jan. 1998.
- ICECS, Lisbon, Portugal, 98.
- Application Specific Array Processing, 1995-97, 2000
- Vehicular Technology Conference, 1995-97.
- Inter. Conf. on Intelligent Information Systems, D.C., 1994-95.
- IEEE Pacific Rim Conference on Communications & Computers, Victoria, BC, Canada, 1991.

Invited talks, Panelist, Session Chairs, Workshop Speaker

- Conference chair, Technical Program committee chair and TPC member, tutorials, workshops, session chair, etc. in RFIC, ISSCC, ISCAS, VLSI, ICASSP, Low-Power Symposium, ICC, Application Specific IC's, IMS, MTT, etc.

CONSULTANT

- Intel Inc. Chandler, AZ, 2002-2006: Development of 3G-4G Wireless transceiver.
- Sony Inc., San Diego, CA and Tokyo, Japan, 2002-2004: Review and development of various telecom cellular system architecture including 3G system architecture, and GPS system.
- Motorola Inc. 2002-2005: Supporting development of BT, WiFi, E911, GPS integrated circuits and systems for the cellular and mobile handsets.
- Hewlett Packard, Corvallis, OR – 1990-1993: Various project on development of custom analog and digital IC's for printer and inkjet system. Some of this work was under consultation, and some under various research grants with Oregon State University.
- Tektronix Inc, Beaverton, OR - 1988-1990: Design and Implementation of Data acquisition system for Spectrum analyzer, development of custom DSP algorithm for the Tektronix spectrum analyzer including system architecture, simulation, analysis, and design of oversampled data acquisition system.
- Boeing Commercial Aircraft, BCAC, Renton, WA - 1985-1987: Development of Airplane Controller Model, Simulation and Implementation of Flight control, Model reduction, and system control.

EXPERT WITNESS (Patent, IP)

Patent litigation, patent validity, IPR, expert reports, deposition, testimony, and trade secrets in the following areas (Complete list of cases available):

- Analog and Digital IC
- Radio Frequency Integrated Circuits

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- Power Management, Battery Management, PMIC
- Wireless communication, 3G, 4G, OFDM, WiFi, 802.11, Bluetooth, and related areas
- Audio and acoustic signal processing, Audio Array processing
- Communication networks, Communication system
- Signal Processing, adaptive signal processing
- DSL, xDSL, VDSL, OFDM, Multi-Tone, and related areas
- Cable MODEM DOCIS MODEM, and related areas.
- Hearing AID
- Bio-Electronics, Heart monitoring system, Bi-sensors
- Satellite communications, Satellite Transceiver, ECHO and Multi-path cancelation circuits
- Wireline Communications, MODEM, Digital Subscriber Line, ADSL, VDSL, MODEM
- Wireless LAN, Wi-Fi, 802.11
- Bluetooth
- ZIGBEE
- GPS system, GPS receiver
- MEMS, Bulk Acoustic Wave Filters, SAW, MEMS resonators, MEMS accelerometer
- Wireless Standards (ITU, ETSI, 3GPPP, LTE) including AMPS, GSM, CDMA, WCDMA, LTE, 1G, 2G, 3G, 4G, BT, WiFi (802.11)
- Wireline standards including DSL, MODEM and DOCIS, and related standards ITU/ETSI

PATENTS, PUBLICATIONS

Patents and Patent Applications

Patent Number	title	inventor/author	priority date	filing/creation date	publication date
US-10653337-B2	Local object detection system	Timothy W. Markison,	8/18/16	8/18/17	5/19/20
US-7372333-B2	Monolithic supply-modulated RF power amplifier and DC-DC power converter IC	Siamak Abedinpour,	2/3/03	2/3/04	5/13/08
US-6661371-B2	Oscillator frequency correction in GPS signal acquisition	Thomas M. King,	4/30/02	4/30/02	12/9/03
US-7218085-B2	Integrated ZVS synchronous buck DC-DC converter with adaptive control	Siamak Abedinpour,	5/24/02	5/27/03	5/15/07
US-7528754-B1	Finite impulse response digital to analog converter	Bertan Bakkaloglu,	2/9/06	2/8/07	5/5/09
US-10791965-B2	Method and apparatus for wirelessly monitoring repetitive bodily movements	Sayfe Kiaei	10/19/15	4/12/19	10/6/20
US-2007033000-A1	Efficient non-iterative frequency domain method and system for nonlinear analysis	Shahin Farahani,	7/19/05	7/19/06	2/8/07
US-2006052988-A1	Compressed vector-based spectral analysis method and system for nonlinear rf blocks	Shahin Farahani,	11/21/02	11/21/03	3/9/06
US-2020266708-A1	Electronic circuit and method of controlling three-level switching converters	Parisa Mahmoudid	2/14/19	2/14/20	8/20/20

Standards Contributions

1. "Spectral Compatibility of ADSL: Frequency Overlap vs. FDM," T1E1, Dec. 97.
2. "Echo Cancellation for G.Lite Universal ADSL," OFDM, Universal ADSL Working Group, Atlanta,

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GA, Jan 98.

3. "8-bit QAM Constellation effects on reach for universal ADSL," OFDM, Universal ADAL Working Group, Atlanta, GA, Jan 98.
4. "Trellis Code Modulation coding gain for OFDM," Universal ADSL Working Group, Atlanta, GA, Jan 98.
5. "Monte Carlo Modeling and simulation of twisted pair wiring for OFDM," Universal ADAL Working Group, Atlanta, GA, Jan 98.
6. "Overlap Upstream/Downstream spectral allocation for OFDM ADSL," International Telecommunication Unit, Chicago, March 98.
7. "Echo Cancellation for ADSL OFDM," International Telecommunication Unit, Antwerp, Belgium, 98.
8. "Performance of Echo Cancellation ADSL in OFDM system in the presence of Near End Cross Talk (NEXT)," International Telecommunication Unit, Honolulu, Hawaii, June 98.
9. Presentations and editorials at various XDSL and OFDM standards: ITU, ETSI, UAWG, and T1E1, 97-99.
10. Presentations and editorials at various 3G and 4G and wireless standards including ITU, 3GPPP, 802.11, BT,

Books

"Design, Modeling and Testing of Data Converters, P Carbone, S Kiaei," F Xu - 2014 – Springer, © Springer-Verlag Berlin Heidelberg 2014

Refereed Journal Papers

1. CMOS Full-Duplex Mixer-First Receiver With Adaptive Self-Interference Cancellation S. -A. Ayati; A. Alizadeh; S. Kiaei, IEEE Transactions on Circuits and Systems I, Jan 2021.
2. A 10-W X-Band Class-F High-Power Amplifier in a 0.25μm GaAs pHEMT Technology, A. Alizadeh; M. Yaghooobi; M. Meghdadi; A. Medi; S. Kiaei, IEEE Transactions on Microwave Theory and Techniques, Jan 2021.
3. An X-Band Class-J Power Amplifier With Active Load Modulation to Boost Drain Efficiency A. Alizadeh; S. Hassanzadehyamchi; A. Medi; S. Kiaei, IEEE Transactions on Circuits and Systems I: Sep 2020
4. In-Field Recovery of RF Circuits from Wearout Based Performance Degradation D. Chang; J. N. Kitchen; S. Kiaei; S. Ozev, IEEE Transactions on Emerging Topics in Computing, Jun 2020
5. A 50-V Isolation, 100-MHz, 50-mW Single-Chip Junction Isolated DC-DC Converter With Self-Tuned Maximum Power Transfer Frequency, C. Liu; D. Mandal; Z. Yao; M. Sun; J. Todsen; B. Johnson; S. Kiaei; B. Bakaloglu, IEEE Transactions on Circuits and Systems II: Express Briefs, May 2019
6. Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier, P. Mahmoudidaryan; D. Mandal; B. Bakaloglu; S. Kiaei, IEEE Journal of Solid-State Circuits, 2019.
7. Low-Power/Low-Voltage Integrated CMOS Sense Resistor-Free Analog Power/Current Sensor Compatible With High-Voltage Switching DC-DC Converter, S. Singh; D. Mandal; B. Bakaloglu; S. Kiaei IEEE Transactions on Circuits and Systems I, 2019
8. Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time, D. Mandal; C. Desai; B. Bakaloglu; S. Kiaei, IEEE Transactions on Circuits and Systems II: Express Briefs, 2019

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9. Chirag Desai; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei, "A 1.66 mV FOM Output Cap-Less LDO With Current-Reused Dynamic Biasing and 20 ns Settling Time," *IEEE Solid-State Circuits Letters* Year: 2018, Volume: 1, Issue: 2, Pages: 50-53
10. Debashis Mandal ; Chirag Desai ; Bertan Bakkaloglu ; Sayfe Kiaei, Adaptively Biased Output Cap-Less NMOS LDO with 19 ns Settling-Time;; *IEEE Transactions on Circuits and Systems II*: Feb 2019
11. Ayati, Mandal, Bakkaloglu, Kiaei, "Integrated Quasi-Circulator With RF Leakage Cancellation for Full-Duplex Wireless Transceivers," *IEEE Trans of Microwave theory and techniques*, Dec 2017.
12. "A 50-mA 99.2% Peak Current Efficiency, 250-ns Settling Time Digital Low-Dropout Regulator With Transient Enhanced PI Controller", ChaiYong Lim ; Debashis Mandal ; Bertan Bakkaloglu ; Sayfe Kiaei; *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*; Year: 2017, Volume: 25, Issue: 8; Pages: 2360 - 2370
13. Doohwang Chang; Jennifer N. Kitchen; Sayfe Kiaei; "Sule Ozev, In-field Recovery of RF Circuits from Wearout Based Performance Degradation", *IEEE Transactions on Emerging Topics in Computing*, 2017.
14. Edgar Martí-Arbona; Debashis Mandal; Bertan Bakkaloglu; Sayfe Kiaei, A High-Voltage-Compliant Current-to-Digital Sensor for DC–DC Converters in Standard CMOS Technology, *IEEE Transactions on Power Electronics*, 2017, Volume: 32, Issue: 3. Pp. 2180 - 2188
15. Michael Cheah ; Debashis Mandal ; Bertan Bakkaloglu ; Sayfe Kiaei, "A 100-mA, 99.11% Current Efficiency, 2-mVpp Ripple Digitally Controlled LDO With Active Ripple Suppression", Aug 2016.
16. Marti-Arbona, E.; Mandal, D.; Bakkaloglu, B.; Kiaei, S., "A High-Voltage Compliant Current-to-Digital Sensor for DC-DC Converters in Standard CMOS Technology," *IEEE Transactions on Power Electronics*, no. 99, 2016.
17. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Monitor-Based In-Field Wearout Mitigation for CMOS LC Oscillators," in *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 183-193, 2016.
18. Chang, D.; Kitchen, J.N.; Bakkaloglu, B.; Kiaei, S.; Ozev, S., "Design-Time Reliability Enhancement Using Hotspot Identification for RF Circuits," in *IEEE transactions on Very Large Scale Integration (VLSI) Systems*, -vol. 24, no. 3, pp. 1179-1183, 2016
19. Seungkee Min; Copani, T.; Kiaei, S.; Bakkaloglu, B., "A 90-nm CMOS 5-GHz Ring-Oscillator PLL With Delay-Discriminator-Based Active Phase-Noise Cancellation," *Solid-State Circuits, IEEE Journal of* , vol.48, no.5, pp.1151,1160, May 2013
20. Junghan Lee; Tino Copani; Terry Mayhugh Jr.; Bhaskar Aravind; Sayfe Kiaei; Bertan Bakkaloglu., "A 280 mW, 0.07% THD+N class-D audio amplifier using a frequency-domain quantizer," *Analog Integrated Circuits and Signal Processing*, 173-186, 2012.
21. Seungkee Min; Copali, T.; Kiaei, S.; Bakkaloglu, B.; , "A 90nm CMOS 5GHz ring oscillator PLL with delay-discriminator based active phase noise cancellation," *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, pp. 173-176, 2012
22. Deligoz, I.; Naqvi, S.R.; Copani, T.; Kiaei, S.; Bakkaloglu, B.; Sang-Soo Je; Junseok Chae; , "A MEMS-Based Power-Scalable Hearing Aid Analog Front End," *Biomedical Circuits and Systems, IEEE Transactions on* , vol.5, no.3, pp.201-213, June 2011
23. Copani, T.; Seungkee Min; Shashidharan, S.; Chakraborty, S.; Stevens, M.; Kiaei, S.; Bakkaloglu, B.; , "A CMOS Low-Power Transceiver With Reconfigurable Antenna Interface for Medical Implant Applications," *Microwave Theory and Techniques, IEEE Transactions on* , vol.59, no.5, pp.1369-1378, May 2011
24. Khalil, W.; Shashidharan, S.; Copani, T.; Chakraborty, S.; Kiaei, S.; Bakkaloglu, B.; , "A ~~700-μA~~ 405-MHz All-Digital Fractional- N Frequency-Locked Loop for ISM Band Applications," *Microwave Theory and Techniques, IEEE Transactions on* , vol.59, no.5, pp.1319-1326, May 2011
25. Lashkarian, N.; Nassiri-Toussi, K.; Jula, P.; Kiaei, S.; , "Performance Bound on Ergodic Capacity of MIMO Beam-Forming in Indoor Multi-Path Channels," *Communications, IEEE Transactions on* , vol.58, no.11, pp.3254-3264, November 2010

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26. Hyungseok Kim; Junghan Lee; Copani, T.; Bazarjani, S.; Kiaei, S.; Bakkaloglu, B.; , "Adaptive Blocker Rejection Continuous-Time $\Sigma\Delta$ ADC for Mobile WiMAX Applications," *Solid-State Circuits, IEEE Journal of* , vol.44, no.10, pp.2766-2779, Oct. 2009
27. Kitchen, J.N.; Chu, C.; Kiaei, S.; Bakkaloglu, B.; , "Combined Linear and Δ -Modulated Switch-Mode PA Supply Modulator for Polar Transmitters," *Solid-State Circuits, IEEE Journal of* , vol.44, no.2, pp.404-413, Feb. 2009
28. Sang-Soo Je; Rivas, F.; Diaz, R.E.; Jiuk Kwon; Jeonghwan Kim; Bakkaloglu, B.; Kiaei, S.; Junseok Chae; , "A Compact and Low-Cost MEMS Loudspeaker for Digital Hearing Aids," *Biomedical Circuits and Systems, IEEE Transactions on* , vol.3, no.5, pp.348-358, Oct. 2009
29. Taleie, S.M.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; , "A Linear Digital IF to RF SD DAC Transmitter With Embedded Mixer," *Microwave Theory and Techniques, IEEE Transactions on* , vol.56, no.5, pp.1059-1068, May 2008
30. Wing-Yee Chu; Bakkaloglu, B.; Kiaei, S.; , "A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters," *Solid-State Circuits, IEEE Journal of* , vol.43, no.12, pp.2809-2819, Dec. 2008.
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33. Chen, X.; Kiaei, S.; , "Pulse generation scheme for low-power low-complexity impulse ultra-wideband," *Electronics Letters* , vol.43, no.1, pp.44-45, Jan. 4 2007
34. Carlosena, A.; Wing-Yee Chu; Bakkaloglu, B.; Kiaei, S.; , "Randomized Carrier PWM With Exponential Frequency Mapping," *Power Electronics, IEEE Transactions on* , vol.22, no.3, pp.960-966, May 2007
35. Abedinpour, S.; Bakkaloglu, B.; Kiaei, S.; , "A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 μ m SiGe Process," *Power Electronics, IEEE Transactions on* , vol.22, no.6, pp.2164-2175, Nov. 2007
36. Kitchen, J. N.; Deligoz, I.; Kiaei, S.; Bakkaloglu, B.; , "Polar SiGe Class E and F Amplifiers Using Switch-Mode Supply Modulation," *Microwave Theory and Techniques, IEEE Transactions on* , vol.55, no.5, pp.845-856, May 2007
37. A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 micron. , S Abedinpour, B Bakkaloglu, S Kiaei - Power Electronics, IEEE Transactions on, Nov. 2007, Volume: 22, pp - 2164-2175
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39. Pulse generation scheme for low-power low-complexity impulse ultra-wideband, Chen, X.; Kiaei, S.; Electronics Letters; Volume: 43 Issue: 1 Jan. 2007 ; Page(s): 44-45
40. Bandwidth extension technique for polar modulated RF transmitters ; Bakkaloglu, B.; Kiaei, S.; Dwyer, R.; Electronics Letters; Volume: 42 Issue: 8 13 April 2006 ; Page(s): 476- 478 ;
41. Frequency modulated bandpass SD chirp synthesizer for sensor applications; Chung, H.H.; Lyles, U.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; Electronics Letters; Volume: 42 Issue: 16 August 3, 2006 ; Page(s): 917- 918
42. Radiation Hardened by Design RF Circuits Implemented in 0.13 mm CMOS Technology; Chen, W.; Pouget, V.; Gentry, G. K.; Barnaby, H. J.; Vermeire, B.; Bakkaloglu, B.; Kiaei, K.; Holbert, K. E.; Fouillat, P. ; Nuclear Science, IEEE Transactions on ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3449-3454 ;

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43. Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers ; Chung, H. H.; Chen, W.; Bakkaloglu, B.; Barnaby, H. J.; Vermeire, B.; Kiaei, S. ; Nuclear Science, IEEE Transactions on ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3539-3543
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50. "Channel Shortening For Discrete Multi-tone Transceivers To Maximize Channel Capacity" OFDM and DSL, G. Arslan, B. Evans, S. Kiaei ; ; IEEE Transactions for Signal Processing, Vol 49; No. 12; Pp: 3123-3135. Dec 2001.
51. Optimum equalization of multicarrier systems: a unified geometric approach, for OFDM Lashkarian, N.; Kiaei, S. ; IEEE Transactions on Communications, Volume: 49 Issue: 10 , Oct. 2001 Page(s): 1762 –1769
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55. Introduction to the special issue on low power wireless communications Kiaei, S.; Friedman, E.G. Circuits and Systems II: IEEE Transactions on Analog and Digital Signal Processing, Volume: 44 Issue: 6 , June 1997 Page(s): 425 –427
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57. "Noise Considerations for Mixed-Signal RF IC Transceivers," ACM Transaction on Wireless Networks, Vol. 4, pp. 41-53, 1998. [S. Kiaei, D. Allstot, N. Verghese, K. Hansen].
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60. "Multi-Rate Transformation of Recurrence Equations for Regular VLSI Arrays, " Application Specific Array Processors, IEEE Press, 1994. [L. Aihua, S. Kiaei]
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62. "Overlapping Transformation for Time-Area Optimal VLSI arrays for Toeplitz Matrices," J. of Computer and Software Engineering, Vol. 3, #4, pp. 461-481, June 95. [S. Kiaei, Yuepeng Zheng]
63. "Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS Logic for Hybrid ICs," IEEE Trans. on Circuits and Systems, Sept. 93. [S.H. Chee, S. Kiaei, D. Allstot]
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65. "Enhancement Source-Couple Logic ESCL," IEEE Trans. on Circuits, and Systems II: Analog and Digital Signal Processing, Vol. 39, No. 6, pp. 399-402, July92. [M. Maleki, S. Kiaei]
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67. "Adaptive self-correcting D-S Modulators," IEE Electronics Letters, Vol. 28, No. 14, pp. 1288-1290, July 92. [S. Abdenadher, S. Kiaei, G. Temes, R. Schreier]
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69. "Piecewise Linear Schedules for Recurrence Equations," VLSI Sig. Proc. VI, IEEE Press, 1992. [S. Rajopadhye, L. Mui, S. Kiaei]
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71. "VLSI Design of Wavefront Array Processors for Recursive Filters," VLSI Signal Processing II, IEEE Press, pp. 152-164, 1988. [S. Kiaei, U.B. Desai]
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Conference Publications

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118. "On-line Adaptive Digital Correction of Dual-Quantization Delta-Sigma Modulators," Electronics Letters, Volume: 28, Issue: 16, 30 July 1992; Pages: 1511 – 1513 [Yaohua Yang; Schreier, R.; Temes, G.C.; Kiaei, S.]
119. "Piecewise Linear Schedules For Recurrence Equations," Workshop on VLSI Signal Processing, Oct. 1992. [Rajopadhye, S.; Mui, L.; Kiaei, S.]
120. "Synthesis Techniques for CMOS Folded Source-Coupled Logic Circuits," IEEE Journal of Solid-State Circuits, Aug. 1992. [Maskai, S.R.; Kiaei, S.; Allstot, D.J.]
121. "A Folding Transformation for VLSI IIR Filter Array Design," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Toronto, Canada, pp. 1237-1240, May 1991. [S. Rajopadhye, S. Kiaei]
122. "Systematic Derivation of Multi-Rate VLSI Arrays for the Solution of Toeplitz Matrices," IEEE Great Lakes Symposium on VLSI, March 1991. Proc. of IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing, Victoria, BC, Canada, pp. 623-626, May 1991. [S. Kiaei]
123. "CMOS Source-Couple Logic for Mixed-Mode VLSI," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, pp. 1608-1611, May 1990. [S. Kiaei, S.H. Chee, D. Allstot]
124. "VLSI Design of Multi-Rate Arrays," Proc. of International Conference on Acoustics, Speech, and Signal Processing, New Mexico, pp. 1049-1052, 1990. [L. Aihua, S. Kiaei]

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125. "Comparison of Low-Noise Current-Mode Logic Circuits for High Performance Mixed-Mode Applications," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, May 1990. [S. H. Chee, S. Chow, S.S. Lee, S. Kiaei, D. Allstot]
126. "VLSI Design of Dynamically Reconfigurable Array Processors-DRAP," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Glasgow, Scotland, 1989. [S. Kiaei, J. Durgham]
127. "VLSI Design of Bit/Serial Adaptive IIR Filters," Proc. of IEEE Pacific Conference on Communications, Computers, and Signal Processing, Victoria, Canada, pp. 650-652, June 1989. [R. Badyal, S. Kiaei]
128. "CCA Approach for ARMA Spectral Analysis," Proc. of IEEE International Symposium on Circuits and Systems, Portland, OR, pp. 1319-1322, May 1989. [S. Kiaei, L. Luo]
129. "Canonical Correlation Analysis (CCA) for ARMA Spectral Estimation," IEEE International Symposium on Circuits and Systems, May, 1989. [Kiaei, S.; Luo, L.]
130. "VLSI Implementation of Adaptive Bit/Serial IIR Filters," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, June 1989. [Badyal, R.; Kiaei, S.]
131. "VLSI design of WAP for Recursive Equations," VLSI Signal Processing, 1988. [S. Kiaei, U. Desai]
132. "Independent Data Flow Wavefront Array Processors for Recursive Equations," Proc. of 20th Annual Conference on Information Sciences and Systems, Princeton University, NJ, 1986. [S. Kiaei, U. Desai]
133. "A Stochastic Realization Approach to Reduced-Order Hierarchical Estimation," Proc. of 24th IEEE Conference on Dec., Ft. Lauderdale, FL, pp. 416-421, December 1985. [U. Desai, S. Kiaei]
134. "Hierarchical Estimation Algorithms," Proc. of IEEE Conference on Man, Cybernetics, and Systems, Tucson, AZ, October 1985. [U. Desai S. Kiaei]
135. "Approximation of Markovian Models with Non-Constant Parameters," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1642-1644, December 1984. [U. Desai, S. Banerjee, S. Kiaei]
136. "A Canonical Correlation Approach to Reduced-Order LQR Design," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1523-1528, December 1984. [U. Desai, S. Banerjee, S. Kiaei]

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GRADUATE STUDENT ADVISEES & RESEARCH PROJECT

*(Partial list of Students graduated, current employment to the best of my knowledge)_*

1. J. Durgam, VLSI Design of Dynamically Reconfigurable Array Processors, MSEE, 1988. Intel.
2. J. Gilbert, Minimization Techniques for PLAs, MSEE, 1988, Tektronix Inc.
3. L. Luo, CCA Methods for ARMA Spectral Estimation, MSEE, 1989. Berkeley Research Center
4. E. Zahl, Enhancement Methods for A/D Noise Reduction, MSEE, 1989. AT&T
5. L. Aihua, Synthesis of MRAs, MSEE, 1990. Intel.
6. F. Aslam, Image Restoration Methods, MSEE, 1990.
7. S.H. Chee, FSCL Circuits for Mixed-Mode IC's, MSEE, 1990. Linear Tech.
8. C. Dawson, MSEE, 1990. Boeing
9. A. Chow, Source-Coupled Logic ALU, MSEE, 1990. Intel
10. S. Maskai, Decimation Filters Using FSCL Circuits, MSEE, 1991. Intel
11. L. Louis, VLSI Implementation of Toeplitz Matrices, MSEE, 1991.
12. R. Badyal, Bit/Serial VLSI Design of IIR Filters, MSEE, 1992, HP
13. Lap Mui, Piece-Wise Linear Schedule for VLSI Arrays, MSEE, 1992. HP
14. S. Abdennadher, Adaptive Sigma-Delta Modulators, MSEE, 1992. Level One / Intel.
15. H. Bribech, Second Order Adaptive A/D Schemes, MSEE, 1992.
16. B. Hickman, MSEE, 92. Tektronix
17. M. Maleki, Current-Mode Flash A/D, MSEE, 1992. University of Oregon
18. Man Wong, Low-Noise Decimation Filter for Mixed-Mode ICs, MSEE, 1993, Motorola.
19. Anu Krishna Swamy, Low Noise IC Blocks for Mixed-mode IC's, MSEE, 1993, Ph.D., 1997.
20. Manu Srivastava, Comparison of Differential Logic (FSCL, CVSL, DSLL), MSEE, 1994, Intel.
21. Joel Oren, VLSI Design of Asynchronous FIR Filters, MSEE thesis, Feb. 1994. E-Systems.
22. Y. Zheng, VLSI Design and Synthesis of Multi-Rate Arrays, Ph.D. March 94, Hughes Research.
23. Satish Kulkarni, Low-Sensitivity Filters, MSEE, 1995, Motorola.
24. Amit Dutta, Multi-user Interference Cancellation, Ph.D, Dec. 97, Faculty, India.
25. Dwight Poplin, Multiplierless MPEG Decoder, MSEE, 1996. HP.
26. Maxim Scarpa, Adaptive I/Q Miss-match Correction for Direct Conversion Receivers, MSEE 1998.
27. Jeff McNeal, Sigma-Delta Frequency-to-Time Conversion, MSEE, 1998. Level One Comm.
28. Julia Vogel, Adaptive DC offset Cancellation, MSEE, 1998. Faculty in Germany.
29. Takao Inoue, MS, Echo Cancellation for ADSL, 1998. MSEE, The U of Texas at Austin.
30. Navid Lashkarian, Frequency off-set estimation and Synchronization of OFDM systems, Ph.D., June 1999. Broadcom Inc. & Faculty at UC San Jose.

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31. Guner Arslan, (co-advisor with B. Evans), "Fast Equalization for DMT systems, with applications to ADSL," Ph.D. The University of Texas at Austin, 2000
32. Salem Abdennadher, I/Q Mismatch Correction for RF Wireless transceivers, Ph.D., Level One Comm/Intel.
33. Can Sandalci, DSL Line Driver, Ph.D., 2001, Intel.
34. Dean Badillo, Low-Cost VCO Ring Oscillators, PhD, 2004, Intel, Chandler,
35. Siamak Abedinpour, PhD, 2005 Freescale, Tempe, Arizona
36. Hemanth Shivalingaiah, Multi-Band Low Noise Amplifiers, Ph.D., 2006, Intel,
37. Shahin Farahani, PhD, 2006, Qualcomm Inc,
38. Nazanin Darbanian, M.S. Freescale, Tempe, Arizona
39. *Joe Rutkowski, Joseph, MS, 2004, Phillips.*
40. *Chaudhuri, Bikram, Synthesizer, MS/PhD, MS 2004.*
41. *Zhang, Jiandong, MEMs, MEMS, December-04*
42. *Afsahi, Ali, MS/PHD, UC San Diego, QUALCOMM, Connection One*
43. *Chen, Xiaomin, UWB, PHD, 2007, SRC/Motorola*
44. *Jali, Hilda, Power Management, MS, June-05,*
45. *Xuejin Wang, RF Optimization, 2006 CAD tools, PhD, Neo-Linear*
46. *Umar Lyles, Power Amplifier, MS, 2006. Texas Instruments*
47. MS, Erika Munoz, RADHARD, 2007, Intel
48. Waleed Khali, (Co-Advisor), Professor at Ohio State
49. Jennifer Kitchen, PhD, 2009, Professor at ASU
50. Shahin Mehdizad Taleie, RFDAC, PhD, 2009, Qualcomm
51. Ilker Deligoz, PHD, 2009, Qualcomm
52. Hyung Kim, PhD, Jan 2010, Intel
53. Jung Le, PhD 2010, Intel, TI
54. Syed Naqvi, PhD, 2012, Intel.
55. Todd Martin, MS, 2011, TI
56. Seungkee Min, PhD, 2011, Intel
57. Ali Meamar, Post Doc, RFIC 2013
58. Hitesh Khunti, MS 2013, Qualcom
59. Debashis Mandal, Post Doc, Research faculty 2015-2018
60. Edgar Martinez, PhD, 2015, Qualcomm
61. Chirag Desai, MS, 2016, Qualcom
62. Sanjay Avasarala, MS, 2016

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- 63. Li Ming, MS, 2017
- 64. Qirong Peng, MS, 2017,
- 65. Yu Geng, PhD, 2018
- 66. Amir Ayati, PhD Aug 2018; Qualcomm
- 67. Pasisa Mahmoudi, PhD, May 2019, Qualcomm
- 68. Chai Yong, MS: 2015, PHD: 2019, Qualcomm
- 69. Shrikant Singh, MS: 2016, PhD, 2019, Movandi
- 70. Amir Alizadeh, Research Faculty 2019-Present
- 71. Ata S. PhD, 2021, Ata Sarrafinejad, PhD, 2021

UNIVERSITY COMMITTEES

Various Committees at ASU, Oregon State University, etc.

INDUSTRY COMMITTEES

- Arizona Telecommunications and Information Council (ATIC), Board Member
- CAS Fellows Committee (ends December 31, 2006)
- *IEEE CAS Phoenix Chapter Organizers (the committee is in the process of determining new chair – current chair not active)*
- *Executive Committee, RFIC 2006.*
- *Technical Program Comm, IEEE RFIC 2006.*
- *Executive Committee, Conferences, International Solid State System's Conference.*
- *IEEE CAS Society, VLSI Technical Comm. Member*
- *Editorial Board, IEEE Communications Surveys & Tutorials*
- *Radio Frequency Integrated Circuits- RFIC 2006*
- *IEEE RF Integrated Circuits Conference, Committee Chair for two workshops*
- *International Microwave Symposium, IMS-MTT 2006*
- *Int. Symposium on Circuits and Systems - ISCAS 2006*
- *Wireless Networks & Emerging Technologies, WNET06*
- *Midwest Symposium on Circuits and System*
- *Arizona Governor IT Advisory Committee – GITA*
- *Arizona Telecom – ATIC*

INSTRUCTIONAL SUMMARY

- Digital IC Design, Analog IC Design, Advance CMOS Analog IC, VLSI, RFIC Design
- Wireless Transceiver Design, Wireless Communications, GPS, Telecomm Systems, Digital Communication

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- Signal Processing, Advance digital signal processing, Communication, Digital Communication, Digital Audio Processing, Adaptive array processing
- Computer Architecture, Microprocessor System Architecture, Pipeline Array Processing