

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANKER INNOVATIONS LTD.,
Petitioner

v.

MYPAQ HOLDINGS LTD.,
Patent Owner

Case IPR2022-01134
Patent 8,477,514

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,477,514

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LIST OF EXHIBITS

1001	U.S. Patent No. 8,477,514 by Artusi et al. (“the ’514 Patent”)
1002	Expert Declaration of Dr. Sayfe Kiaei
1003	Excerpts of the ’514 Patent File History
1004	U.S. Patent No. 6,873,136 to Chagny (“Chagny”)
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1006	U.S. Patent Application Publication No. 2004/0174152 to Hwang et al. (“Hwang”)
1007	U.S. Patent No. 6,748,545 to Helms (“Helms”)
1008	Comparisons of Claims 11-15 to 16-20 of the ’514 Patent
1009	Ned Mohan et al., <i>Power Electronics: Converters, Applications, and Design</i> (John Wiley & Sons, Inc., New York, 2d Ed. 1995)
1010	MyPAQ’s Preliminary Infringement Contentions, Exhibit 16, served in <i>MyPAQ Holdings, Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , 6:21-CV-398-ADA
1011	MyPAQ’s Preliminary Infringement Contentions, Exhibit 21, served in <i>MyPAQ Holdings, Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , 6:21-CV-398-ADA
1012	Alan Grebene, <i>Bipolar and MOS Analog Integrated Circuit Design</i> (John Wiley & Sons, Inc., 1984) (“Grebene”)
1013	MyPAQ’s Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , 6:21-CV-398-ADA
1014	<i>MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd. et al.</i> , No. 21-cv-00398, Dkt. 40 (W.D. Tex. Nov. 29, 2021) (“Scheduling Order”)
1015	S.A. Money, <i>Microprocessor Data Book</i> (Academic Press, Inc., 2 nd ed. 1990)

1016	MyPAQ’s Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Dell Technologies Inc. et al.</i> , 6:21-CV-933-ADA
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1018	MyPAQ’s Preliminary Infringement Contentions, Exhibit 7, served in <i>MyPAQ Holdings, Ltd. v. Dell Technologies Inc. et al.</i> , 6:21-CV-933-ADA
1019	MyPAQ’s Preliminary Infringement Contentions, served in <i>MyPAQ Holdings, Ltd. v. Anker Innovations Ltd.</i> , 6:22-CV-150-ADA

Citations to exhibits including patents and patent applications reference original page, column, paragraph, or line numbers found in the underlying document.

Citations to other exhibits refer to exhibit page numbering.

LIST OF CLAIMS**Claim 1:**

1[pre]	A power converter coupled to a load, comprising:
1[a]	a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and
1[b]	a power converter controller configured to receive a signal from said load indicating a system operational state of said load and
1[c]	control an internal operating characteristic of said power converter as a function of said signal.

Claim 2:

2	The power converter as recited in claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.
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Claim 3:

3	The power converter as recited in claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.
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Claim 4:

4	The power converter as recited in claim 1 wherein said load is a processor and said system operational state is dependent on one of a core state and a performance state of said processor.
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Claim 5:

5	The power converter as recited in claim 1 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.
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Claim 6:

6[pre]	A power system, comprising:
6[a]	a power system controller configured to provide a signal characterizing a power requirement of a processor system; and
6[b]	a power converter coupled to said processor system, comprising:
6[c]	a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and
6[d]	a power converter controller configured to receive a signal from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.

Claim 7:

7	The power system as recited in claim 6 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.
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Claim 8:

8	The power system as recited in claim 6 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.
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Claim 9:

9	The power system as recited in claim 6 wherein said power requirement of a processor system is dependent on one of a core state and a performance state of said processor system.
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Claim 10:

10	The power system as recited in claim 6 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.
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Claim 11:

11[pre]	A power system, comprising:
11[a]	a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof,
11[b]	said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain; and
11[c]	a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and
11[d]	to control an internal operating characteristic of said power converter as a function of said power level.

Claim 12:

12[pre]	The power system as recited in claim 11
12[a]	wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof,
12[b]	said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

Claim 13:

13	The power system as recited in claim 11 wherein said signal is provided upon startup of said processor system.
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Claim 14:

14	The power system as recited in claim 11 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.
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Claim 15:

15	The power system as recited in claim 11 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of a power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.
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Claim 16:

16[pre]	A method of operating a power system, comprising:
16[a]	enabling operation of components of a processor system to establish a state of power drain thereof;
16[b]	providing a signal to identify operation of said processor system in said state of power drain;
16[c]	sensing a power level of said state of power drain in response to said signal; and
16[d]	controlling an internal operating characteristic of a power converter as a function of said power level.

Claim 17:

17[pre]	The method as recited in claim 16, further comprising:
17[a]	inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and
17[b]	controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.

Claim 18:

18	The method as recited in claim 16 wherein said signal is provided upon startup of said processor system.
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Claim 19:

19	The method as recited in claim 16 wherein said controlling said internal operating characteristic comprises occurs over a period of time.
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Claim 20:

20	The method as recited in claim 16 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of a power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.
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I. MANDATORY NOTICES

Real Party in Interest: The real party in interest include Anker Innovations Ltd. (“Anker”) (“Petitioner”).

Related Matters: The ’514 Patent is currently asserted by Patent Owner against Samsung in the case styled: *MyPAQ Holdings Ltd. v. Samsung Electronics Co., Ltd.*, 6:21-CV-00398 (W.D. Tex.) (“Samsung Litigation”), which was originally filed on April 23, 2021. The ’514 Patent is also currently asserted by Patent Owner against Dell in the case styled: *MyPAQ Holdings Ltd. v. Dell Technologies Inc.*, 6:21-CV-00933 (W.D. Tex.) (“Dell Litigation”). The ’514 Patent is further currently asserted by Patent Owner against Anker in the case styled: *MyPAQ Holdings Ltd. v. Anker Innovations Ltd.*, 6:22-CV-00150 (W.D. Tex.) (“Anker Litigation”).

Petitioner is also concurrently filing a Petition for IPR against another patent held by PO, which is related to the ’514 Patent: IPR2022-01131 against U.S. Patent No. 7,675,759. The ’514 Patent is a continuation of an intervening continuation-in-part that claims priority to the ’759 Patent. *See* EX1001.

Lead Counsel and Back-Up Counsel: Petitioners designate lead and back-up counsel as noted below. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

Lead Counsel	Back-Up Counsel
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Service Information: Correspondence to lead and back-up counsel can be provided at the postal and electronic addresses above. Petitioners also consent to service by electronic mail at Anker514IPR@rimonlaw.com.

II. STANDING AND FEES

Standing: Petitioners certify under 37 C.F.R. § 42.104(a) that the '514 Patent is eligible for *inter partes* review and that Petitioners are not barred or estopped from requesting *inter partes* review on the grounds set forth herein.

Fees: The Office is authorized to charge the fee set forth in 37 C.F.R. § 42.15(a) to Deposit Account No. 50-5992 and any additional fees that might be due in connection with this Petition.

III. OVERVIEW OF THE '514 PATENT

A. Subject Matter

The '514 Patent involves power converters, which may convert an input voltage into an output voltage. EX1001, 2:42-45. Figure 2 illustrates an example “buck” power converter:

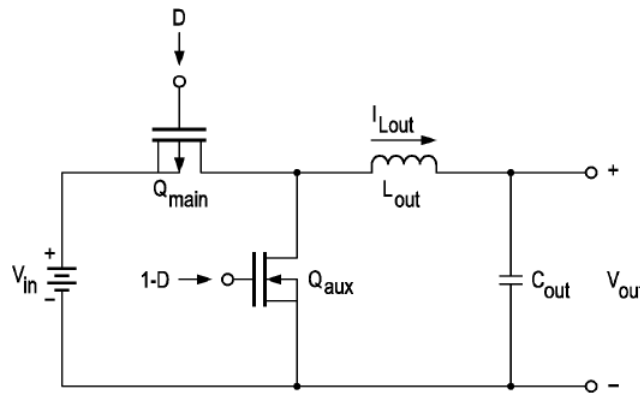


FIG. 2
(PRIOR ART)

EX1001, Fig. 2. The main power switch Q_{main} and auxiliary power switch Q_{aux} are turned on and off by drive signal D and complementary drive signal $1-D$ respectively. *Id.*, 10:56-11:6. When Q_{main} is turned on, Q_{aux} is turned off, and vice versa. As known in the art, and explained in the '514 Patent background, the duty cycle of the switches (i.e., ratio of on-time to the total switching period) in a power converter can be adjusted to regulate the output voltage V_{out} of the power converter. *Id.*, 2:57- 3:9, 11:15-18; EX1002, ¶38.

The '514 Patent purports to improve power converters by using an “adaptive controller.” EX1001, Abstract. The '514 Patent acknowledges that it was “well known” to control output characteristics (e.g., the output voltage) of a converter based on the needs of a microprocessor coupled to the output. *Id.*, 4:63-5:4. But, the '514 Patent purports to improve upon the prior art by adjusting an internal operating characteristic of the power converter based on a signal from an external source. *Id.*, 6:36-44. For example, when a load such as a microprocessor goes into a low-power system

operational state (e.g., a standby mode), the microprocessor may signal the power converter to adjust its internal operating characteristics (e.g., switching frequency) to improve the efficiency of the power converter during such times of low demand from the load.

However, as shown herein, power converters capable of adjusting internal operating characteristics (e.g., switching frequency) to improve efficiency based on the state of the load were well known before the '514 Patent. EX1002, ¶¶39-40.

B. Prosecution History

U.S. Patent Application No. 12/709,795 was filed on February 22, 2010, as a continuation of application No. 12/051,334 filed on March 19, 2008. *See* EX1001.

In a March 18, 2011 office action, the Examiner rejected all pending claims based on anticipation and obviousness grounds. EX1003, 83-90. In response, Applicant distinguished the prior art asserted by the Examiner for failure to disclose a power converter controller “configured to be responsive to an externally generated signal from the power converter.” *Id.*, 76. Thereafter, the Examiner issued a Notice of Allowance.

But, as described herein, Examiner failed to consider any of the prior art references cited herein, each disclosing a power converter controller responsive to an external signal.

IV. SUMMARY OF PRIOR ART

The '514 Patent claims priority to December 1, 2006, and thus is subject to the pre-AIA provisions of 35 U.S.C. §§ 102 and 103. Petitioners reserve the right to challenge whether the claims of the '514 are entitled to the claimed December 1, 2006 priority date. However, each prior art reference relied upon in this Petition is prior art to the '514 Patent regardless of the claimed December 1, 2006 priority date.

Neither *Chagny* nor *Hwang* described below were considered during examination of the '514 Patent.

A. *Chagny* (EX1004)

Chagny (U.S. Patent 6,873,136) issued on March 29, 2005. EX1004. *Chagny* is prior art under 35 U.S.C. §§ 102(a) and (b).

Chagny discloses a voltage regulator module (VRM) 200 (i.e., a power converter) that provides a “regulated DC voltage output 295” to processor 292. EX1004, 3:52-58.

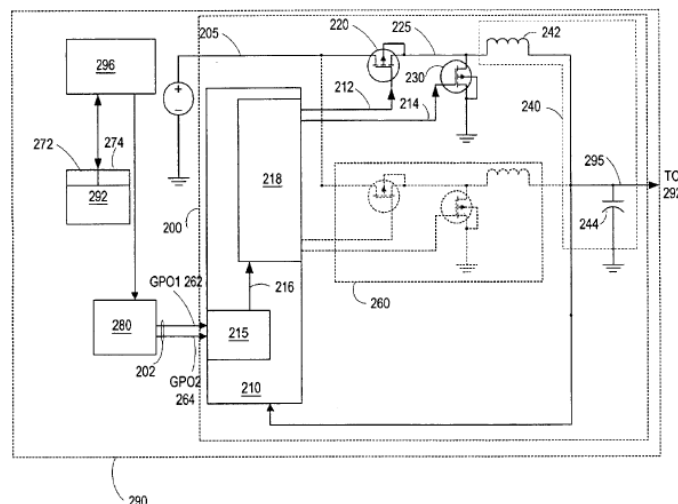
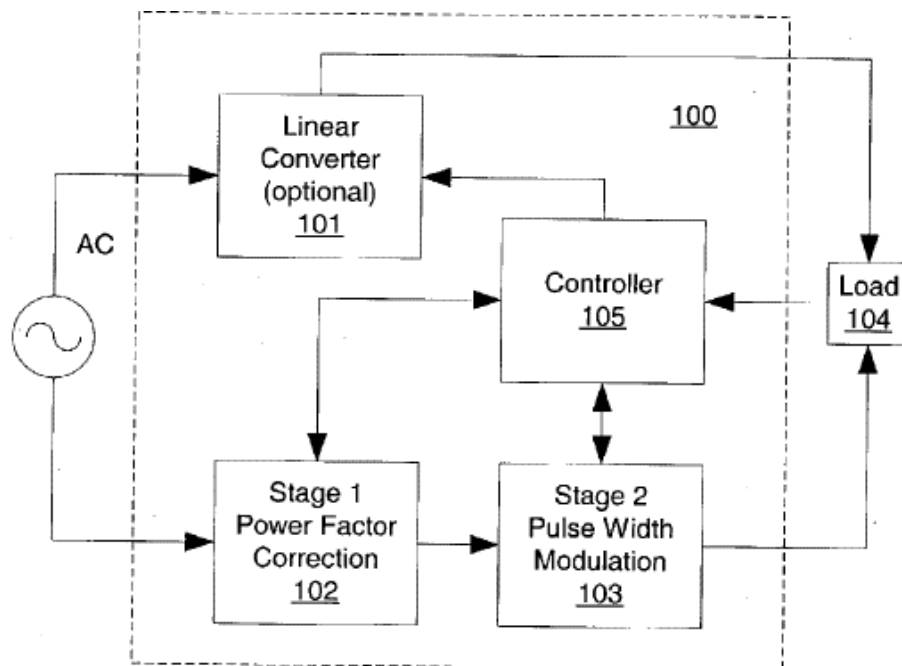


FIG. 2A

EX1004, Fig. 2A. *Changny*'s controller module 210 receives an activity input 202, which is generated outside of VRM 200 and indicates the processor's activity level. *Id.*, 3:60-65. The switching frequency of VRM 200 changes according to activity input 202. *Id.*, 5:9-12. By selecting a low switching frequency during periods of low processor activity, the efficiency of VRM 200 is improved. *Id.*, 5:20-23; EX1002, ¶47.

B. Hwang (EX1006)

Hwang (U.S. Patent Application Publication 2004/0174152) published on September 9, 2004. EX1006. *Hwang* is prior art to the '514 Patent under 35 U.S.C. §§ 102(a) and (b). *Hwang* discloses a power converter 100 coupled to a smart load 104 (e.g., a microprocessor). EX1006, [0019], [0021].



EX1006, Fig. 1. *Hwang* discloses that smart load 104 sends a standby signal to the controller 105 within power converter 100 indicating the level of power drawn by load 104 and thereby causing “PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021])

in order to “improve efficiency” (*id.*, Abstract). EX1002, ¶49.

V. SUMMARY OF GROUNDS

Ground	Claims	Statutory Basis (35 U.S.C. §)	Prior Art
1A	1-12, 14-17, 19-20	102	<i>Chagny</i>
1B	1-20	103	<i>Chagny</i>
2A	1-10, 16-17, 19-20	102	<i>Hwang</i>
2B	11-12, 14-17, 19-20	103	<i>Hwang, Chagny</i>
2C	18	103	<i>Hwang</i>
2D	13, 18	103	<i>Hwang, Chagny</i>

EX1002, ¶50.

VI. LEVEL OF ORDINARY SKILL

A POSITA at the time of the '514 Patent would have had either (i) a Masters of Science in Electrical Engineering, or an equivalent field, or (ii) a Bachelor of Science in Electrical Engineering or an equivalent field as well as at least two years of experience in the design of power electronics. EX1002, ¶35.

VII. CLAIM CONSTRUCTION

Claim terms are construed according to their ordinary and customary meaning as understood by a POSITA and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). For purposes of this Petition, Petitioners interpret all claim terms in

accordance with their ordinary and customary meaning.

VIII. INSTITUTION IS PROPER

A. Institution is Proper Under 35 U.S.C. § 314(a)

The six factors considered for § 314 denial strongly favor institution. See *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). The district court case is at an early stage and no trial date has been set. Petitioner has diligently prepared and filed this petition only about four months after Patent Owner filed its complaint against Anker.

1. No evidence regarding a stay. This petition precedes even the entry of any procedural schedule in the co-pending litigation, within which Anker intends to move for a stay after this petition is instituted, or earlier depending upon circumstances in the Western District of Texas. *Sand Revolution II LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative). Thus, Factor 1 does not support discretionary denial.
2. Parallel proceeding trial date. No schedule has been entered and no trial date set. Without a trial date, this factor weighs heavily against discretionary denial.
3. Investment in the parallel proceeding. Petitioner has filed this Petition at a very early stage of the litigation—a fact that “has weighed against exercising the authority to deny institution.” *Apple, Inc. v. Seven Networks*, IPR2020-00156, Paper 10 at 11-12 (June 15, 2020). Petitioner has not served its invalidity

contentions. The parties have not exchanged preliminary positions on claim construction or invalidity, and fact and expert discovery has not begun. Further, there is no evidence that the district court will conduct a *Markman* hearing or issue a *Markman* ruling before the prospective date for the Board's institution decision. Anker's promptness favors institution. *Fintiv*, Paper 11 at 11 ("If the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed against exercising the authority to deny institution under NHK.").

4. Overlapping issues with the parallel proceeding. The co-pending litigation is in its infancy. Petition challenges claims not asserted by the PO in district court. Compare EX1019 (asserting 16 claims against Anker) with Section V (challenging all 20 claims). Thus, "[i]nstituting trial here serves overall system efficiency and integrity goals ... by resolving materially different patentability issues." *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 at 19 (P.T.A.B. June 15, 2020) (finding the fourth factor "strongly" favored institution even though there was no stipulation). Nevertheless, to eliminate any doubt regarding overlap between the proceedings, Petitioner hereby stipulates that, if the Board institutes *inter partes* review of this Petition, then Petitioner, and the Real Parties in Interest listed herein, will not assert in the Anker Litigation that any of claims 1-20 of the '514 Patent is invalid on any ground involving the prior art relied upon in the grounds of invalidity herein. A lack of such overlap "has

tended to weigh against exercising discretion to deny institution.” *Fintiv*, IPR2020-00019, Paper 11, 12-14.

5. Petitioner is a defendant. Anker is a defendant in the litigation. Because it is “far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same,” panels routinely grant institution when the parties are the same as in a district court proceeding. *See Sand Revolution II* at 12-13. Due to the exceedingly early stage of this litigation, Factor 5 is neutral and should not be a basis for denying institution.
6. Other circumstances. The prior art presented in this Petition renders the Challenged Claims unpatentable as obvious. The merits of Petitioner’s arguments are strong, especially given that the Board has already instituted IPR2022-00311 filed by Samsung/Dell against the same patent using the same grounds. Thus, this factor weighs against discretionary denial.

As such, because the *Fintiv* factors are either neutral or weigh against discretionary denial, and because this Petition was filed more than eight months before the statutory bar date, institution should not be denied on discretionary factors.

B. Discretionary denial under *General Plastic* is not appropriate

The ’514 patent is being challenged in case no. IPR2021-00311, but here, Anker is seeking to join that earlier case by filing this substantively identical Petition along with a motion for joinder. The present petition is permissible under 35 U.S.C. § 315(c), and is not a “follow-on” petition seeking to raise new issues. *Celltrion, Inc. v.*

Genentech, Inc., IPR2018-01019, Paper 11 at 9-11 (PTAB Oct. 30, 2018). As explained by the Board in *Celltrion*, the *General Plastic* factors do not weigh in favor of discretionary denial where, as here, “a different petitioner files a ‘me-too’ or ‘copycat’ petition in conjunction with a timely motion to join.” *Id.* (the motion to join “obviates any concerns of serial harassment”).

C. Institution is Proper Under 35 U.S.C. § 325 (d)

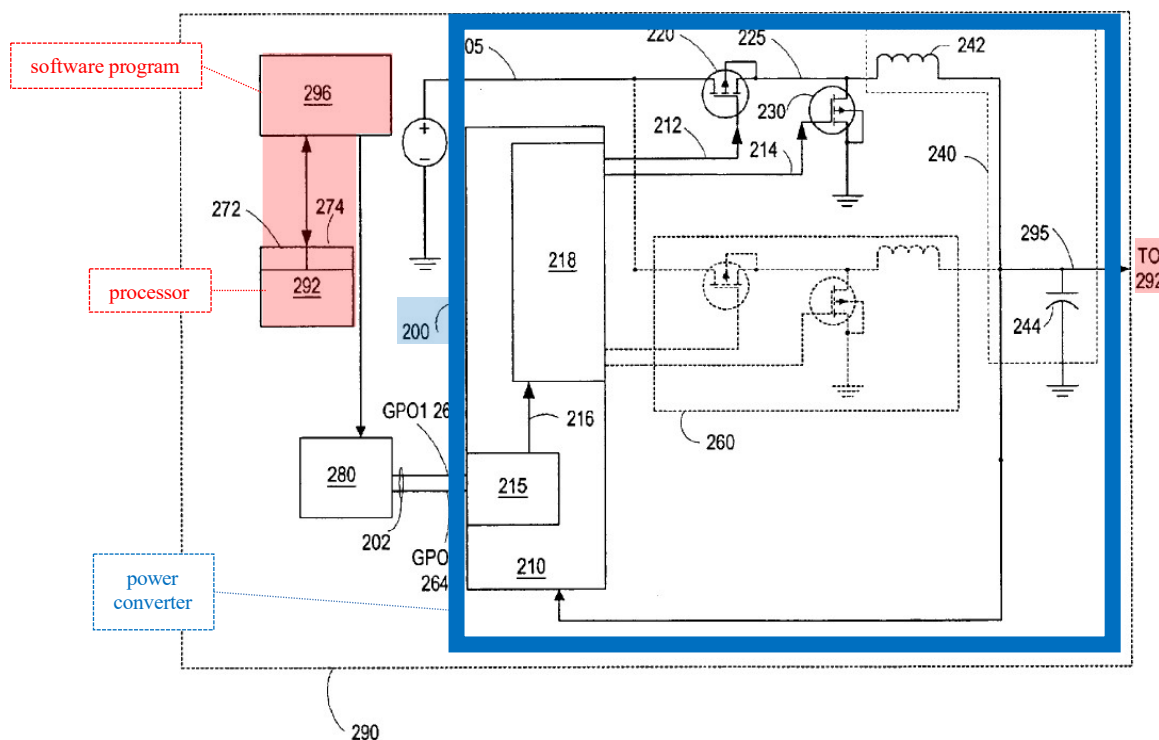
None of the *Becton, Dickinson* factors weigh in favor of discretionary denial under 35 U.S.C. § 325(d). *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential). None of the references relied upon by this Petition were before the Examiner, much less included in a rejection, during prosecution. Thus “the same or substantially the same prior art or arguments” were *not* previously presented to the Office.

IX. GROUND 1A: Chagny Anticipates Claims 1-12, 14-17, and 19-20

A. Claim 1

i. 1[pre]: “A power converter coupled to a load, comprising:”

Chagny discloses a voltage regulator module (“VRM”) (i.e., a power converter). “The VRM 200,” shown in Figure 2A, “is operable to receive a direct current (DC) voltage input 205 and generate a regulated DC voltage output 295.” EX1004, 3:54-56.



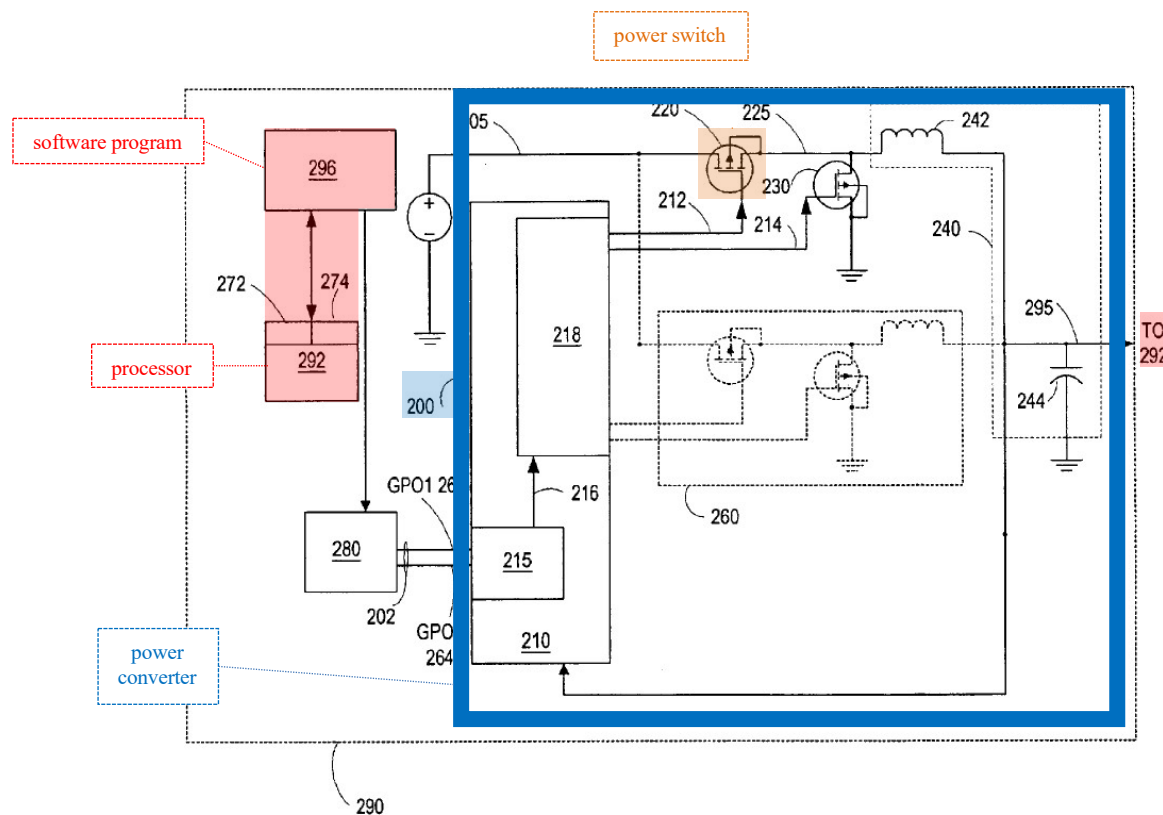
EX1004, Fig. 2A (annotated); EX1002, ¶52. As shown in Figure 2A, the output of VRM 200 is coupled to provide power to a load including processor 292 and software program 296. EX1004, 3:56-60 (“[T]he regulated DC voltage output 295 provides power to a processor 292 included in an information handling system device 290. The output 295 may also be used to power other components (not shown) included in the device 290.”); *see also id.*, 4:35-37 (referring to software program 296 being “included in the operating system (not shown) of the device 290”), 7:36-41 (describing processor “operable to execute instructions and/or operations” including a “software program” stored in memory).

Thus, *Chagny* discloses claim 1[pre]. EX1002, ¶¶52-53.

- ii. 1[a]: “a power switch configured to conduct for a duty cycle to

provide an output characteristic at an output thereof; and”

Switches 220 and 230, inductance L 242, and capacitor C 244, are configured in what is known as a “buck” power-converter topology. See EX1004 (*Chagny*), 1:51-59 (describing “buck” DC-DC converter); EX1001 (’514 Patent), Fig. 2, 10:56- 11:19 (describing “buck” power converter); EX1002, ¶54. *Chagny*’s charge switch 220 serves as a “power switch” configured to conduct for a duty cycle to provide a regulated output as recited in claim 1[a]. EX1002, ¶54.



EX1004, Fig. 2A (annotated); EX1002, ¶55.

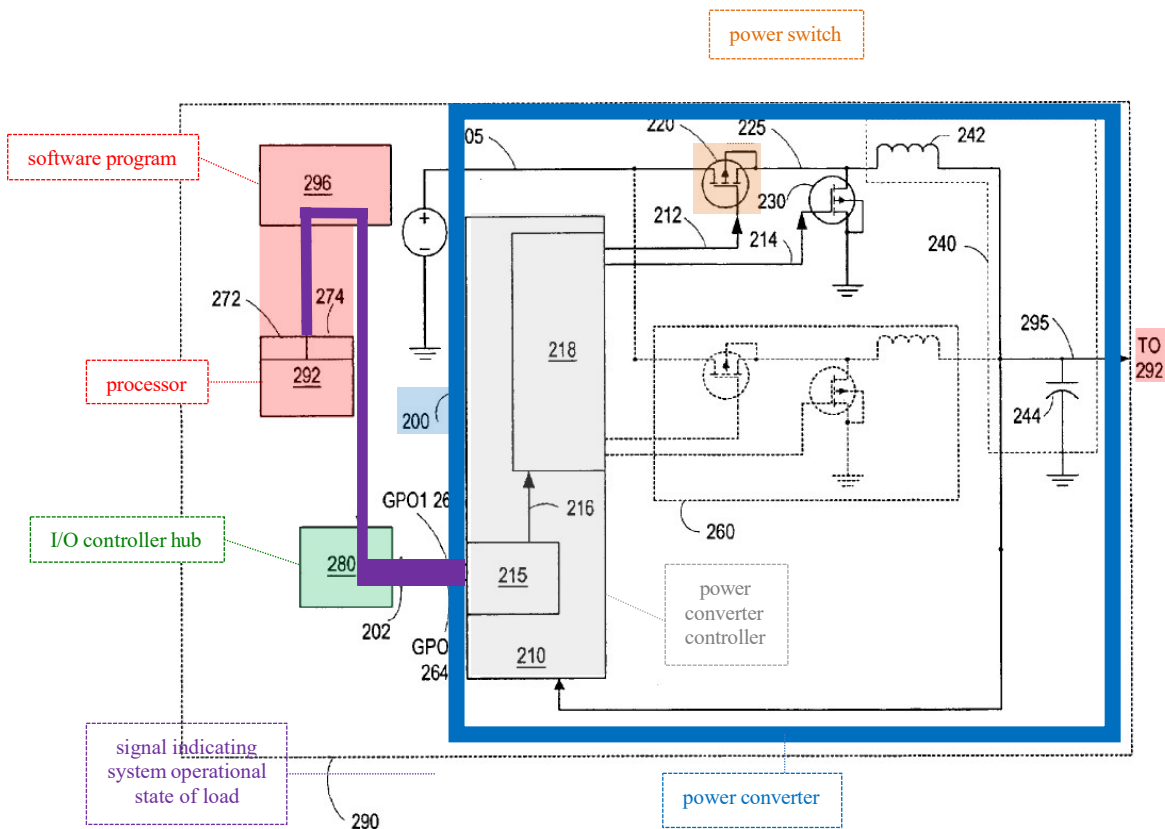
It was well-known in the art that, in the baseline equation for a buck power converter, the output voltage is equal to the input voltage times the duty cycle of the high-side switch (referred to as charge switch 200 in *Chagny*), where the duty cycle is

the ratio of the on-time (i.e., conduction time) of the high-side switch to the overall switching period. EX1002, ¶¶56-57; EX1009, 19 (deriving equation for buck). Consistent with this understanding, *Chagny* describes how charge switch 220 (i.e., the power switch) and discharge switch 230 turn on and off in an alternating fashion from each other. EX1004, 5:34-40, 6:45-49; EX1002, ¶57. A square wave that alternates between the DC voltage input 205 and ground is generated at node 225. EX1004, 5:40-42 (“The DC voltage input 225 is ‘chopped’ by the charge switch 220 to generate the switched DC voltage output 225.”); EX1002, ¶58. The square wave at node 225 therefore has average voltage over time that is equal to the input voltage 205 times the duty cycle of the charge switch 220 (i.e., the power switch). EX1002, ¶58. The square wave at node 225 is filtered by inductance 242 and capacitor 244 to provide a regulated output voltage based on the average value of the square wave (i.e., based on the duty cycle of charge switch 220). *See* EX1004, Fig. 2A, 5:44-46 (“The square wave ... has an average voltage equal to the required output voltage.”); 5:47-51 (describing filtering of switched voltage to generate regulated output voltage), 4:63-65 (describing feedback from output voltage for regulation); EX1002, ¶59.

Accordingly, based on *Chagny*’s disclosure, a POSITA would have understood that “charge switch 220” (i.e., the power switch) is configured to conduct for a duty cycle to provide “DC voltage output 295” (i.e., an output characteristic) at the output of VRM 200 (i.e., at the output of the power converter). *Chagny* thus discloses claim 1[a]. EX1002, ¶¶60-61.

- iii. 1[b]: “a power converter controller configured to receive a signal from said load indicating a system operational state of said load and”

Chagny’s VRM 200 (i.e., the power converter) includes a “controller module 210” (i.e., a power converter controller). EX1004, 3:59-65. As shown in Figure 2A, controller module 210 is configured to receive a signal from the load including processor 292 and software program 296:



EX1004, Fig. 2A (annotated); EX1002, ¶62. As shown above, software program 296 receives a signal from processor 292 indicating the activity level of processor 292. EX1004, 4:35-40 (“In one embodiment, a software program 296, which may be included in the operating system (not shown) of the device 290, monitors the

processor 292 loading.”); EX1002,¶62. In turn, “software program 296 generates activity input 202” and sends that signal to the controller module 210. EX1004, 4:40-43, Fig. 2A. “The controller module 210 includes a frequency selector module 215” that is “operable to receive the activity input 202.” *Id.*, 4:62-67; *see also* 4:59- 61 (describing one embodiment also including the I/O controller hub (ICH) 280 shown in Figure 2A).

Chagny also explains that “activity input 202” is “indicative of the activity level of the processor 292” (i.e., indicating a system operational state of the load).¹ *Id.*, 5:11-12; 4:40-43. Accordingly, a POSITA would have understood that *Chagny*’s controller module 210 (i.e., the power converter controller) is configured to receive a signal from the load indicating the system operational state of said load. EX1002,¶¶63-65.

Chagny thus discloses claim 1[b]. EX1002,¶66.

¹ The ’514 Patent describes “system operational states” as including, for example, the “core state” of a processor that affects the processor’s “level of power consumption.” EX1001, 5:19-27, 5:44-46. The highest core state “describes a processor at its full operational level,” while various “sleep levels” are “achieved by halting instruction execution.” *Id.*, 5:46-55. Like the system operational states described in the ’514 Patent specification, the activity level of *Chagny*’s processor 292 depends “on the number of instructions executed within a predefined time interval” (EX1004, 4:18-20), and thus reflects the “demand for power required by the processor 292” (*see id.*, 5:62-64). EX1002,¶64.

iv. 1[c]: “control an internal operating characteristic of said power converter as a function of said signal.”

Chagny’s controller module 210 “dynamically changes the switching frequency 216” (i.e., controls an internal operating characteristic)² of VRM 200 “responsive to the activity input 202” (i.e., as a function of said signal). EX1004, 5:9-12; *see also id.*, 4:66-5:3 (“The frequency selector module 215 is operable to receive the activity input 202 ... and select a switching frequency 216 from a plurality of switching frequencies”), 5:3-8 and 5:12-18 (listing processor activity levels and corresponding VRM switching frequencies), 4:46-49.

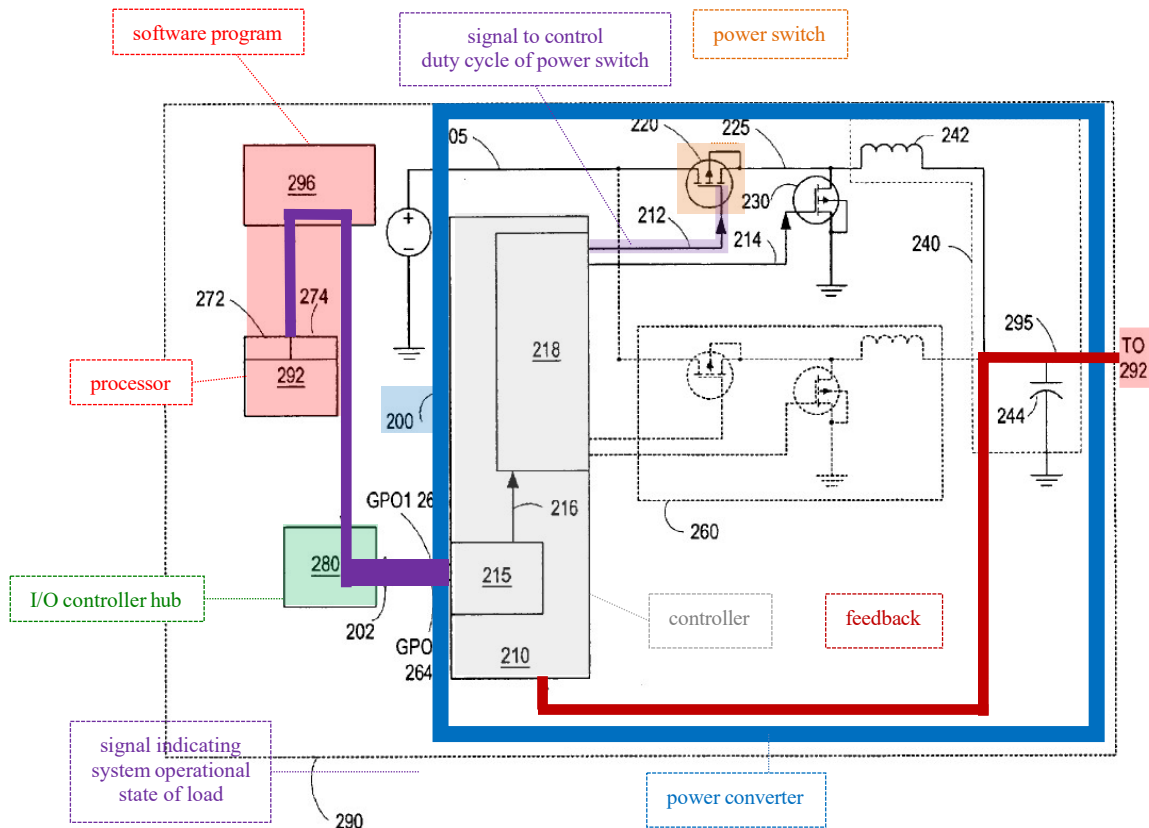
Chagny thus discloses claim 1[c]. EX1002, ¶¶67-69.

B. Claim 2

i. “2. The power converter as recited in claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.”

Chagny’s controller module 210 (i.e., said power converter controller) includes “FET driver module 218.” EX1004, 4:62-63. As shown in Figure 2A, FET driver module 218 provides “charge control signal 212” (i.e., another signal) to control the turning on and off of charge switch 220 (i.e., said power switch). *Id.*, 5:38-40.

² The ’514 Patent lists “switching frequency” among example internal operating characteristics. EX1001, 3:28-35.



EX1004, Fig. 2A (annotated); EX1002, ¶¶70-71.

As described for claim 1[a], the duty cycle of charge switch 220 (i.e., the power switch) determines the voltage level of *Chagny*'s "regulated DC voltage output 295." See Section IX.A.ii. And as shown in Figure 2A, "controller module 210 receives the regulated DC voltage output 295 as a feedback input for regulating the output of the VRM 200." EX1004, 4:63-65; see also *id.*, 9:5-7, 10:14-16. Because it is the duty cycle of charge switch 220 that determines the output voltage, and because *Chagny* explicitly states that controller module 210 regulates the DC output voltage as a function of the feedback, a POSITA would have understood that controller module 210 is configured to control the duty cycle of charge switch 220 as a function of the feedback from the

regulated DC voltage output 295 (i.e., as function of said output characteristic). EX1002,¶72; EX1009, 17-18 (describing known duty cycle control as function of feedback from the output voltage).

In addition, “FET drive module 218” controls charge switch 220 in accordance with “activity input 202” (i.e., said signal). *See* EX1004, 5:28-31 (“The FET driver module 218 is operable to receive the selected value of the switching frequency 216 and generate the charge and discharge control signals 212 and 214, each having the switching frequency 216.”); *see also id.*, 4:66-5:2, 5:34-46; EX1002,¶73.

Chagny thus discloses claim 2. EX1002,¶74.

C. Claim 3

- i. **“3. The power converter as recited in claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.”**

As described for claim 1[c] in Section IX.A.iv, *Chagny*’s controller module 210 is configured to “dynamically” control “the switching frequency 216” (i.e., said internal operating characteristic) of VRM 200 in response to the activity input 202. EX1004, 5:9-12; *see also id.*, 4:66-5:3. Moreover, *Chagny* discloses that activity input 202 “may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis.” *Id.*, 4:43-45. Thus, a POSITA would have understood that *Chagny*’s power converter controller is configured to adjust the switching frequency over a period of time as the processor loading (and thus activity input 202) changes. *See id.*, 4:18-20 (referring to “processor 292 loading, usage or activity level” varying “depending on the

number of instructions executed within a predefined time interval.”), 5:65-66 (“[T]he VRM 200 reacts responsively and on time according to the processor 292 demand.”); EX1002, ¶¶75-77.

Chagny thus discloses claim 3. EX1002, ¶78.

D. Claim 4

- i. **“4. The power converter as recited in claim 1 wherein said load is a processor and said system operational state [of said load] is dependent on one of a core state and a performance state of said processor.”**

The ’514 Patent background explains that a “core state” of a processor is “under software operating system control” and affects the “level of power consumption” of the processor. EX1001, 5:44-46. According to the ’514 Patent, the highest core state is where the processor executes instructions “at its full operational level.” *See id.*, 5:46-57; EX1002, ¶79. On the other hand, various core- state “sleep levels” are “achieved by halting instruction execution.” EX1001, 5:48-57. In other words, the “core state” as described in the ’514 Patent background specifies the activity level (e.g., the rate at which instructions are executed) of the processor. EX1002, ¶79.

Chagny discloses that “the software program 296 generates the activity input 202 indicative of levels of activity of the processor 292,” which “includes 2 bits ... GPO1 262 and GPO2 264 ... used to define up to 4 activity levels of the processor 292.” EX1004, 4:43-49; *see also id.*, 4:23-30 (defining high, medium, and low activity level

based on the processor loading). Moreover, “the software program 296 defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clock cycle.” *Id.*, 5:57-61; *see also id.*, 6:3-4. Accordingly, the activity level of processor 292 (i.e., system operational state of the load) at any of the activity levels disclosed by *Chagny* (e.g., low, medium, high) is dependent on at least a core state of the processor 292. EX1002,¶¶80-81.

Chagny thus discloses claim 4. EX1002,¶82.

E. Claim 5

- i. **“5. The power converter as recited in claim 1 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.”**

As described for claim 1[c], the switching frequency is the identified internal operating characteristic of *Chagny*’s power converter. *See* Section IX.A.iv. *Chagny* thus discloses claim 5. EX1002,¶83.

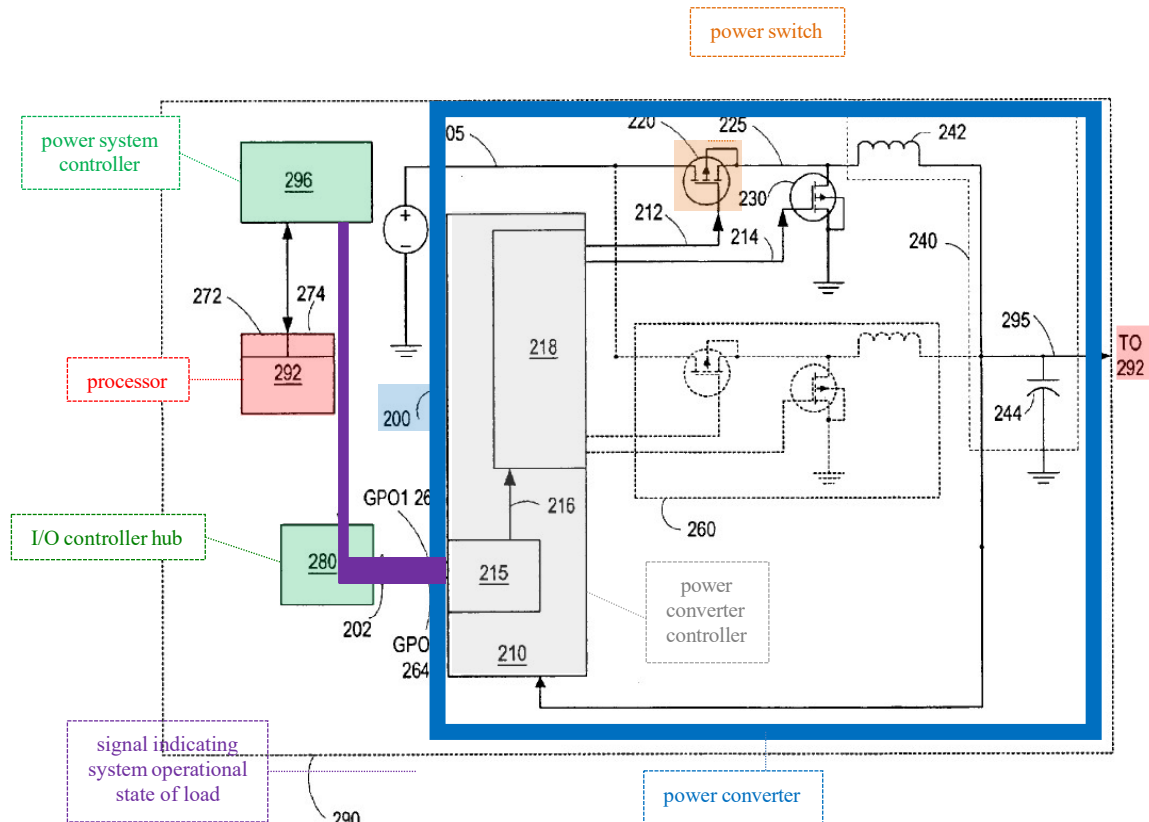
F. Claim 6

- i. **6[pre]: “A power system, comprising:”**

As described below, *Chagny* discloses the recited elements of a “power system,” including a power system controller and a power converter. EX1002,¶84.

- ii. **6[a]: “a power system controller configured to provide a signal characterizing a power requirement of a processor system; and”**

Chagny includes a “software program 296” that “monitors the processor 292 loading.” EX1004, 4:35-37. “Based on the processor 292 loading ... the software program 296 generates the activity input 202” (i.e., a signal), which is “indicative of levels of activity of the processor 292.” *Id.*, 4:40-43. EX1004, Fig. 2A (annotated);



EX1002, ¶85. As noted in *Chagny*, the “demand for power by the processor 292” depends on the activity level—i.e., the “number of instructions executed per clock cycle.” EX1004, 5:62-64; *see also id.*, 4:18-20; EX1002, ¶86. Thus, the “activity input 202 indicative of the activity level of the processor” (EX1004, 5:10-12) is a signal characterizing the power requirement of the processor system.

Chagny states that software program 296 “generates” the activity input 202 signal. EX1004, 4:40-43. And in one embodiment, the bits of activity input 202 are

“stored in an I/O controller hub (ICH) 280 included in the device 290.” *Id.*, 4:59- 61; *see also id.*, 4:46-59. As shown in Figure 2A for embodiments with an I/O controller hub (ICH), the “activity input 202” signal is provided to VRM 200 via I/O controller hub (ICH) 280. *Id.*, Fig. 2A, 4. Accordingly, *Chagny*’s software program 296,³ either alone or collectively with I/O controller hub (ICH) 280, serves as the power system controller⁴ recited in claim 6[a]. EX1002, ¶¶87-88.

Chagny thus discloses claim 6[a]. EX1002, ¶89.

iii. 6[b]: “a power converter coupled to said processor system, comprising:”

As described for claim 1[pre], *Chagny* discloses a “VRM 200” (i.e., a power converter) coupled to provide power to processor 292 (i.e., the processor system). *See* Section IX.A.i; EX1004, 3:52-60, Fig. 2A. *Chagny* thus discloses claim 6[b]. EX1002, ¶90.

³ The ’514 Patent includes embodiments where “the power system controller” is constructed as “an element” of a server (i.e., the load). EX1001, 25:23-27, 21:65- 22:8; *see also id.*, 13:12-13, Fig. 11. Thus, the ’514 Patent contemplates embodiments whereby the “power system controller” is part of the load.

⁴ As an alternative mapping, the I/O controller hub (ICH) 280 alone also serves as the “power system controller” of claim 6[a]. EX1002, ¶88.

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and,”**

Claim 6[c] is identical to claim 1[a] and is disclosed in the manner described for claim 1[a]. *See* Section IX.A.ii; EX1002, ¶91.

- v. **6[d]: “a power converter controller configured to receive a signal⁵ from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.”**

Chagny’s VRM 200 includes a “controller module 210” (i.e., the power converter controller), configured to receive “activity input 202” (i.e., a signal from the power system controller). EX1004, 4:62-67 (“The controller module 210 includes a frequency selector module 215,” which “is operable to receive the activity input 202”); *see also* Section IX.F.ii (claim 6[a]).

As described in Section IX.A.iv for claim 1[c], controller module 210 controls the switching frequency of VRM 200 (i.e., an internal operating characteristic of said power converter) as a function of activity input 202 (i.e., said signal). EX1004, 4:66- 5:3 (“The frequency selector module 215 is operable to receive the activity input 202 ...

⁵ ~~Nothing in the ’514 Patent~~ specification prevents the “signal” of claim 6[d] from being the same “signal” provided by the power system controller in claim 6[a]. *See* EX1001. Indeed, PO’s infringement contentions point to the same signal for both claim 6[a] and 6[d]. *See* EX1010, 5, 11; EX1017, 5, 11.

and select a switching frequency 216 from a plurality of switching frequencies”), 5:3-18; EX1002,¶¶93.

Chagny thus discloses claim 6[d]. EX1002,¶¶92-94.

G. Claim 7

Chagny discloses the additional elements of claim 7 in the same manner described for similar claim 2. *See* Section IX.B; EX1002,¶¶95.

H. Claim 8

Chagny discloses the additional elements of claim 8 in the same manner described for similar claim 3. *See* Section IX.C; EX1002,¶¶96.

I. Claim 9

Claim 9 is similar to claim 4, but recites that “said power requirement of a processor system,” as opposed to the “system operational state,” is dependent on one of a core state and a performance state. As explained in *Chagny*, the processor power requirement depends on the activity level of the processor (i.e., the system operational state). *See* EX1004, 5:62-64 (explaining that “demand for power” depends on activity level, i.e., “number of instructions executed per clock cycle”), 4:18-20; EX1002,¶¶97. Thus, *Chagny* discloses claim 9 for the same reasons described for claim 4. *See* Section IX.D; EX1002¶¶98.

J. Claim 10

Chagny discloses the additional elements of claim 10 in the same manner

described for similar claim 5. *See* Section IX.E; EX1002, ¶99.

K. Claim 11

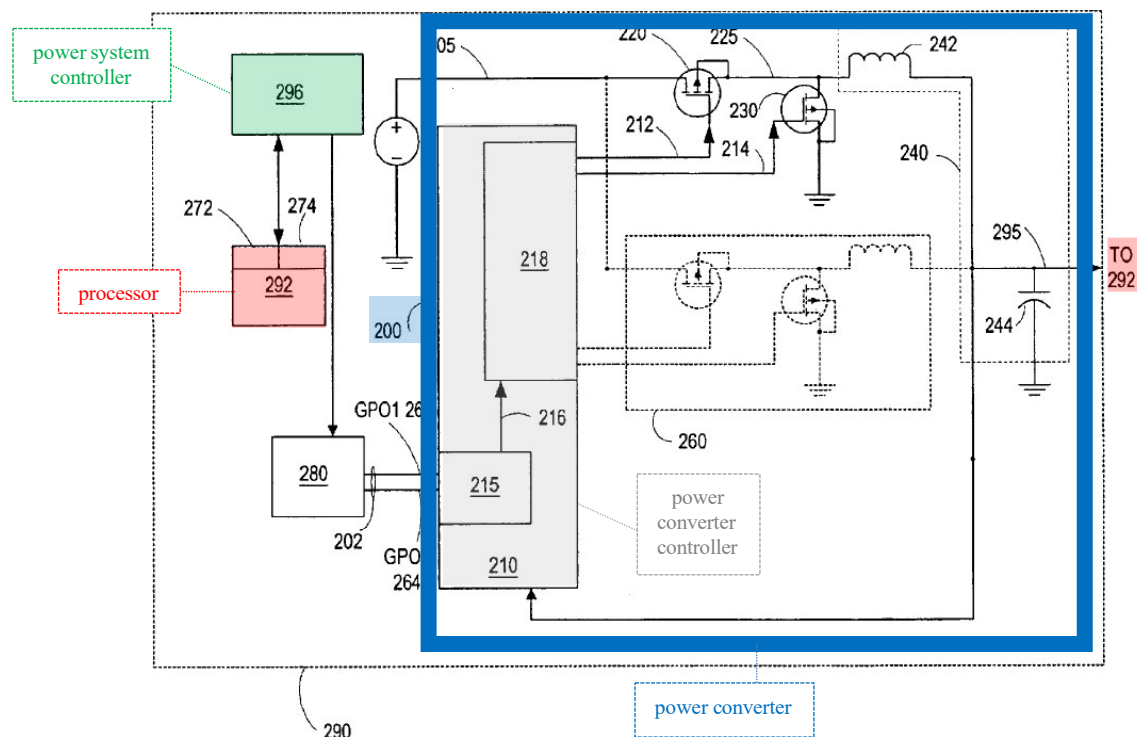
i. 11[pre]: “A power system, comprising:”

As described below, *Chagny* discloses the recited elements of a “power system,” including a power system controller and a power converter comprising a power converter controller. EX1002, ¶100.

ii. 11[a]: “a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof,”

Chagny discloses a device 290 including a processor 292 (i.e., a processor system). *See* EX1004, Fig. 2A, 3:55-60 (referring to “processor 292” and “other components (not shown) included in device 290”).⁶

⁶ The mapping below refers to *Chagny*’s processor 292 as the processor system. But the processor system of *Chagny* also includes other associated components such as “memory” and various “input/output devices.” *See* EX1004, 7:17-30, Fig. 4.



EX1004, Fig. 2A (annotated); EX1002, ¶101.

Chagny includes a “software program 296” (i.e., a power system controller),⁷ that “monitors the processor 292 loading.” EX1004, 4:35-43; *see also* Section IX.F.ii (claim 6[a]). *Chagny* further discloses that the software program 296 “defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clockcycle.” EX1004,

⁷The mapping below refers to *Chagny*’s “software program 296” as the power system controller. But similar to the explanation above for claim 6[a] in Section IX.F.ii, “software program 296” alone or collectively with I/O controller hub (ICH) 280 may serve as the power system controller.

5:57-61; *see also id.*, 6:3-12 (“The UREG B1272 and UREG B2 274 bits are used to define up to 4 activity levels of the processor 292.”). *Chagny* also explains that “demand for power required by the processor 292” depends directly on the activity level of processor 292, i.e., the “number of instructions executed per clock cycle.” *Id.*, 5:62-64; *see also id.*, 4:18-20. Accordingly, *Chagny*’s software program 296 (i.e., the power system controller)⁸ establishes a state of power drain of its processor system by setting the UREG B1 272 and UREG B2 274 bits. EX1002, ¶¶102-103.

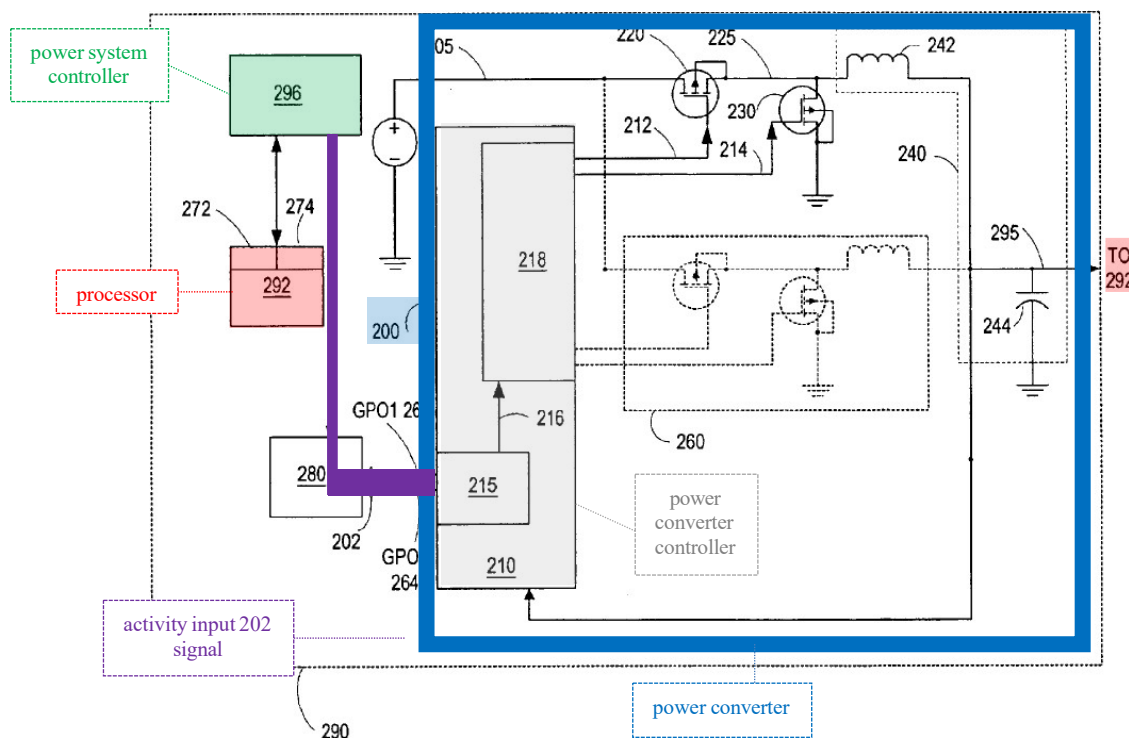
Chagny thus discloses claim 11[a]. EX1002, ¶104.

iii. 11[b]: “said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain; and”

Chagny’s “software program 296” (i.e., said power system controller) “generates the activity input 202” (i.e., provides a signal) to identify the “levels of activity of the processor 292.” EX1004, 4:40-43; *see also id.*, 4:46-49 (“[T]he activity input 202 includes 2 bits ... GPO1 262 and GPO2 264. The 2 bits are used

⁸ ~~The ’514 Patent~~ includes embodiments where “the power system controller” is constructed as “an element” of a server (i.e., the load). EX1001, 25:23-27, 21:65- 22:8; *see also id.*, 13:12-13, Fig. 11. Thus, the ’514 Patent contemplates embodiments whereby the “power system controller” is part of the load.

to defined up to 4 activity levels of the processor 292.”), 4:49-51, 5:10-12; Section IX.F.ii (claim 6[a]).



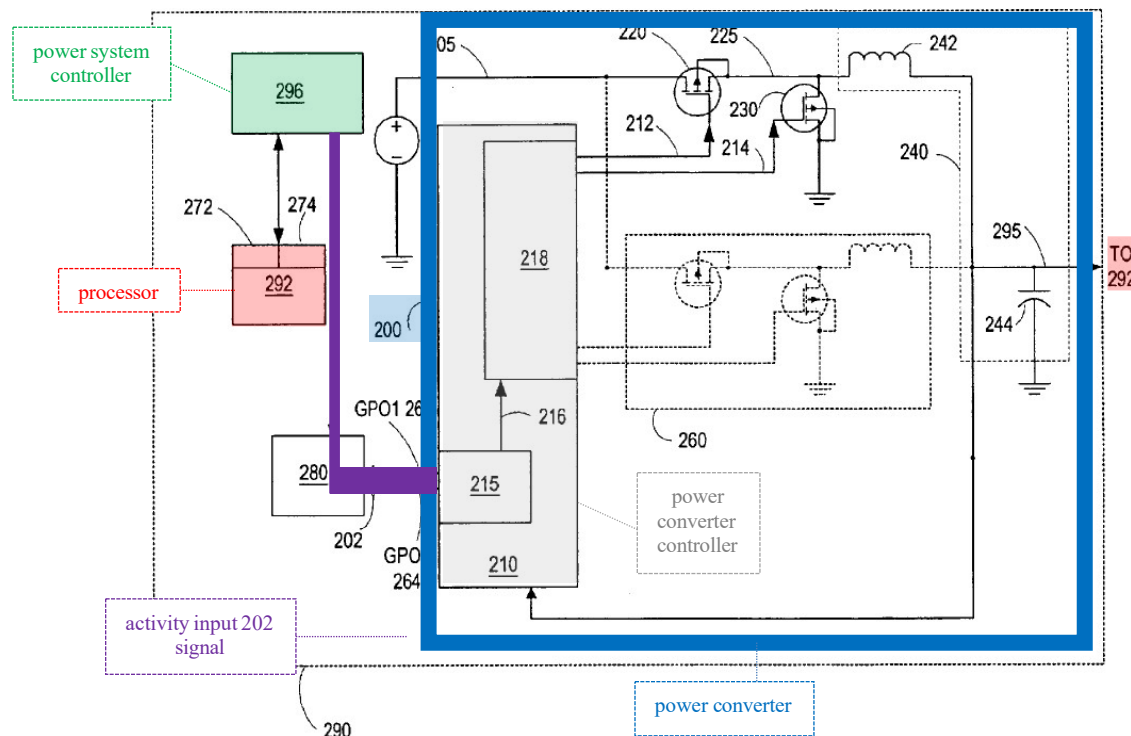
EX1004, Fig. 2A (annotated); EX1002, ¶105.

As explained for claim 11[a], the activity level identified by the “activity input 202” signal corresponds directly to the state of power drain of the processor system. *See* Section IX.K.ii; EX1004, 4:20-30 (describing processor loading under “high,” “medium,” and “low” activity levels); 5:57-64 (describing “demand for power” as function of activity level), 4:18-20; EX1002, ¶106.

Thus, the “activity input 202” signal provided by software program 296 (i.e., the power system controller) identifies the operation of *Chagny*’s processor 292 in the said state of power drain. *Chagny* therefore discloses claim 11[b]. EX1002, ¶¶107-108.

- iv. **11[c]: “a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and”**

As described for claim 1[pre], *Chagny* discloses a voltage regulator module (“VRM”) (i.e., a power converter). *See* Section IX.A.i; EX1004, 3:52-59. *Chagny*’s VRM 200 includes a “controller module 210” (i.e., the power converter controller), configured to receive “activity input 202” (i.e., said signal) from software program 296 (i.e., the power system controller). EX1004, 4:62-67 (“The controller module 210 includes a frequency selector module 215,” which “is operable to receive the activity input 202”); *see also* Section IX.F.ii (claim 6[a]), IX.F.v (claim 6[d]).



EX1004, Fig. 2A (annotated); EX1002, ¶109.

In response to receiving activity input 202 (i.e., said signal), the “frequency

selector module 215” inside controller module 210 selects “a switching frequency 216 ... which dynamically matches the level of activity of the processor 292.” EX1004, 4:63-5:3; *see also id.*, 5:9-27 (describing selection of switching frequencies corresponding to processor activity levels). A POSITA would have understood that the level of the power demanded by *Chagny*’s processor 292 directly depends on the activity level of the processor. EX1002, ¶¶110-111. Indeed, *Chagny* explains that the “demand for power required by the processor 292” depends on the number of instructions executed per clock cycle, i.e., the activity level. *See* EX1004, 5:62-64; *see also id.*, 4:18-20.

Accordingly, based on *Chagny*’s disclosure, a POSITA would have understood that in response to receiving the activity input 202 signal, the “frequency selector module 215” within *Chagny*’s controller module 210 senses the activity input 202 signal and thereby the power level of the state of power drain as indicated by the activity input 202 signal.⁹ EX1002, ¶112. *Chagny* explains how the activity input 202 signal may include,

⁹ Petitioner’s mapping regarding the sensing of *Chagny*’s activity input 202 signal is similar to PO’s position in its district court infringement contentions. For example, PO takes the position that the accused product senses a power level of said state of power drain by receiving a signal allegedly indicative of that power level. *See* EX1011, 9-11 (identifying control channels CC1 and CC2 as signal allegedly representing power level of state of power drain); *see also* EX1018, 9.

for example, 2 bits GPO1 262 AND GPO2 264, that are used to define 4 activity levels of the processor 292. EX1004, 4:46-51. Based on *Chagny*'s disclosure, a POSITA would have understood that the two bits represent 4 power levels corresponding to 4 activity levels of the processor. EX1002, ¶112. These 2 bits are thus utilized by the frequency selector module 215 within *Chagny*'s controller module 210 to sense the power level of the state of power drain.

Notably, *Chagny*'s sensing of the power level in response to the activity input signal 202 is similar to embodiments described in the '514 Patent whereby "a signal" representing "level of power drains" are used "rather than ... an actual drain measurement." EX1001, 13:63-57; EX1002, ¶113.

Chagny thus discloses claim 11[c]. EX1002, ¶114.

v. 11[d]: "to control an internal operating characteristic of said power converter as a function of said power level."

As described in Section IX.A.iv for claim 1[c], *Chagny*'s controller module 210 (i.e., the power converter controller) controls the switching frequency of VRM 200 (i.e., an internal operating characteristic of said power converter) as a function of activity input 202. EX1004, 4:66-5:3, 5:3-18; *see also* Section IX.F.v (claim 6[d]). And as described above for claim 11[c], the activity input 202 signal represents said power level. *See* Section IX.K.iv. *Chagny* thus discloses claim 11[d]. EX1002, ¶¶115-116.

L. Claim 12

- i. **12[a] “The power system as recited in claim 11 wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof,”**

Chagny discloses claim 12[a] in the same manner described for similar claim 1[a]. *See* Section IX.A.ii; EX1002,¶117.

- ii. **12[b] “said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.”**

Claim 12[b] is similar to claim 2, but recites “in accordance with said power level” instead of “in accordance with said signal.” But, as described for claim 11[c], the activity input 202 signal (cited as said signal for claim 2) represents said power level. Thus, *Chagny* discloses claim 12[b] in the same manner as described above for claims 2 and 11[c]. *See* Sections IX.B and IX.K.iv; EX1002,¶118.

M. Claim 14

Chagny discloses the additional elements of claim 14 in the same manner described above for similar claim 3. *See* Section IX.C; EX1002,¶119.

N. Claim 15

Chagny discloses the additional elements of claim 15 in the same manner described above for similar claim 5. *See* Section IX.E; EX1002,¶120.

O. Claim 16

- i. **16[pre]: “A method of operating a power system, comprising:”**
16[a]: “enabling operation of components of a processor system

to establish a state of power drain thereof;”

16[b]: “providing a signal to identify operation of said processor system in said state of power drain;”

16[c]: “sensing a power level of said state of power drain in response to said signal; and”

16[d]: “controlling an internal operating characteristic of a power converter as a function of said power level.”

Claim 16 recites substantially the same elements as claim 11 but in the form of a method claim without the structural requirements of the “power system controller” or the “power converter” comprising a “power converter controller.” *See* EX1008, 1 (side-by-side claim comparison).

As described above for claim 11[pre], *Chagny* discloses a power system, as well as methods for operating the same. *See* Sections IX.F.i (6[pre]) and IX.K.i (11[pre]); EX1004, 2:40-43 (“[T]he present disclosure [] relates to a system and *method* for improving the efficiency of a VRM”). Moreover, *Chagny* discloses the steps of “enabling” (16[a]), “providing” (16[b]), “sensing” (16[c]), and “controlling” (16[d]) in the same manner as described above for claim elements 11[a]-[d], respectively. *See* Sections IX.K.ii-v; EX1002, ¶¶121-124.

P. Claim 17

- i. 17[a]: “The method as recited in claim 16, further comprising: inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and”**

Claim 17[a] is substantially similar to claim 12[a], but in the form of a method

claim. As described for claim 12[a] and claim 1[a], *Chagny* discloses a power converter controller that induces the power switch to perform the claimed step of 17[a]. *See* Sections IX.A.ii (1[a]), IX.L.i (12[a]); EX1002,¶125.

- ii. **17[b]: “controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.”**

Claim 17[b] is substantially similar to claim 12[b] but in the form of a method claim, and is thus disclosed by *Chagny* in the same manner described for claim 12[b]. *See* Sections IX.L.ii (claim 12[b]) and IX.B (claim 2); EX1002,¶126.

Q. Claim 19

Chagny discloses the additional elements of claim 19 in the same manner described above for similar claim 3. *See* Section IX.C; EX1002,¶127.

R. Claim 20

Chagny discloses the additional elements of claim 20 in the same manner described above for similar claim 5. *See* Section IX.E; EX1002,¶128.

X. GROUND 1B: *Chagny* in View of the Knowledge of POSITA Renders Obvious Claims 1-20

A. Claims 1-5

As described in Ground 1A, *Chagny* discloses a load including processor 292 and software program 296. *See* Sections IX.A.i (1[pre]), IX.A.iii (1[b]). To the extent that PO argues that “software program 296” is not part of *Chagny*’s load, a POSITA would have been motivated and found it obvious to execute *Chagny*’s “software program

296,” which may be “included in the operating system” of the device (EX1004, 4:35-37), on processor 292 itself. EX1002, ¶129. Indeed, *Chagny* explains that the “software program 296” monitors the processor loading by “analyzing the processor instruction pipeline stack” (EX1004, 4:30-40), and also sets “bits in a register of processor 292” to control the number of instructions executed per cycle by the processor (*id.*, 5:57-61). Accordingly, claims 1-5 are also rendered obvious by *Chagny* in view of the knowledge of a POSITA. EX1002, ¶130.

B. Claims 6-12 and 14-15

As described in Ground 1A, *Chagny* discloses a software program 296 that serves as the “power system controller” recited in independent claims 6 and 11. *See, e.g.*, Section IX.F.ii (6[a]), IX.K.ii (11[a]). To the extent PO argues that the power system controller must be implemented in hardware, a POSITA would have been motivated and found it obvious to execute *Chagny*’s “software program 296,” which may be “included in the operating system” of the device (EX1004, 4:35-37), on hardware such as processor 292.¹⁰ EX1002, ¶131. For example, *Chagny* explains that the “software program 296” monitors the processor loading by “analyzing the processor

¹⁰ The ’514 Patent includes embodiments where “the power system controller” is constructed as “an element” of a “server” (i.e., the load). EX1001, 25:23-27, 21:65-22:8; *see also id.*, 13:12-13, Fig. 11. Thus, the ’514 Patent contemplates embodiments whereby the “power system controller” is part of the load.

instruction pipeline stack” (EX1004, 4:30-35), and also sets “bits in a register of processor 292” to control the number of instructions executed per cycle by the processor (*id.*, 5:57-61). Moreover, *Chagny* describes that a “processor” is “operable to execute the computing instructions,” which are “also known as a ‘software program,’” stored in memory. *Id.*, 7:36-41; *see also* EX1002, ¶¶132-133; EX1015, 5 (textbook describing processor-based systems with memory to store the instructions to be executed by central processing unit), 10-11 (describing various types of well-known processor-based devices, including those where the central processing unit and the memory are included together on a single chip). Alternatively, a POSITA would have also found it obvious to execute *Chagny*’s “software program 296” on a separate hardware controller configured to monitor and control the processor. EX1002, ¶133.

Accordingly, claims 6-12 and 14-15 are also be rendered obvious by *Chagny* in view of the knowledge of a POSITA. EX1002, ¶134.

C. Claims 11-12, 14-17, 19-20

As described in Ground 1A for claim 11[c] (and similar claim 16[c]), a POSITA would have understood, based on *Chagny*’s disclosure, that in response to receiving the activity input 202 signal, the “frequency selector module 215” within *Chagny*’s controller module 210 senses the activity input 202 signal and thereby the power level of the state of power drain as indicated by the activity input 202 signal. EX1002, ¶135. To the extent PO argues that *Chagny* does not describe any particular sensing circuitry within frequency selector module 215, a POSITA would have found it obvious that the

frequency selector module 215 within *Chagny*'s controller module 210 (i.e., the power converter controller) could include specific circuitry to sense the state of the bits of the activity input 202 signal and thereby sense the power level of the state of power drain as indicated by the activity input 202 signal. EX1002,¶136.

Chagny explains how the activity input 202 signal may include, for example, 2 bits, GPO1 262 and GPO2 264, that are used to define 4 activity levels of the processor 292. EX1004, 4:46-51. Based on *Chagny*'s disclosure, a POSITA would have found it obvious that frequency selector module 215 would include digital circuitry, such as a register or other digital logic, to sense and capture the 2 bits of activity input signal 202, which are then used by frequency selector module 215 to select the appropriate frequency. EX1002,¶136.

Accordingly, claims 11-12, 14-17, and 19-20 are also rendered obvious by *Chagny* in view of the knowledge of a POSITA. EX1002,¶137.

D. Claims 13 and 18

- i. **“13. The power system as recited in claim 11 wherein said signal is provided upon startup of said processor system.”**

“18. The method as recited in claim 16 wherein said signal is provided upon startup of said processor system.”

As described above in Grounds 1A and 1B, *Chagny* alone or in view of the knowledge of a POSITA discloses and/or render obvious independent claims 11 and 16. See Sections IX.K and IX.O (Ground 1A), Sections X.B-C (Ground 1B). When viewed with the knowledge of a POSITA, *Chagny* also discloses and suggests each additional

element of dependent claims 13 and 18, rendering those claims obvious.

As described in Section IX.K.iii for claim 11[b], *Chagny*'s software program 296 "generates the activity input 202" (i.e., provides said signal) to identify the "levels of activity of the processor 292." EX1004, 4:40-43. *Chagny* further explains that the "activity input 202 may be updated on a periodic basis, e.g., once every millisecond, on an event basis or on an on-demand basis." *Id.*, 4:43-45.

A POSITA would have found it obvious that the generation and provision of *Chagny*'s activity input 202 signal (i.e., said signal) would occur throughout the operating time of *Chagny*'s information handling system device 290, including upon startup. EX1002, ¶¶138-140. Moreover, a POSITA would have found it obvious that the startup of *Chagny*'s processor 292 (during the startup of information handling system device 290 as a whole) would be among the "event basis" or "on-demand basis" upon which *Chagny* updates and provides the activity input 202 signal (i.e., provides said signal). See EX1004, 4:40-45; EX1002, ¶140. It was well known in the art that a microprocessor would send control signals to an adaptive power supply coupled to that microprocessor as soon as the microprocessor was powered up to a level where its control signal was valid. EX1002, ¶140; EX1007, 3:57-64, 4:28-40, 4:50-58 (collectively describing processor taking over control of DC/DC converter output after processor has been powered up to an initial voltage level that ensure the processor's control signal outputs are valid), Fig. 3 (illustrating "VID[4:0]" control signal as valid after power-up of processor voltage CPUVCC in response to PWRON# signal).

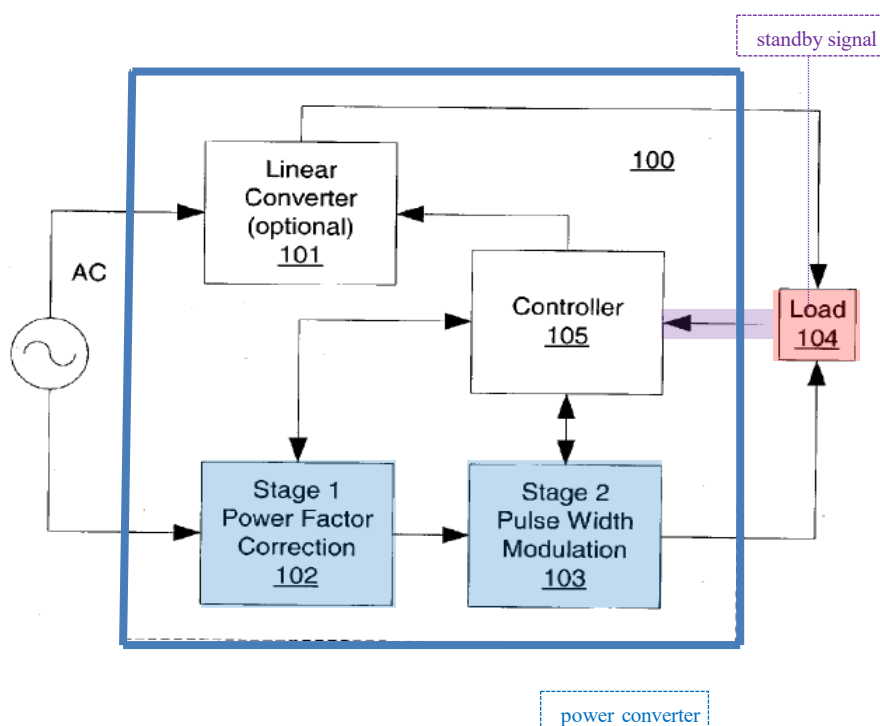
Accordingly, *Chagny* in view of the knowledge of a POSITA renders obvious the additional elements of dependent claims 13 and 18. EX1002, ¶141.

XI. GROUND 2A: *Hwang* Anticipates Claims 1-10, 16-17, and 19-20

A. Claim 1

i. 1[pre]: “A power converter coupled to a load, comprising:”

Hwang discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006]. Like Figure 3 of the ’514 Patent (EX1001, Fig. 3), *Hwang*’s power converter 100 is a “two-stage power converter” with a “power factor correction (PFC) stage 102” and a “PWM stage 103.” (EX1006, [0019]).



EX1006, Fig. 1 (annotated); EX1002, ¶143.

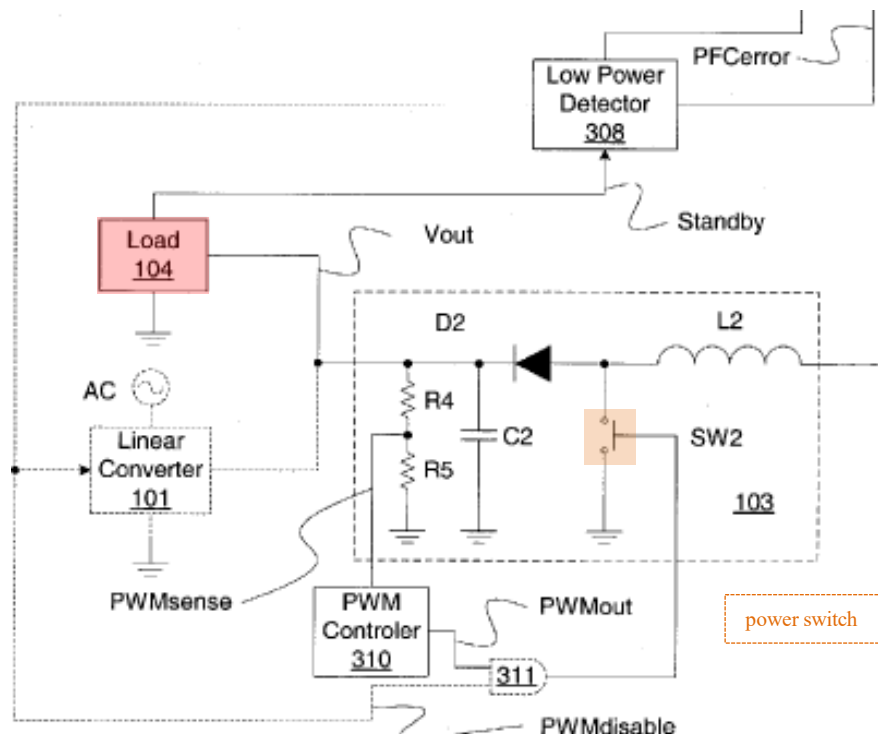
As shown in Figure 1, the output of power converter 100 is coupled to provide

power to a load 104. EX1006, Fig. 1. Power converter 100 is also coupled to load 104 by way of a “standby signal” sent from load 104 to the controller 105 within *Hwang*’s power converter 100. *Id.*, [0021], [0031]; EX1002, ¶144.

Thus, *Hwang* discloses claim 1[pre]. EX1002, ¶145.

ii. 1[a]: “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof; and”

As shown in Figure 3, the PWM stage 103 from Figure 1 includes “switch SW2” (i.e., the power switch). EX1006, [0029].



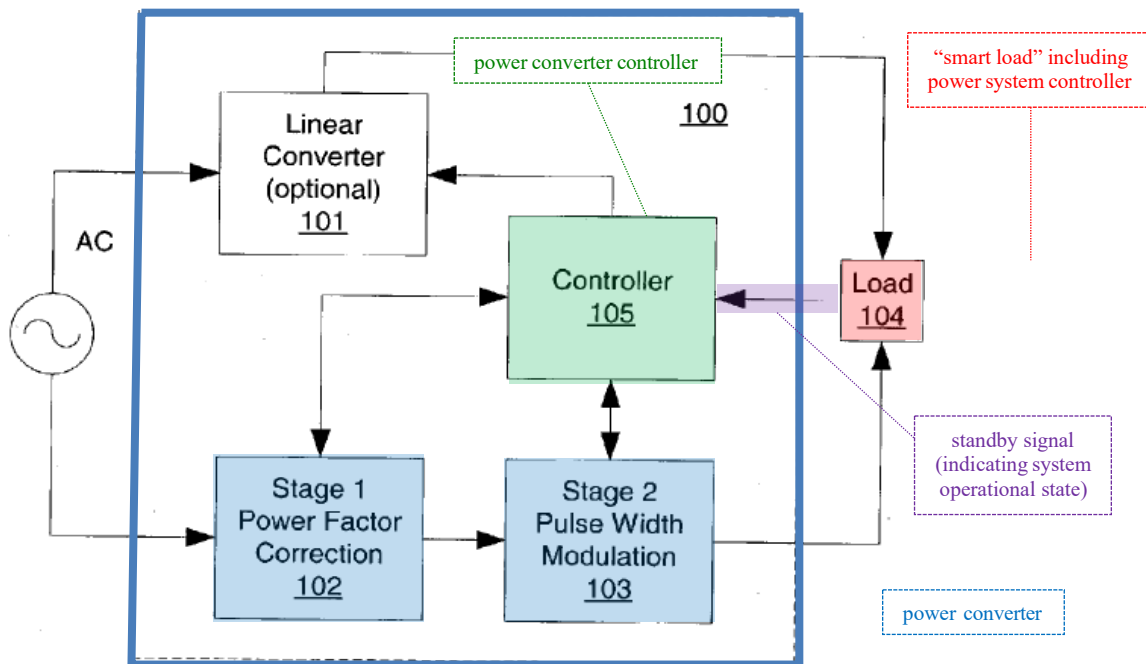
EX1006, Fig. 3 (excerpt) (annotated); EX1002, ¶146. As *Hwang* describes, a PWM controller in a switching power converter adjusts the “duty cycle” of the PWM signal controlling the switch “to regulate the output voltage” (i.e., to provide an output characteristic). EX1006, [0003]. And with respect to Figure 3, *Hwang* states: “The

PWM controller 310 may cause the switch SW2 [i.e., the power switch] to be switched on and off in an attempt to cause the output voltage V_{out} at the output of the power converter “to remain substantially constant.” *Id.*, [0030]; *see also id.*, [0034] and [0036] (both referencing duty cycle), Figs. 7A-7D.

Hwang thus discloses claim 1[a]. EX1002, ¶¶147-149.

- iii. 1[b]: “a power converter controller configured to receive a signal from said load indicating a system operational state of said load and”

Hwang’s power converter 100 includes “controller 105” (i.e., a power converter controller). EX1006, [0019].



EX1006, Fig. 1 (annotated); EX1002, ¶150.

Hwang discloses that load 104 may be a “smart load” that includes “a microprocessor that may enter a standby mode during periods of low activity or non-use.” *Id.*, [0031]; *see also id.*, [0021] (“where the load 104 is a microprocessor or controller, it may enter a standby or ‘sleep’ mode during periods of low activity”). *Hwang* also discloses that smart load 104 may send a “standby signal” to the controller 105 indicating that the smart load 104 is in standby (i.e., a signal from said load indicating a system operational state of said load). *Id.*, [0021], [0031].

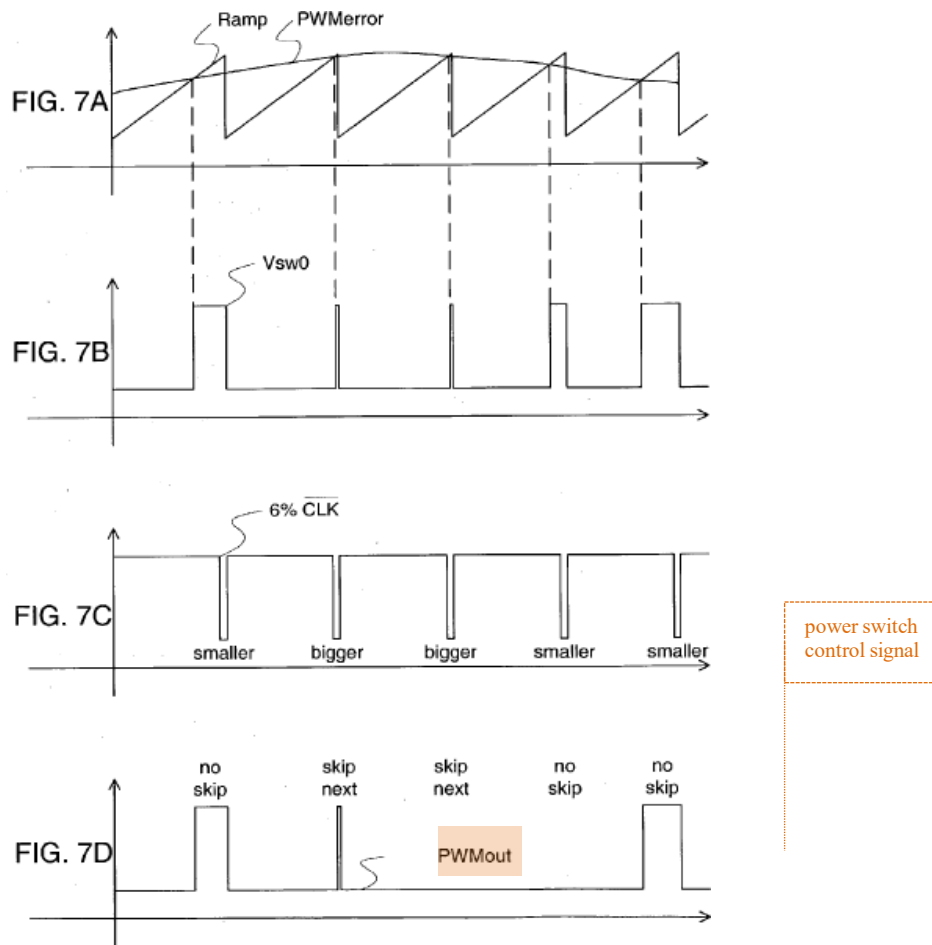
Hwang thus discloses claim 1[b]. EX1002, ¶¶151-152.

iv. 1[c]: “control an internal operating characteristic of said power converter as a function of said signal.”

In response to the “standby signal” from the smart load 104, controller 105 of *Hwang* places the power converter 100 in “standby mode.” EX1006, [0021] (“A standby signal from the load 104 may instruct the controller 105 to enter standby mode.”); [0031]. “While in standby mode, the controller 105 may disable the PFC stage 102” and “may cause PWM stage 103 to enter pulse-skipping mode.” *Id.*, [0021].

The ’514 Patent lists the “disabling of ... power factor correction,” as well as “switching frequency,” among example internal operating characteristics. EX1001, 22:40-51. Thus, the disabling of *Hwang*’s power factor correction (PFC) stage 102 serves as a first internal operating characteristic. *See* EX1006, [0016], [0021]; EX1002, ¶¶153-154. Likewise, the reduction of the PWM stage’s switching frequency during pulse-skipping mode serves as another internal operating characteristic.

Figures 7A-7D provide an example where two cycles are skipped over the period of five cycles. *Id.*, Figs. 7A-7D, [0036] and [0041]-[0042] (describing pulse skipping operation). Thus, during this period, the switching frequency is reduced to 60% of the nominal switching frequency. EX1002, ¶155; EX1012, 37 (Fig. 10.38) (illustrating skipped pulses), 34 (describing pulse skipping as “modified version” of “variable-frequency” operation).



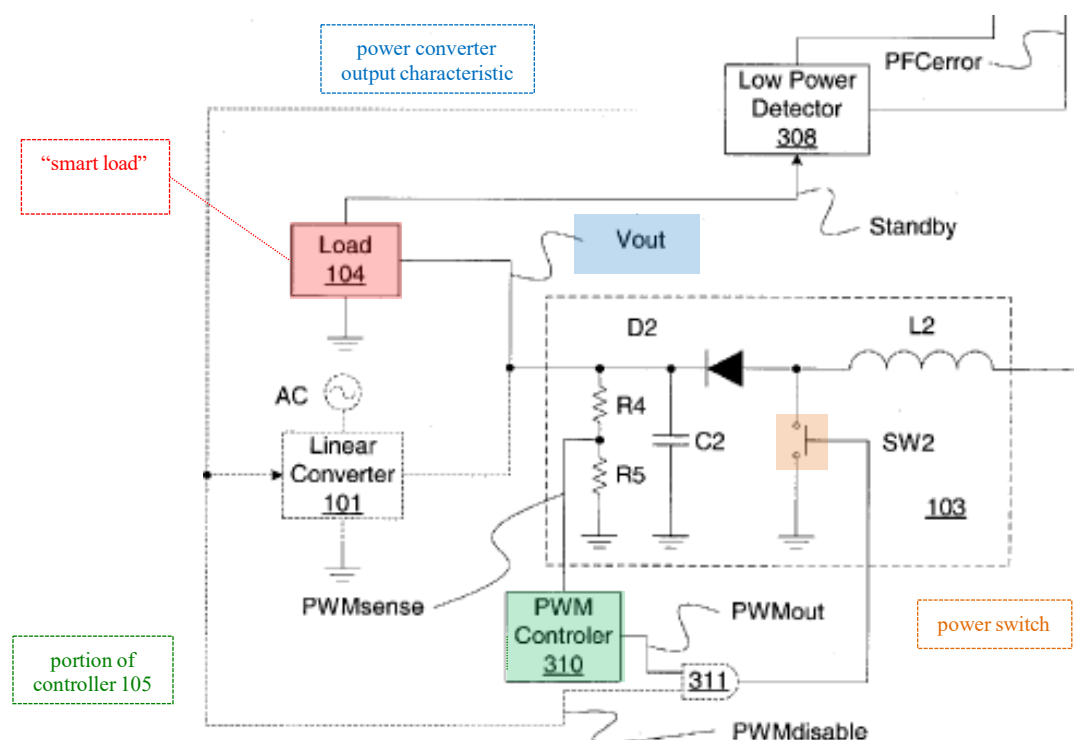
EX1006, Fig. 7A-D (annotated); EX1002, ¶155.

Hwang thus discloses claim 1[c]. EX1002, ¶156.

B. Claim 2

- i. **“2. The power converter as recited in claim 1 wherein said power converter controller is further configured to provide another signal to control said duty cycle of said power switch as a function of said output characteristic and in accordance with said signal.”**

The controller 105 shown in Figure 1 of *Hwang* includes PWM controller 310 shown in Figure 3. EX1006, [0026].

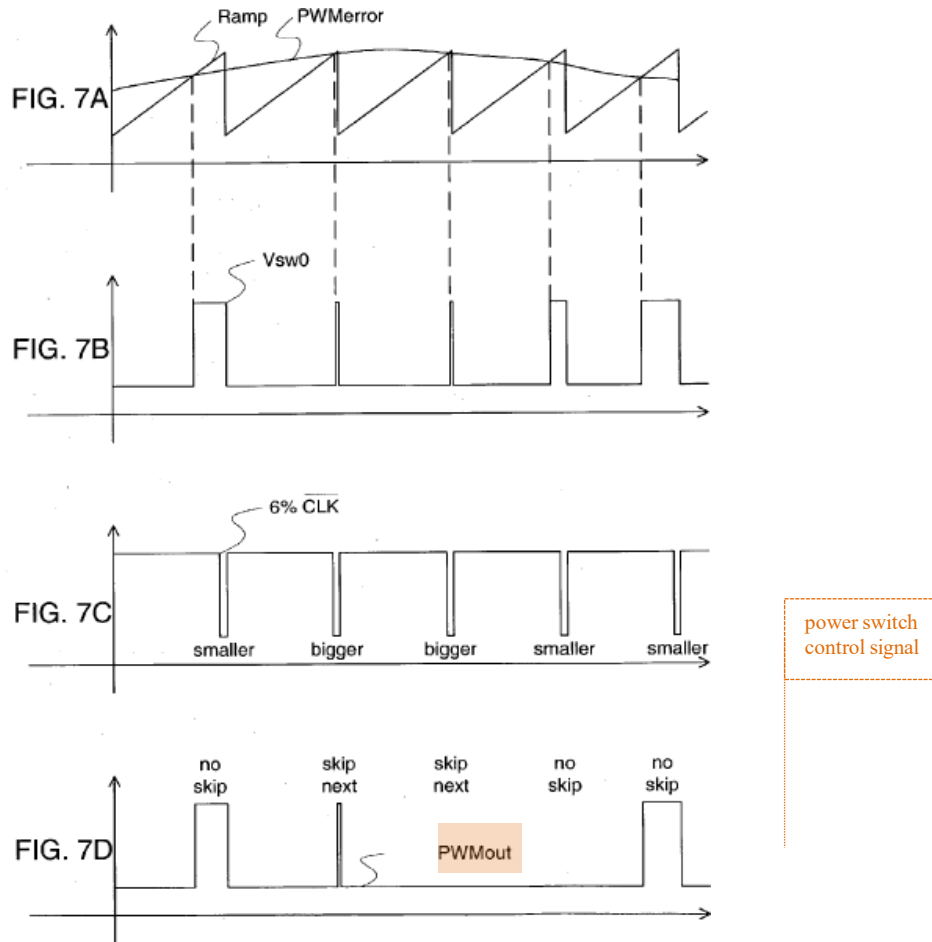


EX1006, Fig. 3 (excerpt) (annotated); EX1002, ¶157.

As shown in Figure 3, PWM controller 310 drives switch SW2 (i.e., the power switch) via AND gate 311 with the PWMout signal (i.e., another signal to control said duty cycle). EX1006, Fig. 3; *see also id.*, [0031]. As also shown in Figure 3, PWM controller 310 receives a feedback signal representative of the output voltage (i.e., an output characteristic) of the converter. *Id.*, Fig. 3, [0030] (“signal PWMsense, representative of the output voltage Vout ... may be coupled into the PWM controller

310”). As described for claim 1[a], the PWM controller controls the duty cycle of switch SW2 (i.e., the power switch) to regulate the output voltage as a function of the feedback to regulate the output voltage. EX1006, [0003] (describing “adjusting the duty cycle of the PWM signal” as a function of “measured output voltage”), [0030]; *see also* Section XI.A.ii; EX1002, ¶¶158-159. *Hwang* thus discloses controlling the duty cycle as a function of V_{out} (i.e., the output characteristic).

Hwang also discloses that the duty cycle of the power switch is controlled in accordance with the “standby signal” (i.e., said signal) from smart load 104. EX1002,160. Although Figure 3 shows that PWM stage 103 may be disabled by a PWMdisable signal feeding AND gate 311 (EX1006, Fig. 3), *Hwang* explicitly discloses that, during standby mode, controller 105 may either (i) “disable the PWM stage,” or (ii) “cause PWM stage 103 to enter pulse-skipping mode” (*id.*, [0021]). And as shown in Figures 7A-7D, during pulse-skipping mode, a switching cycle of the PWM stage are skipped (i.e., the duty cycle forced to zero) if the duty cycle of the previous switching cycle was less than a given threshold. *Id.*, [0036], [0041]- [0042] (describing pulse-skipping operation).



EX1006, Fig. 7A-D (annotated); EX1002, ¶161. Thus, the power switch is also controlled in accordance with the standby signal (i.e., said signal) placing PWM stage 103 into pulse-skipping mode. EX1006, [0021].

Hwang thus discloses claim 2. EX1002, ¶162.

C. Claim 3

- i. **“3. The power converter as recited in claim 1 wherein said power converter controller is configured to adjust said internal operating characteristic over a period of time.”**

As described above for claim 1[c], *Hwang*’s power converter controller is configured to enter a standby mode and thereby adjust an internal operating

characteristic of the power converter *in response* to a “standby signal” from smart load 104. *See* Section XI.A.iv; EX1006, [0021], [0031], Figs. 7A-7D (illustrating reduction of average switching frequency by pulse-skipping). *Hwang* explicitly contemplates changing modes over time as the power demand from the load 104 changes. EX1006, Abstract (describing entry into pulse-skipping mode “[a]s the load decreases”), [0006] (“When the load is high, both stages are enabled. As the power load decreases, one or both of the stages may enter pulse-skipping mode to improve efficiency of the power converter.”), [0021] (describing entry into standby mode and pulse-skipping “*during* periods of low activity” of the microprocessor within load 104). Thus, a POSITA would have understood that *Hwang*’s power converter controller is configured to adjust the internal operating characteristic over a period of time as the loading of microprocessor within smart load 104 changes and the smart load changes between standby and non-standby modes. EX1002, ¶¶163-165.

Hwang thus discloses claim 3. EX1002, ¶166.

D. Claim 4

- i. **“4. The power converter as recited in claim 1 wherein said load is a processor and said system operational state [of said load] is dependent on one of a core state and a performance state of said processor.”**

The ’514 Patent background explains that a “core state” of a processor is “under software operating system control” and affects the “level of power consumption” of the processor. EX1001, 5:44-46. According to the ’514 Patent, the highest core state is

where the processor executes instructions “at its full operational level.” *See id.*, 5:46-57; EX1002, ¶167. On the other hand, various core- state “sleep levels” are “achieved by halting instruction execution.” EX1001, 5:48-57. In other words, the “core state” as described in the ’514 Patent background specifies the activity level (e.g., the rate at which instructions are executed) of the processor. EX1002, ¶167.

As described in Section XI.A.iii for claim 1[b], *Hwang* discloses that smart load 104 includes a microprocessor that enters a “standby mode” (i.e., the system operational state) “during periods of low activity or non-use.” EX1006, [0031]; *see also id.*, [0021] (describing “a standby or ‘sleep’ mode during periods of low activity”). Thus, a POSITA would have understood that the standby mode of *Hwang*’s smart load depends on a core state of its microprocessor. EX1002, ¶¶168-169.

Hwang thus discloses claim 4. EX1002, ¶¶170.

E. Claim 5

- i. “5. The power converter as recited in claim 1 wherein said internal operating characteristic is selected from the group consisting of: a gate drive voltage level of said power switch of said power converter, a switching frequency of said power converter, and an internal direct current bus voltage of said power converter.”**

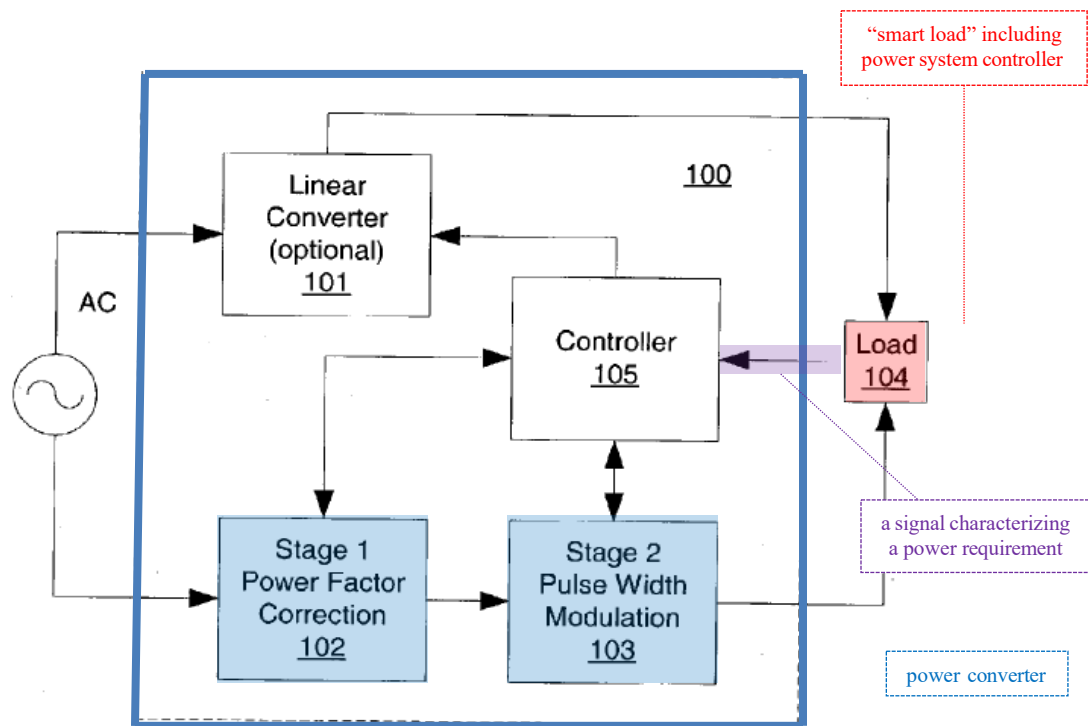
As described above, one of the internal operating characteristics identified for claim 1[c] is the switching frequency of *Hwang*’s power converter. *See* Section XI.A.iv. *Hwang* thus discloses claim 5. EX1002, ¶¶171-172.

F. Claim 6**i. 6[pre]: “A power system, comprising:”**

As described below, *Hwang* discloses the recited elements of a “power system,” including a power system controller and a power converter. *Hwang* thus discloses the “power system” recited by claim 6[pre]. EX1002, ¶173.

ii. 6[a]: “a power system controller configured to provide a signal characterizing a power requirement of a processor system; and”

As shown in Figure 1 below, *Hwang* discloses power converter 100 coupled to a smart load 104. See EX1006, [0019], Fig. 1; see also *id.*, [0031], [0038]. *Hwang* discloses that smart load 104 “may include a microprocessor.” *Id.*, [0031]. The smart load 104 thus serves as a “processor system” recited by claim 6[a].



EX1006, Fig. 1 (annotated); EX1002, ¶174.

Hwang discloses that the microprocessor within smart load 104 “may enter a

standby mode during periods of low activity or non-use.” EX1006, [0031]; *see also id.*, [0021] (describing microprocessor’s entry into “a standby or ‘sleep’ mode during periods of low activity”). *Hwang* also discloses that smart load 104 sends a “standby signal” (i.e., a signal characterizing a power requirement of a processor system) to the controller 105 within power converter 100. *Id.*, [0021], [0031]. The standby signal characterizes the power requirement of the smart load 104 and the microprocessor therein. *See id.*, [0021] (“The controller 105 may sense a signal [i.e., the standby signal] from the load 104 that indicates the level of the power drawn by the load 104.”); EX1002, ¶175.

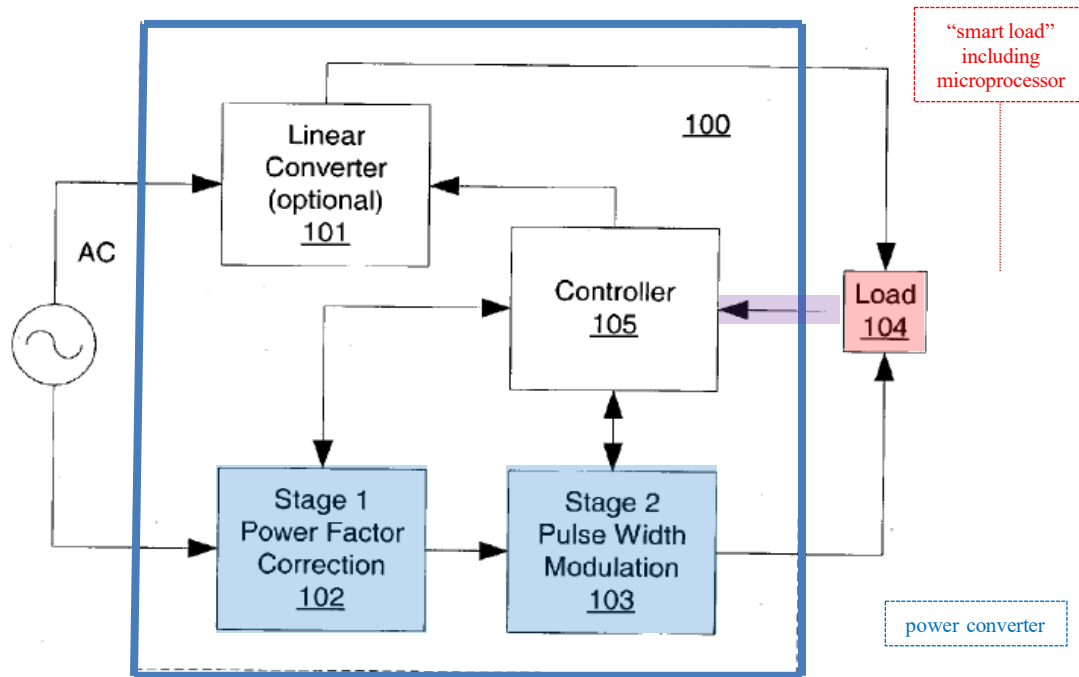
Based on *Hwang*’s disclosure of a smart load 104 that includes a “microprocessor” that enters standby mode during periods of low activity (EX1006, [0031], [0021]), a POSITA would have understood that the microprocessor within smart load 104 serves as the “power system controller” as recited in claim 6[a] by providing a standby signal characterizing a power requirement of smart load 104. EX1002, ¶176. Indeed, *Hwang*’s architecture with a power system controller built into a “smart load” with a microprocessor is similar to embodiments in the ’514 Patent where the “power system controller” is included as “an element” of a “server” (i.e., the load). EX1001, 25:23-27, 21:65-22:8; *see also id.*, 13:12-13, Fig. 11.

Hwang thus discloses claim 6[a]. EX1002, ¶177.

iii. 6[b]: “a power converter coupled to said processor system, comprising:”

As shown in Figure 1, *Hwang* discloses power converter 100 coupled to a load 104.

See EX1006, [0019], Fig. 1; see also *id.*, [0031], [0038]; see also Section XI.A.i (1[pre]). And as described in Section XI.F.ii for claim 6[a], load 104 (i.e., said processor system) may be a smart load including a “microprocessor.” EX1006, [0031], [0021].



EX1006, Fig. 1 (annotated); EX1002, ¶178.

Hwang thus discloses claim 6[b]. EX1002, ¶¶179.

- iv. **6[c]: “a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof, and,”**

Claim 6[c] is identical to claim 1[a] and is disclosed in the manner described for claim 1[a]. See Section XI.A.ii; EX1002, ¶¶180.

- v. **6[d]: “a power converter controller configured to receive a signal¹¹ from said power system controller to control an internal operating characteristic of said power converter as a function of said signal.”**

As described for claim 6[a], *Hwang*’s power system controller within smart load 104 is configured to provide a “standby signal.” *See* Section XI.F.ii; EX1006, [0021], [0031], FIG. 1. And as described above for claim 1[c], *Hwang*’s controller 105 (i.e., the power converter controller) is configured to receive that “standby signal” and to place the power converter in a standby mode and thereby control an internal operating characteristic of the power converter as a function of the “standby signal.” *See* Section XI.A.iv.

Hwang thus discusses claim 6[d] in the manner described above for claims 6[a] and 1[c]. EX1002, ¶¶181-182.

G. Claim 7

Hwang discloses the additional elements of claim 7 in the same manner described above for similar claim 2. *See* Section XI.B; EX1002, ¶183.

H. Claim 8

¹¹ Nothing in the ’514 Patent specification prevents the “signal” of claim 6[d] from being the same “signal” provided by the power system controller in claim 6[a]. *See* EX1001. Indeed, PO’s infringement contentions point to the same signal for both claim 6[a] and 6[d]. *See* EX1010, 5, 11; EX1017, 5, 11.

Hwang discloses the additional elements of claim 8 in the same manner described above for similar claim 3. *See* Section XI.C; EX1002,¶184.

I. Claim 9

Claim 9 is similar to claim 4, but recites that “said power requirement of a processor system,” as opposed to the “system operational state,” is dependent on one of a core state and a performance state. But as explained in *Hwang*, the “level of power drawn by the load 104” depends on the activity of the microprocessor during standby (i.e., the system operational state). *See* EX1006, [0021]; EX1002,¶185. Thus, *Hwang* discloses claim 9 for the same reasons described for claim 4. *See* Section XI.D; EX1002¶186.

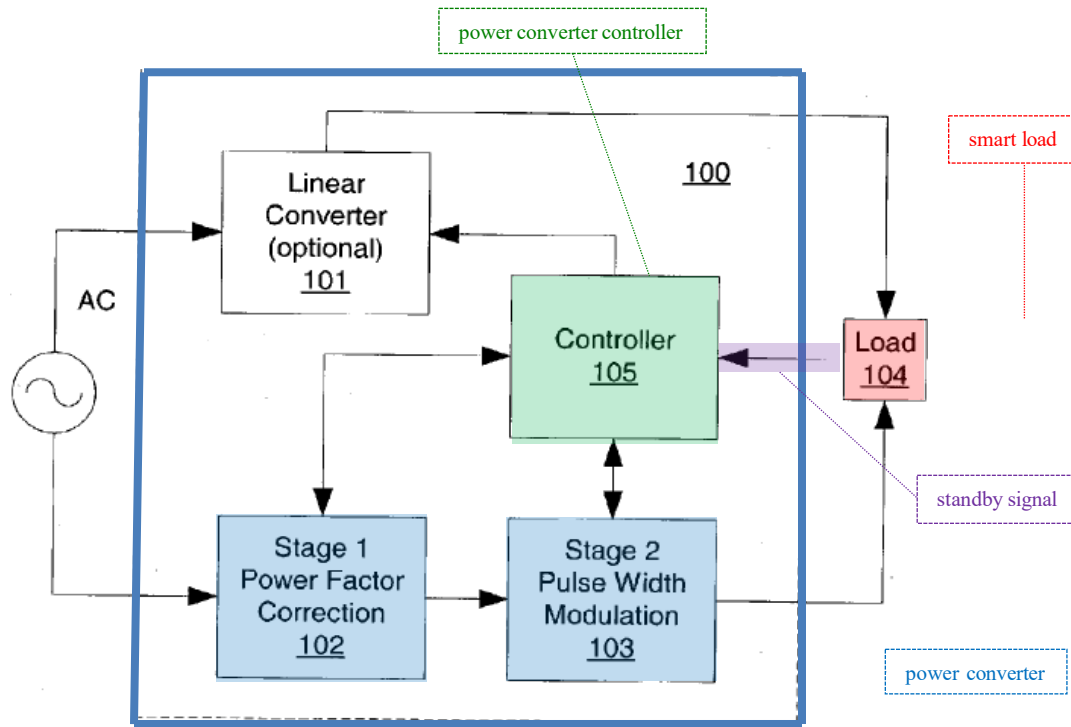
J. Claim 10

Hwang discloses the additional elements of claim 10 in the same manner described above for similar claim 5. *See* Section XI.E; EX1002,¶¶187.

K. Claim 16

i. 16[pre]: “A method of operating a power system, comprising:”

As shown in Figure 1, *Hwang* discloses a power system including a power converter 100 and a smart load 104. EX1006, [0019], [0021], [0031].



EX1006, Fig. 1 (annotated); EX1002, ¶188. And as described below, *Hwang* discloses the method steps for operating the power system recited in claim 16.

ii. 16[a]: “enabling operation of components of a processor system to establish a state of power drain thereof;”

Hwang discloses that its load 104 (i.e., a processor system) may be a “smart load” that includes “a microprocessor.” EX1006, [0031]; *see also id.*, [0021]. *Hwang* also states that load 104 “may enter a standby or ‘sleep’ mode during periods of low activity for power conservation.” *Id.*, [0021]; *see also id.*, [0031] (“[T]he load 104 may include a microprocessor that may enter a standby mode during periods of low activity or non-use.”). By entry of the “standby” or “sleep” mode for “power conservation,” *Hwang* enables operation of the components of the microprocessor to establish a standby-

level of power drain (i.e., a state of power drain). *See id.*, [0021] (referring to “level of power drawn by the load 104” during standby); *see also id.*, [0022] (describing “low power conditions”), [0024] (describing “power drawn by the load” and “levels of load power” and providing an example whereby the power converter enters “standby” when “the load power is below 0.5-1% of its maximum expected load power.”)¹²; EX1002, ¶¶189-190.

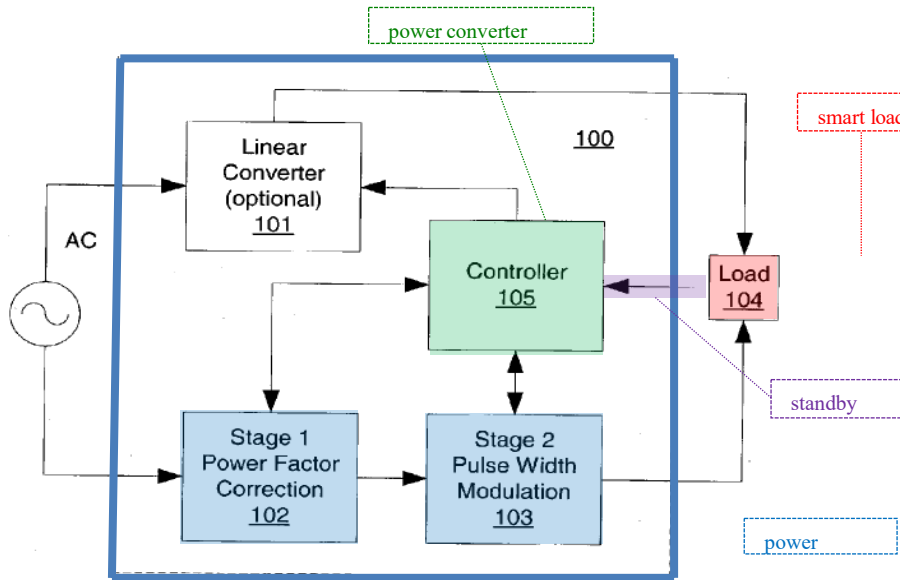
Hwang thus discloses claim 16[a]. EX1002, ¶191.

iii. 16[b]: “providing a signal to identify operation of said processor system in said state of power drain;”

Hwang also discloses that, when load 104 (i.e., said processor system) enters the standby mode referred to above for claim 16[a], load 104 provides a “standby signal” to identify the standby mode (i.e., to identify operation in said state of standby-level power drain). EX1006, [0021] (describing “a signal from the load 104 that indicates the level of the power drawn by the load 104”), [0031] (“The load 104 may send a standby

¹² The ’514 Patent specification describes a “power system controller” as enabling a state of power drain. *See* EX1001, 13:39-43. The ’514 Patent specification also describes how the “power system controller” is constructed as “an element” of a server (i.e., the load). EX1001, 25:23-27, 21:65-22:8; *see also id.*, 13:12-13, Fig. 11. Thus, the ’514 Patent contemplates embodiments, like *Hwang*’s smart load 104, where the processor system enables its own state of power drain. EX1002, ¶190.

signal that may be interpreted by a low power detector 308.”).

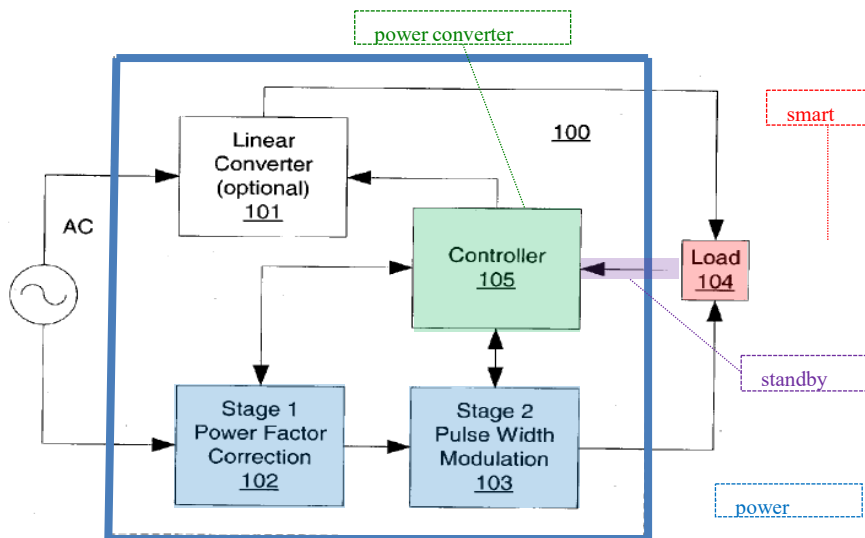


EX1006, Fig. 1 (annotated); EX1002, ¶192.

Hwang thus discloses claim 16[b]. EX1002, ¶193.

iv. 16[c]: “sensing a power level of said state of power drain in response to said signal; and”

As shown in Figure 1, controller 105 receives the “standby signal” from load 104:



EX1006, Fig. 1 (annotated); EX1002, ¶194.

Hwang expressly discloses that “controller 105 may *sense* a signal [i.e., the standby signal] from the load 104 that indicates the level of the power drawn by the load 104” (i.e., a power level of said state of power drain). EX1006, [0021] (emphasis added).¹³ In other words, in response to receiving the “standby signal,” *Hwang*’s controller 105 senses the power level of the state of power drain that is indicated by the standby signal. *See id.*; EX1002, ¶195. Indeed, *Hwang*’s sensing of the power level in response to the standby signal is similar to embodiments described in the ’514 Patent whereby “a signal” representing “level of power drains” are used “rather than ... an actual drain measurement.” EX1001, 13:63-57; EX1002, ¶196.

Hwang also discloses circuitry for performing the sensing described in Paragraph [0021]. For example, controller 105 includes “low power detector 308.” *See* EX1006, [0026], [0031]. *Hwang* discloses that, in response to the “standby signal” provided by

¹³ Petitioner’s mapping regarding the sensing of *Hwang*’s standby signal is similar to PO’s position in its district court infringement contentions. For example, PO takes the position that the accused product senses a power level of said state of power drain by receiving a signal allegedly indicative of that power level. *See* EX1011, 9-11 (identifying control channels CC1 and CC2 as signal allegedly representing power level of state of power drain); *see also* EX1018, 9.

the load 104, the signal “may be interpreted by a low power detector 308,” thereby sensing the power drawn by the load 104. *Id.*, [0031]; EX1002, ¶197.

Figure 6 of *Hwang* illustrates an embodiment of the low power detector 308, which includes circuitry for sensing the standby signal. EX1006, [0039]-[0040].

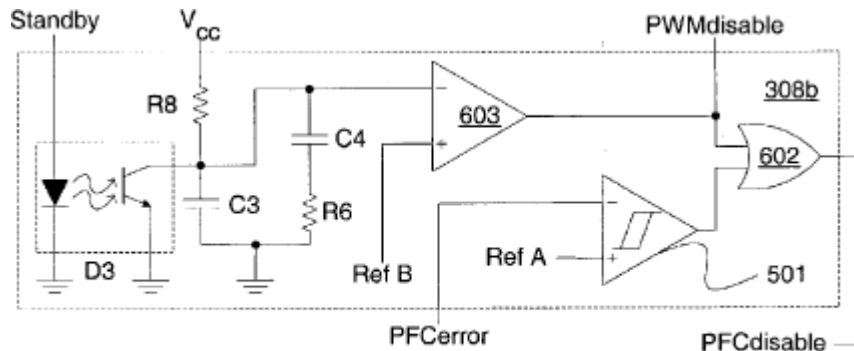


FIG. 6

EX1006, Fig. 6. “The standby signal from the smart load 104 may be coupled to an input of the opto-coupler D3.” *Id.*, [0039]. *Hwang* explains that “passive elements C3, C4, and R6 act as a low pass filter preventing noise in the standby signal from effecting the behavior of the low power detector.” *Id.*, [0040]. In turn, “comparator 603 compares the filtered Standby signal” to a reference voltage. *Id.*; *see also id.*, Fig. 5, [0037]. *Hwang* thereby senses the standby signal “that indicates the level of the power drawn by the load 104” (i.e., a power level of said state of power drain). *Id.*, [0021]; EX1002, ¶198.

Hwang thus discloses claim 16[c]. EX1002, ¶199.

- v. **16[d]: “controlling an internal operating characteristic of a power converter as a function of said power level.”**

As described for claim 1[c], *Hwang* discloses that controller 105 is configured to

control an internal operating characteristic of power converter 100 as a function of the “standby signal” from load 104. *See* Section XI.A.iv. And as described for claim 16[c], the standby signal represents the said power level of said state of power drain. Section XI.K.iv. *Hwang* thus discloses claim 16[d]. EX1002,¶200.

L. Claim 17

- i. 17[a]: “The method as recited in claim 16, further comprising: inducing a power switch of said power converter to conduct for a duty cycle to provide an output characteristic at an output thereof; and”**

Claim 17[a] is similar to claim 1[a], but in the form of a method claim. As described for claim 1[a], *Hwang* discloses a power converter controller that controls, and thereby induces, switch SW2 (i.e., a power switch of the power converter) to conduct for a duty cycle to provide an output voltage (i.e., and output characteristic) at the output of power converter 100. *See* Section XI.A.ii. *Hwang* thus discloses claim 17[a]. EX1002,¶¶201-202.

- ii. 17[b]: “controlling said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.”**

Claim 17[b] recites similar limitations as portions of claim 2, but is in the form of a method claim and recites “in accordance with said power level” instead of “in accordance with said signal.” But, as described for claim 16[c], the standby signal (cited as said signal for claim 2) represents said power level. Thus, *Hwang* discloses claim 17[b] in the same manner as described for claims 2 and 16[c]. *See* Sections XI.B

and XI.K.iv; EX1002, ¶¶203-204.

M. Claim 19

Hwang discloses the additional elements of claim 19 in the same manner described above for similar claim 3. *See* Section XI.C; EX1002,¶205.

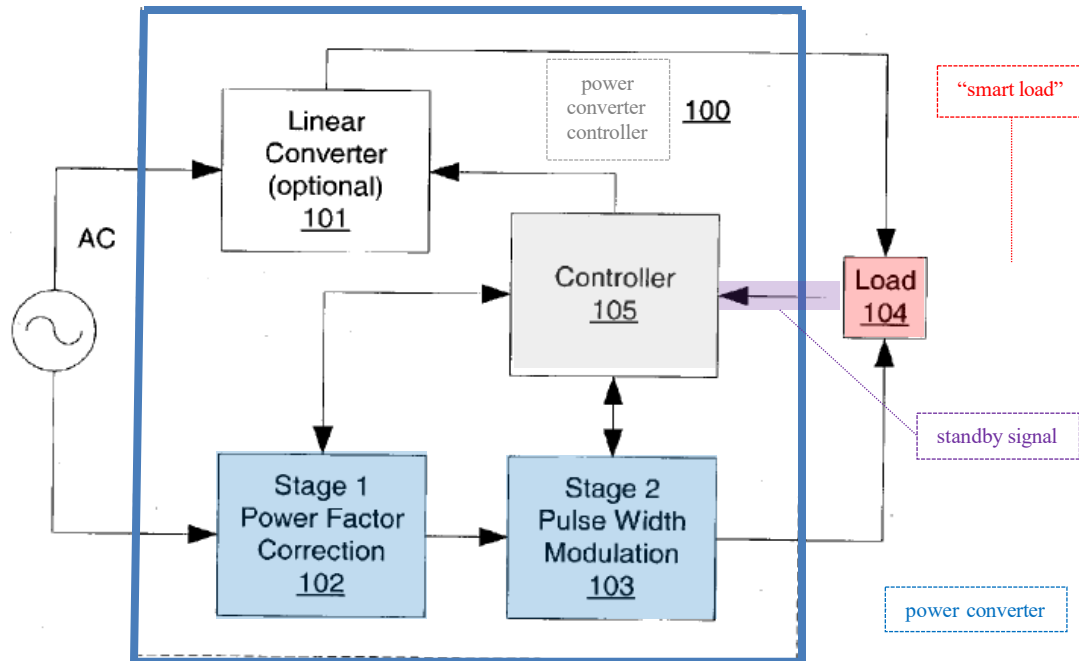
N. Claim 20

Hwang discloses the additional elements of claim 20 in the same manner described above for similar claim 5. *See* Section XI.E; EX1002,¶206.

XII. GROUND 2B: *Hwang* in view of *Chagny* Renders Obvious Claims 11- 12, 14-17, and 19-20

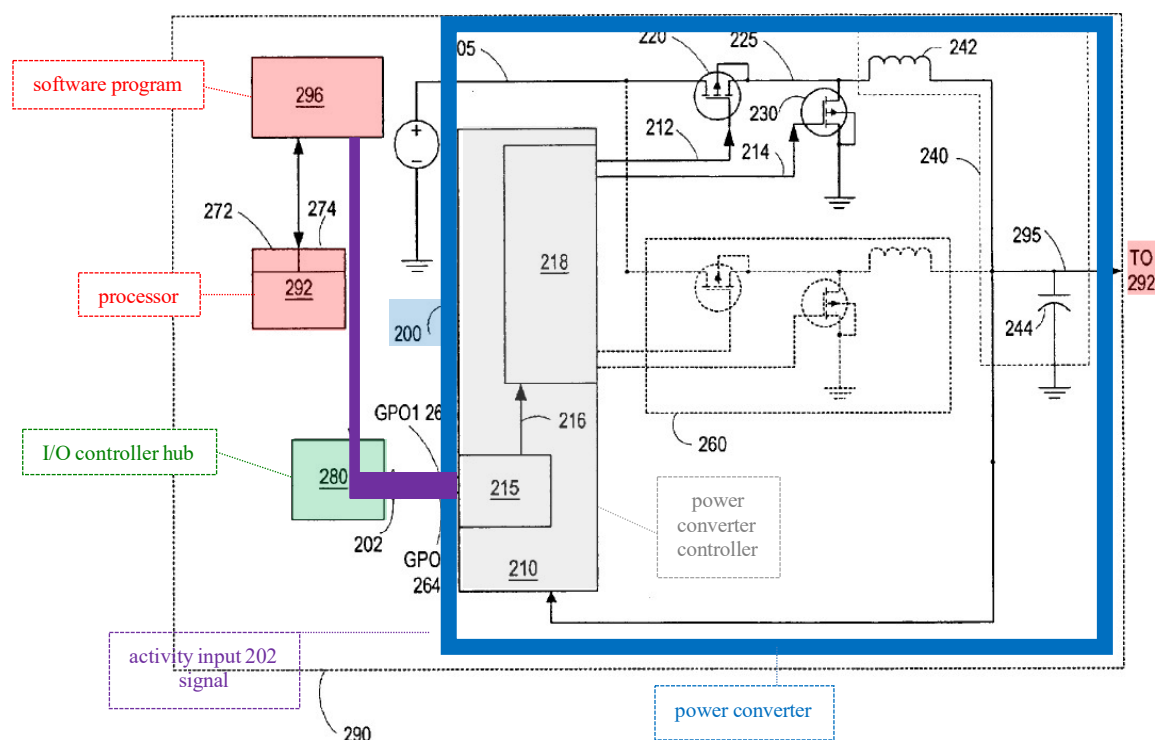
A. Motivation to Combine

Hwang discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006], [0019]. *Hwang*’s power converter provides power to a smart load 104, which “may include a microprocessor that may enter a standby mode during periods of low activity or non-use.” *Id.*, [0031]. When in standby mode, smart load 104 sends a “standby signal” to “instruct the controller 105” of the power converter to also enter a standby mode (*id.*, [0021], [0031]), thereby improving the efficiency of the power converter during times of low power demand (*id.*, [0006]).



EX1006, Fig. 1 (annotated); EX1002, ¶208.

Chagny discloses a voltage regulator module (“VRM”) (i.e., a power converter) that adjusts the internal operating characteristics of the VRM (e.g., the switching frequency) according to the activity level of a processor powered by the VRM. *See* EX1004, 2:59-61. *Chagny* discloses that “a software program 296 ... monitors the processor 292 loading” (EX1004, 4:35-37) and “generates the activity input 202 indicative of levels of activity of the processor 292” (EX1004, 4:40-43).



EX1004, Fig. 2A (annotated); EX1002, ¶209. *Chagny* further discloses “the software program 296 defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clock cycle” (EX1004, 5:57-61) thereby defining the “activity levels of the processor 292” (*id.*, 6:3-12).

A POSITA would have been motivated to combine *Hwang* and *Chagny* in order to implement *Chagny*'s specific teaching regarding how software program 296 coordinates the activity level of the processor (i.e., by setting UREG_B1 272 and UREG_B2 274) with the signal to the power converter indicating that activity level. EX1002, ¶210. Specifically, a POSITA would have been motivated, and found it obvious, to execute *Chagny*'s software program 296 on the microprocessor within

Hwang's smart load 104 in order to provide the specific means to control the entry of *Hwang*'s microprocessor into "standby" mode and to generate the "standby signal" sent by smart load 104 to *Hwang*'s power converter. EX1002,¶210. Such a combination represents the mere combination of prior art elements (e.g., the functionality described for *Hwang*'s microprocessor and *Chagny*'s disclosure of a software program 296) according to known methods to yield a predictable result. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007). It would be an obvious design choice to implement the functionality expressly disclosed by *Hwang* using a software program as taught by *Chagny*. EX1002,¶210. Moreover, a POSITA would have a reasonable expectation of success because, like the "activity input 202" generated by *Chagny*'s software program 296 (EX1004, 4:40-43), the smart load of *Hwang* is already configured to provide a status signal indicating its own operation mode (EX1006, [0021]); EX1002,¶210.

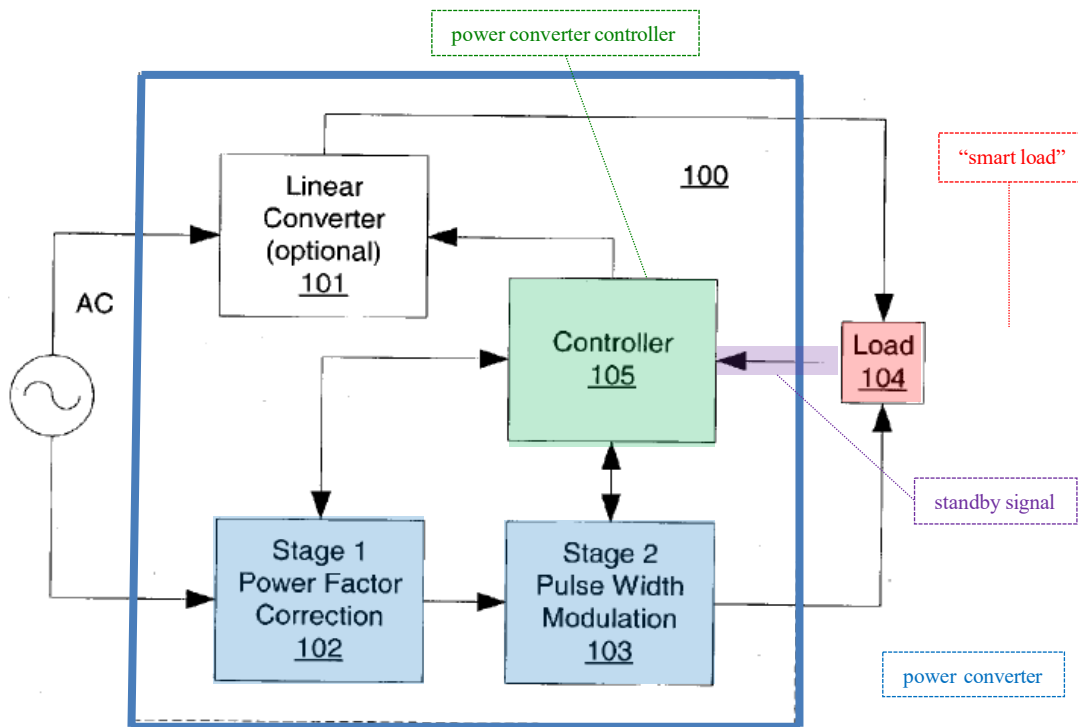
B. Claim 11

i. 11[pre]: "A power system, comprising:"

As described below, the combination of *Hwang* and *Chagny* discloses the recited elements of a "power system," including a power system controller and a power converter comprising a power converter controller. EX1002,¶211.

- ii. 11[a]: “a power system controller configured to enable operation of components of a processor system to establish a state of power drain thereof,”

Hwang discloses a power converter that provides power to a smart load 104, which “may include a microprocessor that may enter a standby mode during periods of low activity or non-use.” EX1006, [0031]. *Hwang* discloses that, when in standby mode, smart load 104 sends a “standby signal” to “instruct the controller 105” of the power converter to also enter a standby mode. *Id.*, [0021], [0031].



EX1006, Fig. 1 (annotated); EX1002, ¶12.

Hwang also describes that load 104 “may enter a standby or ‘sleep’ mode during periods of low activity for power conservation.” EX1006, [0021]; *see also id.*, [0031] (“[T]he load 104 may include a microprocessor that may enter a standby mode during

periods of low activity or non-use.”). By entry into the “standby mode” (or “sleep” mode) for “power conservation,” operation of the components of the microprocessor (i.e., the processor system) are enabled to establish a standby-level of power drain (i.e., a state of power drain). *See id.*, [0021] (referring to “level of power drawn by the load 104” during standby); *see also id.*, [0022] (describing “low power conditions”), [0024] (describing “power drawn by the load” and “levels of load power” and providing an example whereby the power converter enters “standby” when “the load power is below 0.5-1% of its maximum expected load power.”); EX1002, ¶213.

As described above in Section XII.A, a POSITA would have been motivated, and found it obvious, to execute *Chagny*’s software program 296 on the microprocessor within *Hwang*’s smart load 104 in order to provide the specific means to control the entry of *Hwang*’s microprocessor into such a “standby” mode. EX1002, ¶214. *Chagny* discloses that “a software program 296 ... monitors the processor 292 loading” (EX1004, 4:35-37) and “generates the activity input 202 indicative of levels of activity of the processor 292” (*id.*, 4:40-43). *Chagny* further discloses “the software program 296 defines UREG_B1 272 and UREG_B2 274, which are 2 bits in a register of the processor 292 to control the maximum number of instructions executed per clock cycle” (*id.*, 5:57-61) thereby defining the “activity levels of the processor 292” (*id.*, 6:3-12). Accordingly, in the *Hwang/Chagny* combination, *Chagny*’s software program 296 serves as the “power system controller” configured to enable the operation of components of *Hwang*’s smart load 104 (i.e., the processor system) to establish the

standby-level of power drain (i.e., a state of power drain) disclosed by *Hwang*. EX1002,¶¶215-216.

The combination of *Hwang* and *Chagny* thus discloses claim 11[a]. EX1002,¶217.

iii. 11[b]: “said power system controller configured to provide a signal to identify operation of said processor system in said state of power drain; and”

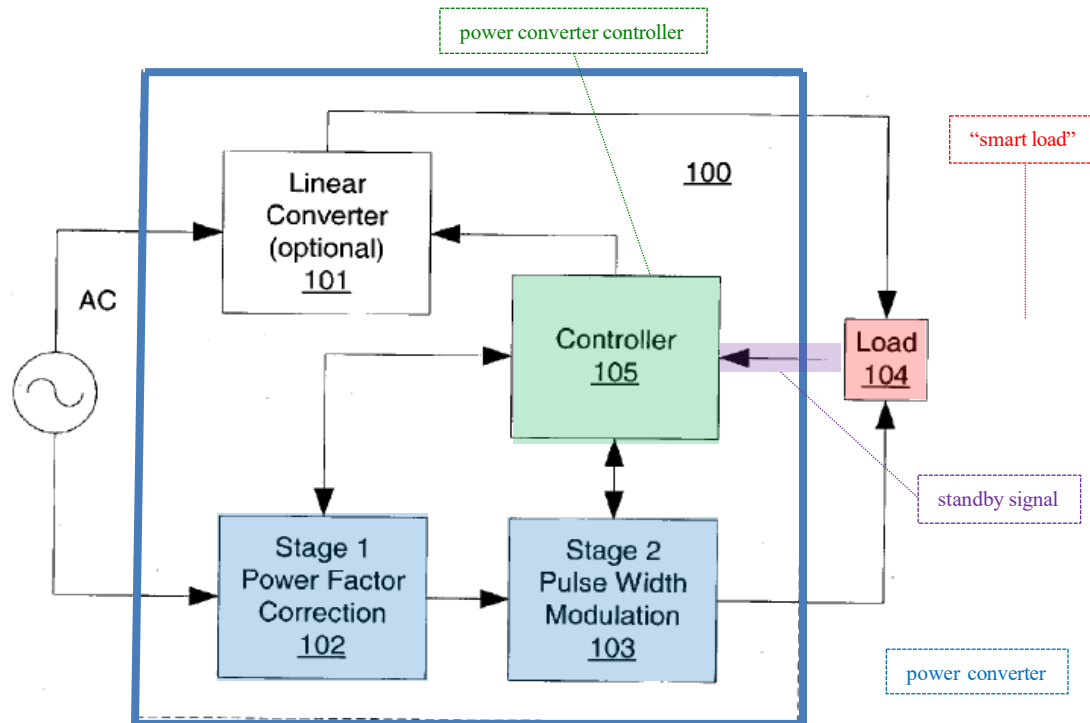
Hwang discloses that, when load 104 enters the standby mode referred to above for claim 11[a], smart load 104 provides a “standby signal” to identify the standby mode (i.e., to identify operation in said state of power standby-level power drain). EX1006, [0021] (describing “a signal from the load 104 that indicates the level of the power drawn by the load 104”), [0031] (“The load 104 may send a standby signal that may be interpreted by a low power detector 308.”).

As described above in Section XII.A, a POSITA would have been motivated, and found it obvious, to execute *Chagny*’s software program 296 on the microprocessor within *Hwang*’s smart load 104 in order to provide the specific means to control the entry of *Hwang*’s microprocessor into “standby” mode and to generate the standby signal disclosed by *Hwang* for indicating the operation of the processor system. EX1002,¶219. Thus, in the *Hwang/Chagny* combination, *Chagny*’s software program 296 serves as the “power system controller” configured to provide the standby signal to identify operation of *Hwang*’s smart load 104 (i.e., said processor system) in the said state of power drain.

The combination of *Hwang* and *Chagny* thus discloses claim 11[b].
EX1002, ¶¶218-221.

- iv. 11[c]: “a power converter, coupled to said processor system, comprising a power converter controller configured to receive said signal from said power system controller, to sense a power level of said state of power drain in response to said signal, and”

Hwang discloses “a pulse-skipping power converter.” EX1006, Abstract, [0006], [0019]. As shown in Figure 1, the output of power converter 100 provides power to the smart load 104 (i.e., said processor system) referred to above for claims 11[a]-[b].



EX1006, Fig. 1 (annotated); EX1002, ¶222.

As shown in Figure 1, controller 105 receives the “standby signal” (i.e., said signal) from load 104. *Hwang* expressly discloses that “controller 105 may *sense* a signal [i.e., the standby signal] from the load 104 that indicates the level of the power

drawn by the load 104” (i.e., a power level of said state of power drain). *Id.*, [0021].¹⁴ In other words, in response to receiving the “standby signal,” *Hwang*’s power converter controller 105 senses the power level of the state of power drain that is indicated by the standby signal. *See id.*; EX1002, ¶223. *Hwang*’s sensing of the power level in response to the standby signal is similar to embodiments described in the ’514 Patent whereby “a signal” representing “level of power drains” are used “rather than ... an actual drain measurement.” EX1001, 13:63-57; EX1002, ¶224.

Hwang also discloses circuitry for performing the sensing described in Paragraph [0021]. For example, controller 105 includes “low power detector 308.” EX1006, [0026], [0031]. *Hwang* discloses that, in response to the “standby signal” provided by the load 104, the signal “may be interpreted by a low power detector 308,” thereby sensing the power drawn by the load 104. *Id.*, [0031]; EX1002, ¶225. Figure 6 of *Hwang* illustrates an embodiment of low power detector 308, which includes circuitry for sensing the standby signal. EX1006, [0039]-[0040].

¹⁴ Petitioner’s mapping regarding the sensing of *Hwang*’s standby signal is similar to PO’s position in its district court infringement contentions. For example, PO takes the position that the accused product senses a power level of said state of power drain by receiving a signal allegedly indicative of that power level. *See* EX1011, 9-11 (identifying control channels CC1 and CC2 as signal allegedly representing power level of state of power drain); *see also* EX1018, 9.

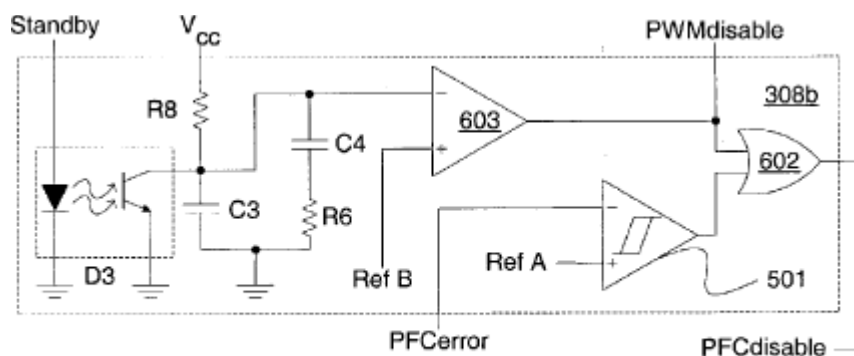


FIG. 6

EX1006, Fig. 6. “The standby signal from the smart load 104 may be coupled to an input of the opto-coupler D3.” *Id.*, [0039]. *Hwang* explains that “passive elements C3, C4, and R6 act as a low pass filter preventing noise in the standby signal from effecting the behavior of the low power detector.” *Id.*, [0040]. In turn, “comparator 603 compares the filtered Standby signal” to a reference voltage. *Id.*; *see also id.*, Fig. 5, [0037]. *Hwang* thereby senses the standby signal “that indicates the level of the power drawn by the load 104” (i.e., a power level of said state of power drain). *Id.*, [0021]; EX1002, ¶226.

The combination of *Hwang* and *Chagny* thus discloses claim 11[c].
EX1002, ¶227.

v. 11[d]: “to control an internal operating characteristic of said power converter as a function of said power level.”

As described above for claim 1[c], *Hwang* discloses the power converter controller is configured to control an internal operating characteristic of a power converter as a function of the standby signal from the load 104. *See* Section XI.A.iv. And as described above for claim 11[c], the standby signal corresponds to a power level of

said state of power drain. Section XII.B.iv.

The combination of *Hwang* and *Chagny* discloses claim 11[d]. EX1002, ¶¶228-229.

C. Claim 12

- i. **12[a] “The power system as recited in claim 11 wherein said power converter further comprises a power switch configured to conduct for a duty cycle to provide an output characteristic at an output thereof,”**

The combination of *Hwang* and *Chagny* discloses claim 12[a] for the same reasons described above regarding *Hwang*’s disclosure of similar claim 1[a]. See Section XI.A.ii; EX1002, ¶230.

- ii. **12[b] “said power converter controller further configured to control said duty cycle of said power switch dependent on said output characteristic and in accordance with said power level.”**

Claim 12[b] is similar to claim 2, but recites “in accordance with said power level” instead of “in accordance with said signal.” But, as described for claim 11[c], the “standby signal” (cited as said signal for claim 2) represents said power level. Thus, the combination of *Hwang* and *Chagny* discloses claim 12[b] for the same reasons described above regarding *Hwang*’s disclosure of claims 2 and 11[c]. See Sections XI.B and XII.B.iv; EX1002, ¶¶231-232.

D. Claim 14

The combination of *Hwang* and *Chagny* discloses the additional elements of claim 14 for the same reasons described above regarding *Hwang*’s disclosure of similar

claim 3. *See* Section XI.C; EX1002,¶233.

E. Claim 15

The combination of *Hwang* and *Chagny* discloses the additional elements of claim 15 for the same reasons described above regarding *Hwang*'s disclosure of similar claim 5. *See* Section XI.E; EX1002,¶234.

F. Claims 16-17 and 19-20

Claim 16 recites substantially the same elements of claim 11 but in the form of a method claim without the structural requirements of the “power system controller” or the “power converter” and “power converter controller” recited in claim 11. Thus, the combination of *Hwang* and *Chagny* disclose the preamble and the steps of “enabling” (16[a]), “providing” (16[b]), “sensing” (16[c]), and “controlling” (16[d]) in the same manner as described above for claim 11[a]-[d], respectively. *See* Sections XII.B.i-v; EX1002,¶235.

Likewise, dependent claims 17, 19, and 20 recite similar subject matter as claims 12, 14, and 15 respectively. Thus, the combination of *Hwang* and *Chagny* disclose claims 17, 19, and 20 in the same manner described above for claims 12, 14, and 15.

See Sections XII.C (claim 12), XII.D (claim 14), XII.E (claim 15); EX1002,¶236.

XIII. GROUND 2C: *Hwang* in view of the knowledge of a POSITA Renders Obvious Claim 18

As described above in Ground 2A, *Hwang* discloses each element of independent

claim 16. *See* Section XI.K (claim 16). When viewed with the knowledge of a POSITA, *Hwang* also discloses and suggests each additional element of dependent claim 18, rendering claim 18 obvious. EX1002,¶237.

A. Claim 18

- i. “18. The method as recited in claim 16 wherein said signal is provided upon startup of said processor system.”**

Hwang discloses that its load 104 (i.e., said processor system) may be a “smart load” that includes “a microprocessor.” EX1006, [0031]; *see also id.*, [0021]. As described in Section XI.K.iii for claim 16 [b], *Hwang* also discloses that, when smart load 104 enters the standby mode, smart load 104 provides a “standby signal” (i.e., said signal). EX1006, [0021] (“The controller 105 may sense a signal from the load 104 that indicates the level of the power drawn by the load 104.”), [0031] (“The load 104 may send a standby signal that may be interpreted by a low power detector 308.”).

A POSITA would have found it obvious that the provision of *Hwang*’s standby signal (i.e., said signal) could occur at any time during the operation of *Hwang*’s smart load 104, including upon startup of the smart load 104 and/or the microprocessor within smart load 104. EX1002,¶¶238-239. For example, *Hwang* describes the power converter being placed in standby when the power drawn by smart load 104 is below 0.5-1% of the maximum expected load power. EX1006, [0021], [0023]-[0024]. Thus, a POSITA would have found it obvious that during use cases where activity level of the microprocessor is low upon startup, *Hwang*’s smart load 104 would provide the standby

signal upon startup. EX1002,¶239. Indeed, it was known in the art that a microprocessor would send control signals to an adaptive power supply coupled to that microprocessor as soon as the microprocessor was powered up to a level where its control signal was valid. EX1002,¶239; EX1007, 3:57-64, 4:28-40, 4:50-58 (collectively describing processor taking over control of DC/DC converter output after processor has been powered up to an initial voltage level that ensure the processor's control signal outputs are valid), Fig. 3 (illustrating "VID[4:0]" control signal as valid after power- up of processor voltage CPUVCC in response to PWRON# signal).

Accordingly, *Hwang* in view of the knowledge of a POSITA renders obvious dependent claim 18. EX1002,¶240.

XIV. GROUND 2D: *Hwang* in view of *Chagny* and the Knowledge of a POSITA Renders Obvious Claims 13 and 18

As described above in Ground 2B, the combination of *Hwang* and *Chagny* discloses each element of independent claims 11 and 16. *See* Sections XII.B (claim 11) and XII.F (claim 16). When further viewed with the knowledge of a POSITA, the combination discloses and/or suggests to a POSITA the additional elements of dependent claims 13 and 18, rendering those claims obvious. EX1002,¶241.

A. Claims 13 and 18

- i. **"13. The power system as recited in claim 11 wherein said signal is provided upon startup of said processor system."**
- "18. The method as recited in claim 16 wherein said signal is**

provided upon startup of said processor system.”

Aside from dependency on claim 11 instead of claim 16, claim 13 is identical to claim 18. And as described above in Section XIII.A, *Hwang* in view of the knowledge of a POSITA renders obvious claim 18. For the same reasons described therein, the combination of *Hwang* and *Chagny* in view of the knowledge of a POSITA discloses the additional elements of both dependent claims 13 and 18. EX1002, ¶242.

XV. CONCLUSION

Petitioners respectfully request that IPR be instituted and the challenged claims be cancelled.

DATE: June 15, 2022

Respectfully Submitted,

/s/ Ping Wang
Ping Wang
Registration No. 48,328

CERTIFICATE OF COMPLIANCE

1. Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. §42.24(a), contains 13988 words which is no more than 14,000 words and therefore complies with the type-volume limitations of 37 C.F.R. §42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, Claims List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word in 14-point Times New Roman.

DATE: June 15, 2022

Respectfully Submitted,

/s/ Ping Wang
Ping Wang
Registration No. 48,328

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§42.6(e) and 42.105, the undersigned certifies that on June 15, 2022, a complete and entire copy of the PETITION FOR *INTER PARTES* REVIEW (“petition”), Petitioner’s power of attorney, and related Exhibits were served on Patent Owner via Express Mail or by means at least as fast and reliable as Express Mail at the correspondence address of record for the subject patent,

BOISBRUN HOFMAN, PLLC
1255 West 15th Street, Suite 400
Plano TX 75075

And a courtesy copy is also being forwarded to Patent Owner’s Litigation Counsel via electronic mail to:

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