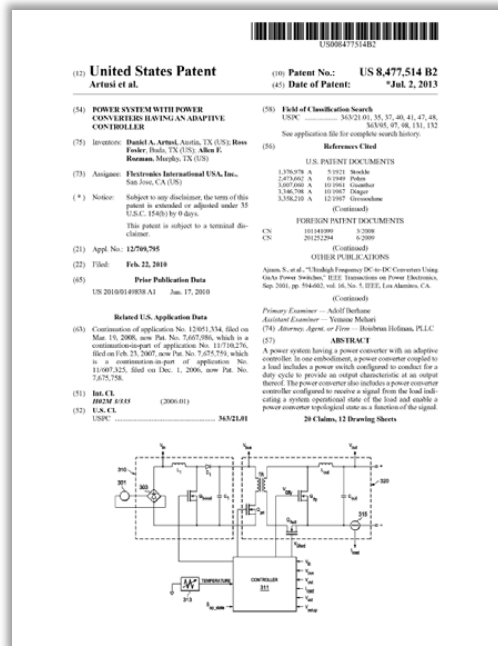


U.S. Patent No. 8,477,514 – Samsung S2MM101



Title: POWER SYSTEM WITH POWER CONVERTERS HAVING AN ADAPTIVE CONTROLLER

Priority Date: Dec. 01, 2006

Filed Date: Feb. 22, 2010

Issued Date: Jul. 02, 2013

Expiration Date: Dec. 01, 2026

Inventors: Daniel A. Artusi; Ross Fosler; Allen F. Rozman

Claims: 16, 17, 20



- All the claim elements identified herein are literally and equivalently present in the Accused Instrumentalities.
- For clarity, the portion of a cited reference that is relied upon for support may also be reproduced in the chart. Also, earlier, later or otherwise different versions of the reference may be available but not specifically cited.
- This claim chart illustrates infringement contentions for the Samsung S2MM family, and would cover, for example, family members S2MM101 and S2MM102.
- The portion of the Accused Instrumentality covered by a claim element is typically identified by an arrow and/or outlined in color. Such identification is exemplary, not exclusive or exhaustive. The Asserted Claims are open ended, not close ended or improperly restricted. Additional portions of the Accused Instrumentality might also be covered by the claim element but might not be identified in the chart.
- All quantitative figures, qualitative figures and data cited in the chart are subject to measurement and/or computational variation.

Claim 16

A method of operating a **(SYS) power system**, comprising:
enabling operation of components of a **(PRO) processor system** to establish a **(DRN) state of power drain** thereof;
providing a **(S) signal** to identify **(OPN) operation** of said **(PRO) processor system** in said **(DRN) state of power drain**;
sensing a **(PL) power level** of said **(DRN) state of power drain** in response to said **(S) signal**; and
controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.

Claim 17

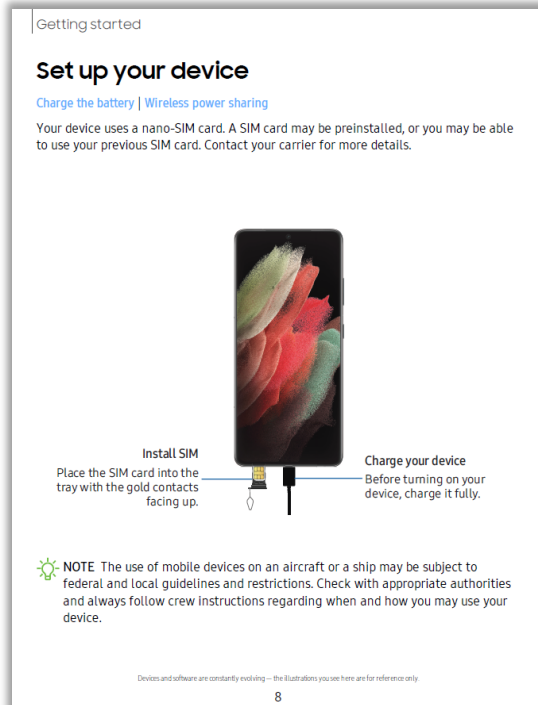
The method as recited in claim 16, further comprising:
inducing a **(PS) power switch** of said **(PC) power converter** to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output** thereof; and
controlling said **(DC) duty cycle** of said **(PS) power switch** dependent on said **(OC) output characteristic** and in accordance with said **(PL) power level**.

Claim 20

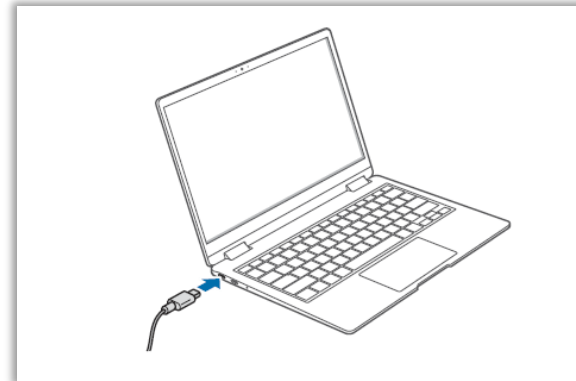
The method as recited in claim 16 wherein said **(IOC) internal operating characteristic** is selected from the group consisting of:
a gate drive voltage level of a **(PS) power switch** of said **(PC) power converter**,
a switching frequency of said **(PC) power converter**, and
an **(DCBV) internal direct current bus voltage** of said **(PC) power converter**.

Claim 16

A method of operating a **(SYS) power system**, comprising:

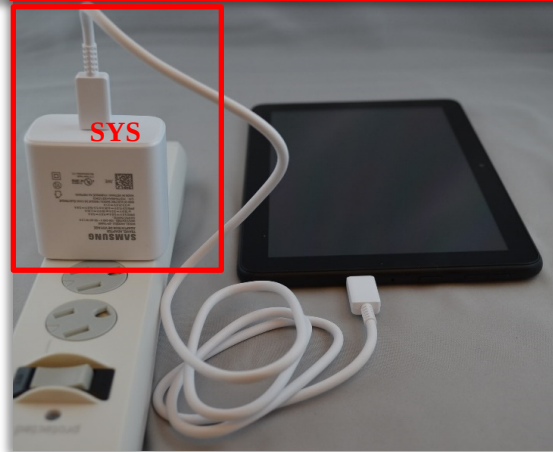


Samsung Electronics America, Inc., User Manual for Samsung Galaxy S21 5G, S21+ 5G, and S21 Ultra 5G at p. 8 (2021).



Samsung Electronics Co., Ltd., Users Guide for Samsung EP-TA865 at p. 71.

These are typical examples of Samsung generally instructing users of its power converters to couple them to loads.



Claim 16

enabling operation of components of a (PRO) processor system to establish a (DRN) state of power drain thereof;

4.5.2.2 Connection State Machine Requirements PRO

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

DRN

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	Open, Rp	Above v_{OPEN}
SRC.Rd	Rd	Within the v_{Rd} range (i.e., between minimum v_{Rd} and maximum v_{Rd})
SRC.Ra	Ra	Below maximum v_{Ra}

Table 4-15 Sink Port CC Pin State

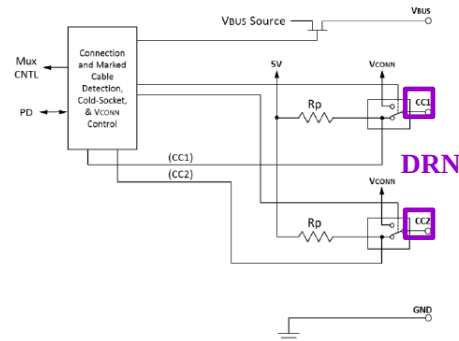
CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	Rp	Above minimum $v_{Rd-Connect}$
SNK.Open	Open, Ra, Rd	Below maximum v_{Ra}

Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
------	---



DRN

Figure 4-7 Source Functional Model for CC1 and CC2



Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (R_p) on CC1 and CC2 and monitors both to detect a Sink. The presence of an R_d pull-down resistor on either pin indicates that a Sink is being attached. The value of R_p indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.
5. The Source can dynamically adjust the value of R_p to indicate a change in available USB Type-C Current to a Sink.

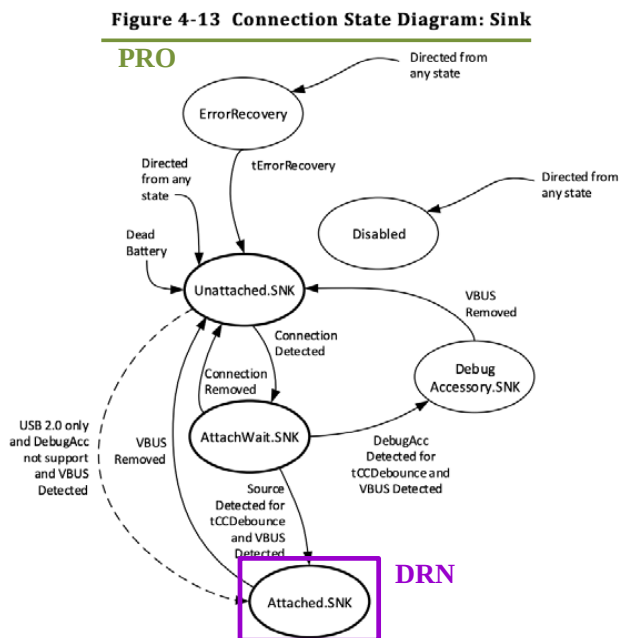
The source functional model detects CC1/CC2 and dynamically adjusts the current, voltage x current is the state of power drain.

Source(s): [1]

Claim 16

enabling operation of components of a (PRO) processor system to establish a (DRN) state of power drain thereof;

Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).



4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the [Attached.SNK](#) state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using [USB PD](#) commands.

A port that entered this state directly from [Unattached.SNK](#) due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use [USB PD](#).

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the [SNK.Rp](#) state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a [USB PD](#) PR_Swap.

If the port has entered the [Attached.SNK](#) state from the [AttachWait.SNK](#) or [TryWait.SNK](#) states, only one of the CC1 or CC2 pins will be in the [SNK.Rp](#) state. The port shall continue to terminate this CC pin to ground through [Rd](#).

If the port has entered the [Attached.SNK](#) state from the [Attached.SRC](#) state following a [USB PD](#) PR_Swap, the port shall terminate the connected CC pin to ground through [Rd](#).

The port shall meet the [Sink Power Sub-State](#) requirements specified in Section 4.5.2.2.22.

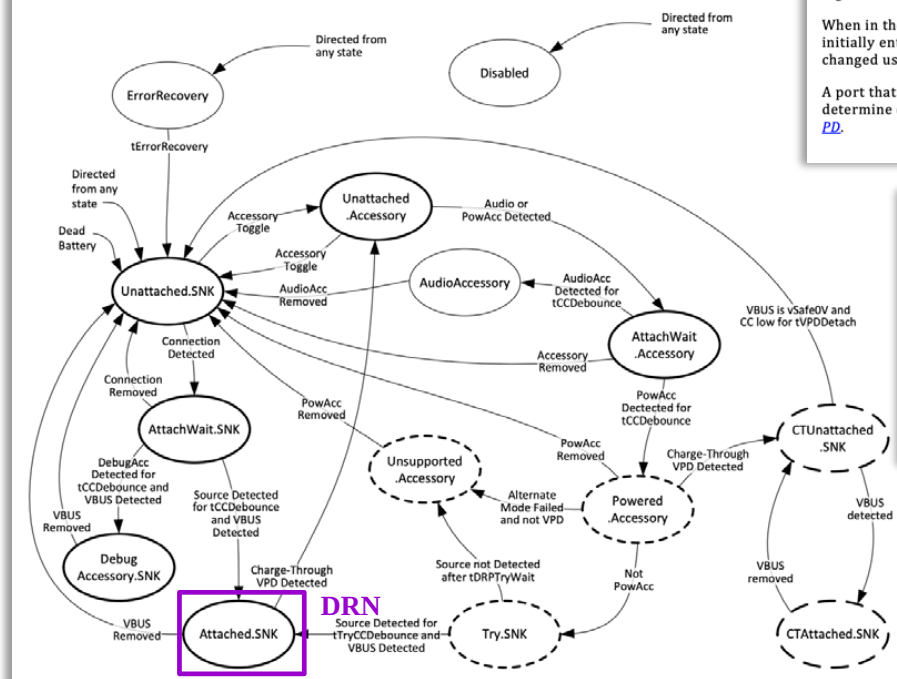
Source(s): [1]

Claim 16

enabling operation of components of a (PRO) processor system to establish a (DRN) state of power drain thereof;

Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

Figure 4-14 Connection State Diagram: Sink with Accessory Support
PRO



4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using USB PD commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use USB PD.

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a USB PD PR_Swap.

If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.

If the port has entered the Attached.SNK state from the Attached.SRC state following a USB PD PR_Swap, the port shall terminate the connected CC pin to ground through Rd.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.

Source(s): [1]

Claim 16

providing a (S) signal to identify (OPN) operation of said (PRO) processor system in said (DRN) state of power drain;

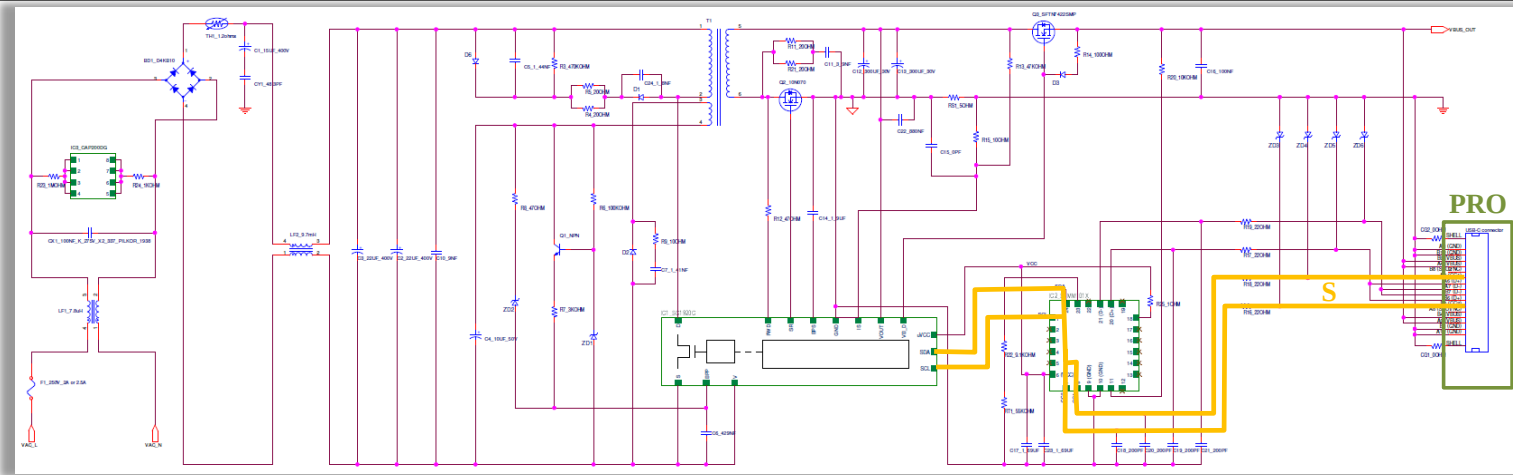


Table 3-4 USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	TXp1	Positive half of first TX differential pair	Second	B11	RXp1	Positive half of first RX differential pair	Second
A3	TXn1	Negative half of first TX differential pair	Second	B10	RXn1	Negative half of first RX differential pair	Second
A4	Vbus	Bus Power	First	B9	Vbus	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the USB 2.0 differential pair - Position 1	Second	B7	Dn2	Negative half of the USB 2.0 differential pair - Position 2	Second
A7	Dn1	Negative half of the USB 2.0 differential pair - Position 1	Second	B6	Dp2	Positive half of the USB 2.0 differential pair - Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	Vbus	Bus Power	First	B4	Vbus	Bus Power	First
A10	RXn2	Negative half of second RX differential pair	Second	B3	TXn2	Negative half of second TX differential pair	Second
A11	RXp2	Positive half of second RX differential pair	Second	B2	TXp2	Positive half of second TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

Source(s): [1]

S

Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	Open	Nothing attached	N/A
Rd	Open	Sink attached DRN	①
Open	Rd	Sink attached DRN	②
Open	Ra	Powered cable without Sink attached OPN	①
Ra	Open	Powered cable without Sink attached OPN	②
Rd	Ra	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	①
Rd	Rd	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	②
Rd	Rd	Debug Accessory Mode attached (Appendix E)	N/A
Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

- The Source uses a FET to enable/disable power delivery across Vbus and initially the Source has Vbus disabled.
- The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
- The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying Vconn.
- Once a Sink is detected, the Source enables Vbus and Vconn.
- The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

Claim 16

providing a (S) signal to identify (OPN) operation of said (PRO) processor system in said (DRN) state of power drain;

4.5.2.2 Connection State Machine Requirements PRO

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	Open, Rp	Above vOPEN
SRC.Rd	Rd	Within the vRd range (i.e., between minimum vRd and maximum vRa)
SRC.Ra	Ra	Below maximum vRa

Table 4-15 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	Rp	Above minimum vRd-Connect
SNK.Open	Open, Ra, Rd	Below maximum vRa

Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
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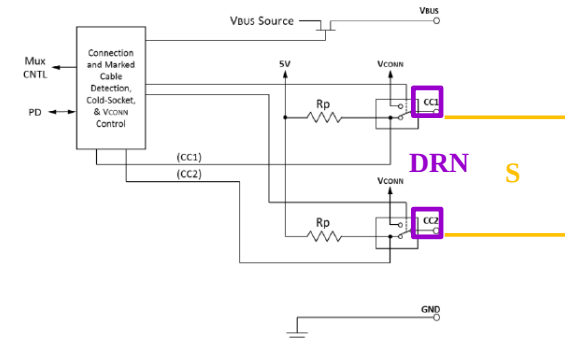
Below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I²C interface.

In this design, (U2) is the USB PD controller. It gets its supply from the μ VCC pin of the InnoSwitch3-Pro IC. Output voltage requests are sent by the IC (U2) to InnoSwitch3-Pro through the I²C communication lines (SDA and SCL) when sink requests for the same. The μ VCC pin needs a decoupling capacitor C14.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected.

Source(s): [1]; [2]

Figure 4-7 Source Functional Model for CC1 and CC2



Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

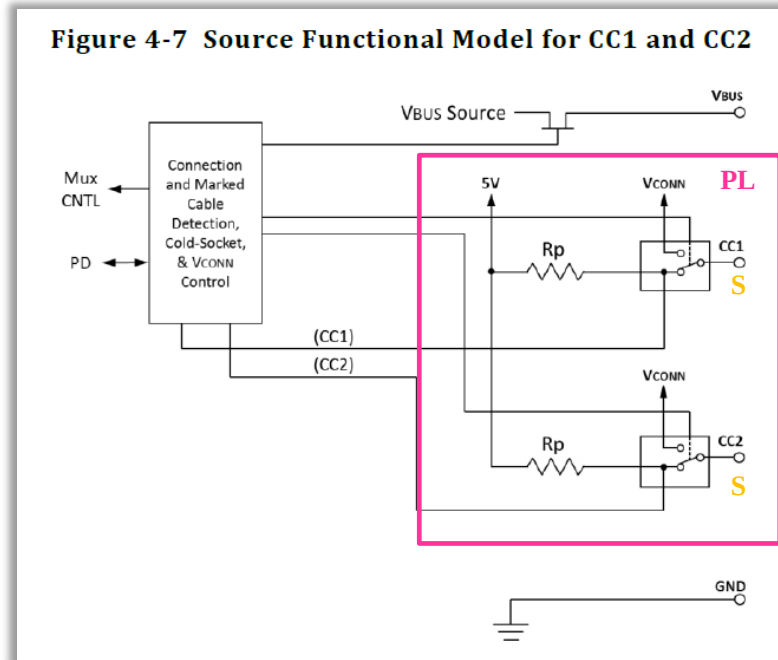
1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.
4. Once a Sink is detected, the Source enables VBUS and VCONN.
5. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.

The source functional model detects CC1/CC2 and dynamically adjusts the current, voltage x current is the state of power drain.

Claim 16

sensing a **(PL) power level** of said **(DRN) state of power drain** in response to said **(S) signal**; and

Figure 4-7 Source Functional Model for CC1 and CC2



The Source can dynamically adjust the value of R_p to indicate a change in available USB Type-C Current to a Sink.

Source(s): [1]

Claim 16

sensing a (PL) power level of said (DRN) state of power drain in response to said (S) signal; and

Table 2-1 Summary of power supply options

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See USB 2.0	
USB 3.2	5 V	See USB 3.2	
USB4	5 V	1.5 A	
USB BC 1.2	5 V	1.5 A ¹	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 20 V	Configurable up to 5 A	Directional control and power level management

Figure 4-36 illustrates how the USB PD BMC signaling is carried over the USB Type-C cable's CC wire.

Figure 4-36 USB PD over CC Pins

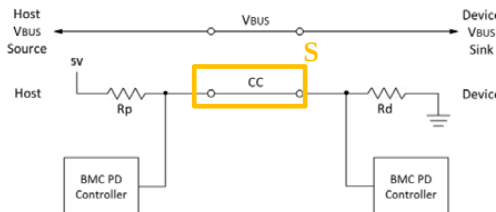


Table 4-11 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	- Sense CC pins for attach - Do not apply VBUS or VCONN	Sense VBUS for attach
Sink attached	- Sense CC for orientation - Sense CC for detach - Apply VBUS and VCONN	- Sense CC pins for orientation - Sense loss of VBUS for detach
Powered cable without Sink attached	- Sense CC pins for attach - Do not apply VBUS or VCONN	Sense VBUS for attach
Powered cable with Sink, VCONN-Powered Accessory, or VCONN-Powered USB Device attached	- Sense CC for orientation - Sense CC for detach - Apply VBUS and VCONN - Detect VPD and remove VBUS	If accessories or VPDs are supported, see Source Behavior with exception that VBUS is not applied, otherwise, N/A.
Debug Accessory Mode attached	- Sense CC pins for detach - Reconfigure for debug	- Sense VBUS for detach - Reconfigure for debug
Audio Adapter Accessory Mode attached	- Sense CC pins for detach - Reconfigure for analog audio	If accessories are supported, see Source Behavior, otherwise, N/A

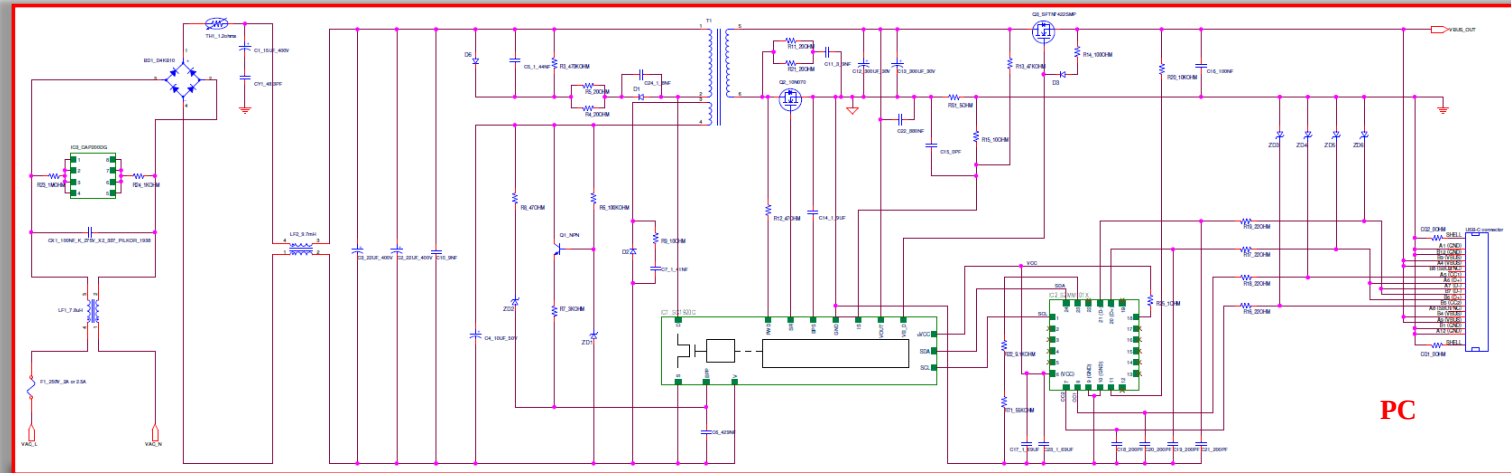
Table 4-17 Precedence of power source usage

Precedence	Mode of Operation	Nominal Voltage	Maximum Current
Highest	USB PD	Configurable	5 A
	USB Type-C Current @ 3.0 A	5 V	3.0 A
	USB Type-C Current @ 1.5 A	5 V	1.5 A
	USB BC 1.2	5 V	Up to 1.5 A ¹
↓	Default USB Power	USB 3.2	See USB 3.2
		USB 2.0	See USB 2.0
Lowest			

Source(s): [1]

Claim 16

controlling an (IOC) internal operating characteristic of a (PC) power converter as a function of said (PL) power level.



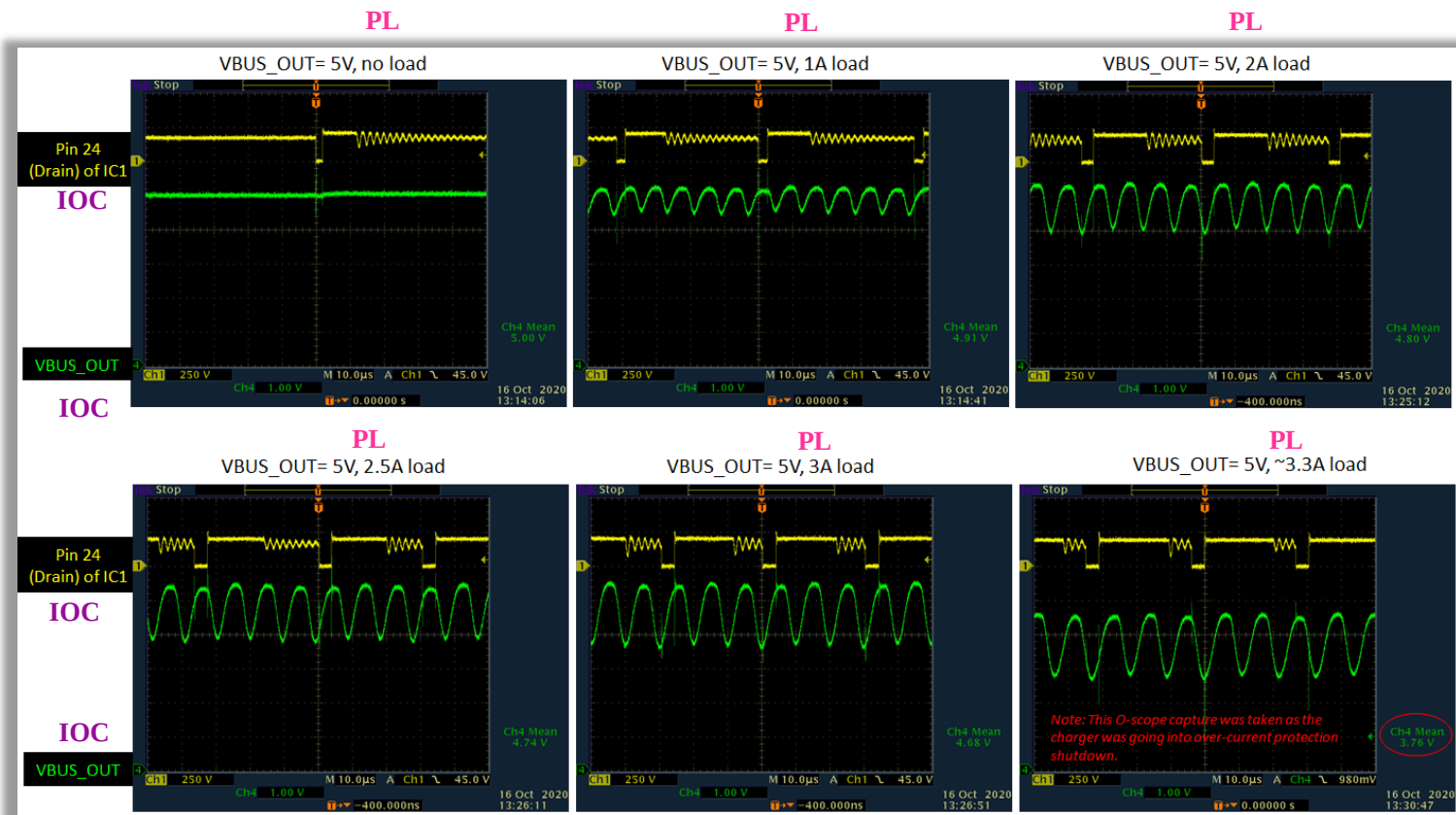
Claim 16

controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.



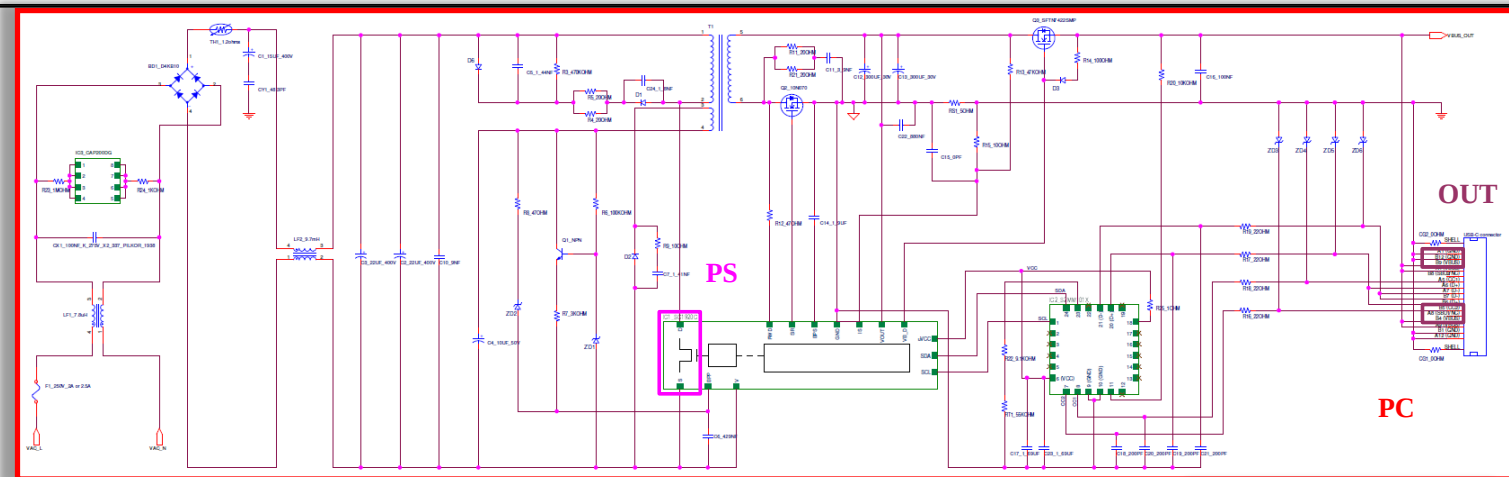
Claim 16

controlling an **(IOC) internal operating characteristic** of a **(PC) power converter** as a function of said **(PL) power level**.



Claim 17

The method as recited in claim 16, further comprising:
 inducing a **(PS) power switch** of said **(PC) power converter** to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output** thereof; and



4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

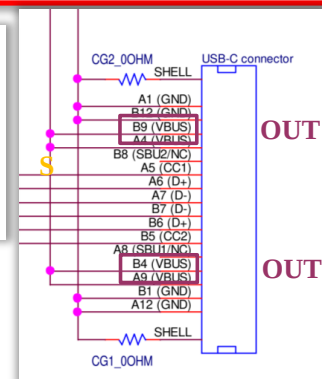
- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or USB Power Delivery

OC

Below the CC threshold, the device operates in constant voltage mode. The output voltage is set by the I²C interface.

In this design, (U2) is the USB PD controller. It gets its supply from the μ VCC pin of the InnoSwitch3-Pro IC. Output voltage requests are sent by the IC (U2) to InnoSwitch3-Pro through the I²C communication lines (SDA and SCL) when sink requests for the same. The μ VCC pin needs a decoupling capacitor C14.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected.

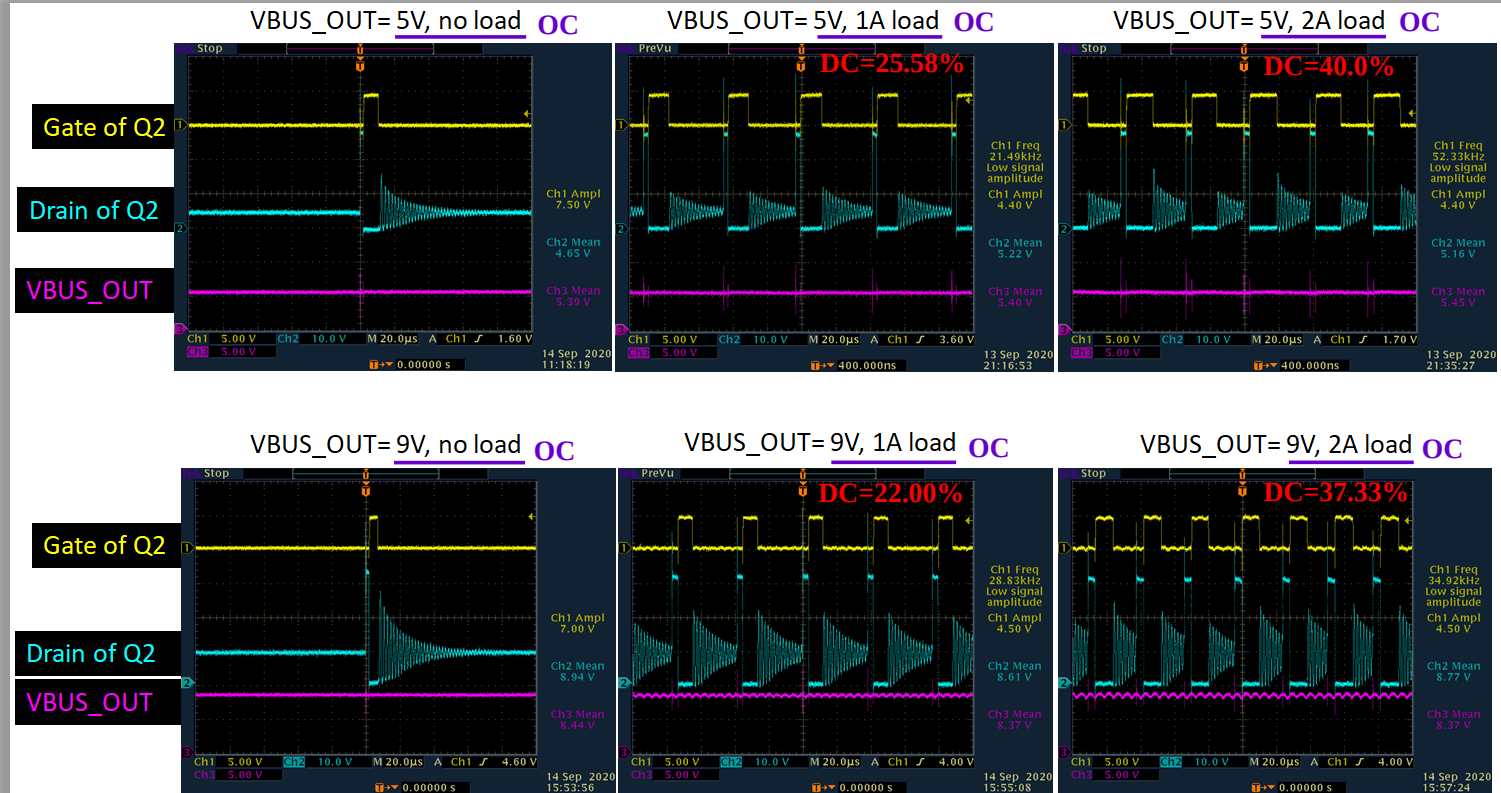


Source(s): [1]; [2]

Claim 17

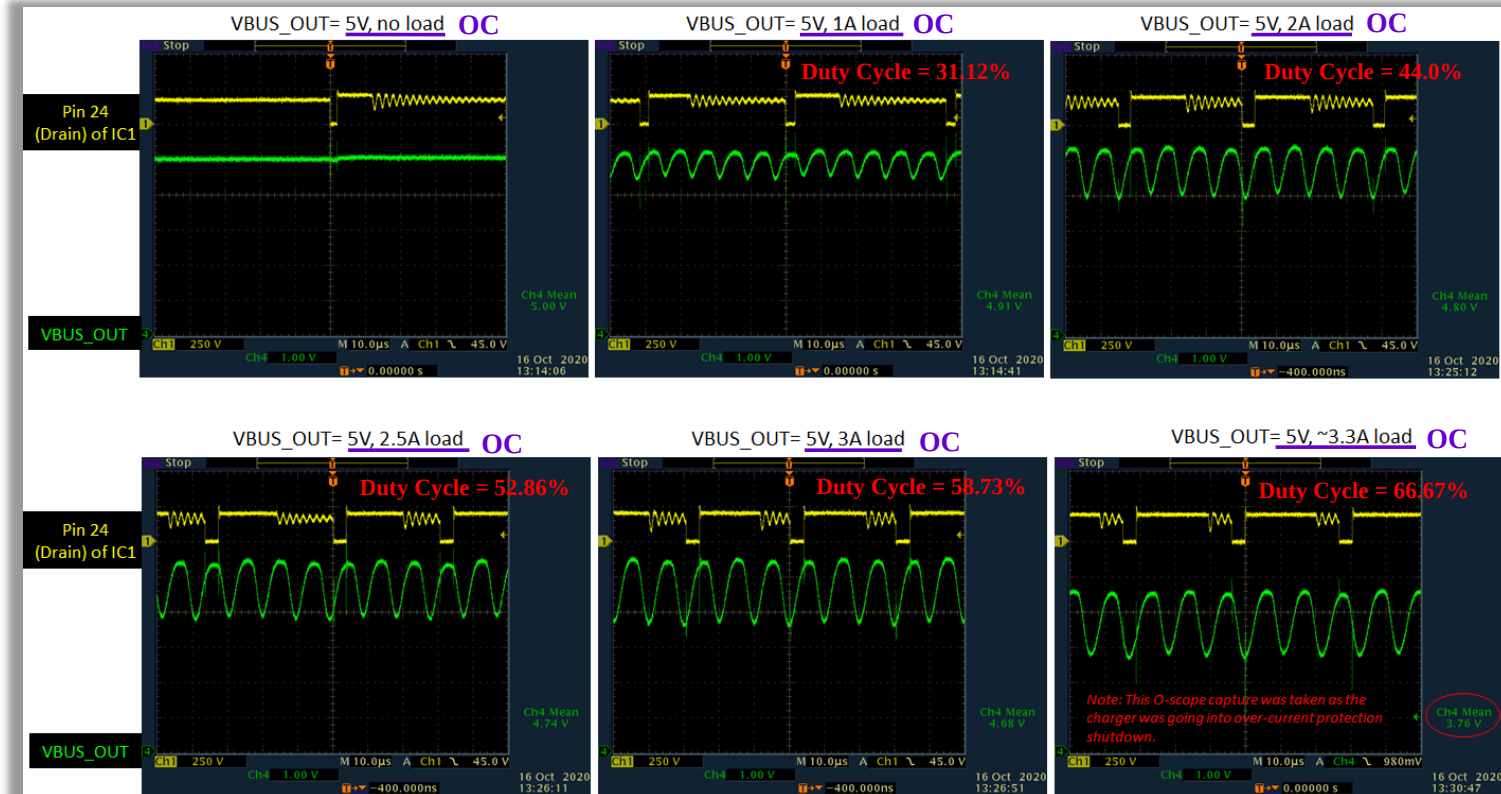
The method as recited in claim 16, further comprising:

inducing a **(PS) power switch** of said **(PC) power converter** to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output** thereof; and



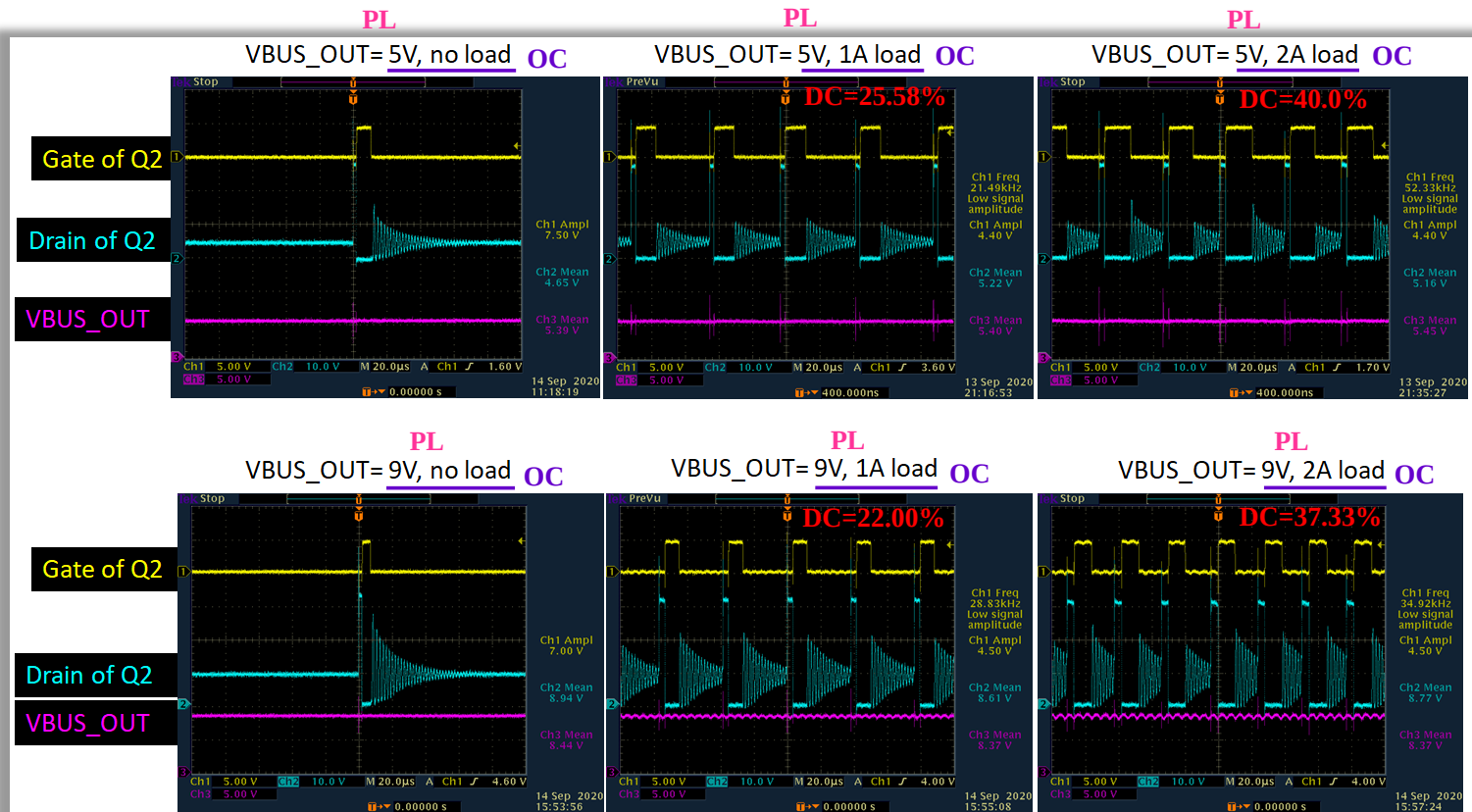
Claim 17

The method as recited in claim 16, further comprising:
 inducing a **(PS) power switch** of said **(PC) power converter** to conduct for a **(DC) duty cycle** to provide an **(OC) output characteristic** at an **(OUT) output** thereof; and



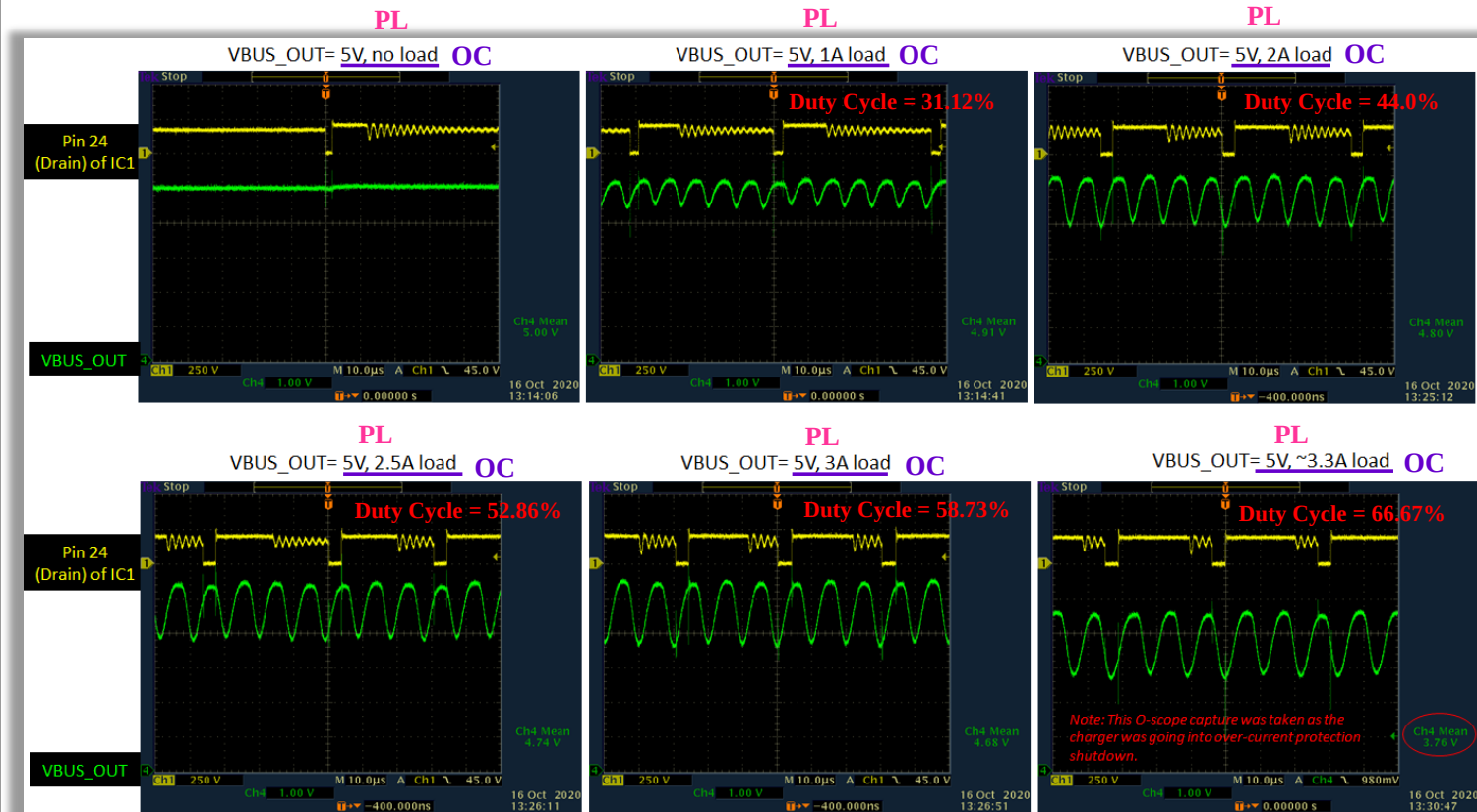
Claim 17

controlling said **(DC) duty cycle** of said **(PS) power switch** dependent on said **(OC) output characteristic** and in accordance with said **(PL) power level**.



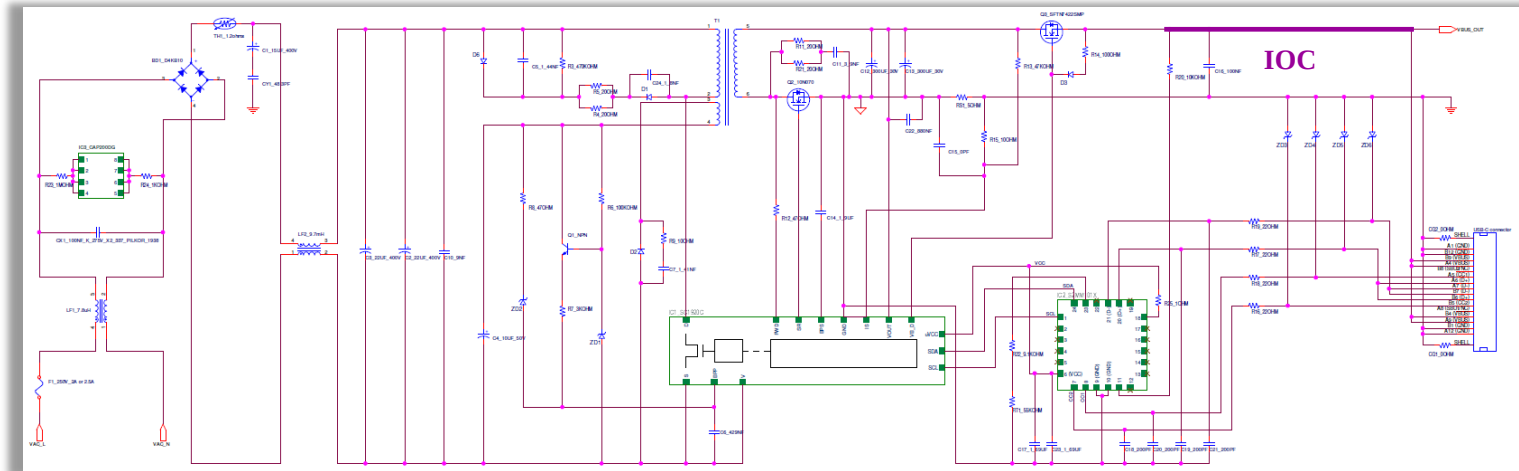
Claim 17

controlling said (DC) duty cycle of said (PS) power switch dependent on said (OC) output characteristic and in accordance with said (PL) power level.



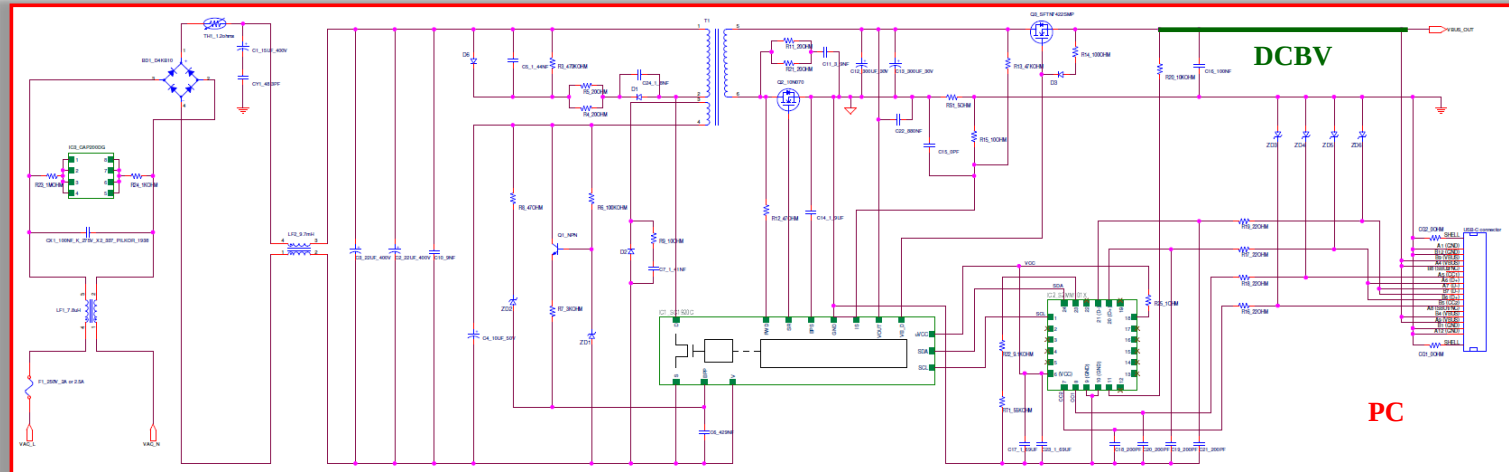
Claim 20

The method as recited in claim 16 wherein said **(IOC) internal operating characteristic** is selected from the group consisting of:



Claim 20

a gate drive voltage level of a **(PS) power switch** of said **(PC) power converter**, a switching frequency of said **(PC) power converter**, and an **(DCBV) internal direct current bus voltage** of said **(PC) power converter**.



Sources and citations

1. Universal Serial Bus Type-C Cable and Connector Specification, Release 2.0, August 2019;
2. Power Integrations InnoSwitch3-Pro Family, Rev. E 08/18;

Note: The citations may pertain to only specific document excerpts and not the schematics or other data.