

**BIPOLAR AND MOS
ANALOG INTEGRATED
CIRCUIT DESIGN**

ALAN B. GREBENE

BIPOLAR AND MOS ANALOG INTEGRATED CIRCUIT DESIGN

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*MICRO-LINEAR CORPORATION
SUNNYVALE, CALIFORNIA*

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PREFACE

The contents and organization of this book are primarily aimed at the practicing engineer in the field of solid-state electronics. It is intended as a valuable reference for the IC designer and user alike. For the analog IC designer, it provides rigorous design guidelines and examples, while for the user, it offers a detailed analysis of various classes of analog circuits, points out their design philosophy, capabilities, and limitations, and presents application examples and guidelines.

It is intended to be an easy and smooth reading book on a rapidly evolving, high-technology subject. To this end, the lengthy and detailed mathematical treatment of the subject matter is minimized. Long derivations of device or circuit equations are avoided whenever possible; instead, the emphasis is placed on the end result, and the basic design philosophy leading up to it, with a clear understanding of the underlying assumptions and trade-offs. Whenever possible, each new design idea or concept is also demonstrated with a practical example.

The advent of integrated circuit technology has altered many of the established circuit design techniques and principles. This is particularly evident in the field of analog integrated circuits where the designer is faced with a new set of design constraints and ground rules. In writing this book, it is my intention to educate the practicing electronics engineer in the fundamental design principles, capabilities, and applications of monolithic analog circuits. However, the subject matter is treated rigorously and from a fundamental viewpoint, to make this book suitable as a text for graduate study in semiconductor circuits.

This book is an updated sequel to an earlier book by the author, *Analog Integrated Circuit Design* (published by Van Nostrand Reinhold, 1972) which covered the analog IC design technology of the 1960's. Since then, many significant changes have occurred in the world of microelectronics. Perhaps the most important of these has been the "microprocessor revolution," which has resulted in a truly revolutionary growth of digital signal-processing techniques. In turn, this has led to a rapid evolution and advancement of analog circuit methods, particularly in the areas that interface with digital techniques and technologies. As a result, complete LSI systems have evolved which combine complex analog and digital functions on the same chip.

A great deal of this development has been possible by extending the capabilities of MOS devices and process technology to cover analog functions. Consequently, analog IC design using MOS technology has rapidly evolved into a major area of growth. These developments of recent years are profoundly reflected in the contents and the organization of this book.

In the preparation of the text, it is assumed that the reader is familiar with the basic theory and principles of solid-state devices. Therefore, the solid-state device theory, which is already well covered elsewhere in the literature, is reviewed only briefly, and almost all of the space is devoted to circuit approaches unique to monolithic integrated circuits. Hybrid integrated circuits, which represent an area of overlap between discrete and monolithic circuits, are not covered explicitly.

The text of the book is comprised of fifteen chapters which follow a logical sequence in the form of three "sections." The first section of the book, comprised of Chapters 1–3, reviews the basic "tools" of analog IC design and fabrication, namely, process technology, IC components, and techniques for placing these components on the chip, that is, the chip layout. These chapters are intended to familiarize the designer with the physical structures, advantages, and limitations of monolithic components. This knowledge is imperative to an analog IC design engineer since a successful design is one that efficiently utilizes the advantages of monolithic devices while avoiding their shortcomings.

The second section of the text, made up of Chapters 4–6, covers the basic "building blocks," or subcircuits, of analog IC design. One important chapter in this section, Chapter 6, deals with the use of MOS technology in analog or combined analog/digital LSI design. All the subcircuits covered in this section serve as essential building blocks of the complex IC designs that are covered in the remainder of the book.

The third and main section of the book, comprised of Chapters 7–15, covers the entire field of analog integrated circuits by dividing them into functional categories and then examining each category separately. Thus, for example, circuit classes such as operational amplifiers, multipliers, oscillators, phase-locked loops, filters, and data conversion circuits are examined separately. In this section, particular emphasis is given to the recent developments in the field of analog circuits, particularly in the areas of switched-capacitor filters, switching regulators, voltage-controlled oscillators, high-resolution data conversion circuits, and the precision reference circuitry associated with them.

Part of the material in this book is patterned after a sequence of graduate level courses in integrated electronics which I taught at Santa Clara University. Therefore, when preceded by courses on solid-state circuits and semiconductor electronics, this book will be well suited for a senior or graduate level course.

I am grateful to many people who have contributed directly or indirectly to the preparation of this book. In particular, I would like to thank my wife, Karen, who has been a constant source of encouragement for me during the long years of effort that have gone into this book. I would also like to extend my appreciation to many colleagues and associates in the IC industry for their assistance and guidance in the

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organization and technical accuracy of the text. I am particularly grateful to the management of Exar Integrated Systems, Inc., for providing me the time to work on this book, and to Ms. Sue Wooldridge who has patiently typed and retyped the draft of the manuscript several times over.

ALAN B. GREBENE

Saratoga, California
August 1983

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The thickness of a metal interconnection layer may be reduced at the points where the metal trace is forced to run over oxide steps on the chip surface, due to different mask layers. This results in a reduction of the conductor cross section, and correspondingly, is an increase of the current density within the metal trace at these localized spots. In order to avoid potential metal-migration problems at such points within the circuit, the high-current interconnection paths should not be routed over such oxide steps.

PART II: SWITCHING REGULATORS

10.6. FUNDAMENTALS OF SWITCHING REGULATORS

The switching regulators, which are also called *switch-mode regulators*, find a wide range of applications in power supply design where high power and high efficiency are important. The principle of operation of a switching regulator differs significantly from that of a conventional series regulator circuit discussed in the first part of this chapter. In the case of series regulators, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. In the case of switching regulators, the pass transistor is used as a "controlled switch" and is operated at either the cutoff or the saturated state. In this manner, the power is transmitted across the pass device in discrete current pulses, rather than as a steady current flow.

The most important advantage of switching regulators over the conventional series regulators is their greater efficiency, since the pass device is operated as a low-impedance switch. When the pass device is at cutoff, there is no current through it, thus it dissipates no power. When the pass device is in saturation, it is nearly a short circuit with negligible voltage drop across it, thus it dissipates only a small amount of average power, provided that it can handle the peak current loads. In either case, very little power is wasted in the regulator and pass devices, and almost all the power is transferred to the load. In this manner, a very high degree of regulator efficiency is achieved, typically in the range of 70–90%, relatively independent of the input–output voltage differentials. The efficiency of switching regulators is particularly apparent when there is a large input–output voltage difference across the regulator. For example, if one considers the case of a regulator operating with a 28-V input and delivering a 5-V output at 1-A current, a conventional series regulator would require a drop of 23 V across the series pass transistor. Thus, a total of 23 W of power is wasted in the regulator, resulting in an overall regulator efficiency of approximately 18% [see Eq. (10.12)]. As will be described in later sections, a switching regulator can be readily designed to perform the same function with greater than 75% efficiency under similar operating conditions.

Another important advantage of the switching regulator circuit is its versatility. It can provide output voltages which can be less than, greater than, or of opposite polarity to the input voltage, as determined by the mode of operation of the circuit. In this manner, one can step up, step down, or invert the polarity of an input voltage to generate any arbitrary set of dc voltages within a system.

Switching regulators also have some drawbacks. They are more complex and require external components such as inductors or transformers. They generate more noise and output ripple than conventional series regulators, and are slower responding to transient load changes. One area of caution, when using switching regulators, is the generation of electromagnetic and radio-frequency interference (RFI). This interference problem is usually solved by the use of feedthrough low-pass filters isolating the power lines into the regulator, and by using ground shields around the regulator to suppress the interference. However, even with these precautions, switching regulator circuits are not recommended for powering very-low-level signal-processing circuitry, where noise characteristics are very critical.

A switching-regulator power supply system is made up of three basic blocks: (1) the switching element which is normally a power transistor, (2) control circuitry which sets the duty cycle (i.e., on-off time) of the switching element, and (3) output circuitry which converts the pulsed input power to a steady output power flow. The switching-regulator power supplies are classified into three categories, depending on the type of output circuitry used. These classes are

1. Single-ended inductor circuits.
2. Diode-capacitor circuits.
3. Transformer-coupled circuits.

Figure 10.22 shows the three basic configurations for the output circuitry of single-ended inductor-type switching regulators. These are among the most frequently used output circuit configurations, since they are by far the easiest to design and control for medium- and high-current applications.

Figure 10.23 shows the switching regulator configurations using diode-capacitor circuits. These circuits are typically used for very-low-current applications, and primarily as voltage multipliers, to increase the voltage level available from a low-voltage battery. Examples of such applications are the generation of voltage drive for LCD displays in watch circuits from a 1.5- or 3-V battery and in low-voltage hearing aid amplifiers.

Figure 10.24 shows the two basic configurations of transformer-coupled output circuits. The circuit of Figure 10.24a is the so-called *push-pull circuit* used in conventional dc-to-dc converters, with each switch controlled for 0–45% duty cycle modulation. The configuration of Figure 10.24b is the so-called single-ended *flyback converter*, which is useful at low- to medium-current loads.

The design of power supply systems using discrete circuits, and the various types of output circuitry shown in Figures 10.22 through 10.24, are well covered

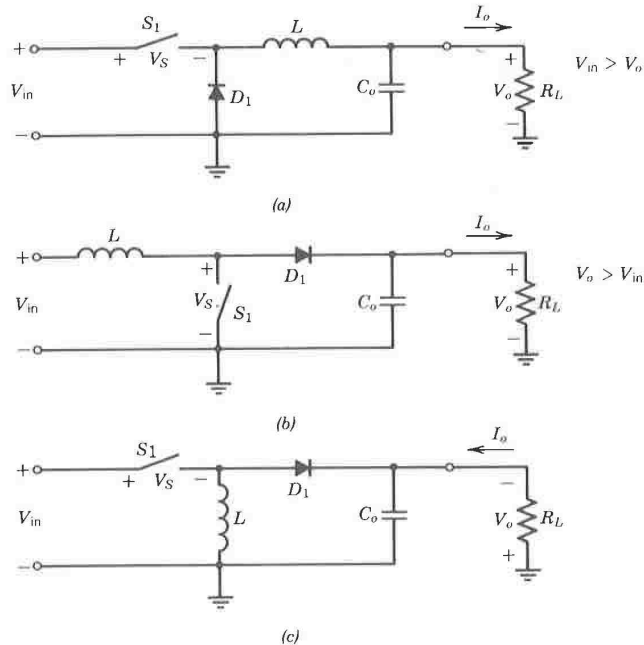


FIGURE 10.22. Inductive switching regulator configurations: (a) Step-down; (b) step-up; (c) polarity-inverting.

in the literature.⁽¹⁴⁾ In the following discussions, we will primarily focus on switching regulator circuits using the single-ended inductor-type output circuit shown in Figure 10.22, since they represent by far the most common and general categories of application, and are especially suited to high-current applications.

The control circuitry section of a switching regulator system, which controls the on-off duty cycle of the switch transistors, can be readily integrated in a monolithic IC form. In many cases, the switching transistors up to 1-A current rating can also be incorporated into the monolithic chip. If higher power levels are required, the switch transistor on the chip is used as a drive for an external high-current switch.

Figure 10.25 shows a simplified block diagram of a typical switching regulator integrated circuit used in conjunction with the single-ended inductor configuration of Figure 10.22a. The circuit generates a stream of pulses which turn switch S_1 on and off. The output dc level is sensed through the sampling resistors R_1 and R_2 and compared against an internal voltage reference V_{ref} , and the on-off time on the duty cycle of the switch S_1 is varied accordingly to keep the output voltage constant under changing load conditions.

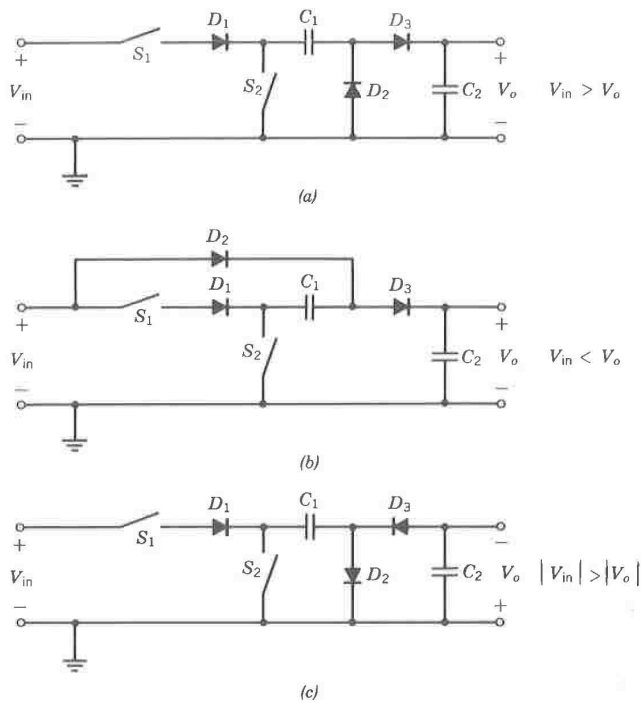


FIGURE 10.23 Diode-capacitor-type switching regulator configurations: (a) Step-down; (b) voltage multiplier; (c) polarity inverting.

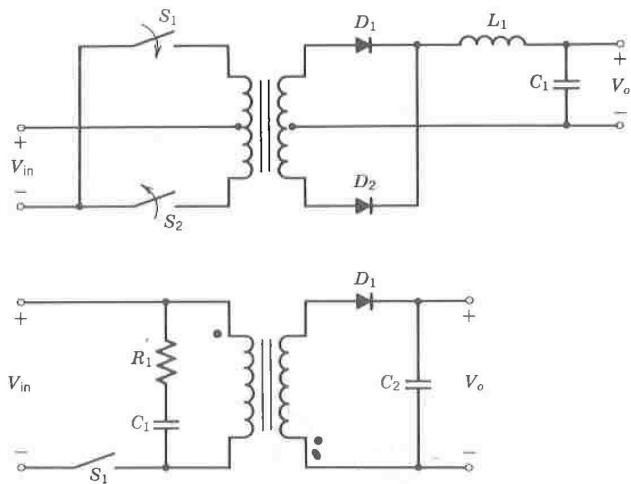


FIGURE 10.24 Transformer-coupled switching regulator configurations: (a) Push-pull; (b) flyback.

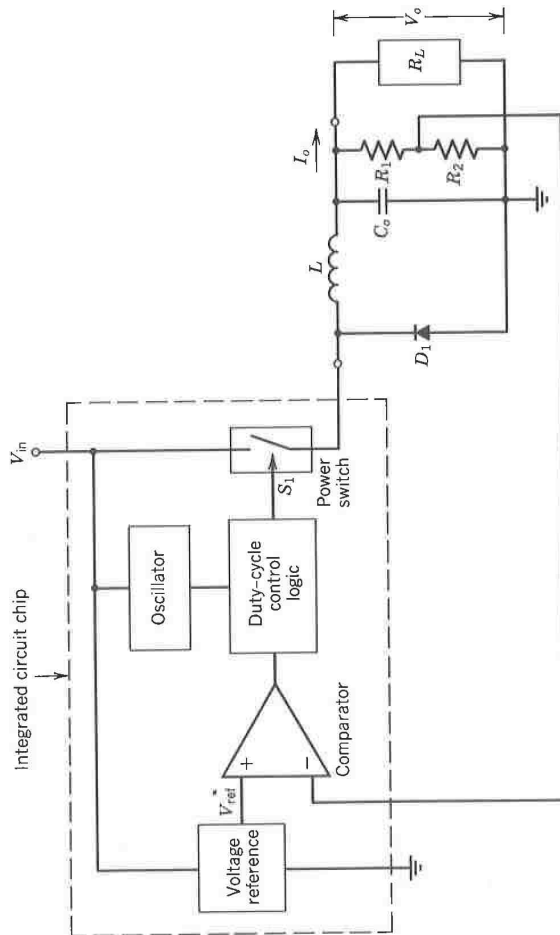


FIGURE 10.25. Simplified block diagram of switching regulator integrated circuit in step-down configuration.

Neglecting the current in the sampling resistors, the average or dc value of the output current I_o delivered to the load is proportional to the duty cycle of the power switch S_1 , as shown in Figure 10.26. If the sampled output voltage is lower than V_{ref} , the polarity of the comparator output signal causes the control logic to increase the duty cycle of S_1 and, thus, causes the output voltage level to increase until the equilibrium is reached such that the output voltage, scaled down by the sampling resistors, is equal to the internal reference voltage. Similarly, if the output load current I_o is decreased, this would cause the output voltage to increase, which in turn would be sensed by the control circuitry and would reduce the duty cycle of the switch accordingly.

Control of the Duty Cycle

The switch duty cycle t_{on}/T can be controlled by pulse-width modulation methods at a fixed frequency, or by fixing the on or off time and controlling the frequency. The relative merits and disadvantages of these techniques are briefly examined below.

Fixed-Frequency, Variable-Duty Cycle Operation. In this type of a switching regulator, the operating frequency is fixed, and the duty cycle of the pulse train is varied to change the average power. This method is often referred to as

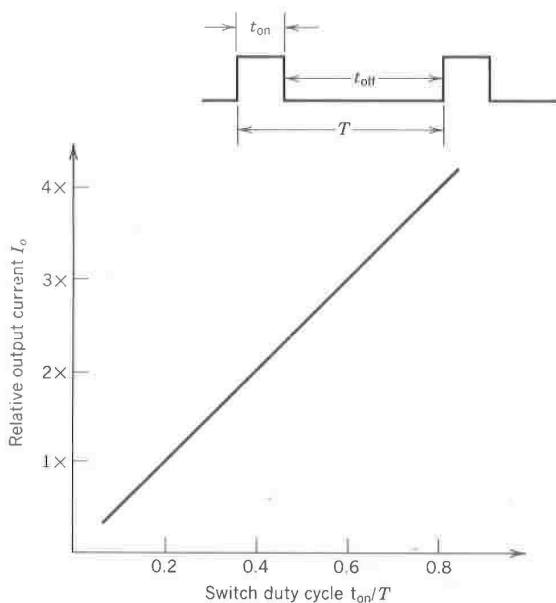


FIGURE 10.26. Output load current I_o as a function of switch duty cycle.

pulse-width modulation (PWM). The fixed-frequency concept is particularly advantageous for systems employing transformer-coupled output stages. The fixed-frequency aspect enables the efficient design of the associated magnetics. In addition, filtering or shielding the surroundings from the radio-frequency or electromagnetic interference generated by the regulator is somewhat simplified because of the fixed frequency of switching. Because of these features, the majority of the monolithic switching regulators utilize the fixed-frequency, variable-duty-cycle control method.

Fixed-On-Time, Variable-Frequency Operation. In this method, the switch has a fixed or predetermined on time; and the duty cycle is varied by varying the frequency or repetition rate of the control pulses. This method provides ease of design in voltage conversion applications using the single-ended inductive output circuit configurations of Figure 10.22, and simplifies design calculations for the inductor value. The fixed-on-time method is also advantageous for inductive output circuitry since a consistent amount of charge is developed in the inductor during the fixed on time. This eases the design or the selection of the inductor by defining the operating area to which the inductor is subjected under transient load conditions. Figure 10.27a shows the typical frequency versus load current characteristics of a fixed-on-time, variable-frequency regulator, where the frequency increases *linearly* with increasing load.

Fixed-Off-Time, Variable-Frequency Operation. In this type of a voltage regulator, the dc voltage at the output is varied by changing the on time t_{on} of the switch while maintaining a fixed off time T_{off} . As shown in Figure 10.27b, the fixed-off-time switching regulator behaves in an opposite manner to the fixed-on-time system: as the load current increases, the on time becomes longer, thus decreasing the frequency. This approach is advantageous for the design of switching regulators that will operate at a well-defined minimum frequency and low-ripple current under full-load conditions. One basic drawback of the

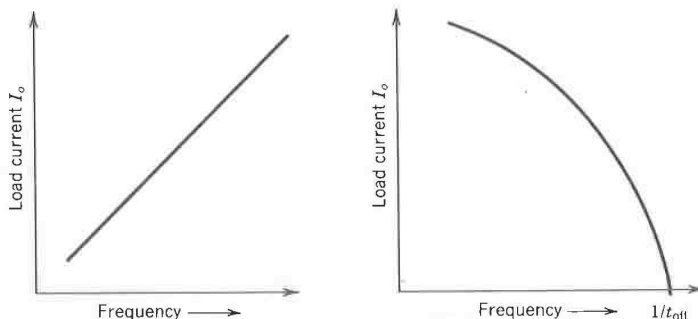


FIGURE 10.27. Typical load current versus frequency characteristics of variable-frequency switching regulators: (a) Fixed on time; (b) fixed off time.

fixed-off-time system is that the maximum current in the inductor, under transient load conditions, is not well-defined. Thus, additional care is required to ensure that the saturation characteristics of the inductor are not exceeded.

10.7. MODES OF OPERATION WITH INDUCTIVE OUTPUT CIRCUITS

Two of the most important advantages of switched regulators are their high efficiency and their ability to step up, step down, or change polarity of an input voltage. These basic features can be best understood by examining the voltage and current waveforms at the output of the regulator. In this section, some of the waveforms and key design equations associated with the inductive output circuits of Figure 10.22 will be examined for various modes of operation under steady-state load conditions. The rigorous derivations of the circuit equations associated with the basic current and voltage waveforms is straightforward and is available in the literature.^(14,15) Therefore, for the sake of brevity, rigorous derivations will be omitted and only their conclusions will be presented.

Step-Down Operation

In the step-down mode of operation, the switching regulator produces an output dc voltage V_o which is *lower* than the input voltage V_{in} . Figure 10.28 shows the basic voltage and current waveforms associated with the circuit under steady-state operation. The switch S_1 is assumed to have a voltage drop of V_{sat} in its on condition, and the diode D_1 has a forward drop of V_D when it is conducting.

When S_1 is closed or on, D_1 is off and the current I_L in the inductor rises linearly from zero to its peak value I_{pk} , with the slope

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{in} - V_{sat} - V_o}{L} \quad (10.22)$$

At the end of the switch on-time t_{on} , this current reaches its maximum value I_{pk} . When S_1 is off, the inductor generates the necessary voltage to forward bias D_1 and keep I_L from changing instantaneously. During this portion of the cycle, I_L linearly decays to zero at the end of the off time t_{off} .

At steady state, average, or dc current through C_o is zero; therefore, the output dc current I_o is equal to the average value of I_L or

$$I_o = (I_L)_{av} = \frac{I_{pk}}{2} \quad (10.23)$$

From the waveforms shown in Figure 10.28, the switch on and off times can be related to the voltage levels at the input and output of the circuit as

$$\frac{t_{on}}{t_{off}} = \frac{V_o + V_D}{V_{in} - V_{sat} - V_o} \quad (10.24)$$

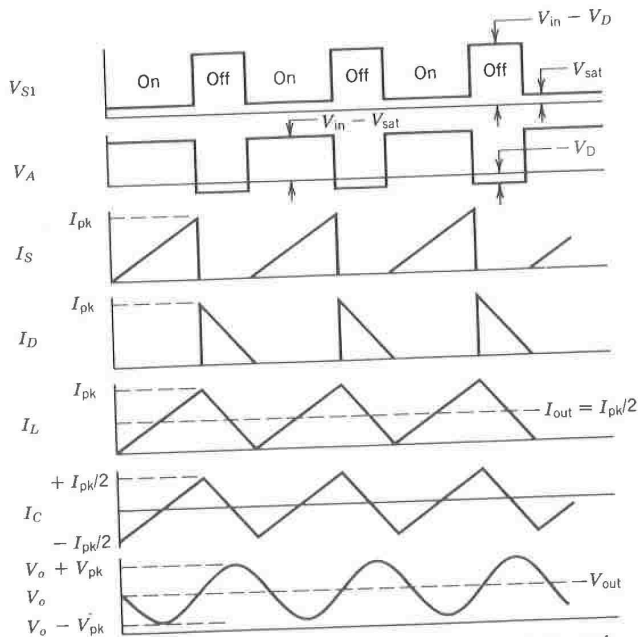
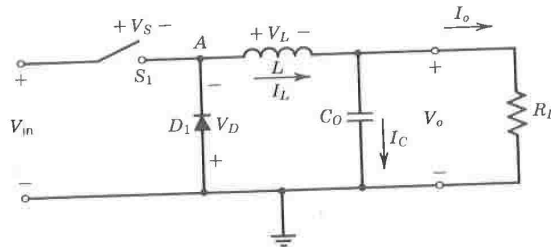


FIGURE 10.28. Voltage and current waveforms in step-down mode.

or, V_o can be related to the rest of the voltages as

$$V_o = \frac{t_{\text{on}}}{T} (V_{\text{in}} - V_{\text{sat}}) - \frac{t_{\text{off}}}{T} V_D \quad (10.25)$$

Assuming the ideal case where both the saturation and the diode voltages are zero or negligible, this reduces to

$$(V_o)_{\text{ideal}} = \frac{t_{\text{on}}}{T} V_{\text{in}} \quad (10.26)$$

Equation (10.26) implies that, ideally, the switching regulator in its step-down mode provides a down scaling of the input voltage by a scale factor equal to the duty cycle of the switch transistor.

Another important parameter of the step-down regulator is the peak-to-peak output ripple voltage $(\Delta V_o)_{pp}$. Assuming that C_o is sufficiently large so that the ripple voltage is much lower than the average or dc value of the output, $(\Delta V_o)_{pp}$ can be expressed as

$$(\Delta V_o)_{pp} \approx \frac{I_{pk}}{8C_o}(t_{on} + t_{off}) = \frac{I_{pk}}{8C_o f} \quad (10.27)$$

where $f = 1/T$ is the frequency or the repetition rate at which the switch opens and closes.

Step-Up Operation

In the step-up mode, the switching regulator produces an output dc voltage V_o which is *higher* than V_{in} . The circuit configuration for this mode of operation, along with the associated voltage and current waveforms, is shown in Figure 10.29 under steady-state operation.

With reference to Figure 10.29, the operation of the circuit can be summarized as follows. Assuming that S_1 is open and closes at the moment $I_L = 0$, the current in the inductor rises linearly from zero to a peak value I_{pk} during t_{on} . At the end of the on time, S_1 is opened. Since I_L cannot change instantaneously, the inductor generates the necessary voltage at node A to forward bias D_1 and keep the current continuous. During the off time, I_L decays linearly, and reaches zero at t_{off} . Then S_1 closes again, and the cycle repeats itself. While D_1 is conducting, it supplies current both to the load and to the holding capacitor C_o ; and when D_1 is nonconducting, the output current is drawn from C_o . Note that at steady state, the average or dc current through D_1 is equal to the output or load current I_o and the net charge supplied to C_o , per cycle of operation, is zero.

The peak current I_{pk} is related to the steady-state output current as

$$I_{pk} = 2I_o \frac{V_D + V_o - V_{sat}}{V_{in} - V_{sat}} \quad (10.28)$$

and the on-off times of the switch, necessary for I_L to ramp from zero to I_{pk} and back to zero, are related as

$$\frac{t_{on}}{t_{off}} = \frac{V_D + V_o - V_{in}}{V_{in} - V_{sat}} \quad (10.29)$$

Solving Eq. (10.29) for V_o , one obtains

$$V_o = V_{in} \frac{T}{t_{off}} - V_{sat} \frac{t_{on}}{t_{off}} - V_D \quad (10.30)$$

where $T (= t_{off} + t_{on})$ is the period of one full cycle of operation. In the idealized

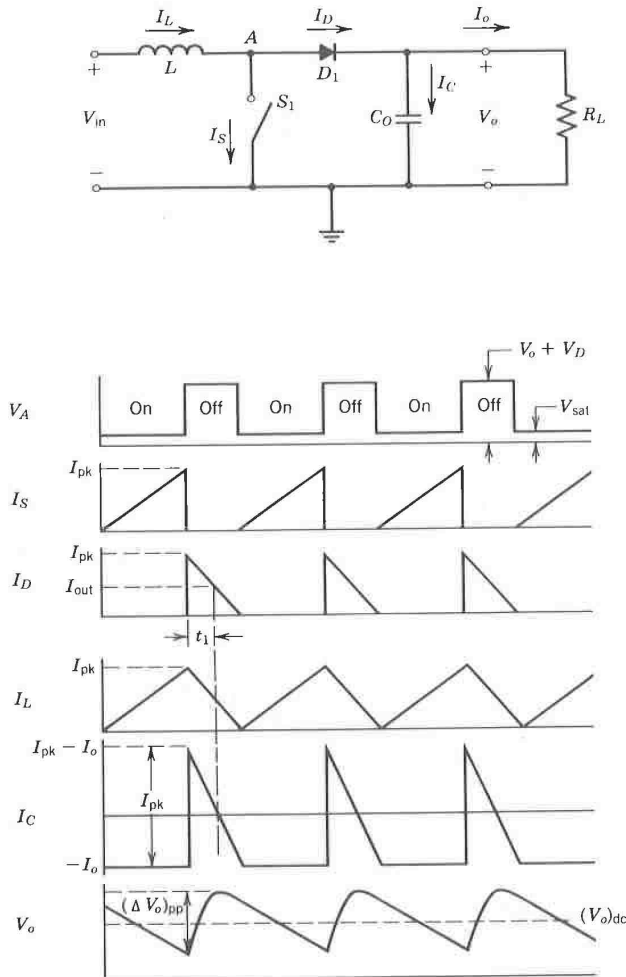


FIGURE 10.29. Voltage and current waveforms in step-up mode.

case, where the diode drop and V_{sat} of the switch are negligible, Eq. (10.30) reduces to

$$(V_o)_{ideal} = V_{in} \frac{T}{t_{off}} \quad (10.31)$$

or, in other words, the step-up mode of operation results in up-scaling the input voltage by the ratio T/t_{off} .

The peak-to-peak output ripple voltage can be expressed as⁽¹⁵⁾

$$(\Delta V_o)_{pp} \approx \frac{(I_{pk} - I_o)^2 t_{off}}{2I_{pk} C_o} \quad (10.32)$$

with the assumption that $(\Delta V_o)_{pp} \ll V_o$.

Polarity-Inverting Operation

In the polarity-inverting mode of operation, the switching regulator produces an output voltage across the load which has the *opposite* polarity of the input. Figure 10.30 shows the basic circuit configuration for this mode of operation, along with the associated voltage and current waveforms under steady-state operation. The polarity inversion is achieved by making the inductor force a current in the opposite direction through the load.

The operation of the circuit in its inverting mode can be briefly described as follows. The current I_L through the inductor ramps up from zero to I_{pk} during t_{on} , and ramps down to zero during t_{off} , similar to the other two modes of operation described earlier. During t_{off} , with S_1 open, the inductor generates a negative voltage at node A to forward bias D_1 and keep I_L continuous. As in the case of step-up circuits, the average value of the diode current I_D is the steady-state load current I_o since C_o can not carry any dc current. Thus, from the waveforms and timing relations of Figure 10.30, one can express the peak current I_{pk} as

$$I_{pk} = 2I_o \frac{V_{in} + V_D - V_o - V_{sat}}{V_{in} - V_{sat}} \quad (10.33)$$

and the ratio of the on-off times of the switch necessary for I_L to ramp up from zero to I_{pk} and back to zero are

$$\frac{t_{on}}{t_{off}} = \frac{V_D - V_o}{V_{in} - V_{sat}} \quad (10.34)$$

Solving the above equation for V_o , one gets

$$V_o = - \left[\frac{t_{on}}{t_{off}} (V_{in} - V_{sat}) - V_D \right] \quad (10.35)$$

In the idealized case, where V_D and V_{sat} are neglected, Eq. (10.35) will reduce to

$$(V_o)_{ideal} = - \frac{t_{on}}{t_{off}} V_{in} \quad (10.36)$$

or, in other words, the polarity-inverting mode of operation results in the reversal of the polarity of the output voltage as well as its being scaled by the t_{on}/t_{off} ratio.

The peak-to-peak output ripple $(\Delta V_o)_{pp}$ associated with the inverting operation

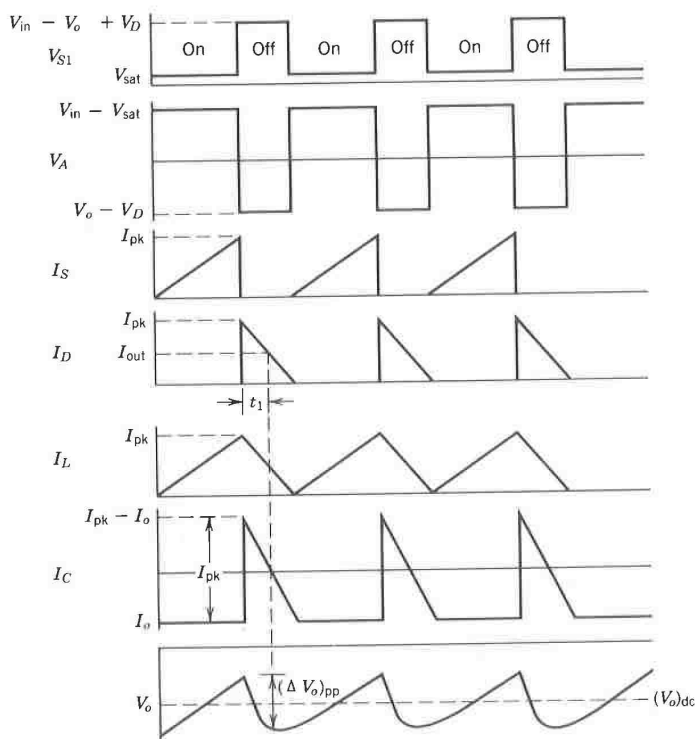
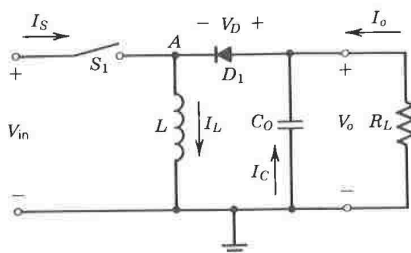


FIGURE 10.30. Voltage and current waveforms in polarity-inverting mode.

can be expressed as⁽¹⁵⁾

$$(\Delta V_o)_{pp} \approx \frac{(I_{pk} - I_o)^2 t_{off}}{2I_{pk} C_o} \quad (10.37)$$

which is identical to the case of step-up operation [see Eq. (10.32)].

One word of caution is in order when using the polarity-inverting configuration. Since the output polarity is reversed, the feedback polarity from the sampling resistors to the voltage comparator in the control circuitry (see Fig. 10.25) must be reversed. Normally, this is done by reversing the reference and feedback inputs into the voltage comparator.

10.8. EFFICIENCY CONSIDERATIONS

One of the most important features of switching regulators is efficiency. Using the basic analysis of the previous section, one can readily derive quantitative expressions for the efficiency of each of the three basic switching regulator configurations discussed.

The regulator efficiency is defined by Eq. (10.9) as

$$\eta = \frac{P_o}{P_{in}} = \frac{I_o V_o}{I_{in} V_{in}} \quad (10.38)$$

where I_o and I_{in} are the average (i.e., dc) values of the output and input currents.

For the case of the step-down regulator circuit, from Eq. (10.23) through (10.25), one can derive an expression for efficiency as

$$\eta_{\text{stepdown}} = \frac{V_o}{V_o + V_D} \frac{V_{in} + V_D - V_{sat}}{V_{in}} \quad (10.39)$$

In a similar manner, the efficiency expression for step-up operation can be derived from Eqs. (10.28) through (10.30) as

$$\eta_{\text{stepup}} = \frac{V_o}{V_o + V_D - V_{sat}} \frac{V_{in} - V_{sat}}{V_{in}} \quad (10.40)$$

The efficiency expression for inverted-polarity operation can be derived from Eq. (10.33) through (10.35) as

$$\eta_{\text{inverter}} = \frac{|V_o|}{V_D + |V_o|} \frac{V_{in} - V_{sat}}{V_{in}} \quad (10.41)$$

The efficiency expressions given above do not take into account the quiescent power dissipation in the control circuitry, which can cause the efficiency to decrease at very low current levels, when the average input current is of the same order of magnitude as the quiescent current. The switching transient losses in the switch transistor and diode, as well as the parasitic resistances associated with the inductor are also not included in the above expressions. In practical regulator systems, these latter losses will cause a small but finite reduction in the observed efficiency, as compared to the theoretical results given in Eqs. (10.39) through (10.41). The exact nature of this reduction in efficiency depends on the specific transistor, diode, and inductor characteristics used, as well as on the selection of the operating frequency.

There are two additional observations which can be made regarding the efficiency expressions:

1. In the ideal case, where both V_{sat} and V_D go to zero, all three regulator configurations provide an ideal efficiency of 100%.
2. The efficiency expressions of Eqs. (10.39) through (10.41) are not sensitive to input-output voltage differential across the regulator. This is very different from the case of a conventional series regulator, where the efficiency varies *inversely* with the input-output voltage differential [see Eq. (10.12)].

As an illustration, it is worthwhile to compare the efficiency of a power supply system with a 20-V input and a 5-V output, with a conventional series regulator, to that with a step-down switching regulator. For simplicity, quiescent power dissipation associated with the control circuitry will be neglected.

In the case of a conventional series regulator, the efficiency is

$$\eta \approx \frac{5}{20} = 25\%$$

For the case of a step-down regulator, assuming typical values of $V_D = 1$ V and $V_{\text{sat}} = 1.5$ V, one gets from Eq. (10.39)

$$\eta = \frac{5}{6} \frac{19.5}{20} = 81.25\%$$

which illustrates one of the most important features of switching regulators, namely, the efficient transfer of power.

10.9. PRACTICAL SWITCHING REGULATOR CIRCUITS

The basic control circuitry associated with a switching regulator system is readily suitable for monolithic integration. In terms of circuit implementation, this corresponds to the circuitry within the dashed area of Figure 10.25. Normally, a switching transistor capable of handling several hundred milliamperes of current is also incorporated into the chip. For high-power regulator applications, this internal transistor is used as a switch to activate an external high-current switching transistor.

At present a variety of monolithic switching regulator integrated circuits is available, which are designed to perform the basic control functions shown within the dashed area of Figure 10.25. These circuits often include overload protection circuitry to protect both the monolithic integrated circuit and the entire switching power supply system from permanent damage or burn-out under accidental overload or transient conditions. Many of these circuits also contain two switching transistors, rather than one, which can be used in push-pull switching systems such as the one shown in Figure 10.24a.

In this section, the basic architecture and performance characteristics of some

of these monolithic integrated circuits will be reviewed. The design examples are chosen because they represent widely accepted commercial products and because they also provide an excellent demonstration of some of the design considerations discussed in the earlier sections.

The two circuits which will be examined are the SG-1524 switching regulator control circuit introduced by Silicon General Corporation, and the μ A-78S40 switching regulator integrated circuit introduced by Fairchild Semiconductor. The first circuit operates on the pulse-width-modulation principle, the second one operates on a modified version of the constant-on-time, variable-frequency principle.

SG-1524 Pulse-Width-Modulating Regulator

The SG-1524 pulse-width-modulating regulator circuit, introduced by Silicon General Corporation in the mid-1970s, contains all of the necessary low-level detection and control circuitry for a switching regulator system.⁽¹⁶⁾ The functional block diagram of the SG-1524 switching regulator circuit is shown in Figure 10.31. The circuit is available in a 16-pin DIP package and, in addition

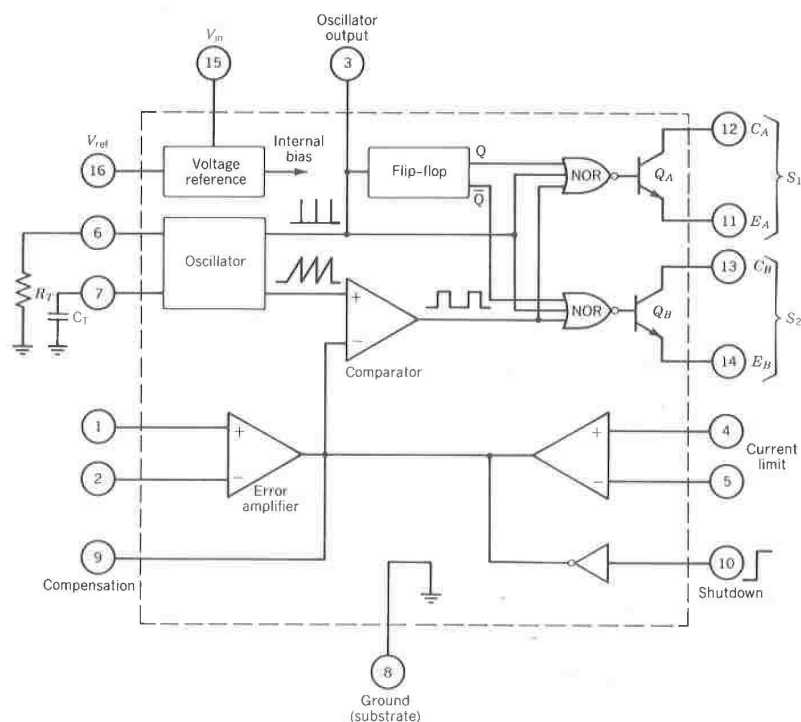


FIGURE 10.31. Functional block diagram of SG-1524 switching regulator.

to the control circuitry, also contains two switching output transistors Q_A and Q_B , each of which is designed to handle up to 100 mA of load current. These two output transistors can be used as independent alternating switches in push-pull systems (see Fig. 10.24a) or can be connected in parallel for driving single-ended output circuits.

As shown in Figure 10.31, the control circuitry is comprised of the following functional blocks:

1. Internal voltage reference.
2. Saw-tooth oscillator.
3. Voltage comparator.
4. Error amplifier.
5. Output driver logic.
6. Output switch transistors.
7. Overload protection and shutdown circuitry.

The operation of the overall circuit can be easily described in terms of the interconnection of these basic blocks. The internal voltage reference section is essentially a temperature-compensated Zener reference with a low-impedance buffered output. It provides a temperature-stabilized 5-V reference voltage and also biases all the rest of the internal oscillator and control circuitry.

The oscillator section is a linear ramp generating R - C oscillator. Its circuit configuration is similar to that shown in Figure 11.19. The Schmitt-trigger section of the oscillator uses a single-comparator-type sensing circuit as shown in Figure 11.15. The oscillator operates by charging an external capacitor C_T with a constant current from a lower threshold voltage V_A to an upper threshold voltage V_B . Once the linear ramp voltage across the capacitor reaches the upper threshold voltage, the capacitor is quickly discharged back to the lower threshold voltage, and the cycle repeats itself. The charging current for the capacitor is set by the external resistor R_T . By proper choice of the internal voltage threshold levels, the frequency of oscillation is set as

$$f_o \approx \frac{1}{R_T C_T} \quad (10.42)$$

The oscillator section produces two output waveforms: a linear ramp voltage across the timing capacitor C_T and a narrow positive pulse (typically on the order of a few microseconds) corresponding to the rapid discharge cycle of the timing capacitor. These two waveforms, which are basic to linear-ramp-type R - C oscillators, are shown as the top two waveforms in the timing diagrams of Figure 10.32 and serve two separate functions.

The linear-ramp, or *saw-tooth*, waveform is compared with the filtered and amplified error voltage at the input of the comparator section, and is used to generate a variable-width pulse output from the comparator. Note that the width of the output pulse from the comparator is directly proportional to the error

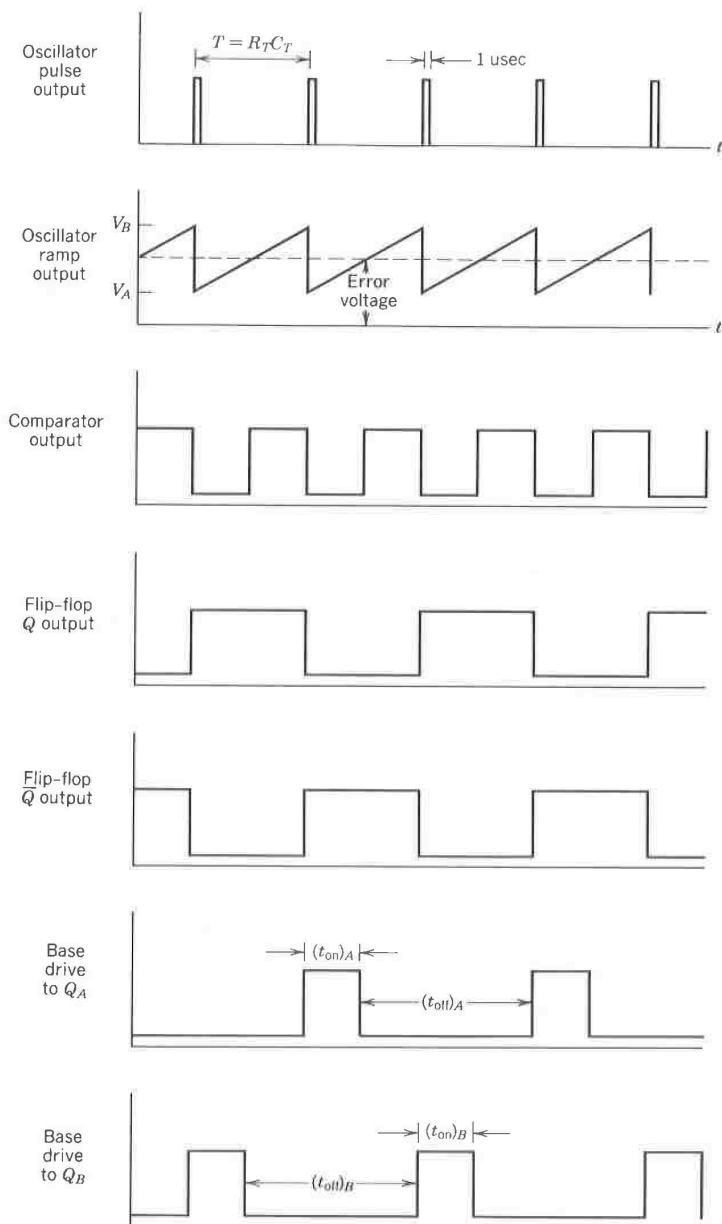


FIGURE 10.32. Oscillator and timing waveforms SG-1524 switching regulator.

voltage level at the comparator input, as indicated by the timing diagram of Figure 10.32. The narrow positive output pulse from the oscillator is used as a timing signal to the output-driver logic section.

The output-driver logic is comprised of an R - S flip-flop and a set of NOR gates which drive the two parallel output-switch transistors Q_A and Q_B . The flip-flop is set and reset alternately by the narrow timing pulse from the oscillator output, and alternately enables one or the other of the two NOR gates. The narrow-pulse output of the oscillator is also directly applied to the output NOR gates, and serves as a blanking pulse to ensure that there is no possibility of having both outputs on simultaneously during transitions. In this manner, the output-driver logic section steers the variable-width output pulse from the voltage comparator alternately to one or the other of the two output transistors, as shown in Figure 10.32.

The two output transistors Q_A and Q_B are identical transistors with both the collector and emitter terminals of each device left uncommitted. Figure 10.33 shows the typical internal circuit configuration for one of these output switch transistors. The output peak-current capability is limited to approximately 100 mA by means of the active current-limit circuit made up of the sensing resistor R_{SC} and the transistor Q_3 . The diode D_1 , along with the lateral pnp transistor Q_2 , serve as antisaturation clamps to keep Q_A out of deep saturation and to improve its switching response. Note that the output transistor Q_A is activated only when all three digital signals appearing at the base of Q_1 are at low state.

The error amplifier section is basically a single-stage transconductance amplifier with a 200- μ A full-scale output current capability. Its output is directly connected to the inverting input of the comparator. The output of the error

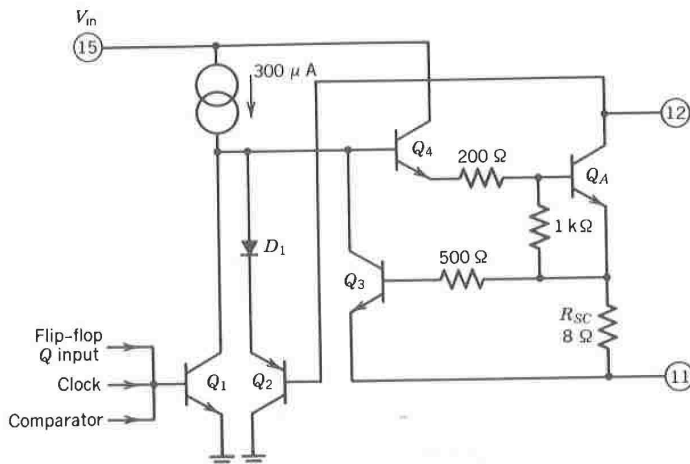


FIGURE 10.33. Current-limited output switch transistor stage of SG-1524 switching regulator. (Note: One of two outputs shown only.)

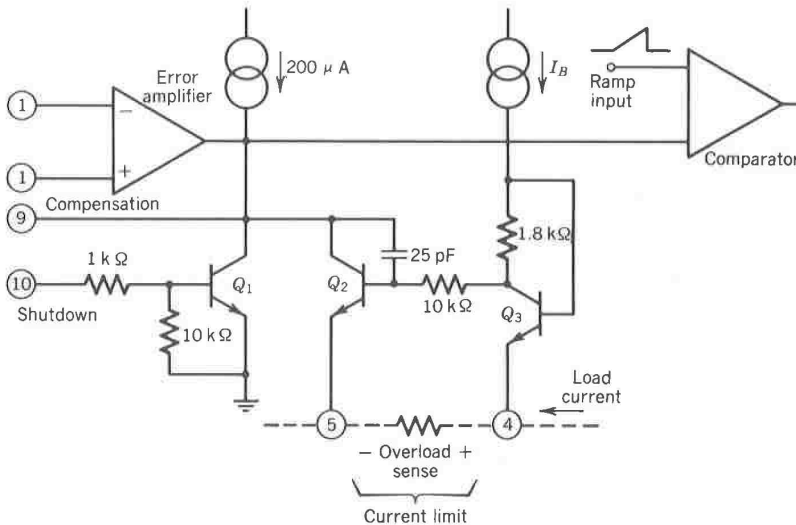


FIGURE 10.34. Overload current-limit and shutdown circuit of SG-1524 switching regulator.

amplifier provides a convenient point in the circuit for shutdown control and overload protection, as shown in Figure 10.34. By shunting away the limited current drive ($\approx 200 \mu\text{A}$) available at the output of the error amplifier, this node can be pulled down to ground potential, which in turn shuts off the comparator output, reduces the output pulse width to zero, and keeps both output transistors in the off state. Both the shutdown amplifier Q_1 and the current-limit circuit, made up of Q_2 and Q_3 of Figure 10.34, operate on this principle. The current-limit amplifier has a temperature-compensated sensing threshold of 200 mV across its inputs, and is used for sensing the total current delivered to the load (see application circuits of Figs. 10.35 and 10.36). If the load current increases beyond a set threshold, due to either transient load changes or an accidental short circuit, the current-limit circuitry causes the output pulse width to decrease and, thus, limits the total current delivered to the load.

Another protection circuit often used in switching regulators is the so-called *soft-start* circuit, which ensures that the output pulse width starts from zero and builds up to its proper level gradually when the regulator is first powered up. This avoids sudden current surges into the output circuitry when the regulator is first activated and lets the output voltage build up to its operating value with a relatively slow transient (typically in several milliseconds or more).

The soft-start circuitry is not directly included in the SG-1524. However, it can be incorporated by connecting an external R - C network to the output of the error amplifier (pin 9) through a disconnect diode.⁽¹⁶⁾

The SG-1524 is designed to operate with supply voltages of 8–40 V. The entire circuit consumes less than 10 mA of quiescent current. Figures 10.35 and

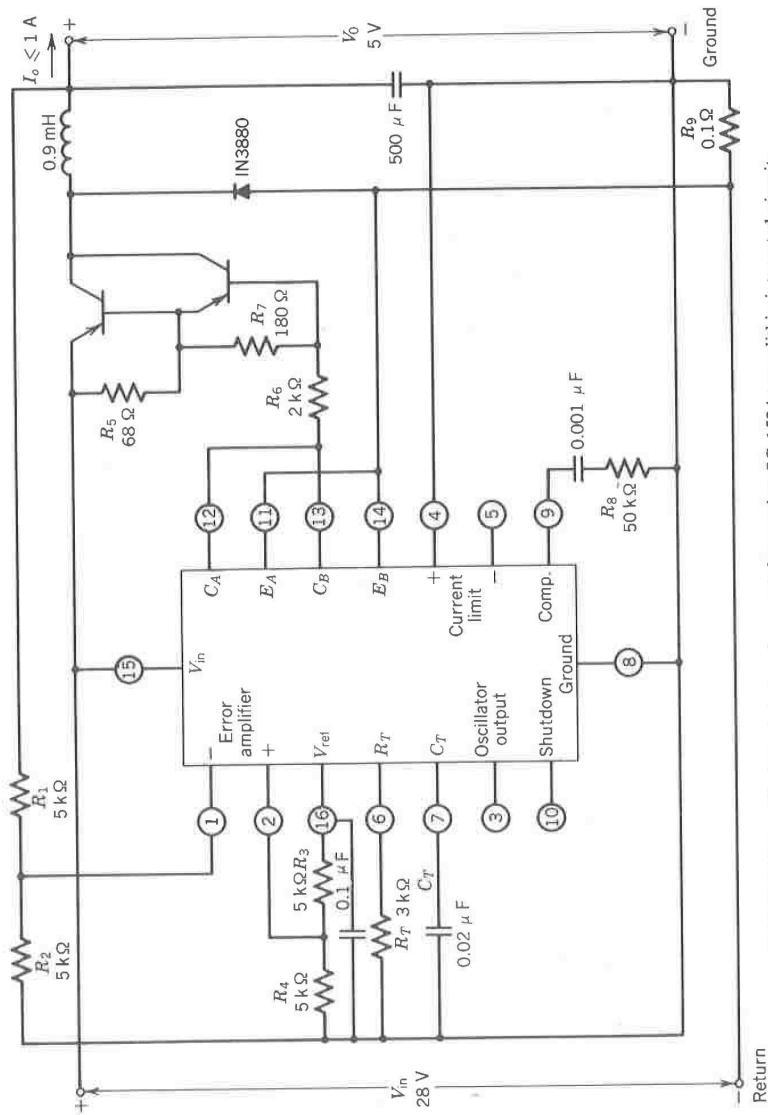


FIGURE 10.35. Single-ended step-down regulator using SG-1524 monolithic integrated circuit with external switch transistors. (Note: In the configuration shown, input = 28 V, output = 5 V, with $I_o < 1$ A.)

10.36 show some typical applications of the circuit, both as a single-ended and as push-pull type switching regulators.

Figure 10.35 shows the use of the SG-1524 in a 1-A single-ended switching regulator, with an external Darlington *pnp* transistor as a switch. This is basically a step-down type regulator configuration similar to that shown in Figures 10.25 and 10.28. The appropriate circuit terminals are identified in the figure. The two output transistors of the SG-1524 are connected in parallel by short-circuiting their collectors and emitters, and provide the switching signal to the external switch transistors. The output signal is fed back to the control circuit by the two sampling resistor R_1 and R_2 . In this particular configuration, the circuit is designed to generate a 5-V output from a 25-V input. Since the output level is comparable to the level of the internal voltage reference, both V_{ref} and the output are scaled down by resistive divider circuits made up of R_1 through R_4 before they are applied to the inputs of the error amplifier.

Figure 10.36 shows the application of the SG-1524 in a transformer-coupled push-pull dc-to-dc converter application. The basic circuit configuration is similar to that shown in Figure 10.24a and is designed to deliver a 5-V output with a 5-A drive capability from a 28-V input. The circuit uses external *nnp* switch transistors, driven in a push-pull manner from the emitters of the on-chip switch transistors. The input current limit to the transformer primary is set at approximately 2 A by the choice of the current-limit resistor. The feedback control loop is closed by sensing the output through the resistors R_1 and R_2 and comparing it to the internal reference voltage, which is divided down by the resistors R_3 and R_4 .

μ A-78S40 Switching Regulator

The μ A-78S40 switching regulator, introduced by Fairchild Semiconductor in 1978, is primarily intended for single-ended load circuits using the inductive switched regulator configurations shown in Figure 10.23. The circuit architecture for the μ A-78S40 is shown in Figure 10.37. Unlike the SG-1524 circuit described in the previous section, the μ A-78S40 operates in a modified version of the fixed-on-time, variable-frequency mode discussed in Section 10.6.

With reference to the block diagram of Figure 10.37, the principle of operation for the circuit can be described as follows. The oscillator section produces a constant stream of timing signals which are then gated through internal logic circuitry, and are used to turn the internal switch transistor Q_1 on and off. The oscillator frequency is determined by the choice of the external timing capacitor C_T and can be set to be anywhere in the range of 100 Hz to 100 kHz. In most applications, a frequency range of 20–30 kHz is used. The oscillator output is a fixed-duty-cycle pulse train, whose on-off time is fixed internally at a ratio of 6:1. This waveform is shown in Figure 10.38, along with other timing signals in the circuit. The high-gain comparator section of the circuit compares the filtered and scaled output voltage level with the 1.3-V internal reference and generates a gating signal which inhibits the oscillator output from reaching the

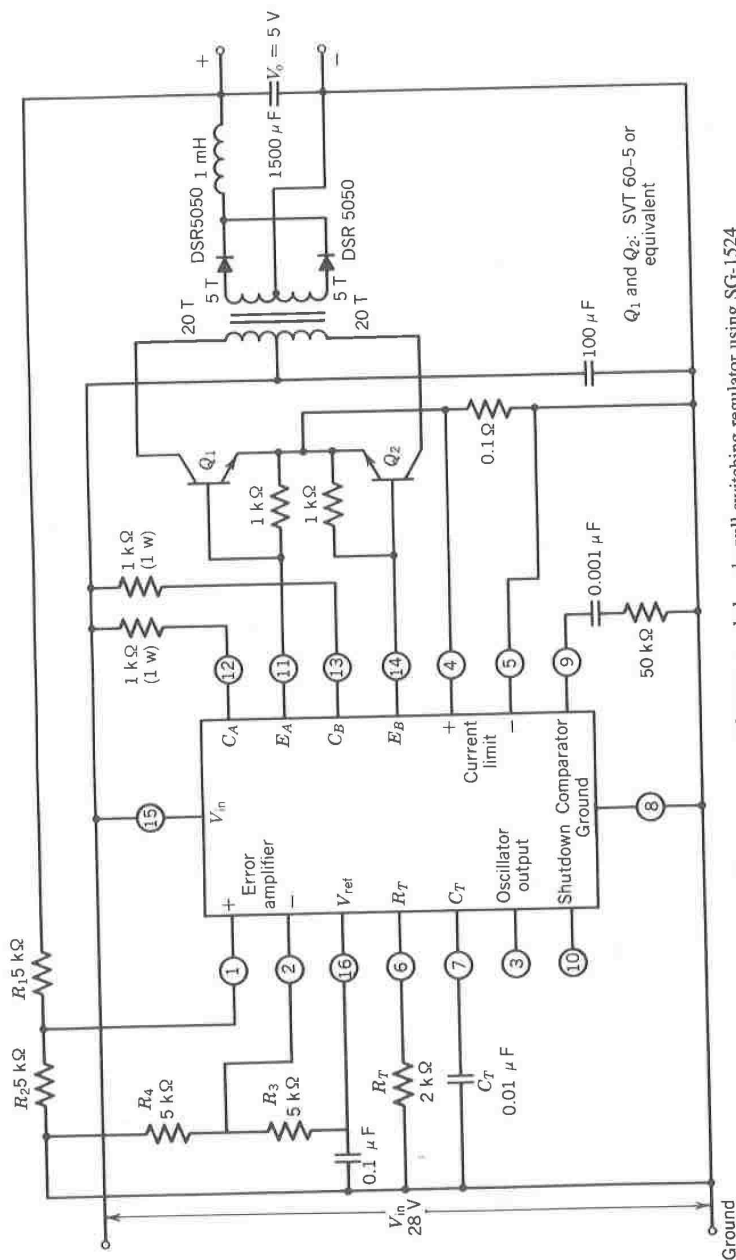


FIGURE 10.36. High-current transformer-coupled push-pull switching regulator using SG-1524 integrated circuit. ($V_{in} = 28$ V, $V_o = 5$ V, $I_o < 5$ A.)

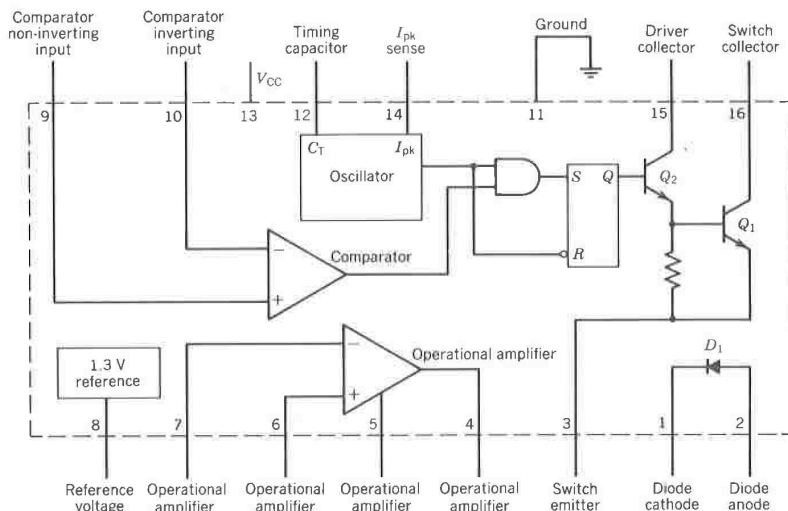


FIGURE 10.37. Functional block diagram of $\mu\text{A-78S40}$ switching regulator.

output transistors whenever the sampled or scaled output voltage is too high. In this manner, the drive to the output switch transistor is essentially an intermittent pulse train, which is occasionally interrupted or inhibited, as shown in Figure 10.38.

The on-chip Darlington switch transistor and the switch diode D_1 are both rated at 1.5 A peak current capability, with 40-V breakdown voltage, and have typical switching times of 500 nsec.⁽¹⁵⁾

The internal voltage reference circuit is a temperature-compensated band-gap reference. The operational amplifier section is a general-purpose 741-type operational amplifier with a power output stage which can source up to 150 mA or sink up to 35 mA. Although the operational amplifier is not used in implementing the basic regulator function, it is included on the chip as a general-purpose building block for auxiliary functions.

The overload protection is achieved by a current-sense circuit associated with the oscillator section. This current-sense circuit senses the total current drawn by the output switch transistor or the switching diode. If this current exceeds the rated limit, the current-sense circuit reduces the oscillator duty cycle, which in turn limits the peak current.

Figure 10.39 illustrates the operation of the $\mu\text{A-78S40}$ as a step-up voltage regulator operated in the circuit configuration of Figure 10.22b. In the circuit of Figure 10.39, the device is interconnected to generate a +15 V output voltage from a +5 V input. The output is sampled by resistors R_1 and R_2 and compared with the 1.3 V V_{ref} to maintain the regulation. The current-limit function is

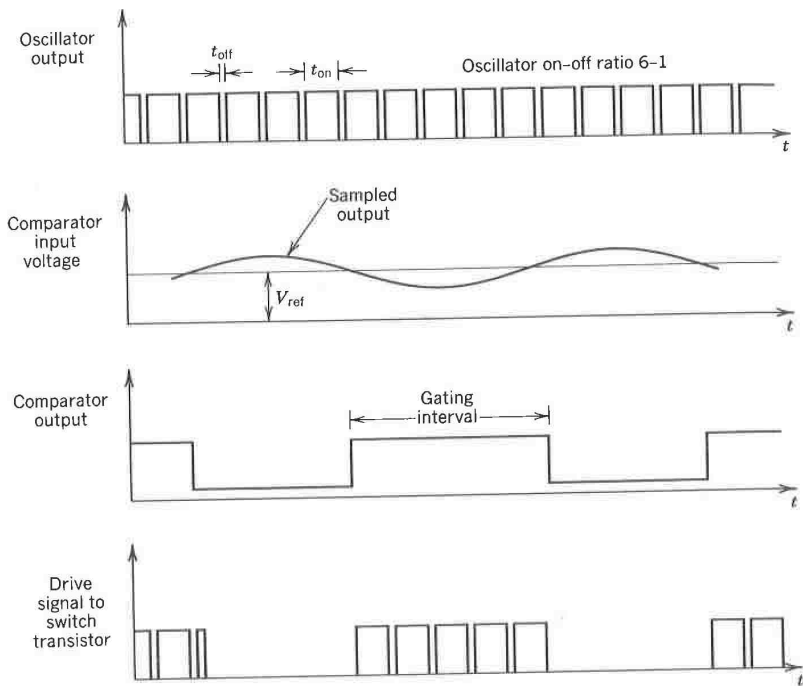


FIGURE 10.38. Timing waveforms for various sections of μA -78S40 switching regulator.

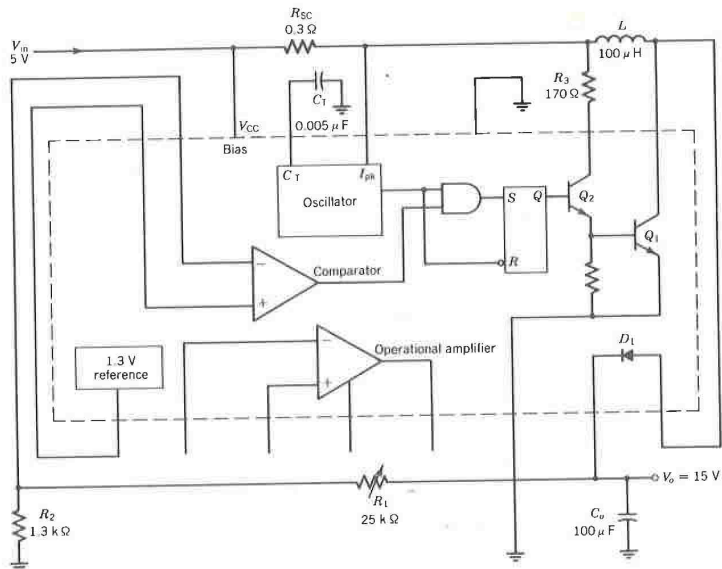


FIGURE 10.39. Operation of μA -78S40 as a 5 V to 15 V step-up regulator.

accomplished by sensing the total supply current delivered to the output circuitry by means of the voltage drop across the external resistor R_{SC} and reducing the oscillator duty cycle, if the rated current limit is exceeded. This protection circuit also functions as a *soft-start* circuit when the regulator is first powered up and limits the transient surge currents.

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