

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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WESTERN DIGITAL TECHNOLOGIES, INC.,  
Petitioner,

v.

VIASAT, INC.,  
Patent Owner.

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IPR2022-01171  
Patent 8,966,347 B2

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Before THU A. DANG, KEVIN F. TURNER, and  
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

### A. *Background and Summary*

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) seeking an *inter partes* review of claims 1–11 and 13–23 (the “challenged claims”) of U.S. Patent No. 8,966,347 B2 (Ex. 1001, “the ’347 Patent”). Viasat, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 12 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2022). An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

After considering the information presented in the Petition and the Preliminary Response, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing that at least one of the challenged claims is unpatentable, and we do not exercise our discretion to deny institution. Therefore, we grant institution of an *inter partes* review.

Our findings and conclusions below are based on the record developed thus far. This is not a final decision as to the patentability of any challenged claim. Any final decision will be based on the full record developed during trial.

### B. *Related Matters*

The parties identify the following district court case as a related matter: *Viasat, Inc. v. Western Digital Corp.*, No. 6:21-CV-01230-ADA (W.D. Tex.). Pet. 3; Paper 4, 1 (Patent Owner’s mandatory notices).

The '347 Patent is related to U.S. Patent No. 8,615,700 B2, which is being challenged by Kioxia Corporation and Kioxia America, Inc. in IPR2022-01067 and by Petitioner in IPR2022-01126.

*C. The '347 Patent (Ex. 1001)*

The '700 Patent was issued from an application filed August 18, 2010. Ex. 1001, code (22). Petitioner contends that the '700 Patent claims are not entitled to the August 18, 2009 filing date of the provisional application. *Id.* at code (60); Pet. 15–17. At this stage, Patent Owner does not dispute Petitioner's contention.

The '347 Patent discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57), 1:34–35, 2:29–30. The '347 Patent discloses a system having multiple error correction sub-modules and further discloses monitoring an error rate for data retrieved from flash memory and powering up additional error correction sub-modules to handle an increase in error rate. *Id.* at 1:35–52, 2:30–41.

An embodiment is shown in Figure 3, reproduced below.

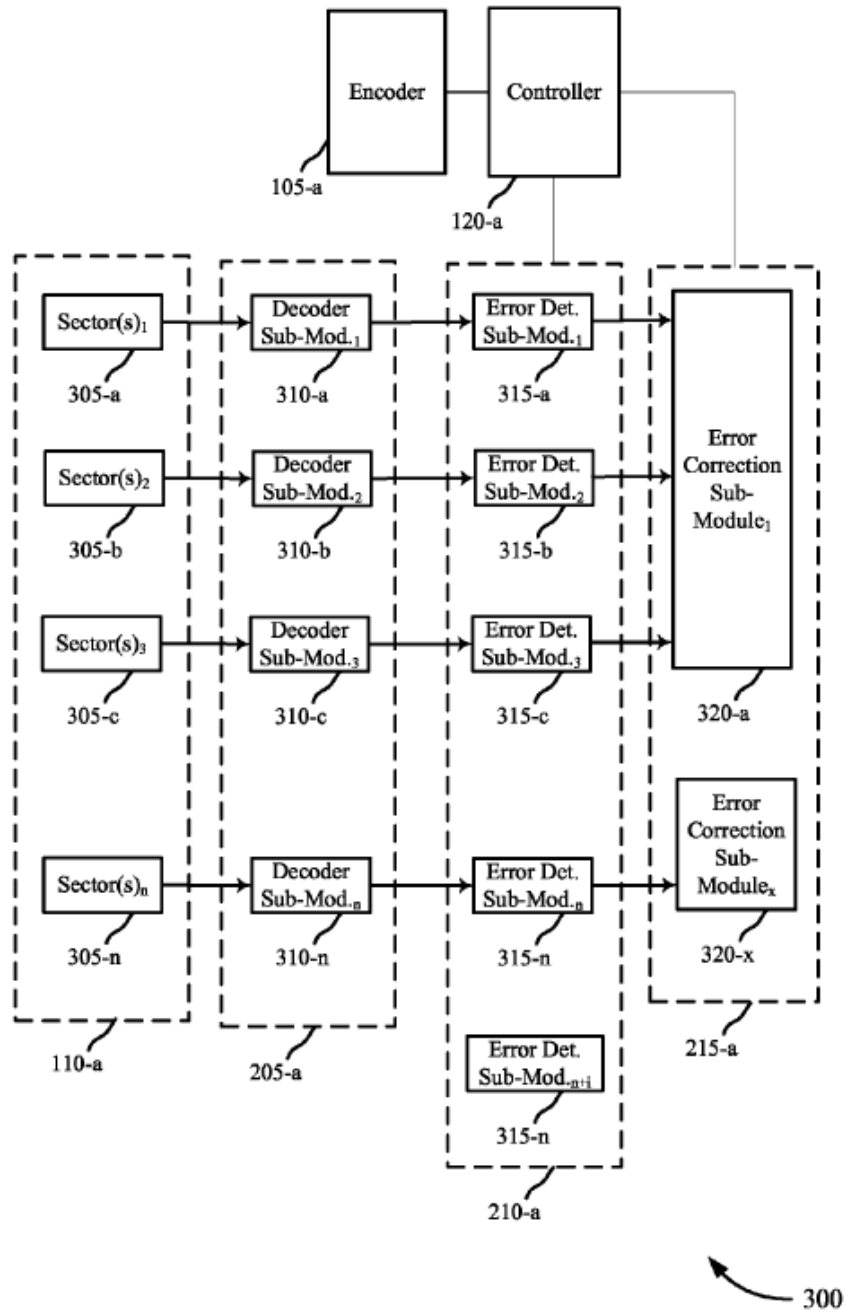


FIG. 3

Figure 3 “is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules.” Ex. 1001, 2:11–13, 6:31–34.

As shown in Figure 3, flash memory decoder system 300 includes encoder 105-a, flash memory 110-a, controller 120-a, decoder module 205-a, error detection module 210-a, and error correction module 215-a. Ex. 1001,

6:35–39. Encoder 105-a receives data to be stored and encodes the data for storage in the flash memory 110-a as encoded data. *Id.* at 3:48–50. Flash memory 110-a includes a number of different sets of one or more active sectors 305. *Id.* at 6:41–42. Decoder module 205-a includes a number of decoder sub-modules 310, each of which may be associated with a different set of sectors 305. *Id.* at 6:42–45. Error detection module 210-a includes a number of error detection sub-modules 315, each of which may be associated with a different set of sectors 305. *Id.* at 6:45–48.

According to the '347 Patent, each error detection sub-module 315 evaluates a data stream read from flash memory 110 to determine whether it contains an error and forwards the portion of the stream containing an error to error correction module 215-a. Ex. 1001, 6:63–7:2. Error correction module 215-a includes a number of error correction sub-modules 320, each of which handles errors from a number of error detection sub-modules 315 and corrects the portions of the data streams containing an error. *Id.* at 7:2–9.

The '347 Patent discloses that “controller 120-a may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-a.” Ex. 1001, 7:14–17. Controller 120-a monitors an age or error rate associated with each sector of flash memory 110-a, selectively powers-up one or more error correction sub-modules 320 to serve sectors 305 where the error rates exceed a threshold, and adapts the coding rate to be used by the encoder on a per sector basis. *Id.* at 7:17–28.

*D. Illustrative Claims*

Petitioner challenges claims 1–11 and 13–23 of the '347 Patent. Claims 1 and 13 are the only independent claims and are reproduced below with Petitioner's bracketed claim element designations added and paragraphs adjusted.

1. [a] A method comprising: encoding data using forward error correction coding;

[b] storing the encoded data in a flash memory;

[c] retrieving the encoded data stored in the flash memory to generate a data stream;

[d] processing, using at least a first error correction sub-module, the data stream to correct errors in the data stream associated with the flash memory;

[e] monitoring a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;

[f] determining that the monitored metric exceeds a threshold;

[g] in response to the determination, modifying the forward error correction coding for use in subsequently encoding data for storage in the flash memory; and

[h] in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.

Ex. 1001, 10:50–11:2; Pet. 31–44.

13. [a] A system comprising: an encoder to encode data using forward error correction coding;

[b] a flash memory to store the encoded data;

[c] a decoder to retrieve the encoded data stored in the flash memory to generate a data stream, and

[d] to process the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module; and

[e] a controller to: monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;

[f] determine that the monitored metric exceeds a threshold;

[g] in response to the determination, modify the forward error correction coding for use by the encoder in subsequently encoding data for storage in the flash memory; and

[h] in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.

Ex. 1001, 11:40–12:10; Pet. 71–73.

*E. Asserted Challenges to Patentability and Evidence*

Petitioner asserts the following challenge to patentability:

| Claims Challenged | 35 U.S.C. § <sup>1</sup> | Reference(s)/Basis                     |
|-------------------|--------------------------|----------------------------------------|
| 1–11, 13–23       | 103(a)                   | Diggs, <sup>2</sup> Cheng <sup>3</sup> |

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<sup>1</sup> The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the ’347 Patent has an effective filing date before that date, we refer to the pre-AIA version of § 103. Ex. 1001, code (63).

<sup>2</sup> Ex. 1004, US 2009/0070651 A1, published Mar. 12, 2009 (“Diggs”). Petitioner asserts that Diggs is prior art to the ’347 Patent under 35 U.S.C. § 102(b). Pet. 22.

<sup>3</sup> Ex. 1005, US 2009/0276570 A1, filed April 30, 2008 and published Nov. 5, 2009 (“Cheng”). Petitioner asserts that Cheng is prior art to the ’347 Patent under 35 U.S.C. § 102(a). Pet. 27–28.

Pet. 5. Petitioner submits the declaration of Lara Dolecek, Ph.D. Ex. 1003.

## II. DISCRETION UNDER 35 U.S.C. § 314(a)

Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 314(a) based on the *Fintiv* factors.

Prelim. Resp. 7–13. Prelim. Resp. 6–14; *see Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv I*”). Petitioner argues the opposite. Pet. 5–9.

### A. *Fintiv* Factors

In assessing whether to exercise discretion under *Fintiv*, the Board weighs the six non-exclusive factors. *Fintiv I* at 6. Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* A Memorandum from the Director provides “binding agency guidance” regarding how the Board’s discretion under 35 U.S.C. § 314(a) and the *Fintiv* factors apply to “sample fact patterns.” Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022) (“Interim Procedure”),<sup>4</sup> 3.

#### 1. *Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted*

Petitioner states that it intends to move for a stay of the parallel district court litigation “if the Board institutes this IPR proceeding.” Pet. 5.

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<sup>4</sup> Available at [https://www.uspto.gov/sites/default/files/documents/interim\\_proc\\_discretionary\\_denials\\_aia\\_parallel\\_district\\_court\\_litigation\\_memo\\_20220621\\_.pdf](https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf).

Patent Owner argues that the district court is unlikely to grant a stay.  
Prelim. Resp. 7–8.

There is no evidence that a stay has been requested or ordered in the parallel district court litigation. We decline to speculate on how the district court would rule on a stay, if one were requested. *Sand Revolution II, LLC v. Cont'l Intermodal Grp.-Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”) (declining to predict whether or not the district court would grant a stay, if requested); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (informative) (“*Fintiv IP*”) (explaining that factor 1 generally “does not weigh for or against discretionary denial” when neither party has requested a stay). Accordingly, this factor is neutral.

2. *Proximity of the Court’s Trial Date to the Board’s Projected Statutory Deadline*

Petitioner states that the district court has set a tentative trial date of October 2, 2023, but argues that circumstances make it “highly unlikely the actual trial will occur before the Board issues a final decision” and that the median time-to-trial for civil actions in the Western District of Texas demonstrate that “the tentative trial date is unrealistic.” Pet. 6–7. Patent Owner asserts that “[t]rial has been set . . . for October 2, 2023” in the parallel district court litigation and that “the median time to trial . . . would place trial around January 2024.” Prelim. Resp. 8–9.

In this *inter partes* review proceeding, the projected statutory deadline for a final written decision is December 2023. Based on the parties’ representations, it appears that trial in the parallel district court litigation may begin either shortly before or within a few months after the projected statutory deadline for a final written decision in this proceeding. Under

these circumstances, this factor weighs neither for nor against the exercise of discretion to deny institution.

3. *Investment in the Parallel Proceeding by the Court and Parties*

Petitioner states that, in the parallel district court litigation, “almost no discovery has occurred,” and “the district court has invested no time on the merits.” Pet. 8. Patent Owner states that the parties have exchanged preliminary infringement and invalidity contentions, initial document disclosures, and claim construction briefs; that claim construction briefing was completed in mid-September 2022; that fact discovery was scheduled to commence October 3, 2022; and that final infringement and invalidity contentions are due in November. Prelim. Resp. 10–11. According to a Scheduling Order entered in the parallel district court litigation on May 10, 2022, fact discovery closes May 1, 2023; expert discovery closes June 26, 2023; and dispositive motions are due July 10, 2023. Ex. 1019.

Based on the parties’ representations, it appears that much work remains to be done in the parallel district court litigation as it relates to invalidity: there is no claim construction order, fact discovery has just begun, expert reports are not yet due, there have been no fact or expert depositions, and substantive motion practice is yet to come. Pet. 8; Prelim. Resp. 10–11; *see Sand Revolution* at 11. Thus, although the parties and the district court have invested some effort in the parallel district court litigation, the bulk of the work to prepare the invalidity case for trial is yet to be done.

We also acknowledge Petitioner’s diligence in filing the Petition less than 7 months after Patent Owner filed the complaint in the parallel district court litigation. Pet. 7; Ex. 1010.

Under these circumstances, we determine that this factor weighs slightly against exercising our discretion to deny institution.

4. *Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

Petitioner states that, “if the Board institutes here, Petitioner will stipulate that it will not pursue invalidity on the same grounds in district court.” Pet. 8.

Patent Owner asserts that Petitioner’s district court invalidity contentions rely on the art presented in the Petition. Prelim. Resp. 11. Patent Owner criticizes Petitioner for not providing a *Sotera*-style stipulation that covers grounds that could have reasonably been raised in the Petition, including the grounds raised in the Kioxia petition. *Id.* at 1–2, 11–12; *see Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A) (“*Sotera*”).

The Interim Procedure states, “Consistent with *Sotera Wireless, Inc.*, . . . the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure, 3 (footnote omitted; citing *Sotera*). In other words, under the Interim Procedure, a petitioner may avoid discretionary denial of the petition based on a parallel district court litigation by providing a *Sotera*-style stipulation. The Interim Procedure does not, however, make a *Sotera*-style stipulation a prerequisite for institution. Under our informative precedent, an *inter partes* review may be instituted despite the absence of a *Sotera*-style stipulation. *Sand Revolution* at 12 n.5 (instituting *inter partes* review notwithstanding the

absence of a stipulation not pursue any ground that could have been reasonably raised in an *inter partes* review).

We find that Petitioner’s stipulation (Pet. 8) is the same as the one in *Sand Revolution*, where the petitioner stipulated that, if the IPR is instituted, the petitioner will not pursue the same grounds in the district court litigation. *Sand Revolution* at 11–12. In that case, the panel held that petitioner’s stipulation “mitigates to some degree the concerns of duplicative efforts between the district court and the Board as well as concerns of potentially conflicting decisions” and that *Fintiv* factor 4 “weighs marginally in favor of not exercising discretion to deny institution.” *Id.* at 12.

Consistent with our informative precedent in *Sand Revolution*, we find that this factor weighs marginally against exercising discretion to deny institution under 35 U.S.C. § 314(a).

5. *Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party*

The Petitioner here is a defendant in the parallel district court litigation, and, thus, this factor weighs in favor of exercising our discretion to deny institution under § 314(a). *Fintiv II* at 15 (“Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.”).

6. *Other Circumstances that Impact the Board’s Exercise of Discretion, Including the Merits*

Petitioner argues that the asserted grounds are “especially strong.” Pet. 9. Patent Owner contends that the merits are “not strong,” asserting that it “identifies multiple weaknesses related to every ground and every independent claim that the Petition challenges.” Prelim. Resp. 13.

According to the Interim Procedure, “*Fintiv* factor six reflects that the PTAB considers the merits of a petitioner’s challenge when determining whether to institute a post-grant proceeding in view of parallel district court litigation.” Interim Procedure, 4. The Interim Procedure requires us to determine whether the information presented at the institution stage (1) “is merely sufficient to meet the statutory institution threshold” or (2) “presents a compelling unpatentability challenge.” *Id.* at 4–5. In the first case, we have “the authority, where warranted, to exercise discretion to deny institution in view of the other *Fintiv* factors,” and in the second case, we do not have such authority. *Id.*

Here, for the reasons discussed below, we determine that the information presented is sufficient to meet the statutory threshold, but does not present a compelling unpatentability challenge. Therefore, consistent with the Interim Procedure, *Fintiv* factor six is neutral.

### *B. Balancing the Fintiv Factors*

After considering the circumstances and facts before us in view of the *Fintiv* factors and the Interim Procedure, we determine that the circumstances presented here do not support exercising our discretion under § 314(a) to deny institution.

## III. REASONABLE LIKELIHOOD UNDER 35 U.S.C. § 314(A)

### *A. Legal Standards*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the

grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

*B. Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSA”) would have had “at least a [bachelors of science degree] in electrical engineering or computer science or a related field, and four years’ experience designing, developing, or researching forward error correction (‘FEC’) or error correction coding (‘ECC’) systems.” Pet. 21 (citing Ex. 1003 ¶¶ 23–25). Petitioner states that “a higher education or skill level might make up for less experience, and vice-versa.” *Id.*

For purposes of the preliminary response, Patent Owner does not dispute Petitioner’s definition of a POSA. Prelim. Resp. 7.

For purposes of this Decision, we apply Petitioner’s articulation of the level of ordinary skill in the art, which is consistent with the level of skill in the art at the time of the invention as reflected in the asserted prior art.

*C. Claim Construction*

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting

*Vivid Techs., Inc. v. Am. Sci. Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Neither party seeks express constructions of any claim terms. *See* Pet. 21; *see generally* Prelim. Resp. We do not need to provide an express construction for any claim terms for purposes of this Decision.

#### *D. Petitioner's Challenge*

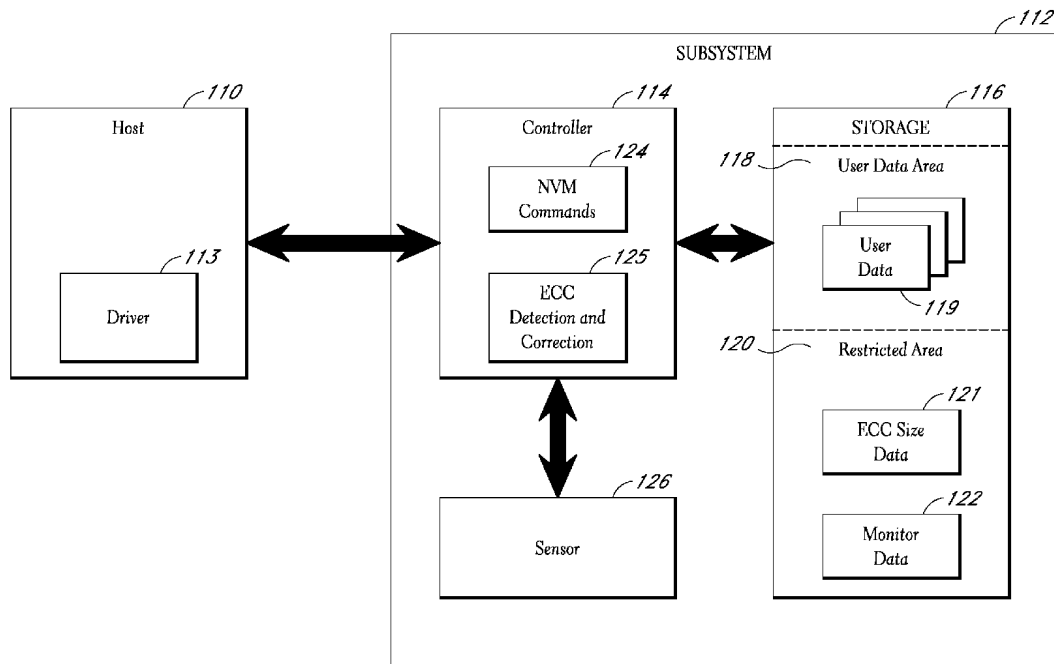
Petitioner challenges claims 1–11 and 13–23 as unpatentable and obvious based on Diggs and Cheng. Pet. 31–73. Patent Owner opposes. Prelim. Resp. 13–40. We provide an overview of the references before turning to our analysis, which focuses on the disputed issues.

##### *1. Diggs (Ex. 1004)*

Diggs discloses a storage subsystem that monitors one or more conditions, such as the rate at which ECC errors are detected on read operations, and adjusts an error correction setting based on the monitored conditions. Ex. 1004, code (57), ¶ 7. According to Diggs, “[w]hen the monitored condition or conditions reveal an increased probability of data errors, the ECC level and thus the quantity of ECC data generated is increased, increasing the level of protection against data errors.” *Id.* ¶ 7.

Figure 1 of Diggs is reproduced below.

FIG. 1



Diggs Figure 1 is a block diagram illustrating host system 110 linked to solid-state storage subsystem 112, which is “capable of automatically adjusting ECC settings.” Ex. 1004 ¶¶ 11, 17. Storage subsystem 112 includes controller 114, storage array 116, and sensor 126. *Id.* ¶¶ 18, 28. Controller 114 is configured with non-volatile memory (“NVM”) commands 124 for writing data to, and reading data from, storage array 116 in response to data and instructions received from host system 110. *Id.* ¶¶ 21, 22. Controller 114 further includes ECC detection and correction module 125, which performs encoding and decoding operations. *Id.* ¶ 23.

Storage subsystem 112 implements multiple ECC levels or settings, where a relatively high ECC level (more ECC bits per unit data) corresponds to a relatively high capacity to detect and correct errors. Ex. 1004 ¶ 24. Sensor 126 transmits data/signals indicative of sensed environmental conditions, such as temperature, humidity, altitude, or movement. *Id.* ¶ 28.

Controller 114 stores these data/signals in storage array 116 as monitor data 122. *Id.* ¶¶ 28, 29. Other types of monitor data 122 include parameters that may be sensed or generated by controller 114, such as data descriptive of how frequently ECC errors are detected. *Id.* ¶ 29. Controller 114 accesses and analyzes monitor data 122 to select the appropriate ECC settings for encoding data. *Id.* ¶ 30. When writing encoded user data 119 to storage array 116, ECC module 125 also stores ECC size data 121, which indicates the error correction setting used to encode the user data. *Id.* ¶ 33. When a block of user data 119 is read by controller 114 and processed by ECC module 125, ECC size data 121 is read to determine the appropriate error correction setting to use for decoding the accessed data. *Id.*

2. *Cheng (Ex. 1005)*

Cheng discloses methods for maintaining the performance of memory systems until end-of-life. Ex. 1005 ¶ 1. Cheng explains that “flash memory [has] endurance limits, and as a memory approaches its end-of-life (‘EOL’), degradation of the floating-gate transistors leads to an increase in the number of data errors.” *Id.* ¶ 18. According to Cheng, “as the number of errors increases, latencies are introduced as more time and system resources are spent on correcting these errors, which contributes to the overall degradation of the memory performance.” *Id.*

Figure 1 Cheng is reproduced below.

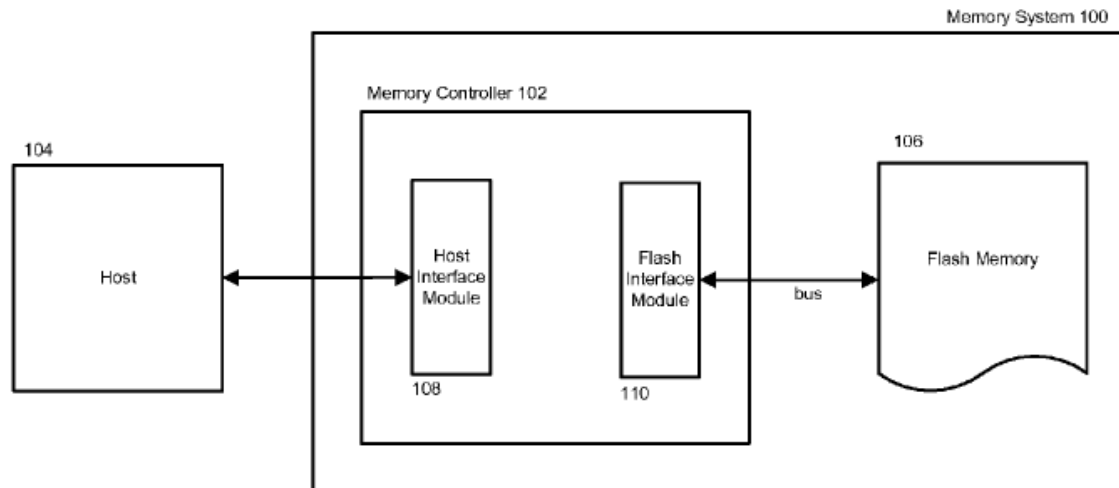


**FIG. 1**

Cheng Figure 1 shows memory system 100, including memory controller 102, which interfaces with host 104 and flash memory 106.

Ex. 1005 ¶¶ 9, 13.

Figures 2 and 3 of Cheng show alternative embodiments of memory controller 102 of Figure 1. *Id.* ¶¶ 10, 11, 19, 22. The Figure 2 embodiment includes error correction code (“ECC”) circuit 206, and the Figure 3 embodiment includes ECC circuits 206 and 208. *Id.* ¶¶ 7, 19, 22, Figs. 2, 3. Both embodiments include a flash interface module (“FIM”), which detects data errors “on the fly” during the process of transferring data between the memory controller and the flash memory. *Id.* ¶ 21, Figs. 2, 3.<sup>5</sup> In both embodiments, the FIM and ECC circuit(s) are driven by separate clock signals. *Id.* ¶¶ 20, 22, Figs. 2, 3. Referring to the Figure 2 embodiment, Cheng discloses:

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<sup>5</sup> In Cheng Figures 2 and 3, the flash interface module is labeled with reference numeral 110, but the written description identifies the flash interface module with reference numeral 216. Ex. 1005 ¶¶ 19–21, Figs. 2, 3.

The frequency of these clock signals can be adjusted. For example, if the ECC circuit 206 encounters a large number of data errors, its clock signal frequency can be increased such that it can operate at a faster rate. Similarly, the clock signal frequency for FIM 216 can be increased to speed up the bus connecting the module with the flash memory array.

*Id.* ¶ 20. Referring to the Figure 3 embodiment, Cheng discloses:

ECC circuit 206 can serve as the primary ECC circuit and ECC circuit 208 can serve as a supplemental ECC circuit. The supplemental ECC circuit can be enabled as the impact of error correction activity on the memory system increases. When the supplemental ECC engine is enabled, both ECC engines can be operated in parallel to complete the necessary error correction tasks faster. The speed at which each ECC engine operates can also be tuned independently by adjusting each ECC engine's clock signal frequency.

*Id.* ¶ 22.

### 3. *Claim 1*

Petitioner contends that Diggs discloses all elements of claim 1, except for element [h]. Pet. 31–49. For claim element 1[d], Petitioner contends that “a first error correction sub-module” corresponds to Diggs’ ECC module 125. Pet. 39. For claim element 1[h], which recites “a second error correction sub-module arranged in parallel with the first error correction sub-module,” Petitioner contends that “modifying Diggs to include this limitation would have been obvious in view of Cheng.” Pet. 44. According to Petitioner, a “POSA would . . . have found it obvious, and beneficial, to incorporate Cheng’s second ECC circuit into Diggs’ ECC module 125 as a ‘second error correction sub-module’ in parallel with Diggs[’] existing ECC decoding module, *i.e.*, the claimed ‘the first error correction sub-module.’” Pet. 47. Petitioner contends that “a POSA would have found the use of a second error correction sub-module, as taught by

Cheng, advantageous to reduce processing time and, thereby avoid reductions in the operation speed of the memory system and extend the operational lifetime of the memory system.” Pet. 48.

Patent Owner argues that Diggs’ ECC detection and correction module 125 is not a “first error correction sub-module,” as recited in claim element 1[d], and Petitioner does not propose any combination or modification that converts Diggs’ ECC detection and correction module 125 into the recited first error correction sub-module. Prelim. Resp. 13–20. Alternatively, Patent Owner argues that Petitioner’s combination of Diggs and Cheng lacks “any reasoned explanation for why and how these two references should be combined in the way Petitioner argues.” *Id.* at 20. According to Patent Owner, “Petitioner never analyzes how the disparate components from the two references would be combined; it merely assumes without explanation that they would work together.” *Id.* at 21.

After considering the parties’ arguments and evidence, we determine that, for purposes of institution, Petitioner makes a sufficient showing for claim 1 based on Diggs and Cheng. We are persuaded that Petitioner’s identification of Diggs’ ECC module 125 as “a first error correction sub-module” is sufficient for purposes of institution. Pet. 39. Patent Owner argues that “modules and sub-modules are not the same thing” and directs us to Figure 3 of the ’347 Patent, which shows two error correction sub-modules 320-a and 320-x within error correction module 215. Prelim. Resp. 16–18 (citing Ex. 1001 Fig. 3, 5:49–7:28). In contrast to the written description, however, the claims of the ’347 Patent do not recite both an error correction module and an error correction sub-module. Instead, claim 1 recites a “first error correction sub-module” and a “second error correction sub-module.” Ex. 1001, 10:55–56, 10:67–11:2. Petitioner

identifies Diggs' ECC module 125 as a "first error correction sub-module" and Cheng's second ECC circuit as a "second error correction sub-module," which is sufficient for purposes of institution. Pet. 39, 47.

After considering Patent Owner's arguments, we are also persuaded that, for purposes of institution, Petitioner provides a sufficient explanation for why and how the teachings of Diggs and Cheng would have been combined. As for the "why" aspect of the explanation, Petitioner states that adding a second error correction sub-module would have "compensate[d] for Diggs['] longer processing time associated with higher ECC levels" and would have been "advantageous to reduce processing time and, thereby avoid reductions in the operation speed of the memory system and extend the operational lifetime of the memory system." Pet. 48 (citing Ex. 1003 ¶ 134). As for the "how" aspect of the explanation, Petitioner states that states that a POSA would have "incorporate[d] Cheng's second ECC circuit into Digg's ECC module 125 as a 'second error correction sub-module' in parallel with Diggs['] existing ECC decoding module." Pet. 47. Petitioner also suggests that the combination could have been implemented as one or more Application Specific Integrated Circuits ("ASICs"). Pet. 48.

After considering Patent Owner's arguments, we are also persuaded that, for purposes of institution, Petitioner provides a sufficient explanation of how the components from Diggs and Cheng would have worked together. Petitioner contends that

A POSA would also have found it obvious, and beneficial . . . to power-on and use this second error correction sub-module for subsequent data stream processing when the monitored metric exceeds a threshold, i.e., when a higher ECC level is needed for reading and writing to memory and the computational burden of error correction activity on the memory system increases.

Pet. 47 (citing Ex. 1003 ¶ 132; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22).

Patent Owner argues there is a “mismatch” between Diggs’ ECC module 125, which is responsible for both error detection and correction, and Cheng’s ECC circuit 206, which Patent Owner asserts is responsible only for error correction, not error detection. Prelim. Resp. 22, 25. In Cheng’s Figure 2 and 3 embodiments, error detection is performed by “FIM 216,” and “[i]f errors are detected, [then] ECC circuit 206 could be utilized to correct such errors.” Ex. 1005 ¶ 21. We note, however, that Cheng also discloses “an error detection and correction code (ECC) circuit,” that detects and corrects errors. *Id.* at claims 3, 9, 18, 22.

In any event, we are persuaded that, for purposes of institution, Petitioner provides a sufficient explanation of how a POSA would have combined the teachings of Diggs and Cheng. Pet. 47–49. Patent Owner is correct that the Petition does not specify where error detection would take place and does not specify how or whether Cheng’s independent clock signals would be implemented in the combination. Prelim. Resp. 22–23, 25–26. Although the Petition would have been stronger if it had addressed error detection and clock signals, Petitioner’s explanation is sufficient for purposes of institution. The parties are invited to address these issues in more detail during trial to the extent permitted under the rules. 37 C.F.R. § 42.23(b); Consolidated Trial Practice Guide November 2019 (“CTPG”)<sup>6</sup> at 73–75.

#### 4. *Claim 13*

Petitioner relies on the same analysis for claim 13 as it presents for claim 1. Pet. 71. In addition, Petitioner contends that “the ‘decoder’ of

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<sup>6</sup> Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

limitations 13[c]-13[d] and the ‘controller’ of limitation 13[e]-13[h] are disclosed by Diggs’ controller 114 as modified by Cheng.” *Id.*

Patent Owner relies on the same arguments for claim 13 as it presents for claim 1. Prelim. Resp. 27. In addition, Patent Owner argues that Petitioner ignores claim 13’s structural limitations and does not demonstrate how Diggs teaches an encoder or a decoder that performs the functions recited in claim elements 13[a], [c], and [d] and does not explain how the combination of Diggs and Cheng includes a controller that performs the function recited in claim element 13[h]. *Id.* at 28–39.

After considering the parties’ arguments and evidence, we determine that, for purposes of institution, Petitioner makes a sufficient showing for claim 13 based on Diggs and Cheng.

Regarding an “encoder,” there is no dispute at this stage that Diggs discloses the function “to encode data using forward error correction coding,” as recited in claim element 13[a]. Petitioner identifies Diggs’ controller 114 and ECC module 125 as performing this function. Pet. 32 (citing Ex. 1004 ¶ 23). Diggs paragraph 23 discloses in part:

The controller 114 further includes an ECC detection and correction module 125. During write operations, the ECC detection and correction module 125 (hereinafter “ECC module”) uses a currently-selected ECC level or method to generate ECC values for the write data received from the host. As is conventional, these ECC values are stored in conjunction with the data to which they correspond. The process of generating and storing ECC values is referred to as “encoding,” and the process of performing ECC checking and correcting is referred to as “decoding.”

Ex. 1004 ¶ 23. Patent Owner argues that “claim 13 requires both an encoder and a decoder, but Petitioner does not specify where one ends and the other begins in Diggs’ ECC module 125.” Prelim. Resp. 29.<sup>7</sup>

We observe that, although Petitioner does not identify a particular portion of Diggs’ controller 114 or ECC module 125 called an “encoder,” the absence of the express words of the claim in the prior art is not fatal to the Petition. On this record, it appears to be undisputed that Diggs’ ECC module 125 performs the recited function of an “encoder.” As Patent Owner acknowledges, Diggs discloses that “[a]lthough depicted as a single module or unit in FIG. 1, the ECC module 125 may include one module or circuit that handles ECC encoding, and another module or unit that handles ECC decoding.” Ex. 1004 ¶ 27; Prelim. Resp. 16; *see also* Pet. 62 (relying on this disclosure in Diggs for dependent claim 9).

Regarding a “decoder,” there is no dispute at this stage that Diggs discloses the function “to retrieve the encoded data stored in the flash memory to generate a data stream,” as recited in claim element 13[c]. Petitioner identifies Diggs’ controller 114 as performing this function. Pet. 37–38 (citing Ex. 1004 ¶¶ 34, 40, 41). Patent Owner argues that Petitioner “nowhere identifies a *decoder*” and “it is actually Diggs’ controller, not its decoder, that is responsible for data retrieval.” Prelim. Resp. 31. According to Patent Owner, Petitioner does not explain what part of Diggs’ controller 114 is the decoder, and Diggs does not disclose that a decoder retrieves encoded data. *Id.* at 33.

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<sup>7</sup> When quoting the Preliminary Response, we omit Patent Owner’s italicization of reference names.

Again, although Petitioner does not identify a particular portion of Diggs' controller 114 called a "decoder," the absence of the express words of the claim in the prior art is not fatal to the Petition. On this record, it appears to be undisputed that Diggs' controller 114 performs the data retrieval function of a "decoder." *See* Ex. 1004 ¶ 21 ("controller 114 is configured to . . . read data from . . . storage array 116"). Controller 114 includes ECC module 125, which may include a "module or unit that handles ECC decoding." Ex. 1004 ¶ 27. Although data retrieval and ECC decoding are performed by different parts of Diggs' controller 114, we are persuaded that Petitioner's identification of controller 114 as a "decoder" that retrieves data is sufficient for purposes of institution. Pet. 37–38, 71.

Regarding claim element 13[d], Petitioner identifies Diggs' ECC module 125 as corresponding to a "a first error correction sub-module." Pet. 39. Patent Owner argues that Petitioner fails to identify any error correction sub-module, cross-referencing its arguments about claim 1. Prelim. Resp. 36. We have addressed Patent Owner's arguments in the preceding subsection.

Regarding claim element 13[h], there is no dispute at this stage that Cheng discloses the function of "powering-up, from an inactive mode, a second error correction sub-module." *See* Ex. 1005 ¶ 22. Petitioner identifies "Diggs' controller 114 as modified by Cheng" as the recited "controller" that performs this function. Pet. 71; *see also* Pet. 47–48 (discussing modification of Diggs in view of Cheng). Patent Owner argues that "the Petition has no explanation of which part of controller 114 constitutes the claim 13 'controller' versus the 'decoder'" and does not explain "what from Diggs would power up the second error correction sub-module." Prelim. Resp. 38.

After considering Patent Owner’s arguments, we are persuaded that Petitioner’s contentions regarding the combination of Diggs and Cheng for claim element 13[h] are sufficient for purposes of institution. We understand Petitioner to contend that it would have been obvious to modify Diggs’ controller 114 to perform the function of “powering-up, from an inactive mode, a second error correction sub-module.” Pet. 47–48, 71. At this stage, we do not view Petitioner’s reliance on a single numbered element in the prior art (Diggs’ controller 114, as modified in view of Cheng) to teach multiple elements in claim 13 (encoder, decoder, controller) as an unsurmountable hurdle, particularly in view of Diggs’ disclosure that controller 114 includes sub-components, including NVM commands 124 and ECC module 125, and may comprise multiple distinct devices. Ex. 1005 ¶¶ 21–23, 27, Fig. 1. Also relevant is the ’347 Patent’s disclosure that the encoder, decoder, and controller “may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) . . . [or] by one or more other processing units (or cores), on one or more integrated circuits.” Ex. 1001, 3:34–40. The parties are invited to address this issue in more detail during trial including with citations to applicable case law.

5. *Claims 2–11 and 14–23*

Claims 2–11 depend, directly or indirectly, from claim 1, and claims 14–23 depend, directly or indirectly, from claim 13. Petitioner contends that the additional limitations of dependent claims 2–10 are disclosed by Diggs, and that the additional limitation of dependent claim 11 would have been obvious in view of Diggs and Cheng. Pet. 49–70. Claims 14–23 recite the same limitations as method claims 2–11, except in system form, and

Petitioner relies on the same arguments and evidence for claims 14–23 as it presents for claims 2–11. Pet. 73. At this stage, Patent Owner does not present arguments for dependent claims 2–11 separate from its arguments for independent claim 1. For dependent claims 14–23, Patent Owner argues that Petitioner does not specify the prior art structure that performs the functions recited in the claims. Prelim. Resp. 39–40.

The guidance we provide above regarding claim 13 is also relevant to dependent claims 14–23. In view of our determinations for independent claims 1 and 13, as discussed above, it is not necessary for us to provide additional claim-by-claim analysis for the dependent claims at this stage.

#### IV. CONCLUSION

After considering the Petition and the Preliminary Response, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that at least one of claims 1–11 and 13–23 of the '347 Patent is unpatentable based on Diggs and Cheng. Accordingly, we institute an *inter partes* review of all challenged claims on all grounds asserted in the Petition. 37 C.F.R. §§ 42.107(e), 42.108(a). *See* Guidance on the Impact of SAS on AIA Trial Proceedings (April 26, 2018);<sup>8</sup> *see also SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018).

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<sup>8</sup> Available at <https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial>.

V. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims of claims 1–11 and 13–23 of the '347 Patent is instituted commencing on the entry date of this Decision; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial.

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