

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

VIASAT, INC.,
Patent Owner.

IPR2022-01171
Patent 8,966,347 B2

Before THU A. DANG, KEVIN F. TURNER, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

ROESEL, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. *Background and Summary*

Western Digital Technologies, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) seeking an *inter partes* review of claims 1–11 and 13–23 (the “challenged claims”) of U.S. Patent No. 8,966,347 B2 (Ex. 1001, “the ’347 Patent”). Viasat, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 12 (“Prelim. Resp.”). We instituted an *inter partes* review. Paper 13 (“Institution Decision” or “Inst. Dec.”).

After institution, Patent Owner filed a Patent Owner Response (Paper 16, “PO Resp.”), Petitioner filed a Reply (Paper 25, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 27, “PO Sur-reply”). We held an oral hearing on September 27, 2023, and a transcript is in the record. Paper 32 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that the challenged claims of the ’347 Patent are unpatentable.

B. *Related Matters*

The parties identify the following district court case as a related matter: *Viasat, Inc. v. Western Digital Corp.*, No. 6:21-CV-01230-ADA (W.D. Tex.). Pet. 3; Paper 4, 1 (Patent Owner’s mandatory notices).

The ’347 Patent is related to U.S. Patent No. 8,615,700 B2, which was challenged by Kioxia Corporation and Kioxia America, Inc. (collectively, “Kioxia”) in IPR2022-01067 and by Petitioner and Kioxia in IPR2022-01126.

C. The '347 Patent (Ex. 1001)

The '347 Patent was issued from an application filed November 21, 2013, which claims the benefit of an application filed August 18, 2010, and a provisional application filed August 18, 2009. Ex. 1001, codes (22), (60), (63). Petitioner contends that the '347 Patent claims are not entitled to the filing date of the provisional application (Pet. 15–17), and Patent Owner does not dispute that contention.

The '347 Patent discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57), 1:34–35, 2:29–30. The '347 Patent discloses a system having multiple error correction sub-modules and further discloses monitoring an error rate for data retrieved from flash memory and powering up additional error correction sub-modules to handle an increase in error rate. *Id.* at 1:35–52, 2:30–41.

An embodiment is shown in Figure 3, reproduced below.

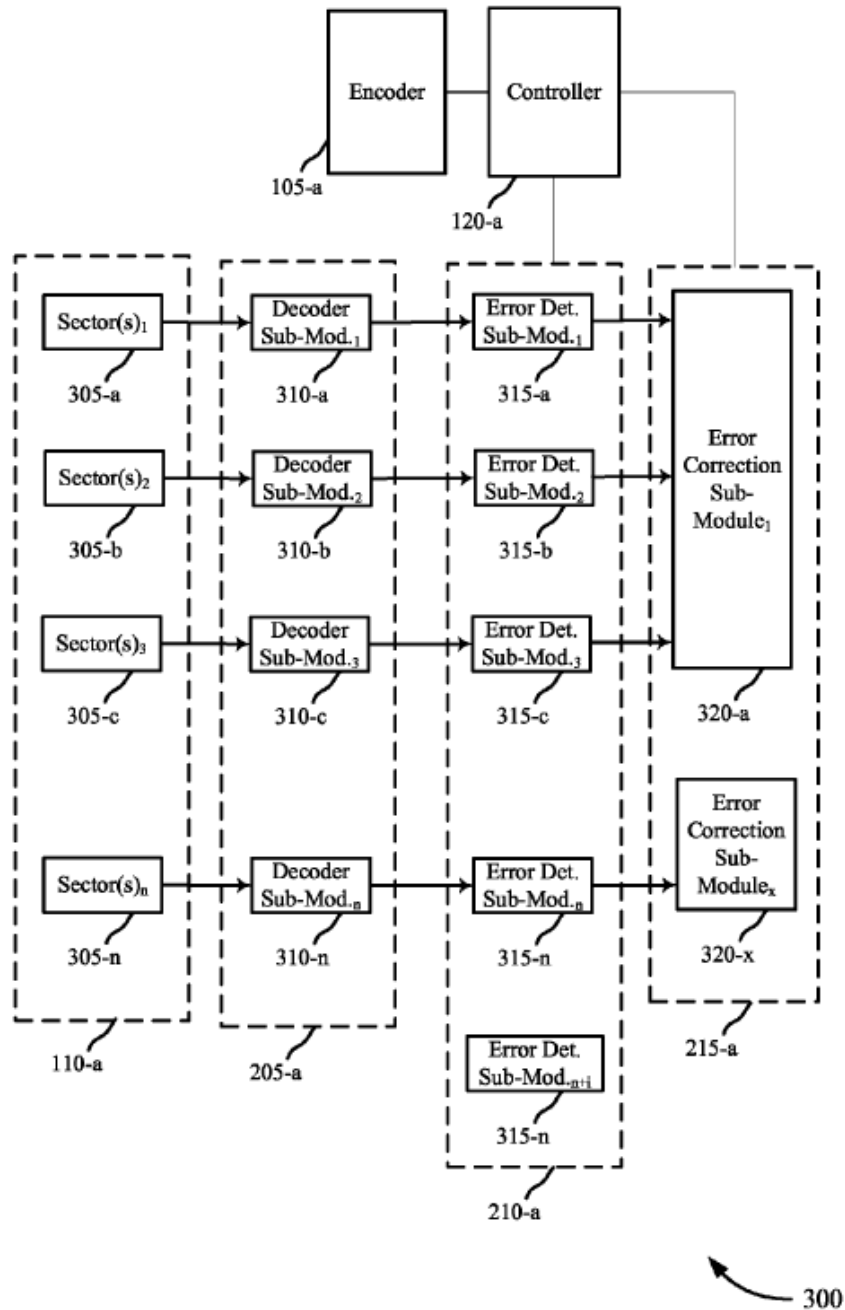


FIG. 3

Figure 3 “is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules.” Ex. 1001, 2:11–13, 6:31–34.

As shown in Figure 3, flash memory decoder system 300 includes encoder 105-a, flash memory 110-a, controller 120-a, decoder module 205-a, error detection module 210-a, and error correction module 215-a. Ex. 1001,

6:35–39. Encoder 105-a receives data to be stored and encodes the data for storage in the flash memory 110-a as encoded data. *Id.* at 3:48–50. Flash memory 110-a includes a number of different sets of one or more active sectors 305. *Id.* at 6:41–42. Decoder module 205-a includes a number of decoder sub-modules 310, each of which may be associated with a different set of sectors 305. *Id.* at 6:42–45. Error detection module 210-a includes a number of error detection sub-modules 315, each of which may be associated with a different set of sectors 305. *Id.* at 6:45–48.

According to the '347 Patent, each error detection sub-module 315 evaluates a data stream read from flash memory 110 to determine whether it contains an error and forwards the portion of the stream containing the error to error correction module 215-a. Ex. 1001, 6:63–7:2. Error correction module 215-a includes a number of error correction sub-modules 320, each of which handles errors from a number of error detection sub-modules 315 and corrects the portions of the data streams containing an error. *Id.* at 7:2–9.

The '347 Patent discloses that “[c]ontroller 120-a may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-a.” Ex. 1001, 7:14–17. Controller 120-a monitors an age or error rate associated with each sector of flash memory 110-a, selectively powers-up one or more error correction sub-modules 320 to serve sectors 305 where the error rates exceed a threshold, and adapts the coding rate to be used by the encoder on a per sector basis. *Id.* at 7:17–28.

D. Illustrative Claims

Petitioner challenges claims 1–11 and 13–23 of the '347 Patent. Claims 1 and 13 are the only independent claims and are reproduced below with Petitioner's bracketed claim element designations added and paragraphs adjusted.

1. [a] A method comprising: encoding data using forward error correction coding;

[b] storing the encoded data in a flash memory;

[c] retrieving the encoded data stored in the flash memory to generate a data stream;

[d] processing, using at least a first error correction sub-module, the data stream to correct errors in the data stream associated with the flash memory;

[e] monitoring a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;

[f] determining that the monitored metric exceeds a threshold;

[g] in response to the determination, modifying the forward error correction coding for use in subsequently encoding data for storage in the flash memory; and

[h] in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.

Ex. 1001, 10:50–11:2; Pet. 31–44.

13. [a] A system comprising: an encoder to encode data using forward error correction coding;

[b] a flash memory to store the encoded data;

[c] a decoder to retrieve the encoded data stored in the flash memory to generate a data stream, and

[d] to process the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module; and

[e] a controller to: monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;

[f] determine that the monitored metric exceeds a threshold;

[g] in response to the determination, modify the forward error correction coding for use by the encoder in subsequently encoding data for storage in the flash memory; and

[h] in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.

Ex. 1001, 11:40–12:10; Pet. 71–73.

E. Asserted Challenges to Patentability and Evidence

Petitioner asserts the following challenge to patentability:

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–11, 13–23	103(a)	Diggs, ² Cheng ³

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103, effective March 16, 2013. Because the ’347 Patent has an effective filing date before that date, we refer to the pre-AIA version of §§ 102 and 103. Ex. 1001, code (63).

² Ex. 1004, US 2009/0070651 A1, published Mar. 12, 2009 (“Diggs”). Petitioner asserts that Diggs is prior art to the ’347 Patent under 35 U.S.C. § 102(b). Pet. 22.

³ Ex. 1005, US 2009/0276570 A1, filed April 30, 2008 and published Nov. 5, 2009 (“Cheng”). Petitioner asserts that Cheng is prior art to the ’347 Patent under 35 U.S.C. § 102(a). Pet. 27–28.

Pet. 5.

F. Testimonial Evidence

The record includes a declaration of Lara Dolecek, Ph.D., submitted by Petitioner (Ex. 1003) and Dr. Dolecek's deposition testimony submitted by Patent Owner (Ex. 2022). Also in the record is a declaration of Nader Bagherzadeh, Ph.D., submitted by Patent Owner (Ex. 2021) and Dr. Bagherzadeh's deposition testimony submitted by Petitioner (Ex. 1022).

II. ANALYSIS

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSA”) would have had “at least a [bachelors of science degree] in electrical engineering or computer science or a related field, and four years’ experience designing, developing, or researching forward error correction (‘FEC’) or error correction coding (‘ECC’) systems.” Pet. 21 (citing Ex. 1003 ¶¶ 23–25). Petitioner states that “a higher education or skill level might make up for less experience, and vice-versa.” *Id.*

Patent Owner proposes that a POSA “would have had at least a [bachelors of science degree] in electrical engineering, computer engineering, or computer science or a related field, and at least two years of experience in the design, development, or research of the hardware implementation of error correction systems.” PO Resp. 5 (citing Ex. 2021

¶¶ 25–31, 36–61). Patent Owner states that “[a]dvanced education may substitute for experience and vice versa.” *Id.* (citing Ex. 2021 ¶ 29).

The parties’ articulations of the level of ordinary skill in the art are similar, and we adopt parts of each party’s description of a POSA’s education and experience. We agree with Patent Owner that computer engineering is a relevant field of study. PO Resp. 5. Our finding is supported by the ’347 Patent, which describes systems, devices, methods, and software for forward error correction for a flash memory system, which may be integrated with a computer, server, or other computing device. Ex. 1001, 3:29–32. We adopt Patent Owner’s proposal regarding the length of a POSA’s practical experience—two years—rather than four years, as proposed by Petitioner. Neither Petitioner nor Dr. Dolecek asserts that two years of practical experience would have been insufficient to acquire ordinary skill in the art. We disagree with Patent Owner’s assertion that a POSA’s experience would have been limited to “hardware implementation.” PO Resp. 5. Our finding is supported by the ’347 Patent, which states that “embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof.” Ex. 1001, 10:29–31. Petitioner’s assertion that a POSA needs to have experience in “forward error correction (‘FEC’) or error correction coding (‘ECC’) systems” (Pet. 21) is consistent with the ’347 Patent, which discloses methods, systems, and devices for forward error correction for flash memory. Ex. 1001, code (57); *see also* Ex. 1003 ¶¶ 14, 72 (explaining that error correction coding (“ECC”) includes forward error correction (“FEC”)).

For these reasons, we find that a POSA would have had a bachelor of science degree in electrical engineering, computer engineering, or computer

science or a related field, and two years of experience designing, developing, or researching forward error correction or error correction coding systems.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Neither party seeks express constructions of any claim terms. *See* Pet. 21; *see generally* PO Resp. We do not need to provide an express construction for any claim terms for purposes of resolving the controversy before us.

D. Petitioner’s Challenge

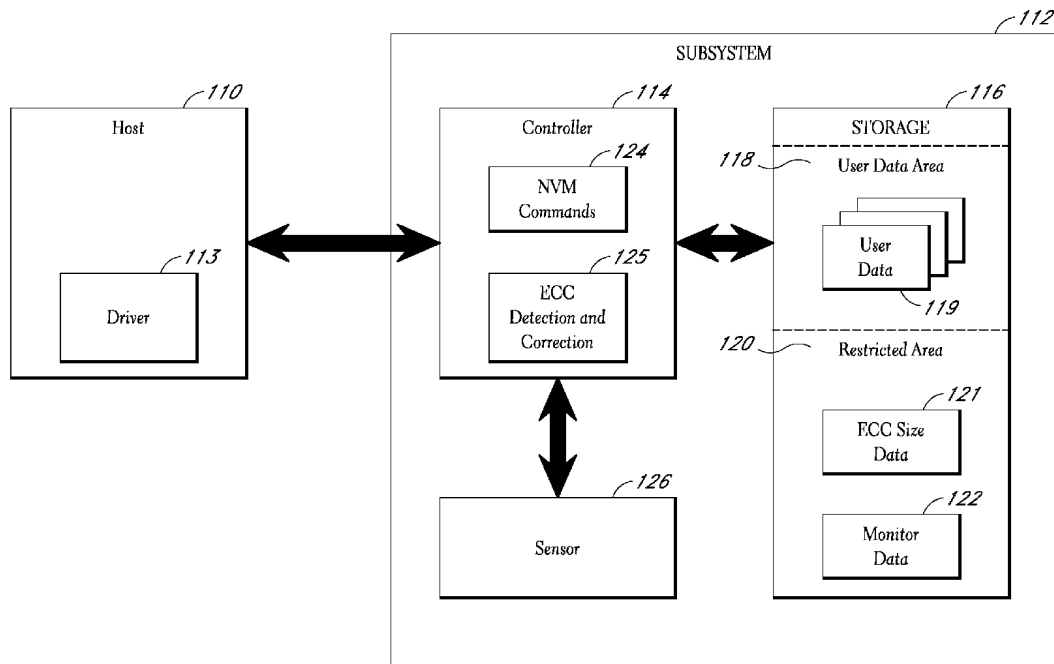
Petitioner challenges claims 1–11 and 13–23 as unpatentable and obvious based on Diggs and Cheng. Pet. 31–73. Patent Owner opposes. PO Resp. 5–47. We provide an overview of the references before turning to our analysis.

1. *Diggs (Ex. 1004)*

Diggs discloses a storage subsystem that monitors one or more conditions, such as the rate at which ECC errors are detected on read operations, and adjusts an error correction setting based on the monitored conditions. Ex. 1004, code (57), ¶ 7. According to Diggs, “[w]hen the monitored condition or conditions reveal an increased probability of data errors, the ECC level and thus the quantity of ECC data generated is increased, increasing the level of protection against data errors.” *Id.* ¶ 7.

Figure 1 of Diggs is reproduced below.

FIG. 1



Diggs Figure 1 is a block diagram illustrating host system 110 linked to solid-state storage subsystem 112, which is “capable of automatically adjusting ECC settings.” Ex. 1004 ¶¶ 11, 17. Storage subsystem 112 includes controller 114, storage array 116, and sensor 126. *Id.* ¶¶ 18, 28.

Controller 114 is configured with non-volatile memory (“NVM”) commands 124 for writing data to, and reading data from, storage array 116 in response to data and instructions received from host system 110. *Id.*

¶¶ 21, 22. Controller 114 further includes ECC detection and correction module 125, which performs encoding and decoding operations. *Id.* ¶ 23.

Storage subsystem 112 implements multiple ECC levels or settings, where a relatively high ECC level (more ECC bits per unit data) corresponds to a relatively high capacity to detect and correct errors. Ex. 1004 ¶ 24.

Sensor 126 transmits data/signals indicative of sensed environmental conditions, such as temperature, humidity, altitude, or movement. *Id.* ¶ 28.

Controller 114 stores these data/signals in storage array 116 as monitor data 122. *Id.* ¶¶ 28, 29. Other types of monitor data 122 include parameters that may be sensed or generated by controller 114, such as data descriptive of how frequently ECC errors are detected. *Id.* ¶ 29. Controller 114 accesses and analyzes monitor data 122 to select the appropriate ECC settings for encoding data. *Id.* ¶ 30. When writing encoded user data 119 to storage array 116, ECC module 125 also stores ECC size data 121, which indicates the error correction setting used to encode the user data. *Id.* ¶ 33. When a block of user data 119 is read by controller 114 and processed by ECC module 125, ECC size data 121 is read to determine the appropriate error correction setting to use for decoding the accessed data. *Id.*

2. *Cheng (Ex. 1005)*

Cheng discloses methods for maintaining the performance of memory systems until end-of-life. Ex. 1005 ¶ 1. Cheng explains that “flash memory [has] endurance limits, and as a memory approaches its end-of-life (‘EOL’), degradation of the floating-gate transistors leads to an increase in the number

of data errors.” *Id.* ¶ 18. According to Cheng, “as the number of errors increases, latencies are introduced as more time and system resources are spent on correcting these errors, which contributes to the overall degradation of the memory performance.” *Id.*

Figure 1 Cheng is reproduced below.

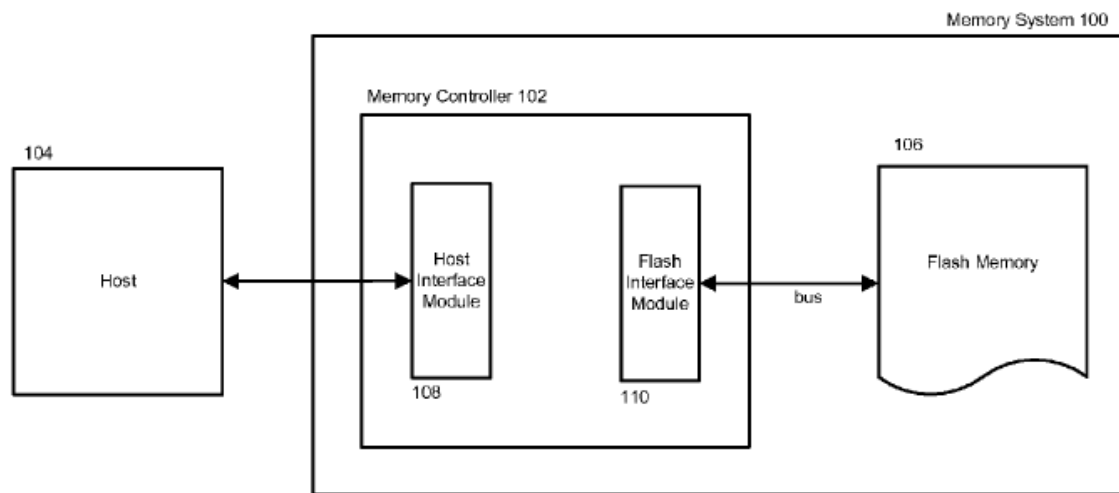


FIG. 1

Cheng Figure 1 shows memory system 100, including memory controller 102, which interfaces with host 104 and flash memory 106. Ex. 1005 ¶¶ 9, 13.

Figures 2 and 3 of Cheng show alternative embodiments of memory controller 102 of Figure 1. Ex. 1005 ¶¶ 10, 11, 19, 22. The Figure 2 embodiment includes error correction code (“ECC”) circuit 206, and the Figure 3 embodiment includes ECC circuits 206 and 208. *Id.* ¶¶ 7, 19, 22, Figs. 2, 3. Both embodiments include a flash interface module (“FIM”), which detects data errors “on the fly” during the process of transferring data

between the memory controller and the flash memory. *Id.* ¶ 21, Figs. 2, 3.⁴

In both embodiments, the FIM and ECC circuit(s) are driven by separate clock signals. *Id.* ¶¶ 20, 22, Figs. 2, 3. Referring to the Figure 2 embodiment, Cheng discloses:

The frequency of these clock signals can be adjusted. For example, if the ECC circuit 206 encounters a large number of data errors, its clock signal frequency can be increased such that it can operate at a faster rate. Similarly, the clock signal frequency for FIM 216 can be increased to speed up the bus connecting the module with the flash memory array.

Id. ¶ 20. Referring to the Figure 3 embodiment, Cheng discloses:

ECC circuit 206 can serve as the primary ECC circuit and ECC circuit 208 can serve as a supplemental ECC circuit. The supplemental ECC circuit can be enabled as the impact of error correction activity on the memory system increases. When the supplemental ECC engine is enabled, both ECC engines can be operated in parallel to complete the necessary error correction tasks faster. The speed at which each ECC engine operates can also be tuned independently by adjusting each ECC engine's clock signal frequency.

Id. ¶ 22.

3. Independent Claim 1

a) Claim Elements 1[a]–[g]

Petitioner shows persuasively, and Patent Owner does not dispute, that Diggs discloses claim elements 1[a]–[g]. Pet. 31–49; Ex. 1003 ¶¶ 75–125; *see* Section I.D. *supra* (claim 1). Selected claim elements are discussed below to provide context for our analysis of claim element 1[h].

⁴ In Cheng Figures 2 and 3, the flash interface module is labeled with reference numeral 110, but the written description identifies the flash interface module with reference numeral 216. Ex. 1005 ¶¶ 19–21, Figs. 2, 3.

For claim element 1[d], Petitioner shows that Diggs discloses “a first error correction sub-module,” namely ECC module 125. Pet. 38–39; Ex. 1003 ¶¶ 100–105; Ex. 1004 ¶¶ 33, 34, 40, 41.

For claim element 1[e], Petitioner shows that Diggs discloses “monitoring a metric of the flash memory.” Pet. 39–41; Ex. 1003 ¶¶ 106–112; Ex. 1004 ¶¶ 7, 16, 29, 54, 55. More specifically, Petitioner shows that Diggs discloses monitoring one or more conditions related to the probability of a data error occurring. Pet. 39–40; Ex. 1004 ¶¶ 7, 16. Petitioner shows that such conditions include, for example, the rate at which ECC errors are detected on read operations (bit error rate) and the wear level of a non-volatile memory array. Pet. 39–40; Ex. 1004 ¶¶ 7, 29.

For claim element 1[f], Petitioner shows that Diggs discloses “determining that the monitored metric exceeds a threshold.” Pet. 41–42; Ex. 1003 ¶¶ 113–118; Ex. 1004 ¶¶ 7, 8, 30, 46, 47, 50, 51, 55. For example, Petitioner shows that Diggs discloses detecting “when specific types of conditions or parameter thresholds” are reached and varying the ECC levels accordingly. Pet. 41 (quoting Ex. 1004 ¶ 8).

b) Claim Element 1[h]

Claim element 1[h] recites “in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.” Ex. 1001, 10:66–11:2.

Petitioner acknowledges that Diggs does not disclose claim element 1[h] but contends that “modifying Diggs to include this limitation would have been obvious in view of Cheng.” Pet. 44 (citing Ex. 1003 ¶ 127). In this subsection, we address whether Petitioner’s combination

discloses or suggests claim element 1[h], and in the following subsection, we address whether Petitioner establishes a rationale for combining the references' teachings.

Petitioner shows persuasively that Diggs in combination with Cheng discloses or suggests claim element 1[h]. As discussed above for claim element 1[d], Petitioner shows that “a first error correction sub-module” is disclosed by Diggs' ECC module 125. Pet. 38–39; Ex. 1004 ¶ 33. For claim element 1[h], Petitioner shows that Cheng's second ECC circuit 208 discloses a “second error correction sub-module.” Pet. 45–47; Ex. 1003 ¶¶ 129–132; Ex. 1005 ¶ 22, Fig. 3 (showing a memory controller that includes two ECC circuits 206 and 208).

Petitioner shows persuasively that the combination of Diggs and Cheng discloses or suggests “powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing,” as recited in claim element 1[h]. Pet. 46–47; Ex. 1003 ¶¶ 130–132; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22. Our finding is supported by Cheng, which discloses two ECC circuits in parallel, where the second ECC circuit is powered up when needed to correct an increased number of memory errors. Ex. 1005 ¶¶ 8, 22, Fig. 3 (showing ECC circuits 206 and 208).

Petitioner shows persuasively that the combination of Diggs and Cheng discloses or suggests powering up a second ECC circuit “in response to the determination,” i.e., in response to a determination that a monitored metric has exceeded a threshold, as recited in claim elements 1[e], 1[f], and 1[h]. Our finding is supported by Cheng, which discloses that, “as the memory error rate increases, the second ECC circuit can be enabled and/or operated at a faster speed to help correct the increased number of memory

errors.” Ex. 1005 ¶ 8; *see also id.* claim 22⁵ (“enabling the second ECC circuit such that the first ECC circuit and the second ECC circuit operate in parallel if the second number of errors is greater than the first number of errors”); *id.* ¶ 22 (“The supplemental ECC circuit can be enabled as the impact of error correction activity on the memory system increases. When the supplemental ECC engine is enabled, both ECC engines can be operated in parallel to complete the necessary error correction tasks faster.”). Our finding is also supported by Diggs, as discussed above for claim elements 1[e] and 1[f]. Notably, Cheng teaches powering up a second ECC circuit “as the memory error rate increases,” which corresponds to one of the conditions Diggs teaches to monitor and compare with a threshold. Ex. 1004 ¶¶ 7, 29; Ex. 1005 ¶ 8, claim 22.

Our finding for claim element 1[h] is supported by Dr. Dolecek’s testimony as follows.

A POSITA would also have found it obvious, and beneficial, to incorporate Cheng’s second ECC circuit into Digg’s ECC module 125 as a “second error correction sub-module” in parallel with Diggs existing ECC decoding module (the claimed “the first error correction sub-module”), and to power-on and use this second error correction sub-module for subsequent data stream processing when the monitored metric exceeds a threshold, i.e., when a higher ECC level is needed for reading and writing to memory and the computational burden of error correction activity on the memory system increases.

Ex. 1003 ¶ 132 (citing Ex. 1004 ¶ 25; Ex. 1005 ¶ 22; repeated at Pet. 47).

Dr. Dolecek’s testimony is credibly supported by Cheng paragraph 22 quoted above (Ex. 1005 ¶ 22), as well as Diggs, which discloses that, when

⁵ As further discussed below, Petitioner cites Cheng paragraph 8 and claims 22 and 23 in the Reply. Pet. Reply 5.

higher ECC levels are used, the processing time is relatively high and the system's performance is relatively low. Ex. 1004 ¶ 25.

Patent Owner argues that “the determination” in claim element 1[h] relates to the *same* monitored metric and threshold as recited in claim elements 1[e]–[g] and that Petitioner's combination of Diggs and Cheng for claim element 1[h] relies on a *different* metric—latency instead of error rate. PO Resp. 8–11; PO Sur-reply 1–4. Although we agree with Patent Owner that claim elements 1[e]–[h] all relate to the same monitored metric, as does Petitioner (Tr. 13:5–13), we disagree with Patent Owner's characterization of Petitioner's combination as relying on two different metrics. Petitioner contends that it would have been obvious “to power-on and use this second error correction sub-module for subsequent data stream processing when *the monitored metric* exceeds a threshold.” Pet. 47 (emphasis added); Ex. 1003 ¶ 132 (same). “[T]he monitored metric” refers to the same metric that Petitioner identified for claim elements 1[e]–[g], for example, bit error rate, as disclosed by Diggs. Pet. 39–43; Pet. Reply 2–3; Tr. 13:14 (“The petition actually does use the exact same metric throughout.”). For claim element 1[g], for example, Petitioner shows that “Diggs discloses that a high level of ECC encoding may be triggered when bit error rate exceeds a certain threshold.” Pet. 43 (citing Ex. 1003 ¶ 122; Ex. 1004 ¶¶ 50, 51). For claim element 1[h], Petitioner shows that it would have been obvious to modify Diggs to power up a second ECC module when the same metric, e.g., bit error rate, exceeds a certain threshold. Pet. 47; Ex. 1003 ¶ 132.

Patent Owner misinterprets the clause of the Petition that reads, “*i.e.*, when a higher ECC level is needed for reading and writing to memory and the computational burden of error correction activity on the memory system increases.” Pet. 47; Ex. 1003 ¶ 132 (same). That clause does not identify a

different monitored metric. Instead, it provides a reason or motivation for powering up a second ECC module, as further discussed on the next page of the Petition. Pet. 48. As Petitioner explains, “[t]he proposed combination of Diggs and Cheng *both* modifies forward error correction coding, *e.g.*, ECC level, *and* powers-up a second error correction sub-module, in response to a single performance metric exceeding some threshold.” Pet. Reply 5 (citing Pet. 39–49). This combination meets the limitation of claim element 1[h], and Patent Owner does not argue otherwise.

We disagree with Patent Owner’s sur-reply argument that, by citing Cheng paragraph 8 and claims 22 and 23 in the Reply, Petitioner relies “for the first time—on embodiments of Cheng which it failed to raise in its Petition.” PO Sur-reply 3 (citing Pet. Reply 5). Contrary to Patent Owner’s argument, Cheng paragraph 8 and claims 22 and 23 relate to the *same embodiment* as shown in Cheng Figure 3 and described in Cheng paragraph 22, which were cited in the Petition. Pet. 46–47 (addressing claim element 1[h]). Cheng paragraphs 8 and 22 and claims 22 and 23 all describe the conditions under which a second ECC circuit can be enabled. Increased error rate (Ex. 1005 ¶ 8, claim 22) is not a different condition than increased error correction activity (*id.* ¶ 22). The record supports that, as the error rate increases, the error correction activity also increases, as does latency. *Id.* ¶ 23 (“[B]aseline latency” is established “for the case where there is no data error, and thus no error correction activity.”); Ex. 2022, 16:25–17:9 (Dr. Dolecek: “Cheng is concerned with . . . minimizing the latency hit that would be incurred by the default ECC schemes, that would be necessary to be employed to deal with an increased rate of errors.”).

In our view, Petitioner’s reliance on Cheng paragraph 8 and claims 22 and 23 in the Reply (Pet. Reply 5) is responsive to and refutes Patent

Owner’s argument that “Cheng teaches—and Petitioner invokes” a different metric than is taught by Diggs. PO Resp. 9. And, in view of the close relationship between Cheng Figure 3 and paragraph 22 cited in the Petition and Cheng paragraph 8 and claims 22 and 23 cited in the Reply (Pet. Reply 5), we find that Petitioner’s reply argument “properly expands on and is a fair extension of its previously raised . . . argument” that the combination of Diggs and Cheng teaches claim element 1[h]. Pet. 44–47; *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1385 (Fed. Cir. 2023).

c) Rationale for Combining Diggs and Cheng

Petitioner shows persuasively that it would have been obvious to modify Diggs’ memory system by incorporating and powering up a second ECC module “to reduce processing time and, thereby avoid reductions in the operation speed of the memory system and extend the operational lifetime of the memory system.” Pet. 47–48 (citing Ex. 1003 ¶¶ 131–135). Relying on express teachings in Diggs and Cheng, Petitioner shows that the addition of a second ECC circuit, as taught by Cheng, would solve a problem discussed in Diggs, namely slower processing times when using a higher ECC level under high error rate conditions. *Id.*; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22.

To begin, we agree with Petitioner that Diggs and Cheng are closely related prior art. Pet. 47 (citing Ex. 1003 ¶ 131). As Petitioner asserts and Dr. Dolecek testifies, Diggs and Cheng are “each directed at improving ECC performance in flash memory systems as error rate increases.” Pet. 47; Ex. 1003 ¶ 131. Diggs discloses a storage subsystem that monitors various conditions related to the probability of a data error occurring and increases an ECC level when a monitored condition reveals an increased probability of

data errors. Ex. 1004, code (57), ¶¶ 7, 16, 29, 51. Cheng is likewise concerned with error correction when the probability of data errors increases. In one embodiment, Cheng teaches a memory system that “includes two ECC circuits which can be operated in parallel to quickly correct memory errors.” Ex. 1005 ¶ 8. “[A]s the memory error rate increases, the second ECC circuit can be enabled and/or operated at a faster speed to help correct the increased number of memory errors.” *Id.*

Petitioner shows persuasively that a POSA would have “found it obvious, and beneficial, to incorporate Cheng’s second ECC circuit into Digg’s ECC module 125 as a ‘second error correction sub-module’ in parallel with Diggs existing ECC decoding module, *i.e.*, the claimed ‘the first error correction sub-module.’” Pet. 47 (citing Ex. 1003 ¶ 132; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22). Petitioner persuades us that it would have been obvious “to power-on and use this second error correction sub-module for subsequent data stream processing when the monitored metric exceeds a threshold, *i.e.*, when a higher ECC level is needed for reading and writing to memory and the computational burden of error correction activity on the memory system increases.” *Id.*

Petitioner’s obviousness rationale is amply supported by Dr. Dolecek’s testimony, as well as the disclosures of Diggs and Cheng. Ex. 1003 ¶¶ 132, 134; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22. As discussed by Dr. Dolecek, Diggs teaches that “as the error rates increase, higher ECC level is needed to correct more errors” and “[h]igher ECC level means that there are more ECC parity symbols.” Ex. 1003 ¶ 134. Dr. Dolecek’s testimony is supported by Diggs, which discloses a storage subsystem that “automatically adjusts the level of ECC (and thus the number of ECC bits stored per unit of data) based on one or more monitored or detected

conditions.” Ex. 1004 ¶ 7. According to Diggs, “[w]hen the monitored condition or conditions reveal an increased probability of data errors, the ECC level and thus the quantity of ECC data generated is increased, increasing the level of protection against data errors.” *Id.*

As Dr. Dolecek explains, Diggs teaches that “additional time is needed to compute and check these additional ECC parity symbols, and in turn the performance degrades.” Ex. 1003 ¶ 134. Dr. Dolecek’s testimony is supported by Diggs, which discloses two ECC levels or settings, the first “appropriate for low risk conditions and/or for non-critical data” and the second “appropriate for high risk conditions and/or for critical data.” Ex. 1004 ¶ 25. According to Diggs, when the higher ECC level is used, “the processing time needed to compute and check ECC values associated with this setting is relatively high.” *Id.* This statement in Diggs supports Petitioner’s rationale and Dr. Dolecek’s testimony that “[t]o compensate for Diggs[’] longer processing time associated with higher ECC levels, a POSA would have found the use of a second error correction sub-module, as taught by Cheng, advantageous to reduce processing time and, thereby avoid reductions in the operation speed of the memory system and extend the operational lifetime of the memory system.” Pet. 48; Ex. 1003 ¶ 134. Diggs provides strong support for Petitioner’s rationale that a POSA would have found it beneficial to modify Diggs by incorporating a second ECC module to operate in parallel with Diggs’ ECC module under high error rate conditions.

Petitioner’s rationale and Dr. Dolecek’s testimony are also supported by Cheng’s embodiment with two ECC circuits, where the second (supplemental) ECC circuit is “enabled as the impact of error correction activity on the memory system increases” so that “both ECC engines can be

operated in parallel to complete the necessary error correction tasks faster.” Ex. 1005 ¶ 22; *see also* Ex. 1003 ¶ 129 (discussing Cheng). We agree with Petitioner and Dr. Dolecek that Cheng’s teaching of enabling a second ECC circuit as the impact of error correction activity on the memory system increases (Ex. 1005 ¶ 22) provides a solution to the problem of high processing times associated with higher ECC levels, as discussed in Diggs (Ex. 1004 ¶ 25). Pet. 48; Ex. 1003 ¶ 134. The teachings of Diggs and Cheng fit together “like the pieces of a puzzle” and provide persuasive support for Petitioner’s obviousness combination. Pet. 47–48; *KSR*, 550 U.S. at 420 (“[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.”).

Patent Owner argues that Petitioner’s combination of Diggs and Cheng is “inoperable” and that Petitioner does not adequately explain how a POSA would have combined the references. PO Resp. 11–18; PO Sur-reply 4–9. According to Patent Owner, there is a “mismatch” between Diggs’ ECC module 125, which is responsible for both error detection and correction, and Cheng’s ECC circuit 206, which Patent Owner asserts does not perform error detection and only receives data for correction if errors were detected in the flash interface module. PO Resp. 12–16. We disagree with Patent Owner’s arguments for two reasons.

First, as noted in the Institution Decision and argued by Petitioner in the Reply, Cheng defines its first and second “ECC circuits” as “error detection and correction code” circuits and confirms that errors are, in fact, “detected and corrected” by these circuits. Ex. 1005, claims 3, 9, 18, 22; Inst. Dec. 23; Pet. Reply 6–7. The experts agree that an ECC circuit performs both error detection and correction. Ex. 1023 ¶ 84 (declaration of Dr. Bagherzadeh in related district court litigation); Ex. 2022, 39:5–18,

41:23–42:9, 70:17–25 (Dr. Dolecek’s deposition testimony); *see* Pet. Reply 7–8 (citing this testimony); *see also* Ex. 3001 ¶ 175 (declaration of Dr. Bagherzadeh in related IPR2022-01067: “as part of error correction, you automatically do some detection” (quoting opposing expert’s deposition testimony)). Patent Owner’s argument is therefore premised on an incorrect assumption that Cheng’s ECC circuits do not perform error detection.

Second, Petitioner persuades us that, regardless of whether Cheng’s ECC circuits perform both error detection and correction, a POSA would have been able to use Diggs’ error detection-performing ECC module 125 as a template for adapting a second ECC circuit, as taught by Cheng, in a way to ensure parallel operation and compatibility with Diggs. Pet. 47; Pet. Reply 9. Our finding is supported by Dr. Dolecek’s deposition testimony. Ex. 2022, 73:1–21 (“[T]his is not here rocket science. It is merely using a conceptual idea from Cheng. There is nothing here in particular that a person of skill in the art would not deem obvious. It suggests, merely, running two ECCs in parallel to reduce the latency.” (cited at Pet. Reply 8)). Patent Owner does not assert that combining Diggs and Cheng in the manner proposed by Petitioner would require skill beyond that possessed by a POSA.

Patent Owner argues that the Board’s citation to Cheng’s claims 3, 9, 18, and 22 in the Institution Decision (Inst. Dec. 23) and Petitioner’s reliance on those claims in the Reply (Pet. Reply 6–7) are procedurally improper. PO Resp. 18–19; PO Sur-reply 6–7. We disagree. Unlike the situation in *Magnum Oil* cited by Patent Owner (PO Resp. 18 (citing 829 F.3d at 1381)), the Board is not making an obviousness argument on behalf of Petitioner. The Institution Decision cites portions of Cheng that contradict Patent Owner’s argument that Cheng’s ECC circuit 206 does not perform error

detection. Prelim. Resp. 22; Inst. Dec. 23. Petitioner’s reliance on Cheng’s claims 3, 9, 18, and 22 (Pet. Reply 6–7) is responsive to and refutes the same argument in the Patent Owner Response (PO Resp. 16) and “properly expands on and is a fair extension of” Petitioner’s argument that a POSA would have found it obvious to combine Cheng’s second ECC circuit in parallel with Diggs’ ECC decoding module. Pet. 47; *Rembrandt Diagnostics*, 76 F.4th at 1385.

We have considered Patent Owner’s argument that “Petitioner does not address other aspects of the Diggs and Cheng combination,” leaving “several other unanswered questions.” PO Resp. 20–22. We are persuaded that the implementation details Patent Owner says are missing are either actually disclosed or are sufficiently routine that a POSA would not need such details to practice the challenged claims. *See* Pet. Reply 10–11 (responding to Patent Owner’s argument). For example, Patent Owner argues that Petitioner does not explain how the combination of Diggs and Cheng would account for changes in the encoding rate or ECC algorithm, as disclosed by Diggs. PO Resp. 20–21. Petitioner shows persuasively that, even if not disclosed in detail, Cheng’s ECC circuit could be adapted to perform an initial ECC setting determination step prior to error detection and correction, such as taught and performed by Diggs. Pet. Reply 10–11. Patent Owner does not assert that such an adaption of Cheng would present any difficulty for a POSA.

We have also considered Patent Owner’s argument that Petitioner’s combination would require an “unaddressed complete redesign.” PO Resp. 31–35; PO Sur-reply 11–12. We are persuaded that the design issues Patent Owner identifies would not have been so difficult or insurmountable that a POSA would not have had a motivation to combine the teachings of

Diggs and Cheng. *See* Pet. Reply 16–20 (responding to Patent Owner’s argument). For example, Patent Owner again points to a supposed “mismatch” between the error detectors and correctors in Diggs and Cheng, arguing that to make Petitioner’s combination, “a skilled artisan would first need to understand what is within Diggs’ ECC detection and correction module 125.” PO Resp. 31, 33. We disagree with Patent Owner’s “mismatch” argument for the reasons discussed above. Petitioner shows persuasively that it would have been obvious to incorporate a second ECC circuit in parallel with Digg’s existing ECC module and to include error detection functionality in both ECC modules. Pet. 47; Pet. Reply 17. Like the ’347 Patent, Diggs and Cheng both rely on well-known ECC circuitry and algorithms, and adapting the ECC circuits of Diggs and/or Cheng to function in combination would require no more than routine skill. *See* Ex. 1001, 10:8–10 (“[W]ell-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.”); *see also* Ex. 2022, 73:1–21 (“[T]his is not here rocket science.”).

Patent Owner argues that a skilled artisan would not have been motivated to adopt Petitioner’s combination of Diggs and Cheng, asserting that Petitioner only borrows the second ECC circuit of one embodiment and ignores Cheng’s other teachings, such as increasing clock frequency, separating error detection from error correction, and sending error-free data directly to the host interface module. PO Resp. 22–30; PO Sur-reply 9–10. Patent Owner argues that a skilled artisan interested in reducing processing time would have started by speeding up the clock, as Cheng teaches. PO Resp. 30; PO Sur-reply 10.

We have considered Patent Owner’s arguments, but are persuaded that Petitioner has shown that a POSA would have had a reason to combine Diggs and Cheng. Pet. 47–48; Pet. Reply 12–13. Patent Owner’s argument that a POSA would have considered other features disclosed in Cheng does not weigh against Petitioner’s showing that it would have been obvious to combine Diggs’ memory system with Cheng’s teaching of a second ECC circuit that powers up when the error rate is high. The existence of other possible combinations of features does not make Petitioner’s combination nonobvious. Petitioner was required to show that its proposed combination would have been desirable, but not necessarily the most desirable option available to a POSA. *Elekta Ltd. v. ZAP Surgical Sys., Inc.*, 81 F.4th 1368, 1374 (Fed. Cir. 2023) (“Nor does an obviousness showing ‘require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention.’” (citing *Novartis Pharms. Corp. v. West-Ward Pharms. Int’l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019))). The pertinent question is “‘whether there is something in the prior art as a whole to suggest the *desirability*, and thus the obviousness, of making the combination,’ not whether there is something in the prior art as a whole to suggest that the combination is the *most desirable* combination available.” *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004) (citing *In re Beattie*, 974 F.2d 1309, 1311 (Fed. Cir. 1992)).

Lastly, Patent Owner argues that a skilled artisan would not have reasonably expected Petitioner’s combination of Diggs and Cheng to achieve reduced processing time and increased performance. PO Resp. 35–42; PO Sur-reply 12–15. We find that, in this case, the issues of motivation to combine and reasonable expectation of success are closely intertwined, and

the evidence discussed above that supports motivation to combine also supports a reasonable expectation of success. *See Elekta*, 81 F.4th at 1376 (“[A] finding of reasonable expectation of success can be [made] implicit . . . by considering and addressing other, intertwined arguments, including . . . a motivation to combine.” (citing *KSR*, 550 U.S. at 418; *Merck & Cie v. Gnosis S.P.A.*, 808 F.3d 829, 836 (Fed. Cir. 2015))). For example, we find that a reasonable expectation of success is supported by the express teaching of Cheng that powering up a second ECC circuit can reduce processing time. Ex. 1005 ¶ 22 (“The supplemental ECC circuit can be enabled as the impact of error correction activity on the memory system increases. When the supplemental ECC engine is enabled, both ECC engines can be operated in parallel to complete the necessary error correction tasks faster.”). Petitioner’s evidence is more than sufficient to establish a reasonable expectation of success. Ex. 1003 ¶¶ 127–131; Ex. 1004 ¶ 25; Ex. 1005 ¶ 22; *see* Pet. Reply 21–23 (responding to Patent Owner’s arguments about reasonable expectation of success).

4. *Independent Claim 13*

Petitioner relies on the same analysis for claim 13 as it presents for claim 1. Pet. 71. In addition, Petitioner contends that “the ‘decoder’ of limitations 13[c]–13[d] and the ‘controller’ of limitation 13[e]–13[h] are disclosed by Diggs’ controller 114 as modified by Cheng.” *Id.*

Patent Owner relies on the same arguments for claim 13 as it presents for claim 1. PO Resp. 42. In addition, Patent Owner argues that Petitioner ignores claim 13’s structural requirement for a decoder and that Diggs does not include a decoder that retrieves the encoded data stored in the flash memory to generate a data stream. *Id.* at 42–47.

To show a “decoder,” as recited in claim element 13[c], Petitioner relies on its contentions for claim element 1[c]. Pet. 71–72 (table showing how limitations of claim 13 correspond to the limitations of claim 1). When discussing claim elements 1[c] and 13[c], Petitioner identifies Diggs’ controller 114 as performing the decoder’s function “to retrieve the encoded data stored in the flash memory to generate a data stream,” as recited in claim element 13[c]. Pet. 36–37, 72. Petitioner relies on Diggs’ disclosure that, when a read instruction is received from host 110, controller 114 reads a block of encoded user data 119 from storage array 116. Pet. 37; Ex. 1004 ¶¶ 33–35, 40, Figs. 1, 2.

Patent Owner agrees that Diggs’ controller 114 performs the function of retrieving the encoded data stored in the flash memory to generate a data stream, as recited in claim element 13[c]. PO Resp. 43 (“Diggs’ controller performs that task.”). Patent Owner argues that “Diggs’ decoder is ECC detection and correction module 125,” which is a “separate component[]” from controller 114, even though it is “within controller 114.” *Id.* at 43–44. According to Patent Owner, Diggs’ “controller, not the decoder, retrieves encoded data stored in flash memory.” *Id.* at 45.

After considering the record as a whole, we are persuaded by Petitioner’s showing for claim element 13[c]. Pet. 36–38, 71–72; Pet. Reply 23–25. Claim 13 recites a “decoder” that performs two functions: “to retrieve the encoded data . . . to generate a data stream,” as recited in claim element 13[c], and “to process the data stream to correct errors . . . ,” as recited in claim element 13[d]. The parties agree that Diggs’ controller 114 performs the function recited in claim element 13[c] and Diggs’ ECC detection and correction module 125 performs the function recited in claim element 13[d]. Pet. 36–39, 71–72; PO Resp. 45 (“[C]ontroller 114 is the

component in Diggs that ‘retrieve[s] the encoded data stored in the flash memory to generate a data stream’ and ECC detection and correction module 125 ‘process[es] the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module.’”).

We are persuaded by Petitioner’s showing that a “decoder,” as recited in claim element 13[c], is disclosed by Diggs’ controller 114. Pet. 36–37, 71–72; Pet. Reply 23–25. It is undisputed that Diggs’ controller 114 *includes* ECC detection and correction module 125. Ex. 1004 ¶ 23 (“The controller 114 further includes an ECC detection and correction module 125.”), Fig. 1 (showing ECC Detection and Correction module 125 within Controller 114); *see also* PO Resp. 44 (“ECC detection and correction module 125 is within controller 114.”) It is also undisputed that Diggs’ controller 114 as a whole (including ECC detection and correction module 125) performs the recited functions of a “decoder.” PO Resp. 44–45. Although ECC module 125 handles the decoding, and another portion of controller 114 handles data retrieval, this division of labor is not inconsistent with claim 13, which does not require that the functions of a decoder reside within one circuit. Pet. Reply 24. To the contrary, the ’347 Patent teaches that the system’s components, including the decoder, may be “implemented with *one or more* Application Specific Integrated Circuits (ASICs) . . . [or] by *one or more* other processing units (or cores), on one or more integrated circuits.” Ex. 1001, 3:34–40 (emphasis added).

Despite a difference in terminology between claim 13 and the prior art, the structure disclosed by Diggs fits comfortably within the structure defined by claim 13. *See Application of Cotner*, 347 F.2d 582, 586 (C.C.P.A. 1965) (“We . . . are not persuaded that the semantic discrepancies

point up unobvious differences in substance between appellant’s claimed invention and the Curtin prior art disclosure.”).

5. *Dependent Claims 2–11 and 14–23*

Claims 2–11 depend, directly or indirectly, from claim 1, and claims 14–23 depend, directly or indirectly, from claim 13. Relying on the testimony of Dr. Dolecek, Petitioner contends that the additional limitations of dependent claims 2–10 are disclosed by Diggs, and that the additional limitation of dependent claim 11 would have been obvious in view of Diggs and Cheng. Pet. 49–70; Ex. 1003 ¶¶ 140–220. Claims 14–23 recite the same limitations as method claims 2–11, except in system form, and Petitioner relies on the same arguments and evidence for claims 14–23 as it presents for claims 2–11. Pet. 73.

Patent Owner does not present arguments for dependent claims 2–11 and 14–23 separate from its arguments for independent claims 1 and 13. *See* PO Resp. 8 (arguing that Petitioner’s challenges to the dependent claims “fail for the same reasons” as the independent claims).

For the reasons discussed above for independent claims 1 and 13 and based on the arguments and evidence set forth in the Petition, we find that Petitioner has shown that dependent claims 2–11 and 14–23 would have been obvious based on Diggs and Cheng.

III. CONCLUSION⁶

In summary:

⁶ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg.

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–11, 13– 23	103	Diggs, Cheng	1–11, 13–23	
Overall Outcome			1–11, 13–23	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown that claims 1–11 and 13–23 of the '347 Patent are unpatentable; and

FURTHER ORDERED that because this Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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