

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANON U.S.A., INC. and CANON INC.,
Petitioner,

v.

SLINGSHOT PRINTING LLC,
Patent Owner.

IPR2022-01414
Patent 7,195,341 B2

Before JO-ANNE M. KOKOSKI, GARTH D. BAER, and
JOHN D. HAMANN, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Canon U.S.A., Inc. and Canon Inc. (together, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–5 and 8 (“the challenged claims”) of U.S. Patent No. 7,195,341 B2 (Ex. 1001, “the ’341 patent”). Slingshot Printing LLC (“Patent Owner”) filed a Preliminary Response (Paper 5, “Prelim. Resp.”) to the Petition.

An *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Further, a decision to institute may not institute on fewer than all claims challenged in the petition. 37 C.F.R. § 42.108(a). Based on the arguments and evidence of record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one of the challenged claims of the ’341 patent is unpatentable. Accordingly, we institute an *inter partes* review as to the challenged claims of the ’341 patent on all the grounds of unpatentability asserted in the Petition.

B. *Related Matters*

The parties indicate that the ’341 patent is the subject of the following district court cases: *Slingshot Printing LLC v. Canon U.S.A., Inc., et al.*, No. 2:22-cv-00123 (E.D.N.Y.) and *Slingshot Printing LLC v. HP Inc.*, No. 6:19-cv-00549, reassigned as No. 2:20-00187 (W.D. Tex.) (dismissed). Pet. 1; Paper 3, 1.

Patent Owner indicates that Petitioner has filed the following concurrent petitions against patents that are asserted along with the ’341

patent in the district court case: IPR2022-01415 (U.S. Patent 7,559,629) and IPR2022-01416 (U.S. Patent 7,938,523). Paper 3, 1.

C. The '341 patent

The '341 patent “relates to micro-fluid ejection head substrates and in particular to improved conductor layouts for reduced substrate size.”

Ex. 1001, 1:6–8. Specifically, the '341 patent resolves the “need for improved substrate conductor routing and layouts that do not adversely affect the electrical properties of the circuits.” *Id.* at 1:33–36. Figure 1 is reproduced below.

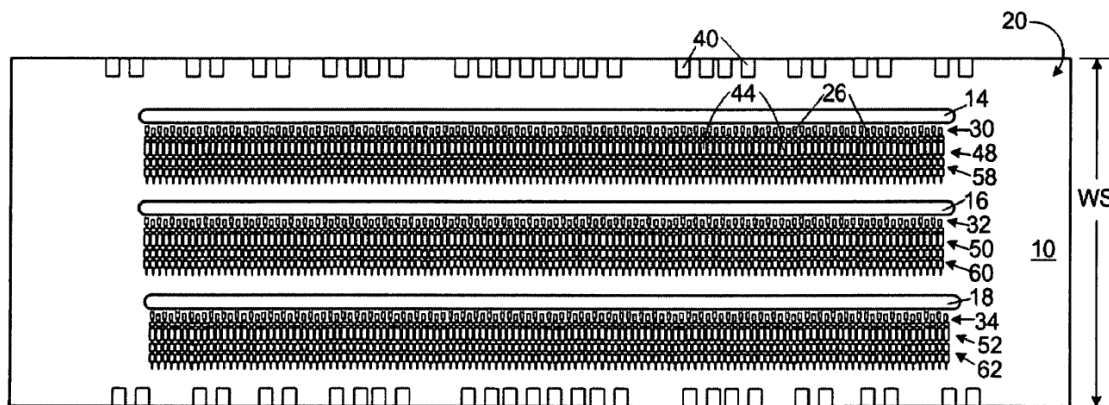


FIG. 1

Figure 1 depicts a semiconductor substrate “for micro-fluid ejection heads.” *Id.* at 2:38–39. Substrate 10 includes fluid supply slots 14, 16, and 18 for allowing flow of fluid, fluid ejection actuators 26 disposed in columnar arrays 30, 32, and 34 and adjacent to fluid supply slots 14, 16, and 18. *Id.* at 2:59–3:5. To selectively activate ejection actuators 26, “driver and control logic are also included on the device surfaces” of the substrate and “[t]he control logic includes power and ground interconnections in a first metal conductor layer.” *Id.* at 3:13–17. Power transistors 44 are included in columnar arrays 48, 50, and 52 that are adjacent to columnar arrays 30, 32,

and 34 and “[c]ontrol logic arrays 58, 60, and 62 are disposed adjacent” to power transistors 44. *Id.* at 3:23–30. The interconnection between control logic arrays 58, 60, and 62 and power transistors 44 “is in a polysilicon layer rather than in the first metal conductor layer or in a second metal conductor layer thereby eliminating the need for a three metal layer process for providing interconnections and power and ground buss routing to the devices.” *Id.* at 3:31–36. A power bus is routed over at least a portion of an active area for the power transistor array 48, 50, or 52 and a ground buss is disposed adjacent the power buss in the second metal conductive layer in which the ground buss overlies at least a portion of the control logic area. *Id.* at 5:48–50, 5:58–61, Fig. 8.

D. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claim 1 is reproduced below.

1. A semiconductor substrate for a micro-fluid ejection device, the substrate comprising:

 a plurality of micro-fluid ejection actuators disposed in a columnar array adjacent a fluid supply slot in the semiconductor substrate;

 a plurality of power transistors disposed in a columnar array adjacent the ejection actuators and connected through a first metal conductor layer to the ejection actuators, the columnar array of power transistors occupying a power transistor active area of the substrate;

 a columnar array of logic circuits disposed adjacent the columnar array of power transistors and connected through a polysilicon conductor layer to the power transistors, the columnar array of logic circuits occupying a logic circuit area of the substrate;

a power conductor for the ejection actuators routed in a second metal conductor layer disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate; and

a ground conductor for the ejection actuators routed in the second metal conductor layer disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate.

Ex. 1001, 6:45–67.

E. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
U.S. 6,412,917 B1, issued July 2, 2002 (“Torgerson”)	1004
U.S. 7,240,997 B2, issued July 10, 2007 (“Bruce”)	1005
Certified English Translation of JP 1996-108536 A (“Furukawa”)	1006
Declaration of Stephen F. Pond, Ph.D.	1007
JP 1996-108536 A, published Apr. 30, 1996 (“Furukawa Original”)	1008

F. Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–5, 8	103	Torgerson, Bruce
1–5, 8	103	Furukawa, Torgerson

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art would have had “at least a Bachelor’s or Master’s level college degree in Mechanical Engineering, Materials Science, Physics, Electrical Engineering, or a related field, and at least two years of training or experience in the design of inkjet

printheads or semiconductor circuit layout.” Pet. 17–18 (citing Ex. 1007 ¶ 58). Patent Owner does not propose a description of the level of ordinary skill in the art or dispute Petitioner’s description. Prelim. Resp. 26–27. At this stage, we agree with and adopt Petitioner’s description.

B. Claim Construction

Neither party proposes an express construction for any claim terms. Pet. 18; Prelim. Resp. 27. We determine that no claim terms require express construction for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Description of Prior Art References

1. Torgerson (Ex. 1004)

Petitioner relies primarily on Torgerson in Ground 1. *See* Pet. 18–52. Torgerson discloses an ink jet printhead having FET (field effect transistor) drive circuits that are configured to compensate for parasitic resistances of power traces, and ground busses that overlap active regions of the FET drive circuits. Ex. 1004, Code (57). Figure 1A of Torgerson is reproduced below.

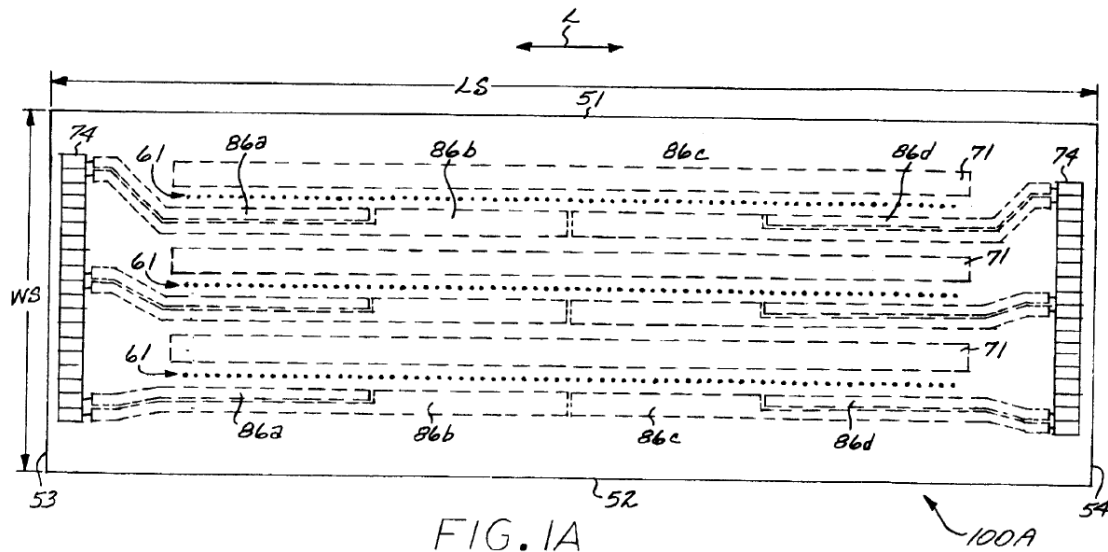


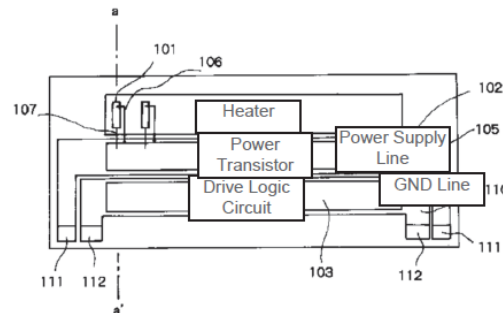
Figure 1A shows a “top plan view illustration of the layout of ink drop generators and primitive select of an ink jet printhead.” *Id.* at 2:9–11. Ink jet printhead 100A includes a thin film substructure “comprising a substrate such as silicon.” *Id.* at 2:57–62. Ink drop generators along with heat resistors “are arranged in columnar arrays or groups 61.” *Id.* at 3:66–4:5. The thin film substructure includes ink feed slots 71 that feed ink drop generator groups 61. *Id.* at 4:36–41. Columnar FET drive circuit arrays are “formed in the thin film substructure” and have circuits with drain electrodes connected to heat resistors. *Id.* at 4:66–5:6, Fig. 6. Ground busses and heater resistor leads “are formed in” a metallization layer of the thin film substructure as are the drain and source electrodes of the FET drive circuits. *Id.* at 5:19–22, Fig. 5. The ink drop generators of a columnar array 61 can be organized into four primitive groups with heater resistors thereof being “electrically connected to the same one of four primitive select traces 86a, 86b, 86c, 86d.” *Id.* at 5:43–50.

2. *Bruce (Ex. 1005)*

Petitioner relies on Bruce for teaching routing a second-metal-layer ground portion through an area of a second metal layer that overlies logic portions. *See* Pet. 16 (citing Ex. 1005, 2:50–63, Fig. 1; Ex. 1007 ¶¶ 110–112), 38–40 (citing Ex. 1005, 5:55–63, 2:40–59, Fig. 1; Ex. 1007 ¶¶ 110–111).

3. *Furukawa (Ex. 1006)*

Petitioner relies primarily on Furukawa in Ground 2. *See* Pet. 52–79. Furukawa’s Figure 3 is reproduced below.



Furukawa discloses, as shown in Figure 1, a recording head having heater 101, power transistor 102, and drive logic circuit 103 that “are mounted onto a board using multilayer wiring technology.” Ex. 1006, code (57). Power supply line 105 is provided in a second layer under power transistor 102 and GND line 110 is provided in the second layer under drive logic circuit 103. *Id.* Heater 101 is connected to power supply line 105 via wiring 106 that is connected to the second layer, and heater 101 is also connected to power transistor 102 is via wiring 107 that is connected to the first layer. *Id.*

D. *Unpatentability Analysis*

1. *Obviousness Based on Torgerson and Bruce*

Petitioner argues that claims 1–5 and 8 would have been obvious over Torgerson and Bruce. Pet. 18–52. Based on Petitioner’s analysis and for the

reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge. Patent Owner raises several arguments contesting Petitioner's challenge. We discuss those arguments below.

a. Petitioner's Proposed Combination of Torgerson and Bruce

In its first ground, Petitioner relies on Torgerson for teaching claim 1's semiconductor substrate, micro-fluid ejection actuators, logic circuits, power transistors, and first metal conductor layer. *See* Pet. 18–52. According to Petitioner, “Torgerson disclose[s] all limitations of claim 1 except for placing a ground conductor in the second metal layer in overlapping relationship with at least a portion of the logic circuit area.” *Id.* at 41. However, according to Petitioner, Bruce teaches this claimed ground-conductor configuration and “it would have been obvious for a [skilled artisan] to implement Bruce's second-metal-layer ground conductor in Torgerson.” *Id.* at 40. Petitioner explains that a skilled artisan would have found it obvious to do so for several reasons. First, given the need to reduce substrate size, Petitioner contends there are two basic options for placing the ground bus: 1) Torgerson's approach of making the first metal layer thicker and placing the ground bus only in the first metal layer, or 2) Bruce's approach of placing the ground bus in a second metal layer. *Id.* at 43; *see* Ex. 1007 ¶ 120. Petitioner explains that these two options are “predictable variation[s]” because, with the first option, “[t]he increased thickness (i.e., height) of the first metal layer means a smaller width can be used to retain the same area occupied by the ground bus,” whereas with the second option, “the ground bus can occupy a wider space in the second metal layer than what is available to it in the first metal layer without having to increase the

width of the substrate itself.” Pet. 43–44; *see* Ex. 1007 ¶¶ 120–122. On this record, we agree with Petitioner that Bruce’s approach would have been a one of “a finite number” of known, “predictable solutions,” and therefore obvious. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007). In addition, as Bruce explains, its approach offers certain advantages beyond reducing substrate size, including “(i) **reduced energy variation** due to decreased ground resistance resulting from the greater ground area”; (ii) “**avoid[ing] costs** associated with increased die sizes which result where ground resistance is decreased by widening ground paths in the first metal layer, with corresponding increases in the die size”; and (iii) “**increas[ing] the improvements in energy variation** that can be achieved by increasing the thickness of the second metal layer 11.” Pet. 54 (quoting Ex. 1005, 2:50–63). Given this analysis, at this stage, Petitioner has articulated sufficient reasoning with rational underpinning to support the legal conclusion that its proffered combination would have been obvious to one skilled in the art. *See KSR*, 550 U.S. at 418.

Patent Owner argues that Petitioner’s rationale for its combination fails for several reasons, none of which we find persuasive at this stage. For example, Patent Owner argues “[t]he primary goals of Torgerson and Bruce are quite different” because Torgerson teaches a power transistor configuration that addresses “varying parasitic resistance,” whereas Bruce’s configuration addresses “avoiding electrical noise.” Prelim. Resp. 42–43. We disagree with Patent Owner’s argument. To the extent Patent Owner is asserting Torgerson and Bruce are non-analogous art, clearly both are from the same field of endeavor as the ’341 patent because all three describe semiconductor substrates for ink-jet printheads. Pet. 42, Ex. 1007 ¶ 117.

Thus, Torgerson and Bruce are analogous to the '341 patent. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

Patent Owner also argues that Petitioner's rationale for combining fails because Torgerson's design already allows for "sufficient ground material as well as compactness." Prelim. Resp. 45; *see id.* at 44–46. Further, according to Patent Owner, Petitioner's proposed modification to Torgerson would "increase the size and complexity of Torgerson's substrate with no resulting benefit." *Id.* at 46. We disagree with these arguments. First, these arguments do not undermine Bruce's benefits related to energy variation, even if those benefits might come at a potential cost, as Patent Owner contends. *See Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) ("The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another."). Second, Petitioner does not need to show that replacing Torgerson's ground-bus design with Bruce's "was an improvement in a categorical sense." *See Intel Corp. v. Pact XPP Schweiz AG*, No. 2022-1037, slip. op. at 13 (Fed. Cir. Mar. 13, 2023) (internal quotation omitted). There is a motivation to combine when, as here, "a known technique 'has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way.'" *Id.* at 12 (quoting *KSR*, 550 U.S. at 417).

b. Torgerson's Polysilicon Conductor Layer

Claim 1 requires "a columnar array of logic circuits . . . connected through a polysilicon conductor layer to the power transistor." Ex. 1001, 6:55–58. Petitioner contends Torgerson teaches the claimed polysilicon

connection because “[a]s seen in Figure 9, the only connection that exists between the decoder logic circuit 35 (yellow) and the FET drive circuit 85 is the polysilicon gate fingers 91 (pink) connecting the decoder logic circuit 35 to the FET drive circuit 85.” Pet. 34 (emphasis omitted). Torgerson’s Figure 9 is reproduced below, with Petitioner’s annotations.

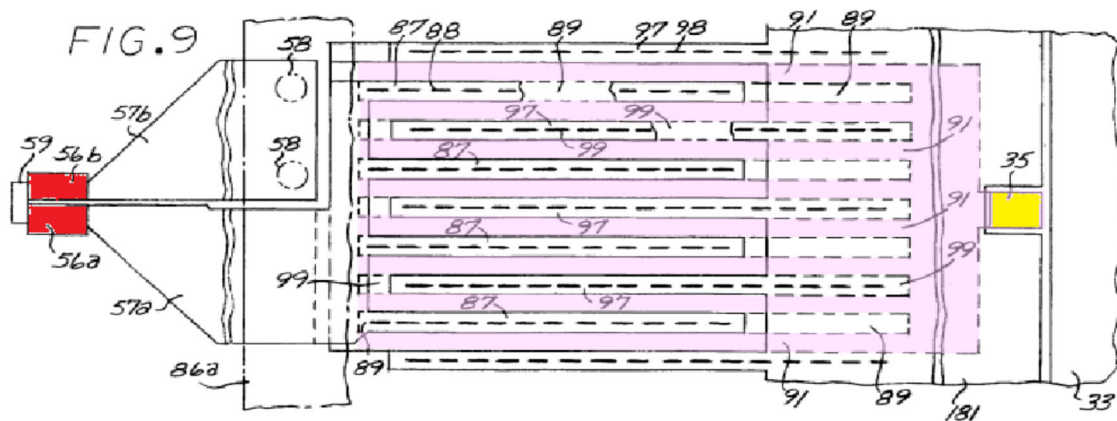


Figure 9 illustrates “a schematic plan view of an illustrative implementation of an FET drive circuit and a ground bus.” Ex. 1004, 2:42–44.

Patent Owner argues that Torgerson does not teach that its logic circuits are connected to power transistors through a polysilicon layer because Torgerson “does not indicate that the polysilicon in gate fingers 91 extends continuously to the logic cells 35,” but instead leaves the area to the right of its polysilicon fingers unlabeled. Prelim. Resp. 33–34. In addition, Patent Owner notes, Torgerson characterizes “the extent” of its polysilicon gate fingers 91 as “the same” as drain regions axis 89 and source regions 99. *Id.* at 36 (emphasis omitted).

At this stage, we disagree with Patent Owner’s argument. Figure 9 gives no indication that the polysilicon layer ends or changes to the right of the fingers labeled as reference number 91. To the contrary, as Petitioner notes, Torgerson characterizes its polysilicon gate fingers 91 as

“interconnected at respective ends.” Pet. 33 (quoting Ex. 1004, 7:40). In addition, Torgerson’s characterization of the fingers’ extent does not undermine that the polysilicon layer extends to the right of the fingers, out to the logic circuits, as claim 1 requires. Although the parties may wish to explore this issue further at trial, at this stage, Petitioner has shown sufficiently that Torgerson’s logic circuits are connected to power transistors through a polysilicon layer.

c. Ground 1 Summary

Other than the arguments addressed above, Patent Owner does not additionally challenge Petitioner’s obviousness analysis in its Preliminary Response. We have reviewed Petitioner’s arguments and the underlying evidence cited in support (*see* Pet. 18–52) and are persuaded that, at this stage, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1–5 and 8 would have been obvious over Torgerson and Bruce.

2. Obviousness Based on Furukawa, and Torgerson

In its second ground, Petitioner argues that claims 1–5 and 8 would have been obvious over Furukawa and Torgerson. Pet. 52–79. Based on Petitioner’s analysis and for the reasons explained below, we find Petitioner has, at this stage, demonstrated a reasonable likelihood of prevailing on this challenge. Patent Owner raises several arguments contesting Petitioner’s challenge. We discuss those arguments below.

a. Petitioner’s Proposed Combination of Furukawa and Torgerson

Petitioner relies on Furukawa for teaching claim 1’s semiconductor substrate, micro-fluid ejection actuators, logic circuits, and metal conductor layers. *See* Pet. 52–79. Because Furukawa “does not disclose the

connection between the power transistors and logic circuits as being through a polysilicon conductor layer,” Petitioner relies on Torgerson for teaching that feature. *Id.* at 68. Specifically, Petitioner explains that it would have been obvious for a skilled artisan “to modify the board (substrate) of Furukawa to use Torgerson’s FET drive circuits (85) as the power transistors and connect these power transistors to the logic circuit group of Furukawa via polysilicon connections.” *Id.* at 75. Petitioner asserts its modification would have been obvious because “a well-known advantage in the art of using FETs is that they provide better operational functions without requiring more space on the substrate.” *Id.* at 75–76. Further, Petitioner explains, “[w]hen FETs are used, those skilled in the art understand that it is common to connect the FETs to the logic groups via polysilicon, as described in Torgerson.” *Id.* at 76 (citing Ex. 1007 ¶ 220). Given this analysis, at this stage, Petitioner has articulated sufficient reasoning with rational underpinning to support the legal conclusion that its proffered combination would have been obvious to one skilled in the art. *See KSR*, 550 U.S. at 418.

Patent Owner argues that Petitioner’s rationale for its combination fails for several reasons, none of which we find persuasive at this stage. For example, Patent Owner argues that Petitioner’s proffered rationale—that FETs provide better operational functions without requiring more space—is conclusory and lacks support. We disagree because Petitioner’s expert Dr. Pond presents testimony, yet un rebutted, supporting Petitioner’s facially reasonable assertion, which is consistent with Torgerson’s teaching regarding FET’s size and operability. *See* Ex. 1007 ¶¶ 220–221; Ex. 1004, 7:49–51 (“The area occupied by each FET drive circuit is preferably small,

and the on-resistance of each FET drive circuit is preferably low.”). Patent Owner also argues that Petitioner “fails to establish why a [skilled artisan] would have been motivated to select polysilicon rather than a metal or other connection material” to connect the power transistors and logic circuits. Prelim. Resp. 59. We disagree with this argument because it does not matter whether polysilicon was a preferable connection material, so long as it was a known one. *See Intel Corp. v. Pact XPP Schweiz AG*, No. 2022-1037, slip. op. at 12–13. Dr. Pond’s testimony and Torgerson support that it was. Ex. 1007 ¶ 220; Ex. 1004, 7:39–40.

b. Whether Furukawa is Analogous Art

Patent Owner argues that Petitioner’s obviousness challenge fails because “Furukawa suggests a device constructed on a printed circuit board, not one in which the electrical circuits are integrated within a single semiconductor substrate.” Prelim. Resp. 56. According to Patent Owner, “[b]ecause Petitioners have not established that Furukawa is directed to semiconductor substrates for micro-fluid ejection devices, the Ground 2 challenge improperly relies on non-analogous art.” *Id.*

At this stage, we disagree with Patent Owner’s argument. As Petitioner’s expert, Dr. Pond, notes, Furukawa—an English translation of a Japanese patent application—states “[t]he thermoelectric conversion element (heater) and its drive circuit in such a recording head . . . is formed on the same board using semiconductor process technology.” Ex. 1006 ¶ 2, *see* Ex. 1007 ¶ 158. Dr. Pond presents testimony, unrebutted at this stage, that one skilled in the art would understand this passage “to mean forming those elements on a semiconductor substrate of the printhead.” Ex. 1007 ¶ 158. We agree with Dr. Pond’s reading of Furukawa. Thus, at this stage and on

the present record, we agree with Petitioner that one skilled in the art would understand that Furukawa is analogous art to the '341 patent. *See id.* ¶¶ 158, 216.

c. Ground 2 Summary

Other than the arguments addressed above, Patent Owner does not additionally challenge Petitioner's obviousness analysis in its Preliminary Response. We have reviewed Petitioner's arguments and the underlying evidence cited in support (*see* Pet. 52–79) and are persuaded that, at this stage, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1–5 and 8 would have been obvious over Furukawa and Torgerson.

III. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

IV. ORDER

It is hereby

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–5 and 8 of the '341 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '341 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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PETITIONER:

Dion M. Bregman
Amanda S. Williamson
Jason E. Gettleman
MORGAN, LEWIS & BOCKIUS LLP
dion.bregman@morganlewis.com
amanda.williamson@morganlewis.com
jason.gettleman@morganlewis.com

PATENT OWNER:

Timothy P. Maloney
Paul B. Henkelmann
Mark A. Borsos
David A. Gosse
FITCH, EVEN, TABIN & FLANNERY LLP
tim@fitcheven.com
phenkelmann@fitcheven.com
mborsos@fitcheven.com
dgosse@fitcheven.com