

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANON U.S.A., INC. and CANON INC.,
Petitioner,

v.

SLINGSHOT PRINTING LLC,
Patent Owner.

IPR2022-01414
Patent 7,195,341 B2

Before JO-ANNE M. KOKOSKI, GARTH D. BAER, and
JOHN D. HAMANN, *Administrative Patent Judges*.

BAER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Canon U.S.A., Inc. and Canon Inc. (together, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–5 and 8 (“the challenged claims”) of U.S. Patent No. 7,195,341 B2 (Ex. 1001, “the ’341 patent”). Slingshot Printing LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 5. Pursuant to 35 U.S.C. § 314, we instituted this *inter partes* review as to all of the challenged claims and all grounds raised in the Petition. Paper 6. Following institution, Patent Owner filed a Response. Paper 10 (“PO Resp.”). Petitioner filed a Reply to Patent Owner’s Response (Paper 12, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 13, “PO Sur-reply”). On January 23, 2024 we held an oral hearing. A transcript of the hearing is included in the record. Paper 19.

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision issued pursuant to 35 U.S.C. § 318(a). For the reasons we discuss below, we determine that Petitioner has proven by a preponderance of the evidence that the challenged claims are unpatentable.

B. Related Matters

The parties indicate that the ’341 patent is the subject of the following district court cases: *Slingshot Printing LLC v. Canon U.S.A., Inc., et al.*, No. 2:22-cv-00123 (E.D.N.Y.) and *Slingshot Printing LLC v. HP Inc.*, No. 6:19-cv-00549, reassigned as No. 2:20-00187 (W.D. Tex.) (dismissed). Pet. 1; Paper 3, 1.

Patent Owner indicates that Petitioner has filed the following concurrent petitions against patents that are asserted along with the ’341

patent in the district court case: IPR2022-01415 (U.S. Patent 7,559,629) and IPR2022-01416 (U.S. Patent 7,938,523). Paper 3, 1.

C. Real Parties in Interest

Petitioner identifies itself as the only real party in interest. Pet. 1.
Patent Owner identifies itself as the only real party in interest. Paper 3, 1.

D. The '341 patent

The '341 patent “relates to micro-fluid ejection head substrates and in particular to improved conductor layouts for reduced substrate size.” Ex. 1001, 1:6–8. Specifically, the '341 patent resolves the “need for improved substrate conductor routing and layouts that do not adversely affect the electrical properties of the circuits.” *Id.* at 1:33–36. Figure 1 is reproduced below.

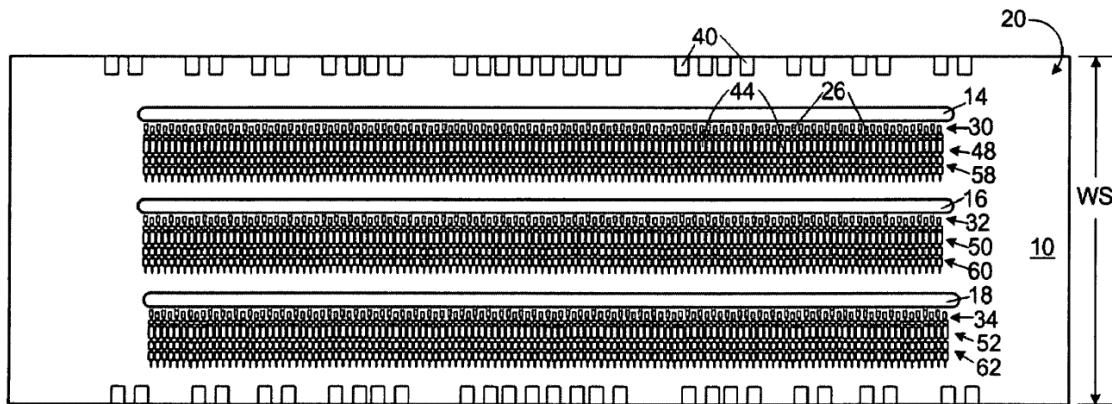


FIG. 1

Figure 1 depicts a semiconductor substrate “for micro-fluid ejection heads.” *Id.* at 2:38–39. Substrate 10 includes fluid supply slots 14, 16, and 18 for allowing flow of fluid, fluid ejection actuators 26 disposed in columnar arrays 30, 32, and 34 and adjacent to fluid supply slots 14, 16, and 18. *Id.* at 2:59–3:5. To selectively activate ejection actuators 26, “driver and control logic are also included on the device surfaces” of the substrate and “[t]he

control logic includes power and ground interconnections in a first metal conductor layer.” *Id.* at 3:13–17. Power transistors 44 are included in columnar arrays 48, 50, and 52 that are adjacent to columnar arrays 30, 32, and 34 and “[c]ontrol logic arrays 58, 60, and 62 are disposed adjacent” to power transistors 44. *Id.* at 3:23–30. The interconnection between control logic arrays 58, 60, and 62 and power transistors 44 “is in a polysilicon layer rather than in the first metal conductor layer or in a second metal conductor layer thereby eliminating the need for a three metal layer process for providing interconnections and power and ground buss routing to the devices.” *Id.* at 3:31–36. A power buss is routed over at least a portion of an active area for the power transistor array 48, 50, or 52 and a ground buss is disposed adjacent the power buss in the second metal conductive layer in which the ground buss overlies at least a portion of the control logic area. *Id.* at 5:48–50, 5:58–61, Fig. 8.

E. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claim 1 is reproduced below.

1. A semiconductor substrate for a micro-fluid ejection device, the substrate comprising:
 - a plurality of micro-fluid ejection actuators disposed in a columnar array adjacent a fluid supply slot in the semiconductor substrate;
 - a plurality of power transistors disposed in a columnar array adjacent the ejection actuators and connected through a first metal conductor layer to the ejection actuators, the columnar array of power transistors occupying a power transistor active area of the substrate;
 - a columnar array of logic circuits disposed adjacent the columnar array of power transistors and connected through a

polysilicon conductor layer to the power transistors, the columnar array of logic circuits occupying a logic circuit area of the substrate;

a power conductor for the ejection actuators routed in a second metal conductor layer disposed in overlapping relationship with at least a portion of the power transistor active area of the substrate; and

a ground conductor for the ejection actuators routed in the second metal conductor layer disposed in overlapping relationship with at least a portion of the logic circuit area of the substrate.

Ex. 1001, 6:45–67.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1–5, 8	103	Torgerson ¹ , Bruce ²
1–5, 8	103	Furukawa ³ , Torgerson

Pet. 3.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art would have had “at least a Bachelor’s or Master’s level college degree in Mechanical Engineering, Materials Science, Physics, Electrical Engineering, or a related field, and at least two years of training or experience in the design of inkjet printheads or semiconductor circuit layout.” Pet. 17–18 (citing Ex. 1007

¹ US 6,412,917 B1, issued July 2, 2002 (Ex. 1004, “Torgerson”).

² US 7,240,997 B2, issued July 10, 2007 (Ex. 1005, “Bruce”).

³ Certified English Translation of JP 1996-108536 A, published Apr. 30, 1996 (Ex. 1006, “Furukawa”).

¶ 58). Patent Owner does not propose a description of the level of ordinary skill in the art or dispute Petitioner’s description. PO Resp. 27. We agree with and adopt Petitioner’s description as it is consistent with the asserted prior art and the challenged patent’s specification. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill).

B. Claim Construction

Neither party proposes an express construction for any claim terms. Pet. 18; PO Resp. 28. We determine that no claim terms require express construction for us to determine unpatentability. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. Unpatentability Analysis

1. Obviousness Based on Torgerson and Bruce

Petitioner argues that claims 1–5 and 8 would have been obvious over Torgerson and Bruce. Pet. 18–52. For the reasons explained below, we find Petitioner has shown by a preponderance of evidence that the challenged claims would have been obvious over the asserted references.

a. Description of Prior Art References in Ground 1

(1) Torgerson (Ex. 1004)

Torgerson discloses an ink jet printhead having FET (field effect transistor) drive circuits that are configured to compensate for parasitic resistances of power traces, and ground busses that overlap active regions of the FET drive circuits. Ex. 1004, code (57). Figure 1A of Torgerson is

reproduced below.

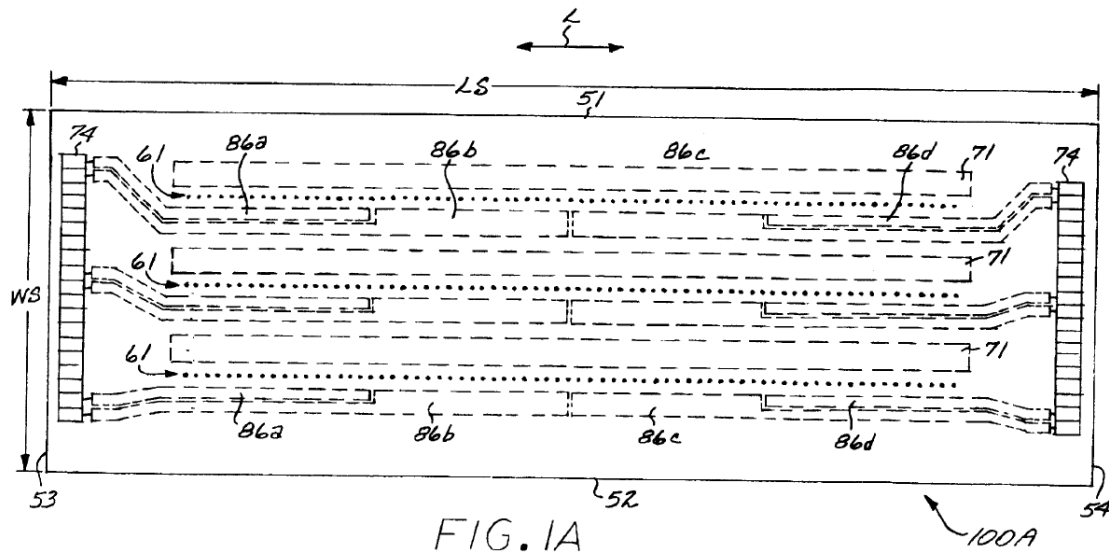


Figure 1A shows a “top plan view illustration of the layout of ink drop generators and primitive select of an ink jet printhead.” *Id.* at 2:9–11. Ink jet printhead 100A includes a thin film substructure “comprising a substrate such as silicon.” *Id.* at 2:57–62. Ink drop generators along with heat resistors “are arranged in columnar arrays or groups 61.” *Id.* at 3:66–4:5. The thin film substructure includes ink feed slots 71 that feed ink drop generator groups 61. *Id.* at 4:36–41. Columnar FET drive circuit arrays are “formed in the thin film substructure” and have circuits with drain electrodes connected to heat resistors. *Id.* at 4:66–5:6, Fig. 6. Ground busses and heater resistor leads “are formed in” a metallization layer of the thin film substructure as are the drain and source electrodes of the FET drive circuits. *Id.* at 5:19–22, Fig. 5. The ink drop generators of a columnar array 61 can be organized into four primitive groups with heater resistors thereof being “electrically connected to the same one of four primitive select traces 86a, 86b, 86c, 86d.” *Id.* at 5:43–50.

(2) *Bruce (Ex. 1005)*

Bruce is directed to a fluid ejection device with two metal layers. Ex. 1006, code (57). Bruce's Figure 1 is reproduced below.

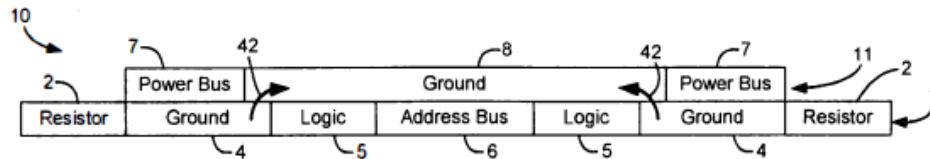


Figure 1 is “a block diagram of relative positions of metal portions of an exemplary embodiment of a fluid ejection device.” *Id.* at 1:32–34. As Figure 1 shows, Bruce teaches a second-metal-layer ground portion that overlies logic portions. *See id.* at 2:40–63, Fig. 1.

b. Claim 1

Petitioner relies on Torgerson for teaching nearly all of claim 1's structural elements. *See* Pet. 18–52. Specifically, Petitioner asserts as follows:

Torgerson discloses “a **plurality of power transistors** [e.g., FET drive circuits 85] disposed in a **columnar array** [e.g., columnar array 81 as shown in Fig. 6] adjacent the **ejection actuators** [e.g., heater resistors 56] and connected through a **first metal conductor layer** [e.g., first metallization layer 111d] to the **ejection actuators** [e.g., heater resistors 56], the columnar array of power transistors occupying a **power transistor active area** . . . of the **substrate** [e.g., die 11 comprising a substrate such as silicon].”

Id. at 29 (citing Ex. 1007 ¶¶ 77–84). Petitioner further corresponds Torgerson's “**decoder logic circuits 35**” to the claimed logic circuits (*id.* at 30), Torgerson's “**primitive select traces 86a, 86b, 86c, 86d**” to the claimed power conductor (*id.* at 35), and Torgerson's “**ground bus 181**” to the

claimed ground conductor (*id.* at 39). According to Petitioner, “Torgerson disclose[s] all limitations of claim 1 except for placing a ground conductor in the second metal layer in overlapping relationship with at least a portion of the logic circuit area.” *Id.* at 41. However, according to Petitioner, Bruce teaches this claimed ground-conductor configuration and “it would have been obvious for a [skilled artisan] to implement Bruce’s second-metal-layer ground conductor in Torgerson.” *Id.* at 40.

*(1) Petitioner’s Rationale for Combining
Torgerson and Bruce*

Petitioner explains that a skilled artisan would have found it obvious to implement Bruce’s second-metal-layer ground conductor in Torgerson’s substrate for several reasons. First, given the need to reduce substrate size, Petitioner contends there are two basic options for placing the ground bus: 1) Torgerson’s approach of making the first metal layer thicker and placing the ground bus only in the first metal layer, or 2) Bruce’s approach of placing the ground bus in a second metal layer. Pet. 43; *see* Ex. 1007 ¶ 120. Petitioner explains that these two options are “predictable variation[s]” because, with the first option, “[t]he increased thickness (i.e., height) of the first metal layer means a smaller width can be used to retain the same area occupied by the ground bus,” whereas with the second option, “the ground bus can occupy a wider space in the second metal layer than what is available to it in the first metal layer without having to increase the width of the substrate itself.” Pet. 43–44; *see* Ex. 1007 ¶¶ 120–122.

In addition, as Petitioner notes and Bruce explains, Bruce’s approach offers certain advantages beyond reducing substrate size, including (i) “**reduced energy variation** due to decreased ground resistance resulting from the greater ground area”; (ii) “**avoid[ing] costs** associated with

increased die sizes which result where ground resistance is decreased by widening ground paths in the first metal layer, with corresponding increases in the die size”; and (iii) “**increas[ing] the improvements in energy variation** that can be achieved by increasing the thickness of the second metal layer 11.” Pet. 44–45 (quoting Ex. 1005, 2:50–63).

Patent Owner argues that Petitioner’s rationale for its combination fails for several reasons, none of which we find persuasive. First, Patent Owner argues “[t]he primary goals of Torgerson and Bruce are quite different” because Torgerson teaches a power transistor configuration that addresses “varying parasitic resistance,” whereas Bruce’s configuration addresses “avoiding electrical noise.” PO Resp. 44. We disagree with Patent Owner’s argument. To the extent Patent Owner is asserting Torgerson and Bruce are non-analogous art, clearly both are from the same field of endeavor as the ’341 patent because they, like the ’341 patent, describe semiconductor substrates for ink-jet printheads. Pet. 42; Ex. 1007 ¶ 117. Thus, Torgerson and Bruce are analogous to the ’341 patent. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

Patent Owner also argues that Petitioner’s rationale for combining fails because Torgerson’s design “already provides sufficient ground as well as the flexibility to adjust the amount of ground conductor in the same layer as necessary.” PO Resp. 47. Patent Owner faults Petitioner for “provid[ing] no analysis of how relocating [Torgerson’s] ground material to a layer above the logic circuit area would provide more ground area, or even adequate ground area, compared to the design actually disclosed in Torgerson.” *Id.* at 47–48.

These arguments, however, do not undermine that Bruce’s approach is an obvious design choice because it is one of just two basic options for placing the ground bus. In addition, Patent Owner’s arguments do not undermine Bruce’s benefits related to energy variation, even if those benefits might come at the potential cost to flexibility as Patent Owner contends. *See Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) (“The fact that the motivating benefit comes at the expense of another benefit, however, should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another.”). Lastly, we disagree with Patent Owner because Petitioner does not need to show that Bruce’s ground-layer design “was an improvement in a categorical sense” over Torgerson’s, so long as Bruce’s technique was known and one skilled in the art would understand that implementing it had advantages. *See Intel Corp. v. Pact XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023) (quotation marks omitted); *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004) (“[O]ur case law does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art.”).

In sum, given the benefits related to energy variation, size, and cost, Petitioner has articulated sufficient reasoning with rational underpinning to support the legal conclusion that its proffered combination would have been obvious to one skilled in the art. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). We also agree with Petitioner that Bruce’s approach would have been one of “a finite number” of known, “predictable solutions,” and therefore obvious. *See id.* at 420.

(2) Torgerson's Polysilicon Conductor Layer

Claim 1 requires “a columnar array of logic circuits . . . connected through a polysilicon conductor layer to the power transistor.” Ex. 1001, 6:55–58. Petitioner contends Torgerson teaches the claimed polysilicon connection because “[a]s seen in Figure 9, the only connection that exists between the decoder logic circuit 35 (yellow) and the FET drive circuit 85 is the polysilicon gate fingers 91 (pink) connecting the decoder logic circuit 35 to the FET drive circuit 85.” Pet. 34 (emphasis omitted). Torgerson's Figure 9 is reproduced below, with Petitioner's annotations.

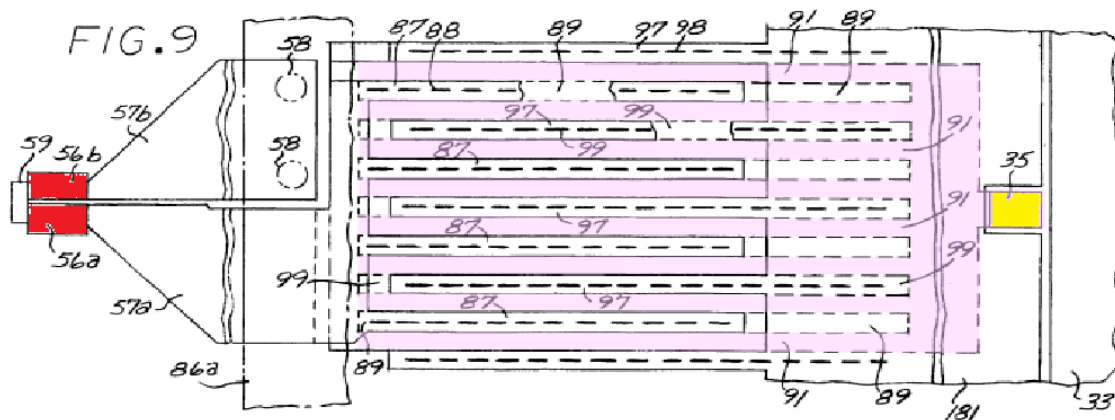


Figure 9 illustrates “a schematic plan view of an illustrative implementation of an FET drive circuit and a ground bus.” Ex. 1004, 2:42–44.

Patent Owner argues that Torgerson does not teach that its logic circuits are connected to power transistors through a polysilicon layer because Torgerson “does not indicate that the polysilicon extends continuously to the logic cells 35,” but instead leaves the area to the right of its polysilicon fingers unlabeled. PO Resp. 34–35. In addition, Patent Owner notes, Torgerson characterizes “**the extent**” of its polysilicon gate fingers 91 as “**the same**” as drain regions axis 89 and source regions 99. *Id.* at 36.

We disagree with Patent Owner’s argument. Torgerson’s Figure 9 gives no indication that the polysilicon layer ends or changes to the right of the fingers labeled as reference number 91. To the contrary, as Petitioner notes, Torgerson characterizes its polysilicon gate fingers 91 as **“interconnected at respective ends.”** Pet. 33 (quoting Ex. 1004, 7:40). Petitioner’s expert, Dr. Pond, explained that “as a practical matter,” a skilled artisan would understand that “it’s necessary” that Torgerson’s polysilicon gate fingers 91 extend to its logic circuits. Ex. 2002, 62:3–7. In addition, Torgerson’s characterization of the fingers’ extent does not undermine that the polysilicon layer extends to the right of the fingers, out to the logic circuits, as claim 1 requires. Based on Petitioner’s analysis and for the reasons outlined above, we agree with Petitioner that Torgerson’s logic circuits are connected to power transistors through a polysilicon layer.

(3) Claim 1 Summary

Other than the arguments addressed above, Patent Owner does not additionally challenge Petitioner’s obviousness analysis. We have reviewed Petitioner’s arguments and evidence (*see* Pet. 18–45) and, based on that analysis, we find Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Torgerson and Bruce.

c. Dependent Claims 2–5 and 8

Petitioner asserts Torgerson teaches the additional features recited in dependent claims 2–5 and 8. Pet. 45–52. Specifically, Petitioner corresponds Torgerson’s heater resistors 56 to claim 2’s heater resistors (*id.* at 45), Torgerson’s three ink feed slots 71 to claim 3’s three fluid supply slots (*id.* at 46), Torgerson’s FET drive circuits 85 to claim 4’s field effect transistors, Torgerson’s logic decoder circuits 35 to claim 5’s primitive

address logic and predrive circuits (*id.* at 50–51), and Torgerson’s printhead 100A to claim 8’s micro-fluid ejection head (*id.* at 51–52). Other than the arguments addressed above for claim 1, Patent Owner does not additionally challenge Petitioner’s obviousness challenge to claims 2–5 and 8. We have reviewed Petitioner’s arguments and evidence (*see id.* at 45–52) and, based on that analysis, we find Petitioner has shown by a preponderance of the evidence that claims 2–5 and 8 would have been obvious over Torgerson and Bruce.

2. Obviousness Based on Furukawa and Torgerson

In its second ground, Petitioner argues that claims 1–5 and 8 would have been obvious over Furukawa and Torgerson. Pet. 52–79. Because we have already determined these same claims would have been obvious based on Petitioner’s first asserted ground, we decline to reach Petitioner’s alternative challenge based on Furukawa and Torgerson.

III. CONCLUSION

For the foregoing reasons, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1–5 and 8 of the '341 patent are unpatentable.⁴ Our conclusions are summarized in the following table.

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1–5, 8	103	Torgerson, Bruce	1–5, 8	
1–5, 8	103	Furukawa, Torgerson ⁵		
Overall Outcome			1–5, 8	

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–5 and 8 of the '341 patent are unpatentable;
and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁴ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

⁵ We do not reach this ground because it would not change the outcome of this case.

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