

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANON U.S.A., INC. and CANON INC.,
Petitioner,

v.

SLINGSHOT PRINTING LLC,
Patent Owner.

IPR2022-01415
Patent 7,559,629 B2

Before JO-ANNE M. KOKOSKI, JON B. TORNQUIST, and
JOHN D. HAMANN, *Administrative Patent Judges*.

HAMANN, Administrative Patent Judge.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Canon U.S.A., Inc. and Canon Inc. (collectively “Petitioner”) filed a petition for *inter partes* review of claims 1–10, 13, and 14 of U.S. Patent No. 7,559,629 B2 (Ex. 1001, “the ’629 patent”). Paper 2 (“Pet.”). Slingshot Printing LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

We have authority to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 (2018) and 37 C.F.R. § 42.4(a) (2022). An *inter partes* review may be instituted if “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

Upon consideration of the papers, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing that at least one challenged claim is unpatentable. Accordingly, we deny the Petition and do not institute *inter partes* review.

A. *Real Parties-In-Interest*

The parties identify themselves as the real parties-in-interest. Pet. 1; Paper 5, 1.

B. *Related Matters*

The parties identify *Slingshot Printing LLC v. Canon U.S.A., Inc.*, No. 2:22-cv-00123 (E.D.N.Y.) and *Slingshot Printing LLC v. HP Inc.*, No. 1:20-00187 (W.D. Tex.) (“HP litigation”) as matters that may affect, or be affected by, a decision in this proceeding. Pet. 1; Paper 5, 2.

C. The '629 Patent

The '629 patent relates “to printer heads, and more particularly to methods and apparatuses for implementing multi-via heater chips.” Ex. 1001, 1:7–9. The '629 patent discloses that “[a] number of printers, copiers, and multi-function products utilize heater chips in their printing heads for discharging ink drops from one or more ink vias.” *Id.* at 1:13–15. “These heater chips typically provide only one heater array for each ink via that is disposed along one side of the ink via.” *Id.* at 1:15–17. The '629 patent discloses that “[e]ach of these heater arrays may include a plurality of individual heaters fabricated as resistors in the heater chips.” *Id.* at 3:60–63. “When the heaters in the heater arrays are activated, they provide thermal energy to the ink via, and the ink is discharged.” *Id.* at 4:2–4.

According to the '629 patent, “the traditional use of [a] single heater array on a single side of an ink via limits the achievable printing resolution, including the vertical resolution.” *Id.* at 1:23–25. The '629 patent further discloses that “connections between . . . logic arrays and the heater arrays they address occupy a significant amount of space on the heater chips.” *Id.* at 1:30–32. “Accordingly, there is a need in the industry for heater chips that can provide for enhanced printing resolutions while reducing chip die sizes,” according to the '629 patent. *Id.* at 1:42–44.

To address this need, the '629 patent teaches having heater arrays “positioned on both sides of at least a portion of the ink vias, which allow[s] the ink vias to provide smaller ink drops in order to achieve higher printing resolutions.” *Id.* at 3:57–60. And “when heater arrays are positioned on both sides of vias in a multi-via heater chip, at least two heater arrays may be adjacent to each other.” *Id.* at 4:5–7. Thus, “a single, hybrid

non-contiguous logic array may be disposed between adjacent heater arrays for addressing the adjacent heater arrays.” *Id.* at 4:7–10. According to the ’629 patent, “[t]his configuration reduces the area needed for the logic arrays, thereby allowing for a much smaller die size compared to the use of the wiring buses of” a traditional heater chip. *Id.* at 3:29–31, 4:10–13.

Figure 3, shown below, illustrates this configuration. *Id.* at 3:29–31.

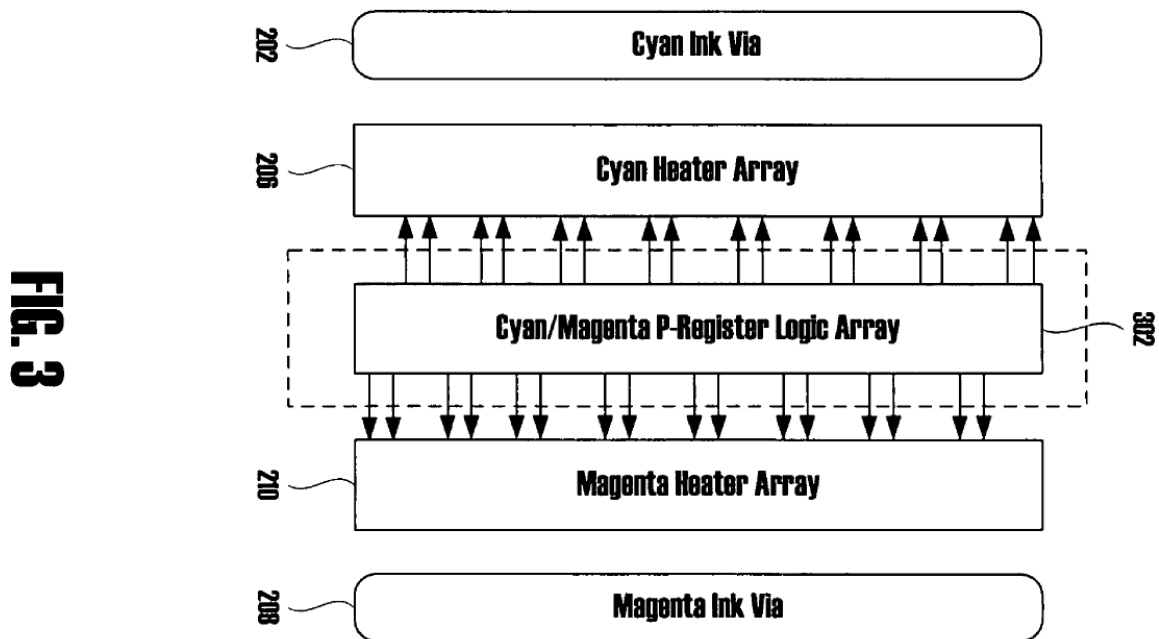


Figure 3 “illustrates an exemplary configuration for a single hybrid, non-contiguous P-register logic array between two heater arrays, according to an embodiment of the” ’629 patent. *Id.* at 3:35–38. As illustrated, this embodiment is “configured to interleave a portion of the cyan P-register logic array 226 with a portion of the magenta P-register logic array 228 to form a single hybrid cyan/magenta P-register logic array 302 positioned between the second cyan heater array 206 and the first magenta heater array 210.” *Id.* at 5:47–53. “According to an exemplary embodiment, the hybrid cyan/magenta P-register logic array 302 may include logic cells providing a[] total of 32 bits—16 bits for addressing eight groups of 40 heaters (a total

of 320 heaters) in the second cyan heater array 206 and 16 bits for addressing eight groups of 40 heaters (a total of 320 heaters) in the first magenta heater array 210.” *Id.* at 5:53–59.

Figure 4 of the '629 patent is shown below.

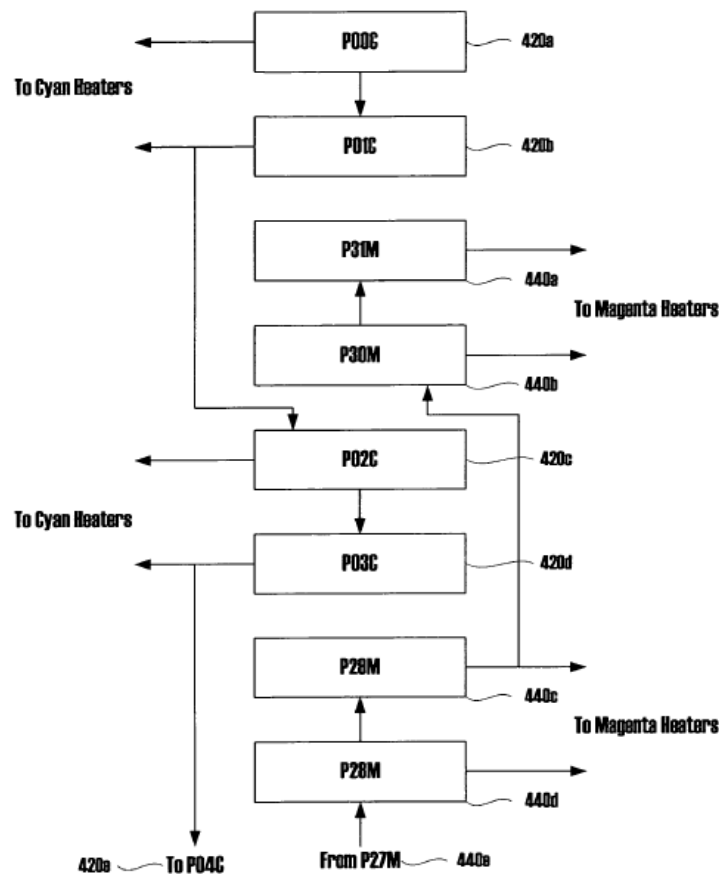


FIG. 4

Figure 4 “shows a configuration of the logic cells for the hybrid cyan/magenta P-register logic array 302 of F[igure] 3 according to an exemplary embodiment of the” ’629 patent. *Id.* at 5:60–63. More specifically, “F[igure] 4 illustrates a plurality of cyan logic cells 420a–n interleaved with the magenta logic cells 440a–n in such a way as to minimize the space necessary between the second cyan heater array 206 and the first magenta heater array 210.” *Id.* at 5:63–67. In particular, “the

magenta logic cells 440a–n [are] interleaved between the cyan logic cells 420a–n in an alternating manner to form a single, linear hybrid cyan/magenta P-logic array 302.” *Id.* at 6:1–4. “Because of this interlacing of cyan P-registers 420a–n and magenta P-registers 440a–n, neither the cyan P-registers 420a–n nor the magenta P-registers 440a–n remain contiguous.” *Id.* at 6:10–13. For this exemplary embodiment, “each pair in logic cells 420a–n or 440a–n . . . may address a block of 40 heaters in the respective heater rays 206 and 210, respectively, according to an exemplary embodiment.” *Id.* at 6:6–10.

D. Illustrative Claim

Of the challenged claims, claims 1 and 8 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below.

1. A chip for use in a printing device, comprising:
 - a first heater array with a left side and a right side;
 - a first ink via placed on the left side of the first heater array;
 - a second heater array with a left side and a right side, wherein a right side of the first heater array faces the left side of the second heater array;
 - a second ink via placed on the right side of the second heater array; and
 - at least one logic array including a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement, the at least one logic array is disposed substantially between the first heater array and the second heater array, wherein the first set of logic cells addresses and controls the first heater array and the second set of logic cells addresses and controls the second heater array, which allows the first ink via and second ink via to be simultaneously controlled by the at least one logic array, and wherein the at least one logic array is substantially parallel with the first heater array and second heater array.

Ex. 1001, 8:12–31.

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims of the '629 patent are unpatentable based on the following grounds:

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)
1–10, 13, 14	102	Hayasaki ²
1–10, 13, 14	103	Hayasaki, Silverbrook ³
1–10, 13, 14	103	Hayasaki, Krouss ⁴

Pet. 3, 17–101. Petitioner submits the Declaration of Charles M. Curley (Ex. 1007) in support of its arguments.

II. LEVEL OF ORDINARY SKILL IN THE ART

To determine whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–63 (Fed. Cir. 1986)). “[O]ne or more factors may predominate.” *Id.*

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. §§ 102 and 103 that became effective on March 16, 2013. Because the '629 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of these bases for unpatentability.

² US 2004/0201639 A1, published Oct. 14, 2004 (Ex. 1004, “Hayasaki”).

³ US 2003/0020784 A1, published Jan. 30, 2003 (Ex. 1005, “Silverbrook”).

⁴ US 6,190,000 B1, issued Feb. 20, 2001 (Ex. 1012, “Krouss”).

Petitioner argues that one of ordinary skill in the art at the time of the invention of the '629 patent would have had “at least a Bachelor’s level college degree in Mechanical Engineering, Electrical Engineering, Physics, Computer Science or a related field, and at least two years of training or experience in the design of inkjet printheads.” Pet. 14–15 (citing Ex. 1007 ¶ 45). Patent Owner does not identify a level of skill in the art that one would have had at the time of the invention of the '629 patent or identify any shortcoming in Petitioner’s formulation. *See* Prelim. Resp. 42–43.

For purposes of this Decision on Institution, we adopt Petitioner’s definition of the level of skill for one of ordinary skill in the art, except we decline to adopt the recitals of “at least” as that language is vague and open-ended. Pet. 14–15. This definition is consistent with the '629 patent and the asserted prior art, and we apply it in our analysis below.

III. CLAIM CONSTRUCTION

Because the Petition was filed after November 13, 2018, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), following the standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019); 83 Fed. Reg. 51,340, 51,340–41, 51,343 (Oct. 11, 2018). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic*

Sofamor Danek, Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

The parties both argue that we should construe “non-contiguous hybrid arrangement” to mean “[a]n arrangement in which the first set of logic cells are interleaved or interlaced with the second set of logic cells.” Pet. 15; Prelim. Resp. 43. Petitioner supports its argument by pointing to the claim construction order from the HP litigation, which provides this construction for this term. Pet. 15 (citing Ex. 1010, 4 (construing non-contiguous hybrid arrangement)).

Patent Owner supports its argument by citing to the written description and figures of the ’629 patent. Prelim. Resp. 43–46 (citations omitted). For example, Patent Owner cites Figure 4 of the challenged patent, and its accompanying text, and argues that Figure 4 illustrates that the “logic cells [are] interleaved in a manner that minimizes the space between heater arrays by forming a single linear array.” *Id.* at 44 (citing Ex. 1001, Fig. 4). The accompanying text teaches that “the magenta logic cells 440a–n may be interleaved between the cyan logic cells 420a–n in an alternating manner to form a single, linear hybrid cyan/magenta P-logic array 302.” Ex. 1001, 5:67–6:4; Prelim. Resp. 45 (citing same). The ’629 patent adds that “[b]ecause of this interlacing of cyan P-registers 420a–n and magenta P-registers 440a–n, neither the cyan P-registers 420a–n nor the magenta P-registers 440a–n remain contiguous,” and that “[f]or example, in F[igure] 4, the cyan logic cell 420b is followed by the magenta logic cell 440a instead of the next cyan logic cell 420c.” Ex. 1001, 6:10–15; Prelim. Resp. 45 (citing same).

We have reviewed the parties' arguments, and we adopt the parties' proposed construction for this term. In addition, we determine that no express construction is needed for any other term for us to render our Decision on Institution. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”).

IV. PRINCIPLES OF LAW

A claim is unpatentable under 35 U.S.C. § 102 “if each and every [claim] limitation is found either expressly or inherently in a single prior art reference.” *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1273 (Fed. Cir. 2017). “A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present.” *Akamai Techs., Inc. v. Cable & Wireless Internet Servs., Inc.*, 344 F.3d 1186, 1192 (Fed. Cir. 2003) (citing *Rosco, Inc. v. Mirror Lite, Co.*, 304 F.3d 1373, 1380 (Fed. Cir. 2002)).

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence

of non-obviousness, if present.⁵ *See Graham*, 383 U.S. at 17–18. When evaluating a claim for obviousness, we also must “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

V. ALLEGED ANTICIPATION BY HAYASAKI

Petitioner argues that Hayasaki anticipates claims 1–10, 13, and 14. Pet. 17–70. We have reviewed the parties’ arguments and the evidence of record. For the reasons that follow, we determine that Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that Hayasaki anticipates at least one of these claims of the ’629 patent.

A. *Summary of Hayasaki*

Hayasaki relates to “a printhead substrate, printhead and printing apparatus having a multi-ink channel capable of supplying a plurality of different colored ink concurrently to a single substrate used to carry out printing according to an inkjet printing method.” Ex. 1004 ¶ 2. Moreover, Hayasaki teaches a printhead substrate that “is capable of controlling the driving of a larger number of printing elements in a reduced surface area.”

Id. ¶ 24. Hayasaki describes its invention as providing the following:

[A] printhead substrate capable of controlling the driving of a large number of printing elements in a reduced surface area, . . . configured so that a plurality of ink supply channels are disposed in parallel on the substrate, [and] includes a plurality of printing element arrays composed of a plurality of printing elements disposed alongside each of the plurality of ink supply channels, a plurality of drive control circuits disposed in an area

⁵ Patent Owner does not present arguments or evidence of such objective evidence of non-obviousness. *See generally* Prelim. Resp.

between the plurality of ink supply channels that control the driving of each of the plurality of printing element arrays, and shared wiring portions disposed in the area between the plurality of ink supply channels and shared by the plurality of drive control circuits.

Id. at code (57). Hayasaki teaches that “by adopting a layout that disposes, in an area between two ink channels on the head substrate, a dedicated circuit block that controls each of two printing element arrays . . . , signal lines associated with the circuit block, and shared signal lines for controlling the printing element arrays . . . , the head substrate can be used more efficiently, and further, the area of the head substrate can be further downsized.” *Id.* ¶ 111.

Hayasaki’s Figure 9, shown below, illustrates such a layout.

FIG. 9

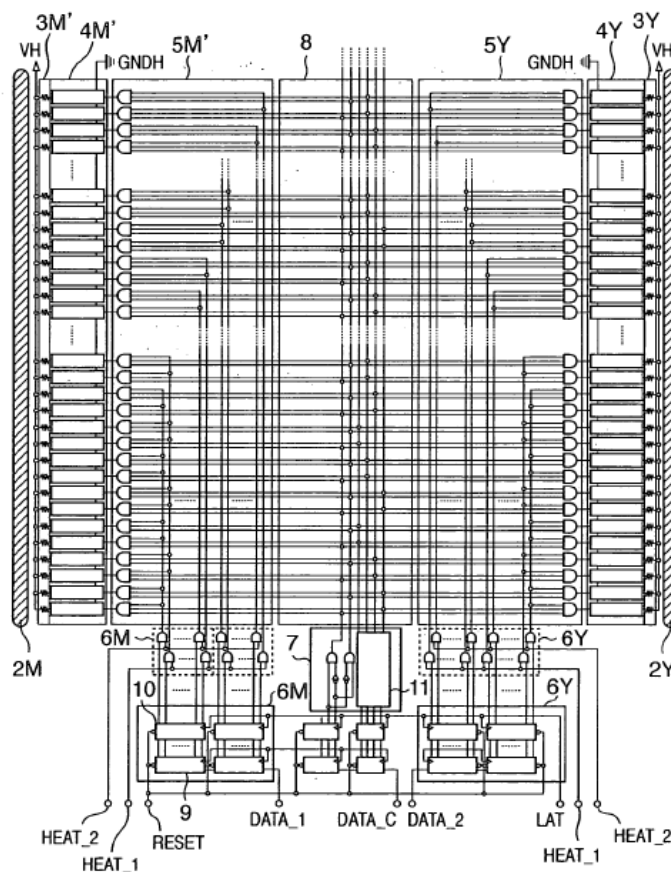


Figure 9 is a “circuit diagram showing the drive control configuration of a head substrate having” a layout “integrating twice the number of printing elements of [a] typical head substrate.” *Id.* ¶¶ 36, 38. As shown, “control wires and AND circuit arrays 5M’ and 5Y . . . enable individual control of” the “elements of the printing element arrays 3M’ and 3Y.” *Id.* ¶ 93.

B. Arranged in a Non-Contiguous Hybrid Arrangement

Petitioner argues that Hayasaki discloses “a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement,” as recited in claim 1. Pet. 25–33. For the reasons discussed below, we find that Petitioner does not show that Hayasaki discloses this limitation.

Petitioner argues that one of ordinary skill in the art would have understood that an AND gate is a type of logic cell, and that Hayasaki’s AND gates comprise logic cells. *Id.* at 27–28 (citing Ex. 1007 ¶ 108; Ex. 1004 ¶ 93). We agree. We also agree with Petitioner that Hayasaki’s columns of AND gates (i.e., AND circuit array 5M’ and AND circuit array 5Y) correspond to a first and a second set of logic cells, respectively.⁶ Pet. 25–26; Ex. 1004 ¶¶ 87, 93, 104–106, Fig. 9; Ex. 1007 ¶¶ 109–112.

However, we agree with Patent Owner that Hayasaki does not disclose that AND circuit array 5M’ and AND circuit array 5Y are arranged in a non-contiguous hybrid arrangement. Prelim. Resp. 51–52, 54–63. Rather, Hayasaki’s AND gates are arranged in a grid, with each magenta

⁶ Petitioner argues that “‘a first and a second set of logic cells’ is indefinite because it is unclear if this requires (i) a first set of logic cells and a second set of logic cells, (ii) first and second sets of logic cells, or (iii) a set of first logic cells and second logic cells.” Pet. 30 n.5. We disagree. The plain reading of this limitation corresponds to a first set of logic cells and a second set of logic cells, which is in accord with the interpretation Petitioner applies in this proceeding. *Id.*

AND gate of AND circuit array 5M' located directly aligned with the corresponding yellow AND gate of AND circuit array 5Y—they are not interleaved or interlaced. Ex. 1004, Fig. 9. Put differently, Hayasaki teaches that AND circuit array 5M' and AND circuit array 5Y comprise two separate columns of logic cells that are not interleaved or interlaced. *See* Ex. 1004, Fig. 9, ¶ 93. Thus, Hayasaki does not teach sets of logic cells in a non-contiguous hybrid arrangement.

We find unavailing Petitioner's argument that claim 1's "preamble ends in the term 'comprising,'" and "[t]hus, although the claim requires the first set of logic cells are interleaved or interlaced with the second set of logic cells, **the claim is not restricted to a device that only has interleaved or interlaced logic cells**, i.e., the prior art may disclose other logic cells that are not relevant to the claims." Pet. 31. Petitioner illustrates its argument by annotating Figure 9, as shown below.

FIG. 9

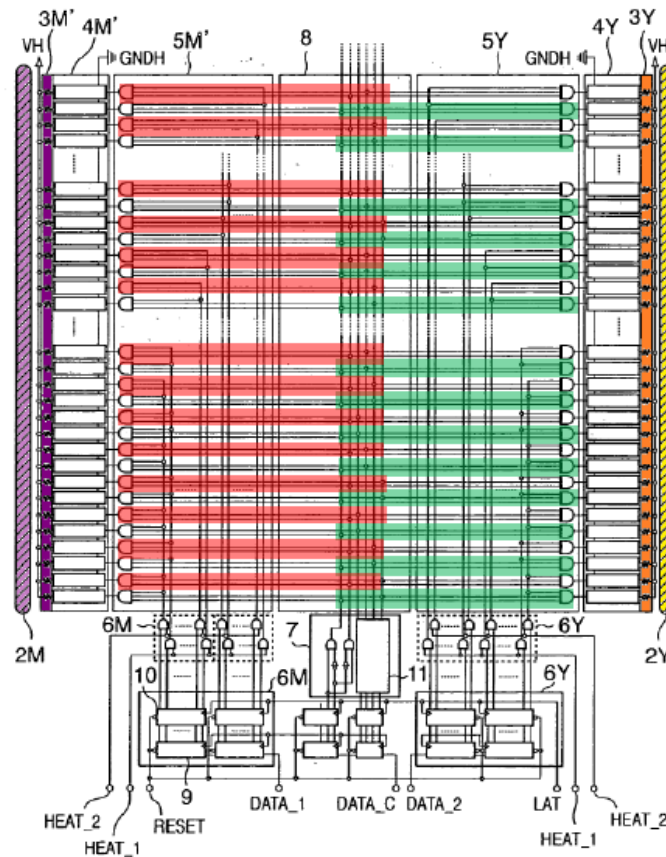


Figure 9 is a “circuit diagram showing the drive control configuration of a head substrate” in accordance with Hayasaki’s teachings. *Id.* ¶¶ 36, 38. Petitioner annotates Figure 9 in relevant part by coloring the odd (i.e., the first, third, fifth, etc.) AND gates of AND circuit array 5M’ red and the even (i.e., second, fourth, sixth, etc.) AND gates of AND circuit array 5Y green. Pet. 32 (annotating Ex. 1004, Fig. 9).

Petitioner argues that Hayasaki’s Figure 9 “discloses numerous logic cells that are interleaved or interlaced with one another because it shows no less than fourteen pairs of interleaved logic cells, each including a **first set of logic cells (red boxes)** interleaved with a **second set of logic cells (green boxes)**.” *Id.* at 31 (citing Ex. 1004, Fig. 9; Ex. 1007 ¶¶ 115–116). “In other

words, as seen in annotated Figure 9 above, Hayasaki discloses a first set of logic cells (red boxes) and a second set of logic cells (green boxes) that are arranged in a **non-contiguous hybrid arrangement** as that term is properly construed,” according to Petitioner. *Id.* at 32–33 (citing Ex. 1007 ¶¶ 117–122).

We disagree with Petitioner that the selectively highlighted alternate AND gates from two separate columns of aligned AND gates evidence that Hayasaki discloses interleaving or interlacing AND gates. Selectively pairing odd and even AND gates does not change the structure of Hayasaki’s AND circuit arrays 5M’ and 5Y—each AND gate in array 5M’ has an AND gate in array 5Y to which it is directly aligned. *See* Ex. 1004, Fig. 9. Nor do we find availing Petitioner’s argument that “comprising” allows for the prior art to disclose other logic cells that are not relevant to the claims. Pet. 31. While we agree as to the meaning of comprising, there still is no teaching in Hayasaki of interleaved or interlaced logic cells. Ex. 1004, Fig. 9. Again, the structure of arrays 5M’ and 5Y is unchanged.

In addition, Petitioner does not explain sufficiently why shared wiring for inputs to the AND gates should be deemed part of the logic cells. *See* Pet. 25–26, 29. In particular, we do not view as sufficient Petitioner’s argument, which repeats Mr. Curley’s testimony, that the AND circuit arrays and their “respective portion[s] of [the] wiring 8” “correspond to the claimed ‘at least one logic array’ because they all work together to provide output logic and address and control the plurality of printing elements.” *Id.* at 29 (citing Ex. 1004 ¶¶ 93, 104–106; Ex. 1007 ¶ 111). Rather, we find that this argument is conclusory as to why the cited shared wiring should be included

as part of the logic cells, and inconsistent with the '629 patent, which treats such wiring as distinct from the logic arrays. *See, e.g.*, Ex. 1001, 1:30–37.

We also find unavailing Petitioner's argument that Hayasaki "operates its printing elements in an alternating or interleaved manner," and that "in operation, no adjacent logic cells in each of the AND circuit arrays 5M' and 5Y are operational at the same time to avoid cross-talk phenomenon, which is consistent with the depiction of the claimed first set of logic cells (red boxes) and the second set of logic cells (green boxes)." Pet. 33 (citing Ex. 1004 ¶ 95; Ex. 1007 ¶¶ 120–122). As Patent Owner argues, how Hayasaki operates does not change the structure of AND circuit arrays 5M' and 5Y, as depicted in Figure 9, and more particularly, that the AND gates of arrays 5M' and 5Y are directly aligned. Prelim. Resp. 58; Ex. 1004, Fig. 9. Moreover, we view the discussion in Hayasaki that Petitioner cites as relating to adjacent logic cells within the same array, rather than between arrays 5M' and 5Y. *See* Ex. 1004 ¶ 95, Fig. 9. Thus, this passage does not support an argument that there is operational interleaving between arrays 5M' and 5Y. *Id.*

Accordingly, Petitioner has not demonstrated a reasonable likelihood of success in challenging independent claim 1, as well as independent claim 8, which comprises a limitation of commensurate scope, and for which Petitioner does not provide separate arguments. In addition, claims 2–7, 9, 10, 13, and 14 depend from these independent claims, and Petitioner's arguments for these dependent claims do not cure the above deficiencies of the independent claims. Pet. 39–70. Thus, Petitioner has not demonstrated a reasonable likelihood of success in challenging claims 1–10, 13, and 14 as being anticipated by Hayasaki.

VI. ALLEGED OBVIOUSNESS OVER HAYASAKI AND SILVERBROOK

Petitioner argues that the combination of Hayasaki and Silverbrook renders claims 1–10, 13, and 14 obvious. Pet. 70–91. For this asserted ground, Petitioner argues that both Hayasaki and Silverbrook teach “a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement.” *Id.* at 70–71. As we discuss above, however, we find that Hayasaki does not teach this limitation. *See supra* Section V.B. And for the reasons we discuss below, we find that Silverbrook also does not teach this limitation. Hence, we determine that Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the Hayasaki and Silverbrook combination renders the challenged claims obvious.

A. *Summary of Silverbrook*

Silverbrook relates to “[a]n inkjet printhead having a series of nozzles for the ejection of ink.” Ex. 1005, code (57). More specifically, Silverbrook teaches “an inkjet printing device which utilises micro-electro mechanical [(“MEMS”)] processing techniques in the construction of a print head driven by thermal bend actuator devices for the ejection of fluid such as ink from an array of nozzle chambers.” *Id.* ¶ 2.

Silverbrook’s preferred embodiment is a 1600 dots per inch “modular monolithic print head suitable for incorporation into a wide variety of page width printers and in print-on-demand camera systems.” *Id.* ¶ 217. Silverbrook teaches that “integration of the drive electronics on the same chip as the print head is essential to achieve low cost,” and that its “preferred embodiment integrates [Complementary Metal Oxide] logic and drive transistors on the same wafer as the MEMS nozzles.” *Id.* ¶¶ 19, 218.

Silverbrook also teaches that its “inkjet print head can consist of a large number of replicated unit cells each of which has basically the same design,” including for the general layout of “the shift register, transfer register and gate and drive transistor.” *Id.* ¶¶ 303, 305.

B. Arranged in a Non-Contiguous Hybrid Arrangement

Petitioner argues that Silverbrook teaches “a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement,” as recited in claim 1. Pet. 70–77. More specifically, Petitioner argues that “Silverbrook describes an inkjet printhead including control logic.” *Id.* at 71. Petitioner repeatedly identifies the control logic in Silverbrook as comprising a shift register, transfer register, and enable gate. *Id.* at 72–74 (citing Ex. 1005 ¶¶ 300–301, 303, Figs. 76–77, 79; Ex. 1007 ¶ 238). For example, Petitioner annotates Figure 79, shown below, to identify Silverbrook’s teaching of a logic cell.

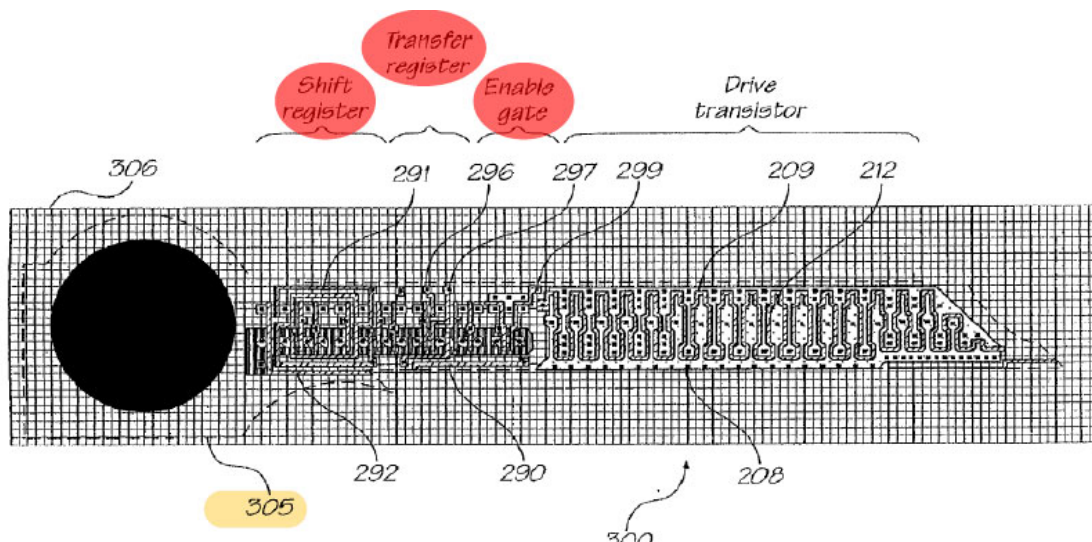


Figure 79 “illustrates the unit cell 305 on a 1 micron grid 306,” in accordance with Silverbrook’s teachings. Ex. 1005 ¶ 305. Petitioner annotates Figure 79 by coloring in red the labels for shift register, transfer

register, and enable gate. Pet. 74 (annotating Ex. 1005, Fig. 79). Petitioner argues that Figure 79 shows that “the logic is placed adjacent the nozzle (black circle),” and that “in Silverbrook the shift register, transfer register, and enable gate (all in red), together form a logic cell.” *Id.* (citing Ex.1007 ¶ 238). Notably, Petitioner’s identification of a logic cell does not include the drive transistor.

Next, Petitioner argues that Silverbrook teaches having arrays of unit cells, which are divided into three groups “with each group providing separate color output (cyan, magenta and yellow) so as to provide full three color printing.” *Id.* at 74–75 (quoting Ex. 1005 ¶ 311). According to Petitioner, Silverbrook teaches that the logic cells for one group are interleaved or interlaced with the logic cells for another group. *Id.* at 75. Petitioner annotates Figure 86, as shown below, in support of its arguments.

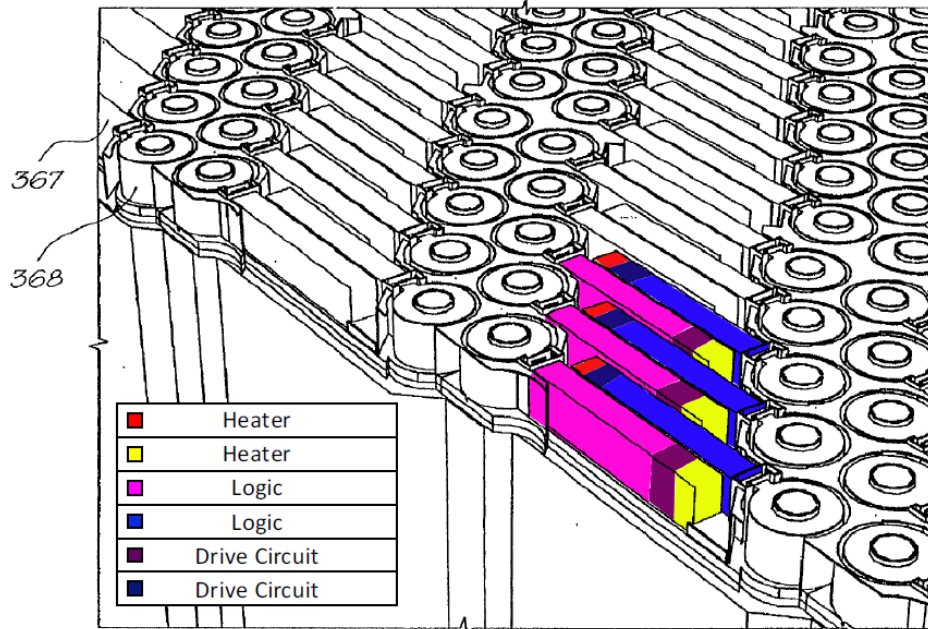


FIG. 86

Figure 86 “illustrates an enlarged view of a side perspective partly in section of a portion of an ink jet head.” Ex. 1005 ¶ 195. Petitioner annotates the

figure by coloring the purported “logic” portion of alternating unit cells pink and blue, respectively. Pet. 76. Petitioner also identifies for each of the alternating unit cells the purported (i) drive circuits in purple and dark blue, respectively, and (ii) heaters in yellow and red, respectively. *Id.*

Petitioner argues that “the logic cells (pink) associated with one group of nozzles (and its associated heaters) is clearly interleaved or interlaced with logic cells (blue) associated with another group of nozzles (and its associated heaters) and thus the sets of logic cells are arranged in a **non-contiguous hybrid arrangement.**” *Id.* at 75 (citing Ex. 1005, Fig. 86; Ex. 1007 ¶ 241).

Patent Owner argues that Petitioner doctored Figure 86 so that it “is arbitrarily colored to make it appear as if the logic portions are much longer and extend into the center of the region between nozzles.” Prelim. Resp. 67. According to Patent Owner, in contrast, Silverbrook’s Figure 87 “actually shows the relationship of logic units within the arrangement of unit cells that make up the printhead of Silverbrook,” and the logic cells are not interleaved or interlaced. *Id.* at 67–68 (citing Ex. 1005, Fig. 87). In support of its arguments, Patent Owner annotates Figure 87 of Silverbrook, shown below.

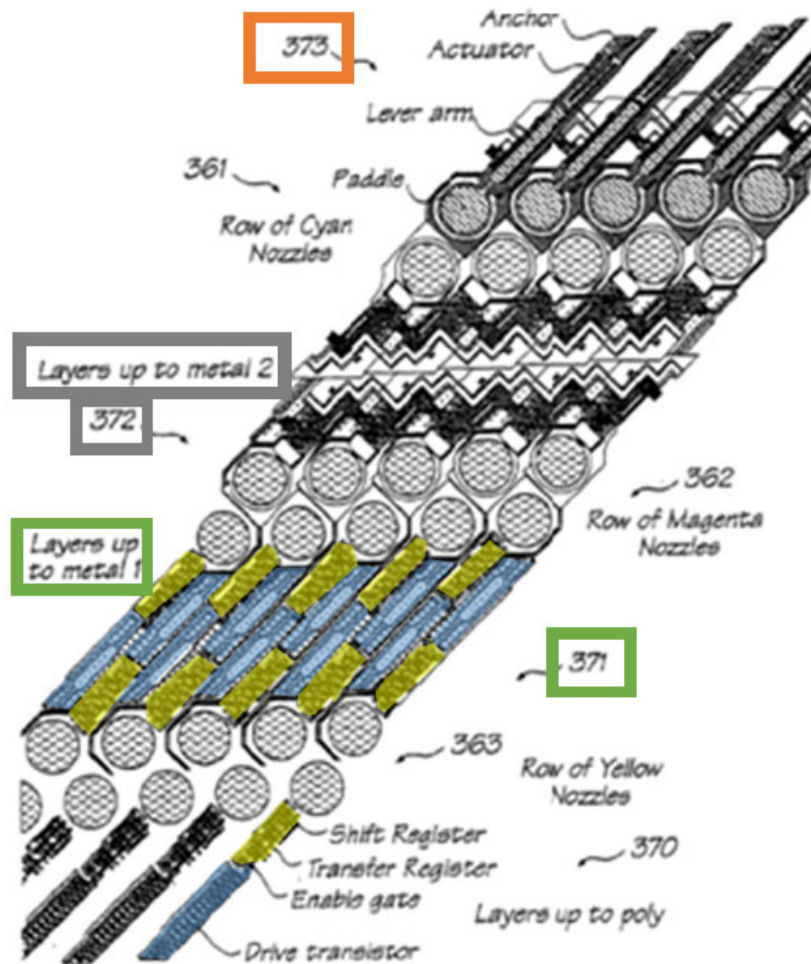


FIG. 87

Figure 87 illustrates a “layout in a cut away manner with a first area 370 illustrating the layers up to the polysilicon level.” Ex. 1005 ¶ 313. Patent Owner annotates the figure, in relevant part, by coloring what Figure 87 identifies as shift registers, transfer registers, and enable gates yellow, and coloring what the figure identifies as drive transistors blue. Prelim. Resp. 66 (annotating Ex. 1005, Fig. 87).

Patent Owner argues that “the figures of Silverbrook show that the logic portions [yellow] are less than about half the size of the drive transistor [blue] in each unit cell, and when multiple unit cells are aligned, the logic

[yellow] and drivers [blue] are interspersed as shown . . . in Fig[ure] 87 with the logic [yellow] located toward the edges of the region rather than in the center.” *Id.* at 65 (alterations in original); *see also id.* at 67 (citing Ex. 1005, Figs. 75, 79, 83).

We agree with Patent Owner and find that Petitioner does not show that Silverbrook teaches “[a]n arrangement in which the first set of logic cells are interleaved or interlaced with the second set of logic cells.” In particular, we find that Silverbrook teaches, as illustrated by Figure 87, that the shift register, transfer register, and enable gate (which Petitioner identifies as a logic cell) in a unit cell of a first set is not interleaved or interlaced with the shift register, transfer register, and enable gate of an alternate unit cell from the second set. *See* Prelim. Resp. 66 (annotating Ex. 1005, Fig. 87). Rather, the alternating unit cells have their logic cells (highlighted in yellow) located toward the edges of the region rather than in the center. *Id.* (showing annotated Figure 87). There is no interleaving or interlacing of the sets of logic cells, as evidenced by the blue highlighting for the drive transistors contiguously occupying the center between the alternating unit cells. *Id.*

In addition, we find that Petitioner’s annotation of Figure 86 is inconsistent with Silverbrook’s teachings, such as in Figure 79 where the logic cell (i.e., shift register, transfer register, and enable gate) is notably shorter than the drive transistor. *See* Ex. 1005, Fig. 79 (illustrating the components on a 1 micron grid), ¶ 305. Despite this teaching, Petitioner annotates Figure 86 by coloring the logic cells to be much longer than (i.e., multiples in length) the drive transistors. *See* Pet. 76 (annotating Ex. 1005, Fig. 86). And neither Petitioner nor its expert, Mr. Curley, provide any

support for why they annotated Figure 86 to show logic cells that are substantially longer than the drive transistors. *Id.* at 75–76; Ex. 1007

¶¶ 241–242.

Accordingly, Petitioner has not demonstrated a reasonable likelihood of success in challenging independent claim 1, as well as independent claim 8, which comprises a limitation of commensurate scope, and for which Petitioner does not provide separate arguments. In addition, claims 2–7, 9, 10, 13, and 14 depend from these independent claims, and Petitioner’s arguments for these dependent claims do not cure the above deficiencies of the independent claims. Pet. 84–91. Thus, Petitioner has not demonstrated a reasonable likelihood of success in challenging claims 1–10, 13, and 14 as being obvious over the combination of Hayasaki and Silverbrook.

VII. ALLEGED OBVIOUSNESS OVER HAYASAKI AND KROUSS

Petitioner argues that the combination of Hayasaki and Krouss renders claims 1–10, 13, and 14 obvious. Pet. 91–101. For this asserted ground, Petitioner argues that both Hayasaki and Krouss teach “a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement.” *Id.* at 91. As we discuss above, however, we find that Hayasaki does not teach this limitation. *See supra* Section V.B. And for the reasons we discuss below, we find that Krouss also does not teach this limitation. Hence, we determine that Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the combination of Hayasaki and Krouss renders the challenged claims obvious.

A. *Summary of Krouss*

Krouss “relates to inkjet printers and the like, and more particularly to an inkjet printing system that makes use of multi-pass printing to form

images and text on print media.” Ex. 1012, 1:4–7. Krouss explains that “[i]nkjet printing systems frequently make use of an inkjet printhead mounted to a carriage which is moved back and forth across print media such as paper,” and that “[a]s the printhead is moved across the print media, a control device selectively activates a plurality of drop generators within the printhead to eject or deposit ink droplets onto the print media to form images and text characters.” *Id.* at 1:8–14. Krouss teaches that “[i]ndividual drop generators are selectively activated by the use of a select or an enable signal,” and that for “thermal inkjet printing, each drop generator is activated by passing an electric current through a resistive element such as a resistor.” *Id.* at 1:18–22. “In response to the electric current the resistor produces heat,” which ultimately leads to ink being ejected from an adjacent nozzle and deposited on print media to accomplish printing. *Id.* at 1:22–30.

In addition, Krouss teaches that “drop generators [are] associated with each particular ink, yellow, magenta, and cyan, [and] are grouped into groupings referred to as primitives.” *Id.* at 6:57–60. According to Krouss, the electric or drive current provided to each resistor or drop generator is sometimes referred to as a primitive signal, and is frequently provided via a transistor, which is activated by a control signal, sometimes referred to as an address signal. *Id.* at 1:31–41. Krouss teaches that for certain prior art arrangements, there are a plurality of primitive signals, each of which are connected to a different group of drop generators within the inkjet printhead. *Id.* at 1:42–45. There also is a plurality of address signals each of which is provided to a transistor associated with a drop generator. *Id.* at 1:45–47. According to Krouss, “[u]sing this technique a drive signal is provided to each primitive containing a drop generator that is to be activated,” and “[t]he

address signal is provided to each primitive to select the particular drop generator for activation within the primitive or grouping of drop generators.” *Id.* at 1:47–52.

According to Krouss, however, the above-described scheme “is susceptible to certain failure modes that can result in deleterious effects on print quality,” such as “a failure of one of the address lines to provide an address signal to each of the primitives or groupings of drop generators[, which] results in a failure of each drop generator associated with that particular address line in each primitive.” *Id.* at 1:55–62.

In response, Krouss teaches “ha[ving] a plurality of drop generators disposed on the printhead that are responsive to first and second select signals for selectively depositing ink on media,” and “a plurality of contacts for receiving first and second select signals from the inkjet printing system.” *Id.* at code (57). “Also included is a plurality of electrical conductors each electrically connected between the plurality of contacts and selected drop generators of the plurality of drop generators, wherein in a multi-pass print-mode, the plurality of electrical conductors ar[e] connected to the plurality of drop generators to uniformly distribute error resulting from a failure of one of the plurality of electrical conductors to provide one of the first and second select signals to the plurality of drop generators.” *Id.*

B. Arranged in a Non-Contiguous Hybrid Arrangement

Petitioner argues that Krouss teaches “a first and a second set of logic cells arranged in a non-contiguous hybrid arrangement,” as recited in claim 1. Pet. 91–101. More specifically, Petitioner argues that “Krouss describes a printhead 24 including ‘drop generators 30, 32, and 34 for depositing yellow, magenta, and cyan inks, respectively, on print media.’” *Id.* at 92

(quoting Ex. 1012, 6:54–57; citing *id.* at Fig. 5). In support of this argument, Petitioner annotates Figure 5, shown below.

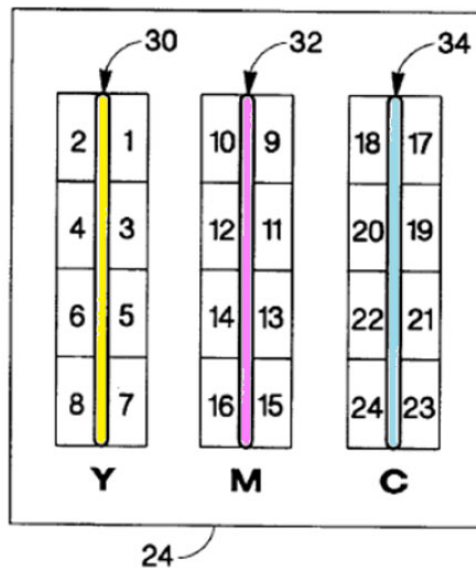


Fig. 5

Figure 5 “depicts a schematic representation of a 3-color printhead . . . with drop generators grouped into 8 primitives.” Ex. 1012, 3:22–24. Petitioner annotates this figure by coloring the center of drop generator portions 30, 32, and 34 yellow, magenta, and cyan, respectively. Pet. 92.

In addition, Petitioner argues that Krouss teaches for the yellow ink arranging the drop generators to have an offset. *Id.* at 93–94. Figure 6, as annotated by Petitioner, is shown below.

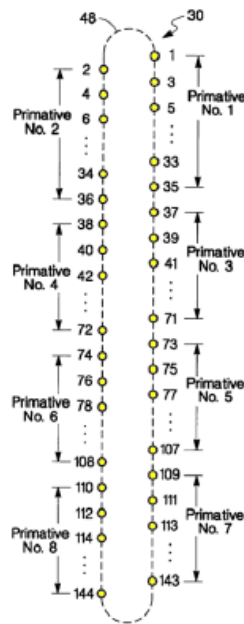


Fig. 6

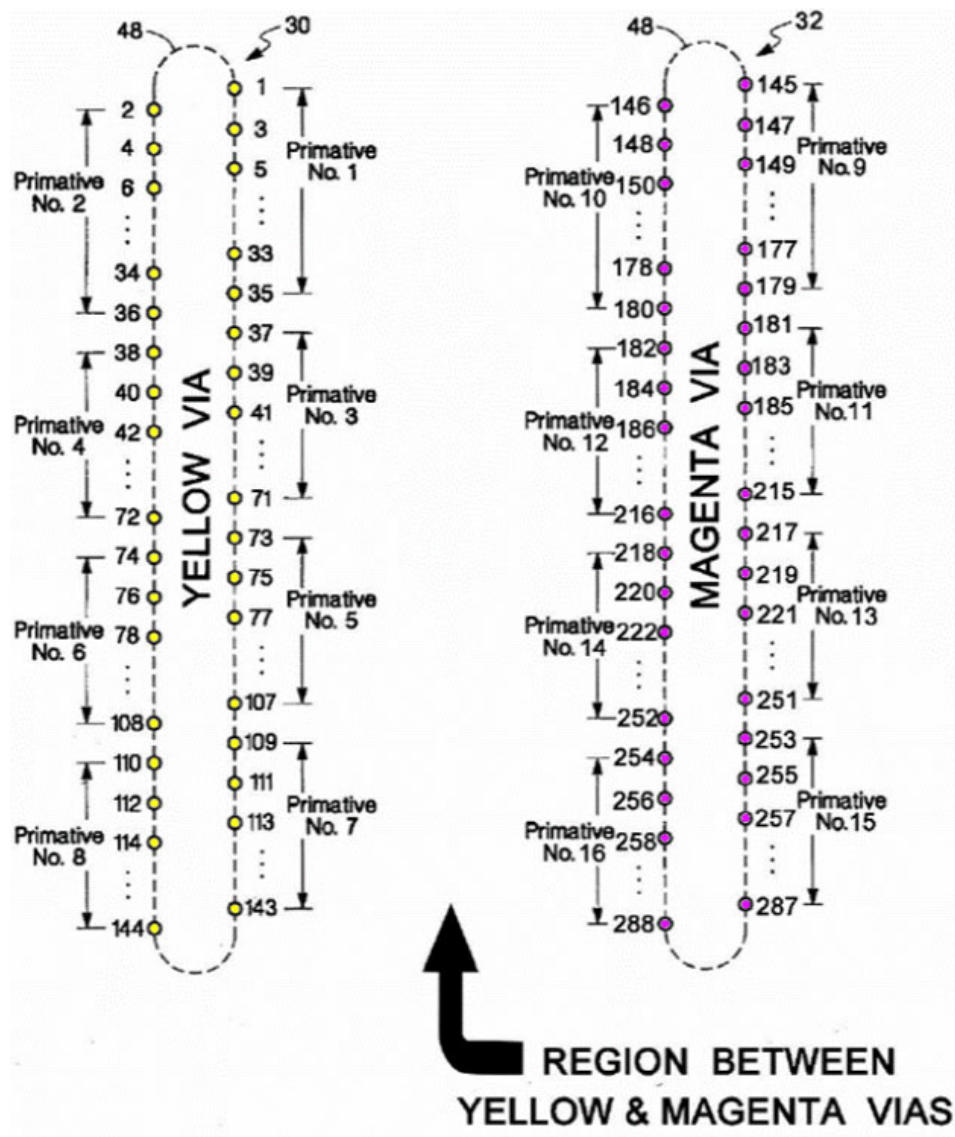
Figure “6 depicts an arrangement of drop generators into the 8 primitive groupings for a single color of [a] 3-color printhead.” Ex. 1012, 3:25–27. Petitioner annotates this figure by coloring in yellow the illustrated plurality of drop generators 30 associated with yellow ink on printhead 24. Pet. 92 (annotating Ex. 1012, Fig. 6; citing *id.* at 6:65–7:5). Petitioner argues that Krouss teaches the following:

In the preferred embodiment, the **drop generators** are **arranged** in parallel rows adjacent the ink feed slot 48. The 144 **nozzles** associated with yellow ink drop (generators [sic] are each **offset** along a longitudinal axis of the ink feed slot 48. Each nozzle is numbered from 1 to 144 based on position along the longitudinal axis of the ink feed slot 48 with odd numbered nozzles on one side of the ink feed slot 48 and even numbered nozzles on the other side of the ink feed slot 48.

Id. at 93–94 (quoting Ex. 1012, 7:18–26) (alterations in original). In addition, Petitioner argues that Krouss teaches that the drop generator layouts for the magenta and cyan ink feed slots are similar to the layout for

the yellow ink feed slot, described above. *Id.* at 94 (citing Ex. 1012, 7:48–57).

Petitioner next argues that “[b]ecause of this drop generator offset arrangement, [one of ordinary skill in the art] would have understood that the magenta ink via’s drop generator layout would also be offset as [M]r. Curley has depicted . . . with the drop generators associated with the magenta ink via vertically offset as they are with the yellow ink via depicted in Figure 6.” *Id.* This illustration created by Mr. Curley is shown below.



Ex. 1007 ¶¶ 310–311. Petitioner then argues that, as shown by Mr. Curley’s illustration, “the drop generators located on the right side of yellow ink via 48 are vertically interleaved with the drop generators located on the left side of magenta ink via 48.” Pet. 95 (citing Ex. 1007 ¶ 312).

We agree with Petitioner that Krouss teaches that the drop generator layouts for the magenta and cyan ink feed slots are similar to the layout for the yellow ink feed slot. Pet. 94; Ex. 1012, 7:48–57. Hence, Mr. Curley’s representation of the layout for the magenta ink feed slot itself seems consistent with Krouss’s teachings. Ex. 1007 ¶ 311; Ex. 1012, 7:18–26. However, as Patent Owner argues, Petitioner and Mr. Curley provide no basis for Mr. Curley’s placement of the magenta layout so that the drop generators located on the right side of yellow ink via are vertically offset from the drop generators located on the left side of magenta ink via. *See* Prelim. Resp. 75–76; Pet. 94–95; Ex. 1007 ¶¶ 310–312. Hence, we find that this testimony from Mr. Curley lacks factual support and is entitled to little weight. *See* Ex. 1007 ¶¶ 310–312; 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

In addition, Petitioner argues that Krouss’s Table 1 supports its positions. Pet. 96–98. Krouss identifies Table 1 as “illustrating address and primitive connections for each drop generator associated with the printhead,” and explains that “[t]he drop generator number refers to the drop generator location along each of the ink feed slots 30, 32, and 34 for the yellow, magenta, and cyan inks, respectively.” Ex. 1012, 7:46–51.

Petitioner argues that one of ordinary skill in the art “would have understood that Table 1 of Krouss teaches how to layout the drop generator

positions and corresponding logic cell interconnects in the region between the yellow and magenta ink feed slots, including the specifics of the shared signal bus.” Pet. 96 (citing Ex. 1007 ¶ 315). We find this argument unavailing. First, Petitioner fails to explain how the positions of drop generators teach the positions of logic cell interconnects, and how such interconnects teach the location of the logic cells themselves. *Id.* In our view, Table 1’s teachings are inapposite to the locations of the logic cells. Ex. 1012, Table 1. Second, Mr. Curley’s cited testimony, upon which Petitioner relies, is conclusory and lacks any factual support. Ex. 1007 ¶ 315. Hence, we afford it little weight. 37 C.F.R. § 42.65(a).

Similarly, we find unavailing Petitioner’s argument that one of ordinary skill in the art “would have understood how to combine [Table 1’s] information with Figures 5–6 to layout the geometry of the drop generators (and the corresponding logic cells) of the printhead.” Pet. 96 (citing Ex. 1007 ¶¶ 313–318). Petitioner fails to explain how the position of a drop generator and its associated address and primitive connections teach the position of a logic cell. *Id.* And we afford little weight to Mr. Curley’s purported diagram of the first ten drop generators because his testimony also is premised on the purported teachings of Figures 5–6 and Table 1, without providing a basis or factual support for his testimony. Ex. 1007 ¶ 316; Pet. 98. Furthermore, Petitioner fails to account for Krouss’s explicit contrary teaching that its print control device (comprising a primitive generator, address generator, and controller) is located in the printer, rather than the printhead (which contains the drop generators) of the printer cartridge. *See* Ex. 1012, Fig. 4, 5:36–44; *see also id.* Figs. 1–3 (showing components of the printer and printer cartridge).

Lastly, we find unavailing Mr. Curley’s testimony regarding his diagram showing that “pitch doubling is used for the nozzles resulting in nozzles being vertically interlaced,” where “[f]or example, nozzle 1 associated with yellow ink via is pitched at a different vertical distance than nozzle 146 associated with the magenta ink via.” Ex. 1007 ¶ 317. As we discuss above, Mr. Curley did not provide factual support for creating the purported diagram. Nor do we view the location of the nozzles as teaching the location of the logic cells. Thus, this testimony is inapposite.

Accordingly, Petitioner has not demonstrated a reasonable likelihood of success in challenging independent claim 1, as well as independent claim 8, which comprises a limitation of commensurate scope, and for which Petitioner does not provide separate arguments. In addition, claims 2–7, 9, 10, 13, and 14 depend from these independent claims, and Petitioner’s arguments for these dependent claims do not cure the above deficiencies of the independent claims. Pet. 101. Thus, Petitioner has not demonstrated a reasonable likelihood of success in challenging claims 1–10, 13, and 14 as being obvious over the combination of Hayasaki and Krouss.

VIII. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition does not demonstrate a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any of the challenged claims of the ’629 patent on any of the asserted grounds.

IX. ORDER

In consideration of the foregoing, it is hereby:
ORDERED that the Petition is denied and no trial is instituted.

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Patent 7,559,629 B2

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