

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

3D SURFACES, LLC,
Patent Owner.

IPR2022-01589
Patent 7,245,299 B2

Before JEFFREY S. SMITH, GEORGE R. HOSKINS, and
ROBERT L. KINDER, *Administrative Patent Judges*.

HOSKINS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation (“Petitioner”) has filed a Petition (Paper 2, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of U.S. Patent No. 7,245,299 B2 (Ex. 1001, “the ’299 patent”), claims 1–4, 9–11, 17, and 18. Petitioner also filed an Explanation (Paper 3) for filing two petitions against the ’299 patent, ranking the present Petition ahead of the petition filed in IPR2022-01588.

3D Surfaces, LLC (“Patent Owner”) filed a Preliminary Response (Paper 7, “Prelim. Resp.”) opposing institution of review. Patent Owner also filed a Response (Paper 8) to Petitioner’s Explanation concerning the two petitions.

Patent Owner argues institution should be denied discretionally under 35 U.S.C. § 325(d) or § 314(a). *See* Prelim. Resp. 1–3, 12–37. Via e-mail communications with the parties, we authorized additional briefing to address Patent Owner’s reliance on § 314(a). Accordingly, Petitioner filed a Reply (Paper 9, “Reply”) to the Preliminary Response, and Patent Owner filed a Sur-reply (Paper 11, “Sur-reply”) to the Reply.

We conclude discretionary denial under either § 325(d) or § 314(a) is not appropriate in the circumstances presented here. We then apply the standard for institution set forth in 35 U.S.C. § 314(a) on behalf of the Director (37 C.F.R. § 42.4(a)), which requires the Petition to demonstrate a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim. We institute an *inter partes* review to determine whether Petitioner demonstrates by a preponderance of the evidence that the challenged claims are unpatentable, considering all grounds asserted in the Petition.

II. BACKGROUND

A. *Real Parties-in-Interest and Related Proceedings*

Petitioner identifies itself (i.e., Intel Corporation), as well as Dell Technologies Inc. and Dell Inc., as real parties-in-interest for Petitioner. *See* Pet. 81. Patent Owner identifies itself (i.e., 3D Surfaces, LLC) as the real party-in-interest for Patent Owner. *See* Paper 4, 1.

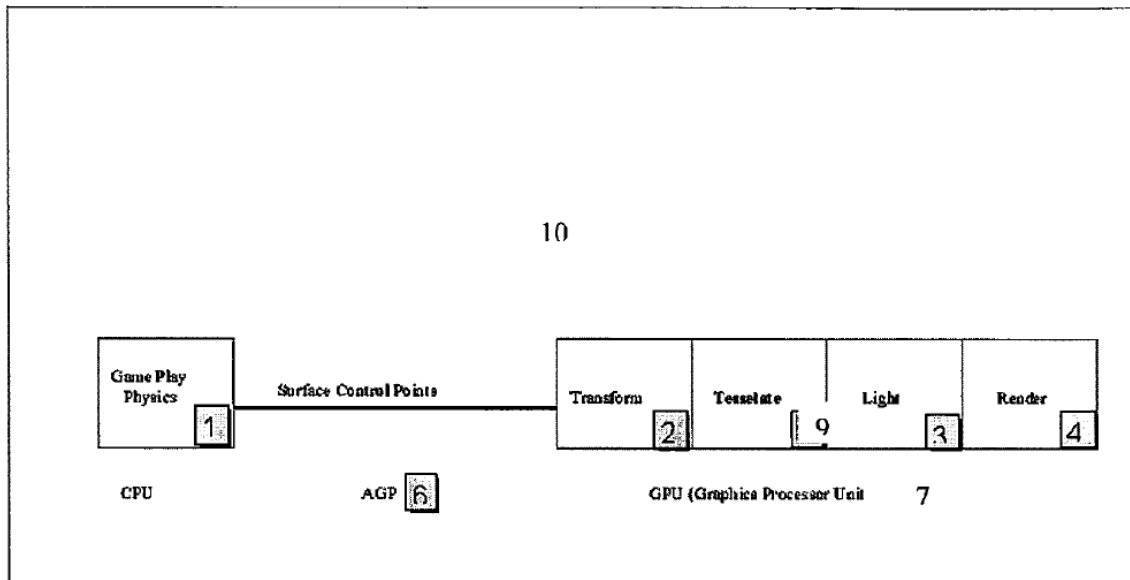
The parties identify one district court litigation involving the '299 patent: *3D Surfaces, LLC v. Dell Techs. Inc., et al.*, Case No. 1:22-cv-00854 (W.D. Tex.) (“the District Court Litigation”). *See* Pet. 81–82; Paper 4, 1 (explaining that the District Court Litigation was previously Case No. 6:21-cv-01107, the case number Petitioner identifies).

The parties further identify three other IPR proceedings challenging the '299 patent: IPR2022-01588; IPR2023-00003; and IPR2023-00004. *See* Pet. 82; Paper 4, 1.

B. *The '299 Patent*

The '299 patent is directed to a method and apparatus for rendering bicubic surfaces in real-time on a computer system. *See* Ex. 1001, 1:15–20. It specifically teaches “a method and apparatus for minimizing the number of computations required for the subdivision of bicubic surfaces into triangles for real-time tessellation.” *Id.* at 4:35–38.

Figure 3 is reproduced below.



The '299 Patent, Figure 3.

Figure 3 is a block diagram of graphics system 10, which includes central processing unit (CPU) 1, accelerated graphics port bus 6, and graphics processing unit (GPU) 7. *See id.* at 2:32–46, 6:66–7:4. “According to the [’299 patent’s] invention, the GPU 7 includes a transform unit 2, a lighting unit 3, a renderer unit 4, and a tessellate unit 9 coupled between the transform unit 2 and the lighting unit 3 for tessellating both rational and non-rational object surfaces in real-time.” *Id.* at 7:4–8. CPU 1 executes a software application and transmits over bus 6 the “control points of the bicubic surfaces” which “are transformed by the transform unit 2, and then the surfaces are tessellated into triangles by the tessellate unit 9.” *Id.* at 7:9–17. “The vertices of the triangles are then lit by the lighting unit 3 and the triangles are rendered by the renderer unit 4.” *Id.* at 7:17–19.

C. The Claims of the '299 Patent

Petitioner challenges a subset of the '299 patent claims, including independent claim 1 and its dependent claims 2–4, 9, and 10, and independent claim 11 and its dependent claims 17 and 18. We reproduce illustrative claim 1 here:

1. A graphics processing unit for rendering objects from a software application executing on a processing unit in which the objects to be rendered are transmitted to the graphics processing unit over a bus as control points of bicubic surfaces, the graphics processing unit comprising:
a transform unit;
a lighting unit;
a renderer unit; and
a tessellate unit coupled between the transform unit and the lighting unit for tessellating both rational and non-rational object surfaces in real-time.

Ex. 1001, 12:38–49.

D. Asserted Prior Art

Petitioner relies principally on the following three prior art references in this proceeding. *See* Pet. 1–2.

Name	Reference	Pub. Date	Exhibit No.
Sfarti ¹	US 2002/0033821 A1	Mar. 2002	1009
Möller	Thomas Möller and Eric Haines, <i>Real-Time Rendering</i> (A K Peters, Ltd., 1999)	Nov. 1999	1008

¹ The Petition and the Preliminary Response both refer to this reference as “501-Pub” for reasons which will become clear below. We instead refer to it as “Sfarti” because the solely-named inventor is Adrian Sfarti.

Name	Reference	Pub. Date	Exhibit No.
Foley	James D. Foley et al., <i>Computer Graphics: Principles and Practice, Second Edition</i> (Addison-Wesley Pub. Co., 1990)	Jan. 1991	1007

E. Asserted Grounds

Petitioner proposes the following two grounds of unpatentability for the challenged claims. *See* Pet. 2.

Ground	Claims Challenged	35 U.S.C. § ²	References
1	1–4, 9, 11, 17	103(a)	Sfarti, Foley
2	10, 18	103(a)	Sfarti, Foley, Möller

F. Testimonial Evidence

Petitioner relies on the declaration testimony of Chandrajit L. Bajaj, Ph.D. (Ex. 1003). Patent Owner does not rely on witness testimony at the present time.

G. Effective Filing Date of the Challenged '299 Patent Claims

The '299 patent was filed as U.S. Patent Application No. 10/732,398 on December 9, 2003. *See* Ex. 1001, codes (21) and (22). The “Related U.S. Application Data” field on the front page of the '299 patent indicates it is a continuation-in-part of U.S. Patent Application No. 10/436,698 (“the '698 Application”) filed on May 12, 2003. *See id.* at code (63).

² The '299 patent issued in July 2007. *See* Ex. 1001, code (45). Therefore, the first-inventor-to-file provisions of the Leahy-Smith America Invents Act (Pub. L. No. 112-29, 125 Stat. 284 (2011)), which took effect in March 2013, do not apply here.

However, the Specification of the '299 patent begins with a "CROSS-REFERENCE TO RELATED APPLICATIONS" paragraph, which differs from the front page data. *See id.* at 1:4–13. The Specification refers to being a continuation-in-part of the '698 Application like the front page does, but the Specification additionally refers to being a continuation-in-part of U.S. Patent No. 6,563,501 B2 (Ex. 1014, "the '501 patent") filed on December 11, 2000, as well as the benefit of U.S. Provisional Application No. 60/222,105 filed on July 28, 2000. *See* Ex. 1001, 1:4–13; Ex. 1014, code (22).

Petitioner contends the effective filing date of the challenged '299 patent claims "is no earlier than May 12, 2003," the filing date of the '698 Application. Paper 3, 3. In particular, according to Petitioner, the challenged '299 patent claims are not entitled to the benefit of the filing date of the '501 patent, for various reasons. *See id.*; Pet. 15–25.

Patent Owner stipulates that: "If the Board declines to institute the [IPR2022-01588] petition under § 314(a), Patent Owner will not challenge the prior art status of [Sfarti] in [IPR2022-01589, the present proceeding]." Paper 8, 1–2. In this event, as characterized by Patent Owner, "there is no priority dispute" in the present proceeding. *Id.* at 3.

Contemporaneously with the present Decision instituting review in this proceeding, we are also entering a decision in IPR 2022-01588 that denies institution in that proceeding under § 314(a). Therefore, we treat Patent Owner's stipulation as an admission, for the purposes of this proceeding, that Sfarti is prior art to the '299 patent.

III. DISCRETION UNDER 35 U.S.C. § 325(d)

Patent Owner urges us to exercise our discretion under 35 U.S.C. § 325(d) to deny institution of review, on the basis that “the Petition is merely a rehashing of art considered during prosecution of the ’299 patent.” Prelim. Resp. 1; *see id.* at 1–2, 10–30. Petitioner provides opposing arguments. *See* Pet. 79–80. For the following reasons, we do not invoke our discretion to deny institution under § 325(d).

A. *Legal Authority*

Pursuant to 35 U.S.C. § 325(d), when determining whether to institute an *inter partes* review, we “*may* take into account whether, and reject the petition . . . because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d) (emphasis added). When applying § 325(d), we utilize a two-part framework. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

First, we determine “whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office.” *Advanced Bionics*, at 8. In this first part, we consider: the similarities and material differences between the asserted art and the prior art involved during examination; the cumulative nature of the asserted art and the prior art evaluated during examination; and the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art. *Id.* at 10

(citing factors (a), (b), and (d) of *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5 ¶ 1).

Second, “if either condition of [the] first part of the framework is satisfied,” then we consider “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, at 8.

B. Whether to Deny Institution Here

1. Prosecution History of the '299 Patent

The prosecution history of the '299 patent is in the record as Exhibit 1002. Here, we summarize the aspects pertinent to the § 325(d) issues presented, for which claim 1 is representative.

As originally filed, claim 1 was identical to the issued version (reproduced above) except that the final limitation simply recited “a tessellate unit for tessellating both rational and non-rational object surfaces in real-time.” *Compare* Ex. 1002, 24 (original claim 1), *with* Ex. 1001, 12:38–48 (issued claim 1).

The Examiner rejected original claim 1 as a nonstatutory obviousness-type double patenting of the '501 patent's claim 21. *See* Ex. 1002, 65–68. In support, the Examiner determined original claim 1 differed from claim 21 of the '501 patent in that the former “describe[s] graphics processing units which contain instructions for subdivision,” whereas the latter “describes a computer readable medium contain[ing] program instructions [for] subdivision.” *Id.* at 67. The Examiner concluded “it would have been obvious to one of ordinary skill to substitute the

computer readable medium of claim 21 with the graphics processing unit of [original claim 1].” *Id.*

In response, the applicant amended the final limitation of claim 1 as follows: “a tessellate unit coupled between the transform unit and the lighting unit for tessellating both rational and non-rational object surfaces in real-time.” Ex. 1002, 127. The applicant argued “[t]he present invention utilizes the method disclosed in [the ’501 patent] for minimizing the number of computations required for the subdivision of bicubic surfaces into triangles in order to provide an improved architecture for the computer graphics pipeline hardware.” *Id.* at 137–138. In particular, according to the applicant, “[t]he improved architecture” of amended claim 1 “replaces triangle mesh transformation and rendering with a system that transforms bicubic patches and tessellates the patches in real-time in a tessellation unit that replaces the conventional transformation unit present in prior art hardware 3D architectures.” *Id.* at 138. The improved architecture, applicant argued, corresponds to “an internal tessellate unit coupled between the transform unit and the lighting unit, thereby providing a new type of a graphics processing unit.” *Id.* “By contrast,” the applicant argued, claim 21 of the ’501 patent “refers to a ‘computer readable medium containing a program’, that is, it refers to the *memory* used to store the *program* used for subdividing and rendering surfaces.” *Id.*

The Examiner then allowed claim 1, without further comment concerning double patenting or the ’501 patent. *See id.* at 175–179.

2. Advanced Bionics *Part One*

Patent Owner applies *Advanced Bionics* part one, arguing Sfarti is the same or substantially the same art as the '501 patent presented to the Examiner during prosecution of the '299 patent. *See* Prelim. Resp. 1, 6–9, 12–13, 16–20. To establish Sfarti and the '501 patent represent the same or substantially the same prior art, Patent Owner notes Sfarti is the pre-issuance publication of the '501 patent, and Petitioner agrees they share a common specification. *See id.* at 1, 10, 11, 17 (citing Pet. 25). To establish the '501 patent was presented to the Examiner, Patent Owner asserts: (1) the '299 patent incorporates the '501 patent by reference and further expressly discusses its disclosure at some length; and (2) the Examiner cited the '501 patent as the basis for a double patenting rejection during prosecution of the '299 patent. *See id.* at 1, 6–8, 10–11, 16–18 (citing Ex. 1001, 1:6–13, 4:53–5:29, 7:37–9:19, 9:44–55; Ex. 1002, 65–69, 112–113, 172–180).

Patent Owner argues Foley was also presented to the Office because it was cited by the Office during prosecution of the '501 patent, and the '299 patent's Specification identifies the '501 patent as a parent application. *See* Prelim. Resp. 2, 21 (citing Ex. 1014, code (56); Ex. 1001, 1:6–13). Patent Owner asserts the Office's Manual of Patent Examining Procedure "instructs that '[t]he examiner will consider information which has been considered by the Office in a parent application . . . when examining . . . a continuation-in-part application.'" *Id.* at 21 (citing MPEP §§ 609.02(II)(A)(2) and 707.05). Patent Owner also argues "[t]he relevant teachings of Foley—that GPUs are implemented with a 'hardware pipeline architecture'—was baseline knowledge, ubiquitously known in the art, and in front of the Examiner during prosecution of the '299 patent." *Id.* at 2, 8–

9, 12, 13, 21–23 (citing Pet. 27–40; Ex. 1003 ¶¶ 120, 142, 148; Ex. 1001, 2:32–48, 5:20–27, Fig. 2; Ex. 1002, 76, 183; Ex. 1032, Fig. 2b, 5:18–22; Ex. 1033, Fig. 1A, 6:27–31, 20:66–21:3).

Patent Owner further argues “the Office even considered the same argument Petitioner asks the Board to reconsider here” in the Petition. Prelim. Resp. 26. Patent Owner specifically asserts “the Examiner already determined that it would not have been obvious to modify the teachings of [Sfarti] to implement the ordered steps in a GPU,” as demonstrated by the prosecution history relating to the Examiner’s double patenting rejection based on the ’501 patent. *Id.* at 26–27 (citing Ex. 1002, 64–69, 112–114, 172–180).

Petitioner responds that “although the Examiner considered the [’501 patent] for purposes of obviousness double-patenting,” “the Examiner did not consider [Sfarti] as prior art against the challenged claims, which include amendments necessary to overcome the obviousness double-patenting rejection.” Pet. 79. Petitioner also asserts Foley was not presented to the Office during prosecution of the ’299 patent, so the Petition’s grounds were never considered. *See id.*

Patent Owner replies that the Examiner did consider Sfarti as prior art, because “the Examiner considered numerous references with a prior art date long after the filing and publication dates of” Sfarti. Prelim. Resp. 16, 18–20 (citing Ex. 1001, code (56); Ex. 1009, codes (22) and (43)).

Upon review of the foregoing, we first consider Foley and determine that, at best for Patent Owner, the Office previously has been presented with only pages 513–527 of Foley in connection with the ’299 patent claims challenged here. Foley is not even identified as a reference considered

during prosecution of the '299 patent. *See* Ex. 1001, code (56). Patent Owner argues that Foley was considered during prosecution of the '501 patent—but, only pages 513–527 of Foley were cited by the Examiner there. *See* Ex. 1014, code (56). By contrast, Petitioner here relies on pages xi–xii, 17, 19–20, 125, 285, 471–474, 502–504, 507–510, 516, 518, 521–522, 721, 736–737, 807, 855, 862, 866–871, 873–879, 888, 890–892, and 920 of Foley in the Petition's unpatentability grounds. *See* Pet. 27–79.

Out of all of the pages of Foley cited in the Petition, only pages 516, 518, 521, and 522 were previously presented to the Office. On the record before us, there is no indication that any of the remaining pages of Foley cited in the Petition were presented to, or considered by, the Office in connection with the '299 patent. For example, the '501 patent and the '299 patent were examined by different Primary Examiners. *See* Ex. 1014, code (56); Ex. 1001, code (56). Thus, even if we assume the Primary Examiner of the '501 patent was presented with the entirety of Foley in connection with the '501 patent but chose to cite only pages 513–527 on the face of the '501 patent, this assumed fact would not establish that the entirety of Foley was presented to the Primary Examiner of the '299 patent.

Further, the overlapping pages 516, 518, 521, and 522 do not teach the feature of the '299 patent claims that the Office determined was patentable over the prior art, like the other pages do. *See* Ex. 1002, 176–177 (stating that “though the prior art discloses tessellate, transform and lighting units, the prior [art] fails to teach a tessellate unit coupled between the transform unit and the lighting unit for tessellating both rational and non-rational object surfaces in real-time”); *see also* Ex. 1007, 807 (Foley teaches that “[t]essellation should occur after transformation into a coordinate system in

which screen size can be determined” for the benefits of “enabl[ing] tessellation size to be determined adaptively, and limit[ing] the amount of data that is transformed.”); *id.* at 866–877. Instead, the overlapping pages 516, 518, and 521–522 concern finer details of processing parametric bicubic surfaces, rather than the graphics hardware pipeline architectures that are discussed elsewhere in Foley. *See, e.g.*, Pet. 52 (citing Foley page 521 as “relating a Bezier surface to a bicubic surface”), 67–68 (citing Foley pages 516 and 518 as establishing that boundary curves of a bicubic patch are cubic curves), 76–77 (citing Foley pages 521–522 as relating to “modeling a surface with a connected set of bicubic surface patches” wherein “control points along a patch’s edge are shared by adjacent patches”). Thus, the pages of Foley cited in the Petition, with the exception of the overlapping pages 516, 518, and 521–522, were not previously presented to the Office in connection with the ’299 patent.

We moreover disagree with Patent Owner’s argument that the Examiner considered other references that are cumulative to and substantially the same as the portions of Foley cited by Petitioner, relating to graphics hardware pipeline architecture. Foley’s disclosure of a pipeline graphics architecture, which teaches the benefits of employing dedicated processors for tessellating after transforming, is both explicit and, so far as we can tell from the record presented, not found in any reference previously cited to the Office. *See* Ex. 1007, 807, 866–877. Thus, the same or substantially the same art as Foley was not previously presented to the Office.

We next turn to Sfarti (cited in the Petition) and the ’501 patent (cited during prosecution of the ’299 patent, as the basis for a double patenting

rejection). We agree with Patent Owner that these two references are the same or substantially the same prior art because Sfarti is the pre-issuance publication of the '501 patent and they share a common specification. *See, e.g.,* Prelim. Resp. 11, 17; Pet. 25.

However, we disagree with Patent Owner's position that the Examiner of the '299 patent considered the same argument presented in the Petition's obviousness combination of Sfarti and Foley, and correspondingly "determined that it would not have been obvious to modify the teachings of [Sfarti] to implement the ordered steps in a GPU" based on Foley. Prelim. Resp. 26–27 (citing Ex. 1002, 64–69, 112–114, 172–180). Specifically, we disagree that the Examiner's double patenting rejection presents the same argument as the Petition's obviousness combination. The Examiner stated "it would have been obvious to one of ordinary skill to substitute the computer readable medium of claim 21 [of the '501 patent] with the graphics processing unit of [original claim 1]." Ex. 1002, 67. The Examiner, in making this obviousness-type double patenting rejection³, did not find a prior art reference that showed a graphics processing unit with separately dedicated processors. Rather, the Examiner attempted to use the graphics processing unit recited in original claim 1 as prior art against itself. The applicant successfully argued against the Examiner's improper use of the pending claims as prior art by stating that the '501 patent did not disclose the graphics processing unit incorporating the tessellation unit as claimed. *See id.* at 138, 175.

³ The Examiner did not make a prior art rejection using the '501 patent. *See, e.g.,* Ex. 1002, 62–74.

Contrary to Patent Owner's contention, during prosecution of the '299 patent, the Examiner did not combine the processing steps of the '501 patent with any prior art that teaches a pipeline graphics processing unit, let alone prior art that teaches both a pipeline GPU and that "[t]essellation should occur after transformation" in order to "enable[] tessellation size to be determined adaptively, and [to] limit[] the amount of data that is transformed," as does Foley. Ex. 1007, 807. Even Patent Owner has not, at this point, disputed in this proceeding that the combination of Sfarti and Foley as presented in the Petition teaches a tessellation unit coupled between the transform unit and the lighting unit. Therefore, we find that the same or substantially the same arguments were not previously presented to the Office.

In sum, we determine the prior art and arguments asserted in the Petition are not substantially the same as those previously presented to the Office, so the first part of the *Advanced Bionics* framework is not met.

3. *Advanced Bionics Part Two*

Having concluded in *Advanced Bionics* part one that the prior art and arguments asserted in the Petition are not the same or substantially the same as those previously presented to the Office, we need not reach part two of the *Advanced Bionics* framework. See *Advanced Bionics*, at 8 (stating part two is reached only "if either condition of [the] first part of the framework is satisfied").

4. *Conclusion as to § 325(d)*

For the foregoing reasons, we do not exercise our discretion to deny institution pursuant to § 325(d).

IV. DISCRETION UNDER 35 U.S.C. § 314(a)

Patent Owner asserts institution should be denied under 35 U.S.C. § 314(a), in deference to the District Court Litigation. *See* Prelim. Resp. 2–3, 30–37; Sur-reply. Petitioner disagrees. *See* Pet. 80–81; Reply.

Under 35 U.S.C. § 314(a), the Director has discretion to deny institution of review. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1356 (2018) (“[Section] 314(a) invests the Director with discretion on the question whether to institute review.” (emphasis omitted)); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

On June 21, 2022, the USPTO Director issued an Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, *available at* https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Interim Procedure” or “Int. Proc.”). The Interim Procedure states “the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Int. Proc. 3 (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)). The Interim Procedure explains that a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and

“duplicative efforts between the district court and the PTAB . . . [and] allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8.

In this case, the District Court Litigation was brought by Patent Owner against defendants Dell Technologies and Dell Inc. (collectively, “Dell”), which Petitioner (Intel Corporation) has also named as real parties-in-interest in this IPR. *See* Pet. 81–82; Paper 4, 1; Prelim. Resp. 32 & n. 4, 34 n.6, 35–36; Reply 1. Petitioner Intel is not a party to the District Court Litigation. *See* Prelim. Resp. 32 & n. 4, 34 n.6, 35–36; Reply 1.

Petitioner Intel asserts Dell has “offered a *Sotera* stipulation agreeing that upon institution Dell will not pursue any grounds in the [District Court Litigation] that were raised or reasonably could have been raised in its IPR petition for the challenged claims.” Reply 1 (citing IPR2023-00004, Paper 13⁴). More precisely, however, Dell has actually stated in IPR2023-00004 that Dell “will stipulate, consistent with *Sotera* Wireless, that *if this IPR [i.e., IPR2023-00004] is instituted*, [Dell] will not pursue in the parallel district court proceeding any grounds raised or that reasonably could have been raised *in this IPR* for the challenged claims.”

IPR2023-00004, Paper 13, 1 (emphases added). Contemporaneously with the present Decision, we are issuing a decision in IPR2023-00004 instituting review of the ’299 patent on the same two grounds being instituted here, and we also are joining the two proceedings together for purposes of trial. Thus, Dell’s stipulation has taken effect.

⁴ The Reply actually cites Paper 12, but in context it is clear that Paper 13 was intended.

Dell offered the stipulation before our Decision on whether to institute, which is appropriate. *See NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 at 4 (PTAB Sept. 7, 2022) (precedential) (Director’s holding “that the only appropriate time for a petitioner to offer a stipulation related to the *Fintiv* factor 4 analysis is prior to the Board’s decision of whether to institute review”).

Patent Owner argues Dell’s *Sotera* stipulation is not dispositive, because Petitioner Intel has not offered a *Sotera* stipulation of its own, or provided assurance that Petitioner Intel will not participate in the District Court Litigation. *See* Sur-reply 1. However, Petitioner Intel is not a party to the District Court Litigation because Patent Owner has not sued Petitioner Intel in district court. Therefore, Petitioner Intel is not obliged to make a *Sotera* stipulation in district court. Further, the guidance under the Interim Procedure does not require a prospective stipulation because *Fintiv*⁵ does not apply to potential litigation, it only applies to active litigation. The Interim Procedure explicitly says “the PTAB will not discretionarily deny institution in view of parallel district court litigation,” not potential district court litigation, “where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Int. Proc. 3. Given the *Sotera* stipulation in the District Court Litigation by Dell (which is the only party sued by Patent Owner in that litigation), and the guidance under the Interim

⁵ The Interim Procedure concerns *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). *See* Int. Proc. 1–2 (“I have determined that several clarifications need to be made to the PTAB’s current application of *Fintiv* to discretionary institution where there is parallel litigation.”).

Procedure, we decline to exercise discretion to deny institution in this proceeding.

V. ANALYSIS OF PETITIONER’S PROPOSED GROUNDS

A. *Law of Obviousness*

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, if made available in the record, which has not happened here. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. *Level of Ordinary Skill in the Art*

Petitioner contends a person having ordinary skill in the art pertaining to the ’299 patent “would have had at least a Bachelor’s degree in computer science, computer engineering, electrical engineering, or a related scientific field, and approximately two years of work experience in computer graphics or, alternatively, two years[’] work towards a masters or doctorate degree in these scientific fields.” Pet. 10; Ex. 1003 ¶¶ 96–97. Patent Owner “applies Petitioner’s definition” in the Preliminary Response. Prelim. Resp. 9.

Based on our review of the record at this preliminary stage, we conclude Petitioner’s formulation of the level of ordinary skill in the art

appears to be consistent with the level of skill reflected in the '299 patent and the prior art of record, and is not presently disputed by Patent Owner. We, therefore, apply Petitioner's formulation in our analysis below.

C. Claim Construction

We interpret the '299 patent claims "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b). This "includ[es] construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." *Id.*

Petitioner asserts the claim terms "transform unit", "lighting unit", "tessellate unit", and "renderer unit" appearing in claims 1, 2 and 11 "require construction in this proceeding" because they are means-plus-function limitations per 35 U.S.C. § 112 ¶ 6. Pet. 11; Ex. 1003 ¶¶ 99–103. Petitioner then provides corresponding constructions of these terms. *See* Pet. 11–14; Ex. 1003 ¶¶ 104–111. Petitioner also discusses Patent Owner's contentions concerning the construction of these terms in the District Court Litigation, where Patent Owner argues the terms are *not* means-plus-function limitations. *See* Pet. 14–15; Ex. 1003 ¶¶ 201–203.

Patent Owner states "Petitioner correctly notes that Patent Owner and Petitioner dispute whether certain terms are subject to § 112, ¶ 6." Prelim. Resp. 9. Patent Owner nonetheless contends "the Petition fails regardless of whether § 112, ¶ 6 applies" so "the Board need not construe any term in denying institution." Prelim. Resp. 9.

On this record, we agree with Petitioner that “unit” does not connote any particular structure, and that the terms “transform unit”, “lighting unit”, “tessellate unit”, and “renderer unit” recite function without reciting sufficient structure for performing that function. Therefore, these terms should be construed as means-plus-function terms. “Construing a means-plus-function claim term is a two-step process.” *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1351 (Fed. Cir. 2015) (en banc) (citation omitted). We “must first identify the claimed function,” then we “must determine what structure, if any, disclosed in the specification corresponds to the claimed function.” *Id.* In cases involving a special purpose computer-implemented means-plus-function limitation, the Federal Circuit requires “that the specification disclose an algorithm for performing the claimed function.” *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015). “A description of the function in words may disclose, at least to the satisfaction of one of ordinary skill in the art, enough of an algorithm to provide the necessary structure under § 112, ¶ 6.” *Typhoon Touch Techs., Inc. v. Dell, Inc.*, 659 F.3d 1376, 1385–86 (Fed. Cir. 2011). “The law is clear that patent documents need not include subject matter that is known in the field of the invention and is in the prior art, for patents are written for persons experienced in the field of the invention.” *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1371 (Fed. Cir. 2001).

I. Transform Unit

Claims 1 and 11 both recite a graphics processing unit (GPU) “comprising . . . a transform unit.” Ex. 1001, 12:42–43, 13:64–65. Claim 2

depends from claim 1 and recites “the transform unit transforms the control points,” which claim 11 also specifies. *Id.* at 12:50–51, 14:2–3.

The ’299 patent specification discloses that the function of transforming is performed by a GPU including a dedicated processor programmed to execute the transform step of the disclosed microcode. *See* Ex. 1001, 5:59–67, 7:4–8, 7:12–13, 12:24–28; Ex. 1003 ¶¶ 104–105. We construe “transform unit” as a means-plus-function limitation with the function of transforming graphic objects into transformed objects (claims 1 and 11) including control points (claims 2 and 11), and with the corresponding structure of a GPU including a dedicated processor programmed to execute the transform step of the microcode disclosed in the specification.

2. *Lighting Unit*

Claims 1 and 11 both recite a GPU “comprising . . . a lighting unit.” Ex. 1001, 12:42–44, 13:64–66. Claim 2 depends from claim 1 and recites “the lighting unit lights vertices of the triangles,” which claim 11 also specifies. *Id.* at 12:53–54, 14:5–6.

The ’299 patent specification discloses that the function of lighting is performed by a GPU including a dedicated processor programmed to execute code to light vertices of triangles. *See* Ex. 1001, 6:55–60, 7:4–8, 7:17–19, 12:24–28; Ex. 1003 ¶¶ 108–109. We construe “lighting unit” as a means-plus-function limitation with the function of lighting surfaces resulting from the tessellate unit (claim 1) or lighting vertices of triangles resulting from the tessellate unit (claims 2 and 11), and with the

corresponding structure of a GPU including a dedicated processor programmed to execute code to light the tessellated objects.

3. *Tessellate Unit*

Claim 1 recites a GPU “comprising . . . a tessellate unit coupled between the transform unit and the lighting unit for tessellating both rational and non-rational object surfaces in real-time.” Ex. 1001, 12:42–48.

Claim 11 recites substantially similar subject matter. *See id.* at 13:64–14:5.

Claim 2 depends from claim 1 and recites “the tessellate unit tessellates the surfaces into triangles by executing a first set of instructions.” *Id.* at 12:51–53.

The ’299 patent specification discloses that the function of tessellating both rational and non-rational object surfaces in real-time is performed by a GPU including a dedicated processor coupled between the transform unit and the lighting unit, where the dedicated processor is programmed to execute the tessellating steps of the disclosed microcode. *See* Ex. 1001, 6:1–54, 7:4–8, 7:15–17, 12:24–28; Ex. 1003 ¶¶ 106–107. We construe “tessellate unit” as a means-plus-function limitation with the function of tessellating the transformed objects into rational and non-rational object surfaces in real-time (claims 1 and 11) including triangles (claim 2), and with the corresponding structure of a GPU including a dedicated processor coupled between the transform unit and the lighting unit, where the dedicated processor is programmed to execute the tessellating steps of the disclosed microcode.

4. *Renderer Unit*

Claims 1 and 11 both recite a GPU “comprising . . . a renderer unit.” Ex. 1001, 12:42–45, 13:64–66. Claim 2 depends from claim 1 and recites “the renderer unit renders the triangles by executing a second set of instructions,” which claim 11 also specifies. *Id.* at 12:54–55, 14:6–8.

The ’299 patent specification discloses that the function of rendering the transformed, tessellated, lighted objects is performed by a GPU including a dedicated processor programmed to execute the rendering steps of the disclosed microcode. *See* Ex. 1001, 6:61–65, 7:4–8, 7:17–19, 12:24–28; Ex. 1003 ¶¶ 110–111. We construe “rendering unit” as a means-plus-function limitation with the function of rendering the transformed, tessellated, lighted objects, and with the corresponding structure of a GPU including a dedicated processor to execute the rendering steps of the disclosed microcode.

5. *Remaining Claim Terms*

Upon review of the arguments and evidence presented at this stage of the proceeding, we determine no further construction of any claim term is needed at the present time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (per curiam) (claim terms need to be construed “only to the extent necessary to resolve the controversy” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Ground One—Obviousness over Sfarti and Foley*

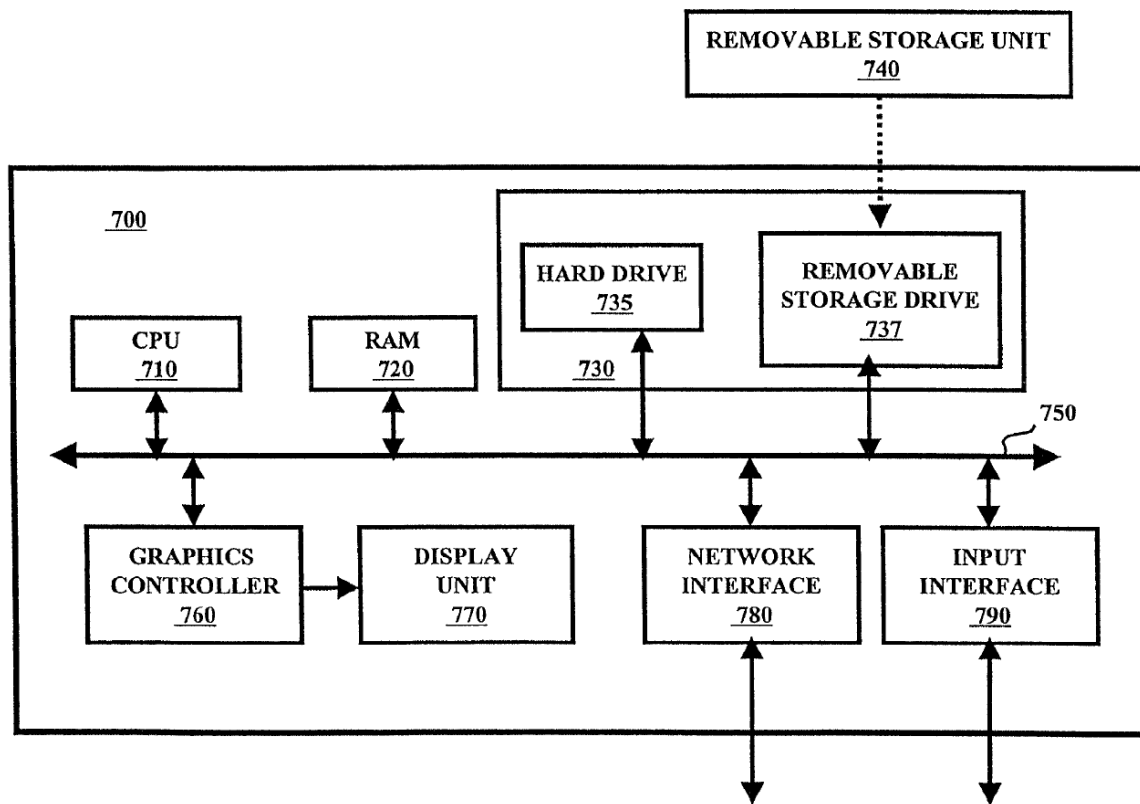
In Ground One, Petitioner argues claims 1–4, 9, 11, and 17 of the ’299 patent would have been obvious over Sfarti and Foley. *See* Pet. 2,

25–71; Ex. 1003 ¶¶ 117–216. The Preliminary Response does not address these arguments apart from urging denial under 35 U.S.C. § 325(d), discussed above in Section III.

We have reviewed the preliminary record, and we conclude Petitioner has demonstrated a reasonable likelihood of prevailing on its assertions as to at least claim 1. We begin our analysis with brief summaries of Sfarti and Foley, then we address Petitioner’s contentions.

1. Overview of Sfarti

Sfarti discloses a method and system for rendering bicubic surfaces of an object on a computer system. *See* Ex. 1009, codes (54), (57). Figure 3 is reproduced below.



Sfarti, Figure 3.

Figure 3 is a block diagram of computer system 100⁶ with CPU 110 and graphics controller 160. *Id.* ¶ 34.

Sfarti indicates graphics controller 160 receives commands and data from CPU 110, and “generates display signals (e.g., in RGB format) to display unit 170 . . . according to the commands and data received.” *Id.* ¶ 36. Sfarti explains the “execution of both subdivision [i.e., tessellation] and rendering is made possible inside the same graphics controller 160,” or alternatively “the subdivision can be executed by the CPU 110 while the rendering is executed by the graphic controller 160.” *Id.* ¶ 41. Sfarti indicates its computer systems perform steps of transforming vertices (Step 0), tessellating (Steps 1–4), calculating lighting (Step 5), and rendering (Step 8). *Id.* ¶ 42.

2. *Overview of Foley*

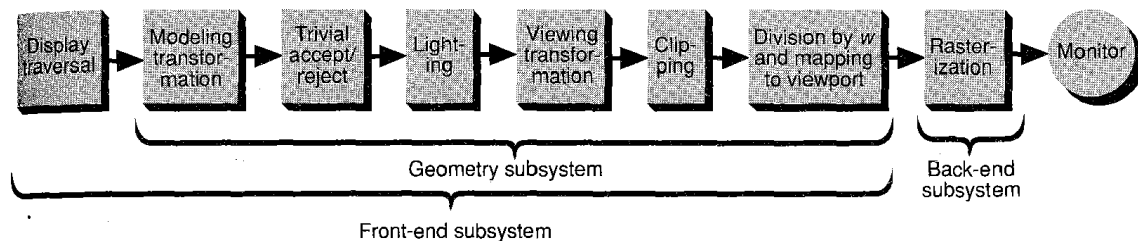
Foley is a reference book on computer graphics that is part of an IBM-sponsored collection of books, called “The Systems Programming Series,” about principles and techniques for various topics. Ex. 1007, ix. The book is designed for course work, but is also a detailed reference book. *Id.*

Within the extensive exploration of computer graphics topics, Foley includes a chapter titled “Advanced Raster Graphics Architecture.” *Id.*

⁶ As Petitioner points out, the element numbers in Figure 3 are in the 7XX range, rather than the 1XX range used in the written description of Sfarti. *See* Pet. 26 n.7. Like Petitioner, we will use the written description’s 1XX range of element numbers, which translate easily to the incorrect element numbers in the figure, as can be seen in the corrected version of Figure 3 in the ’501 patent. *See* Ex. 1014, Fig. 3.

at 855–922. The chapter examines “the major computations performed by raster systems, and the techniques that can be used to accelerate them,” noting that “[g]raphics systems architecture is a specialized branch of computer architecture.” *Id.* at 855. This includes using “speed-up techniques” of general-purpose computer architecture, such as “pipelining” and “parallelism.” *Id.*

Foley presents a logical model, for implementation in software or hardware, of a rendering pipeline for use in a graphics system, in Figure 18.7, reproduced below.



Foley, Figure 18.7.

Figure 18.7 shows a block diagram of a graphics pipeline for “Gouraud- or Phong-shaded polygons.” *Id.* at 867. Foley explains that the pipeline of Figure 18.7 “is typical for systems using conventional primitives (lines and polygons) and conventional shading techniques (constant, Gouraud, or Phong).” *Id.* Foley describes transforming the vertices of graphics primitives from an object-coordinate system to a world-coordinate system, and computing color for each polygon in an illumination model, and the use of parallelization to accelerate rendering. *See id.* at 868–869, 876. Foley also describes a particular algorithm, the Oslo algorithm, for tessellating. *See id.* at 509–510.

3. *Claim 1*

Petitioner provides arguments and evidence in support of contending claim 1 is unpatentable as having been obvious over Sfarti and Foley. *See* Pet. 25–66; Ex. 1003 ¶¶ 117–204.

a) *Reasons to Combine the Teachings of Sfarti and Foley*

Petitioner contends Sfarti teaches a GPU that performs the ordered steps of transforming, tessellating, lighting, and rendering. *See* Pet. 25–27 (citing Ex. 1009, Fig. 3, ¶¶ 16, 33–34, 39, 41–42); Ex. 1003 ¶¶ 117–119. Petitioner contends Foley teaches a graphics pipeline of dedicated processors where tessellating is performed after transforming. *See* Pet. 27–29 (citing Ex. 1007, 125, 807, 866–871); Ex. 1003 ¶¶ 120–125. Petitioner contends Foley teaches that a benefit of implementing the steps of Sfarti in the graphics pipeline of dedicated processors of Foley is providing more processing power than a single CPU can provide. *See* Pet. 29–30 (citing Ex. 1007, 855, 867, 873–874, 877); Ex. 1003 ¶¶ 126–131. Dr. Bajaj testifies that concurrent processing from Foley’s hardware pipeline of dedicated processors provides significant performance improvements, for example, “a non-pipelined construction that is divided into n pipelined stages should give a speed-up factor of n, which is the reason to use it.” Ex. 1003 ¶ 145 (quoting Ex. 1008, 8).

On this record, we agree with Petitioner that a person of ordinary skill would have implemented the steps of transforming, tessellating, lighting, and rendering as taught by Sfarti in a graphics pipeline of dedicated processors as taught by Foley to yield the benefits of providing more processing power than a single CPU can provide, and significantly

improving performance speed. *See* Pet. 31–38; Ex. 1003 ¶¶ 132–147. On this record we agree with Petitioner that a person of ordinary skill in the art would have performed tessellating after transforming using the graphics pipeline of dedicated processors of Foley to yield the benefits of adaptively determining tessellation size and limiting the amount of data that needs to be transformed as taught by Foley.

Petitioner also contends the combination of Sfarti and Foley is the use of Foley’s known technique of using a graphics pipeline of dedicated processors to improve the graphics controller of Sfarti in the same way, namely, to enhance performance via increased concurrent processing. *See* Pet. 38–39 (citing *KSR*, 550 U.S. at 415–21); Ex. 1003 ¶ 148. On this record, we agree with Petitioner, that Foley’s “technique of [using a graphics pipeline of dedicated processors] has been used to improve [a graphics processing] device, and a person of ordinary skill would recognize that it would improve [the graphics controller of Sfarti] in the same way,” therefore, “using the technique is obvious.” *KSR*, 550 U.S. at 417.

Petitioner moreover contends the combination of Sfarti and Foley combines the known prior art elements of Sfarti’s graphics processor performing the ordered functions of transforming, tessellating, lighting, and rendering, with Foley’s known hardware pipelining, according to Foley’s known method of assigning each of the ordered functions to its own dedicated processor, and does no more than yield the predictable result of increasing performance speed by concurrently processing the ordered functions of transforming, tessellating, lighting, and rendering. *See* Pet. 39 (citing *KSR*, 550 U.S. at 415–21); Ex. 1003 ¶ 149. On this record we agree with Petitioner that performing the known steps of transforming, tessellating,

lighting, and rendering as taught by Sfarti, using a separate, dedicated processor for executing each step as taught by Foley, does no more than yield the predictable result of increasing performance speed as taught by Foley.

Petitioner finally contends a person of ordinary skill would have had a reasonable expectation of success in implementing the steps of Sfarti using the graphics pipeline of dedicated processors of Foley, because pipeline architectures have been a popular approach to building high-performance graphics systems since the 1960s, and pipelining is a speed-up technique used in general purpose computer architecture over the several decades prior to Foley. *See* Pet. 39–40 (citing Ex. 1007, 855, 874, 877); Ex. 1003 ¶ 149.

Patent Owner does not presently dispute Petitioner’s foregoing contentions. For purposes of this decision, we find Petitioner cites sufficient evidence to support its contention that a person of ordinary skill in the art would have had reason to combine the teachings of Sfarti and Foley in the fashion proposed by Petitioner, with a reasonable expectation of success.

b) Claim Preamble

The preamble of claim 1 recites: “A graphics processing unit for rendering objects from a software application executing on a processing unit in which the objects to be rendered are transmitted to the graphics processing unit over a bus as control points of bicubic surfaces.” Ex. 1001, 12:38–42.

Petitioner assumes without conceding that the preamble is limiting, and contends Sfarti discloses a graphics processing unit (i.e., graphics controller 160) for rendering objects from a software application executing

on a processing unit (i.e., CPU 110), in which the objects to be rendered are transmitted to GPU 160 over a bus (i.e., communication path 150) as control points of bicubic surfaces. *See* Pet. 40–44 (citing Ex. 1009, code (57), Fig. 3, ¶¶ 1–2, 4, 16, 33–34, 36, 39–41, 43); Ex. 1003 ¶¶ 151–153.

Patent Owner does not presently dispute this contention. Based on the evidence and arguments currently of record, for purposes of institution, we conclude Petitioner has demonstrated Sfarti discloses the preamble of claim 1.

c) Transform Unit

Claim 1 recites that the GPU comprises “a transform unit.” Ex. 1001, 12:42–43. Petitioner contends the combination of Sfarti and Foley teaches this limitation. *See* Pet. 44–47; Ex. 1003 ¶¶ 159–165.

Petitioner contends Sfarti teaches the function of transforming graphic objects into transformed object, in describing software executed by GPU 160 that transforms the sixteen control points for each bicubic surface. *See* Pet. 44–45 (citing Ex. 1009 ¶¶ 16, 39–40, 42–43, claims 1, 21, 41, and 46); Ex. 1003 ¶¶ 160–162. Petitioner contends Foley teaches the structure of the claimed transform unit in describing floating-point processors, or geometry engines (GEs), arranged in a pipeline, where the first GE is programmed to transform vertices and vertex normals. *See* Pet. 45–47 (citing Ex. 1007, 877–879, 890–892, Fig. 18.19); Ex. 1003 ¶¶ 163–164.

Patent Owner does not presently dispute these contentions. Based on the evidence and arguments currently of record, for purposes of institution, we conclude Petitioner has demonstrated the combination of Sfarti and Foley discloses the transform unit of claim 1.

d) Lighting Unit

Claim 1 recites that the GPU comprises “a lighting unit.” Ex. 1001, 12:42–44. Petitioner contends the combination of Sfarti and Foley teaches this limitation. *See* Pet. 47–49; Ex. 1003 ¶¶ 166–173.

Petitioner contends Sfarti teaches the function of lighting surfaces resulting from the tessellate unit, in describing calculating lighting for vertices of the triangles received from the tessellation stage. *See* Pet. 47–48 (citing Ex. 1009 ¶¶ 40–42); Ex. 1003 ¶¶ 167–169. Petitioner contends Foley teaches the structure of the lighting unit in describing a programmable floating-point processor to perform lighting calculations. *See* Pet. 48–49 (citing Ex. 1007, 736–737, 721, 877–879, 891); Ex. 1003 ¶¶ 170–172.

Patent Owner does not presently dispute these contentions. Based on the evidence and arguments currently of record, for purposes of institution, we conclude Petitioner has demonstrated the combination of Sfarti and Foley discloses the lighting unit of claim 1.

e) Tessellate Unit

Claim 1 recites that the GPU comprises “a tessellate unit . . . for tessellating both rational and non-rational object surfaces in real-time.” Ex. 1001, 12:42–48. Petitioner contends the combination of Sfarti and Foley teaches this limitation. *See* Pet. 52–64; Ex. 1003 ¶¶ 181–199.

Petitioner contends Sfarti discloses the function of tessellating rational object surfaces and the function of tessellating non-rational object surfaces, and renders obvious doing both as part of one tessellation. *See* Pet. 52–59 (citing Ex. 1009, code (57), Figs. 5 and 8, ¶¶ 16, 31, 41–43, 48–59, 78, claim 14); Ex. 1003 ¶¶ 182–192. Petitioner’s asserted motivation is that

subdividing rational surface types “allow[s] for precise modeling of certain object types” and separately subdividing non-rational surface types “take[s] advantage of the computational efficiency when such precision is not required for object modeling.” Pet. 58–59; Ex. 1003 ¶ 192. Petitioner further asserts Sfarti discloses performing its tessellations in real-time, based on flatness of bounding boxes for two orthogonal curves that result from iterative subdivisions. *See* Pet. 59–63 (citing Ex. 1009, Fig. 6, ¶¶ 4, 16, 30–31, 41–43, 48–64, 71, 73–74); Ex. 1003 ¶¶ 193–196. Petitioner contends Foley teaches the structure of the claimed tessellate unit in describing that each stage of an object rendering pipeline is implemented as an individual processor, such that the tessellation stage of Sfarti is performed by a dedicated processor in Foley’s pipeline architecture. *See* Pet. 63–64 (citing Ex. 1007, 877, 879); Ex. 1003 ¶ 197.

Claim 1 further recites that the tessellate unit is “coupled between the transform unit and the lighting unit.” Ex. 1001, 12:46–47. Petitioner contends the combination of Sfarti and Foley teaches this limitation. *See* Pet. 64; Ex. 1003 ¶ 199. Petitioner contends the combination of Sfarti and Foley teaches each stage of Sfarti’s object rendering process is implemented as a dedicated processor using the pipeline architecture of Foley, such that the dedicated processor for transformation outputs transformed control points which are used by the dedicated processor for tessellation to generate triangles, and the dedicated processor for tessellation provides the triangle data to the dedicated processor for lighting. *See* Pet. 64; Ex. 1003 ¶ 199.

Patent Owner does not presently dispute the foregoing contentions. Based on the evidence and arguments currently of record, for purposes of

institution, we conclude Petitioner has demonstrated the combination of Sfarti and Foley discloses the tessellate unit of claim 1.

f) Renderer Unit

Claim 1 recites that the GPU comprises “a renderer unit.” Ex. 1001, 12:42–45. Petitioner contends the combination of Sfarti and Foley teaches this limitation. *See* Pet. 50–51; Ex. 1003 ¶¶ 174–178.

Petitioner contends Sfarti teaches the function of rendering the transformed, tessellated, lighted objects, in describing the rendering of all triangles produced after clipping and projection. *See* Pet. 50 (citing Ex. 1009 ¶¶ 41–42); Ex. 1003 ¶¶ 175–176. Petitioner contends Foley teaches the structure of the renderer unit in describing a programmable processor to perform the rendering of triangles. *See* Pet. 50–51 (citing Ex. 1007, 867, 875, 877, 888); Ex. 1003 ¶¶ 177–178.

Patent Owner does not presently dispute these contentions. Based on the evidence and arguments currently of record, for purposes of institution, we conclude Petitioner has demonstrated the combination of Sfarti and Foley discloses the renderer unit of claim 1.

g) Conclusion as to Claim 1

For the foregoing reasons, and based on the present record, we conclude Petitioner has provided sufficient argument and evidence in relation to the proposed obviousness of claim 1 over Sfarti and Foley, to demonstrate a reasonable likelihood that Petitioner would prevail with respect to this challenge at trial.

4. *Claims 2–4, 9–11, 17, and 18*

Pursuant to USPTO policy implementing *SAS*, we must “either (1) institute as to all claims challenged in the petition and on all grounds in the petition, or (2) institute on no claims and deny institution.” PTAB Consolidated Trial Practice Guide (Nov. 2019) (“CTPG”)⁷, 5–6, 64. We “will not institute on fewer than all claims or all challenges in a petition.” *Id.* at 5, 64; *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1359–60 (Fed. Cir. 2018) (stating a decision to institute is “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”). Further, Patent Owner does not argue these claims separately from claim 1. Thus, because we have decided to grant institution on Ground One against claim 1, we must do the same for claims 2–4, 9–11, 17, and 18.

E. *Ground Two—Obviousness over Sfarti, Foley, and Möller*

As discussed above, pursuant to USPTO policy implementing *SAS*, we must either institute as to all claims challenged in the petition and on all grounds in the petition, or deny institution entirely. *See supra* Section V.D.4 (citing CTPG 5–6, 64). Further, Patent Owner does not argue Ground Two separately from Ground One. Thus, because we have decided to grant institution on Ground One, we must do the same for Ground Two.

VI. CONCLUSION

For the above reasons, we decide not to exercise our discretion to deny institution under 35 U.S.C. § 325(d) or § 314(a). We further determine

⁷ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

the information presented in the record establishes there is a reasonable likelihood that Petitioner would prevail with respect to at least one claim of the '299 patent challenged in the Petition. Accordingly, we institute an *inter partes* review of claims 1–4, 9–11, 17, and 18 on all grounds presented in the Petition.

At this preliminary stage, the Board has not made a final determination with respect to the patentability of the challenged claims or any underlying factual or legal issue. The Board's final determination will be based on the record as developed during the *inter partes* review.

VII. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for the '299 patent, claims 1–4, 9–11, 17, and 18, on all grounds presented in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

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Patent 7,245,299 B2

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