

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

3D SURFACES, LLC,
Patent Owner.

IPR2022-01591
Patent RE42,534 E

Before JEFFREY S. SMITH, GEORGE R. HOSKINS, and
ROBERT L. KINDER, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Petitioner filed a Petition (Paper 3, “Pet.”) requesting *inter partes* review of claims 10–20 of U.S. Reissue Patent No. RE42,534 E (Ex. 1001, “the ’534 patent”) pursuant to 35 U.S.C. § 311(a). Patent Owner filed a Preliminary Response (Paper 7, “Prelim. Resp.”) pursuant to 35 U.S.C. § 313. With our authorization, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 9), and Patent Owner filed a Sur-Reply to Petitioner’s Preliminary Reply (Paper 10). Petitioner also filed an explanation for filing multiple petitions ranking its Petition in this proceeding ahead of its petition in Case IPR2022-01590 (Paper 2).

Pursuant to 35 U.S.C. § 314(a), the Director may not authorize an *inter partes* review unless the information in the petition and preliminary response “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition.” For the reasons that follow, we institute an *inter partes* review as to claims 10–20 of the ’534 patent on all grounds of unpatentability asserted in the Petition.

B. Related Matters

Patent Owner indicates that the ’534 patent is at issue in *3D Surfaces, LLC v. Dell Technologies Inc., et al*, Case No. 1-22-cv-00854 (W.D. Tex.). Paper 4, 1. Patent Owner indicates that the case was previously identified as Case No. 6-21-cv-01107, which is the case Petitioner identified. Paper 4, 1; Pet. 84.

Petitioner identifies it also is challenging the ’534 patent in IPR2022-01590. Pet. 82. Patent Owner identifies that same case, as well as *Dell Techs. Inc. et al. v. 3D Surfaces, LLC*, IPR2023-00005, and *Dell Techs. Inc.*

et al. v. 3D Surfaces, LLC, IPR2023-00006, as involving the '534 patent.
Paper 4, 1.

C. The '534 Patent

The '534 patent is directed to a method and apparatus for rendering bicubic surfaces in real-time on a computer system. *See* Ex. 1001, 1:28–30. Specifically, the patent teaches “a method and apparatus for minimizing the number of computations required for the subdivision of bicubic surfaces into triangles for real-time tessellation.” *Id.* at 4:41–44. Figure 3 of the '534 patent is reproduced below.

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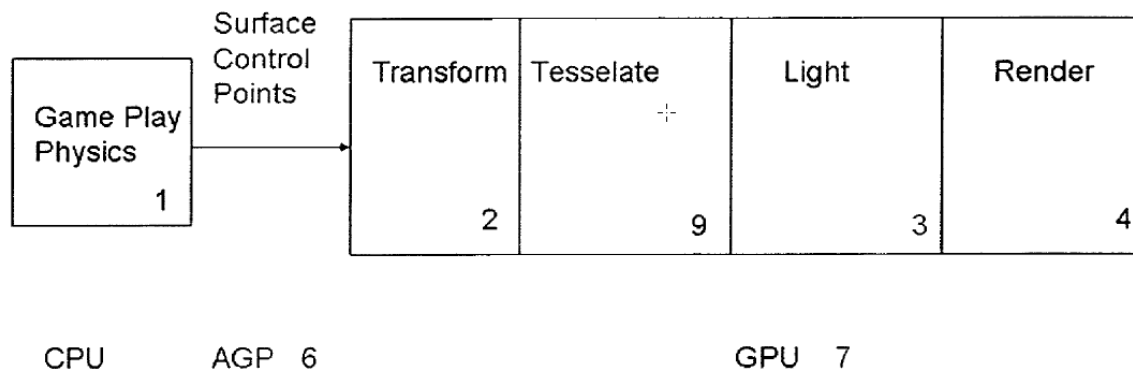


Figure 3

Figure 3 is a block diagram of the graphics system of the '534 patent, which includes CPU 1, AGP bus 6, and Graphics Processing Unit 7, comprised of “transform unit 2, a lighting unit 3, a renderer unit 4, and a tessellate unit 9 coupled between the transform unit 2 and the lighting unit 3 for tessellating both rational and non-rational object surfaces in real-time.” *Id.* at 7:9–14. CPU 1 executes a software application and transmits over the AGP bus 6 control points of the bicubic surfaces, which are transformed by

the transform unit 2, and then the surfaces are tessellated into triangles by the tessellate unit 9. *Id.* at 7:15–21.

D. Illustrative Claim

Challenged claim 10 of the '534 patent recites:

A system comprising:
a central processing unit;
a bus operatively connected to said central processing unit; and
a graphics processing unit operatively connected to said bus;
wherein the central processing unit transmits graphic objects to
said graphics processing unit via said bus; and
wherein said graphics processing unit comprises a transform unit
that transforms the graphic objects into transformed
objects;
a tessellation unit for tessellating the transformed objects,
wherein said tessellation unit is operatively coupled
between said transform unit and a lighting unit; and
said lighting unit comprising means for lighting triangles
resulting from said tessellation unit.

Ex. 1001, 14:48–64.

E. Evidence

Petitioner relies on the following prior art:

Foley, et al., “Computer Graphics: Principles and Practice,” 2nd
Ed., 1990 (Ex. 1007, “Foley”); and

U.S. Patent Appl. Publ. No. 2002/0033821 A1, published
March 21, 2002 (Ex. 1009, “Sfarti”¹).

¹ The Petition and the Preliminary Response both refer to this reference as “501-Pub” for reasons which will become clear below. We instead refer to it as “Sfarti” because the lead solely-named inventor is Adrian Sfarti.

F. Prior Art and Asserted Ground

Petitioner asserts that claims 10–20 of the '534 patent are unpatentable on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
10–20	103(a)	Sfarti, Foley

Pet. 2. Petitioner relies on the declaration testimony of Chandrajit L. Bajaj, Ph.D. (Ex. 1003).

G. Effective Filing Date of the Challenged '534 Patent Claims

The '534 patent was filed as U.S. Patent Application No. 12/767,997 on April 27, 2010. *See* Ex. 1001, codes (21) and (22). The “Related U.S. Application Data” field on the front page of the '534 patent indicates it is a reissue of U.S. Patent No. 7,532,213, which is a continuation of U.S. Patent No. 7,245,299 (“the '299 patent”) filed on Dec. 9, 2003, which is continuation-in-part of U.S. Patent Application No. 10/436,698 (“the '698 Application”) filed on May 12, 2003, which is a continuation-in-part of U.S. Patent No. 6,563,501 (“the '501 patent”) filed on Dec. 11, 2000. *See id.* at code (63). The “Related U.S. Application Data” field also lists U.S. Provisional Application No. 60/222,105 (“the '105 provisional”) filed on July 28, 2000. *See id.* at code (60). The Specification of the '299 patent begins with a “CROSS-REFERENCE TO RELATED APPLICATIONS” paragraph which also lists the '299 patent, the '698 application, the '501 patent, and the '105 provisional. *See id.* at 1:13–24.

Petitioner contends the effective filing date of the challenged '534 patent claims “is no earlier than May 12, 2003,” the filing date of the '698 Application. Paper 2, 4. In particular, according to Petitioner, the

challenged '534 patent claims are not entitled to the benefit of the filing date of the '501 patent, for various reasons. *See id.*; Pet. 17–28.

Patent Owner stipulates that: “If the Board declines to institute the [IPR2022-01590] petition under § 314(a), Patent Owner will not challenge the prior art status of [Sfarti] in [IPR2022-01591, the present proceeding].” Paper 8, 2. In this event, as characterized by Patent Owner, “there is no priority dispute” in the present proceeding. *Id.*

Contemporaneously with the present Decision instituting review in this proceeding, we are also entering a decision in IPR 2022-01590 that denies institution in that proceeding under § 314(a). Therefore, we treat Patent Owner’s stipulation as an admission, for the purposes of this proceeding, that Sfarti is prior art to the '534 patent

II. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is unpatentable under 35 U.S.C. § 103(a) if “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective evidence of obviousness or nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2016) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)). Furthermore, Petitioner does not satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person having ordinary skill in the art (“POSITA”) would have had “a Bachelor’s degree in computer science, computer engineering, electrical engineering, or a related scientific field, and approximately two years of work experience in computer graphics or, alternatively, two years work towards a masters or doctorate degree in these

scientific fields.” Pet. 12 (citing Ex. 1003 ¶ 97). At this stage of the proceeding, Patent Owner “applies Petitioner’s definition.” Prelim. Resp. 10. We agree with Petitioner’s proposed definition of the level of ordinary skill in the art and apply it for purposes of this Decision.

C. Claim Interpretation

We interpret the challenged claims

using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b) (2019). “In determining the meaning of [a] disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006). Claim terms are given their plain and ordinary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner contends that the terms “tessellation unit,” “transform unit,” “lighting unit,” and “rendering unit” require construction in this proceeding. Pet. 12. Petitioner contends that these terms should be construed as means

plus function terms because they recite function without reciting sufficient structure for performing that function. *Id.* Patent Owner contends that “at this time, the Board need not construe any term in denying institution.”

Prelim. Resp. 10.

On this record, we agree with Petitioner that “unit” does not connote any particular structure, and that the terms “tessellation unit,” “transform unit,” “lighting unit,” and “rendering unit” recite function without reciting sufficient structure for performing that function. Therefore, these terms should be construed as means plus function terms. “Construing a means-plus-function claim term is a two-step process. The court must first identify the claimed function. Then, the court must determine what structure, if any, disclosed in the specification corresponds to the claimed function.”

Williamson v. Citrix Online, LLC, 792 F.3d 1339, 1351 (Fed. Cir. 2015) (en banc) (citation omitted). In cases involving a special purpose computer-implemented means-plus-function limitation, the Federal Circuit requires “that the specification disclose an algorithm for performing the claimed function.” *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015). “A description of the function in words may disclose, at least to the satisfaction of one of ordinary skill in the art, enough of an algorithm to provide the necessary structure under § 112, ¶ 6.”

Typhoon Touch Techs., Inc. v. Dell, Inc., 659 F.3d 1376, 1385 (Fed. Cir. 2011). “The law is clear that patent documents need not include subject matter that is known in the field of the invention and is in the prior art, for patents are written for persons experienced in the field of the invention.” *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1371 (Fed. Cir. 2001).

a) Transform unit

Claim 10 recites “a transform unit that transforms the graphic objects into transformed objects.” Claim 15 recites a similar limitation. Claim 12 recites “said transform unit transforms the spatial coordinates of said graphic objects.” The specification discloses that the function of “transform[ing] the graphic objects into transformed objects” and “transform[ing] the spatial coordinates of said graphic objects” is performed by a graphics processing unit (GPU) including a dedicated processor programmed to execute the transform step of the disclosed microcode. Ex. 1001, 5:63–6:3; 7:10–15, 7:19–20, 12:49–52; Ex. 1003 ¶¶ 106–107. We construe “transform unit” as a means plus function limitation with the function of transforming graphic objects into transformed objects (claims 10 and 15), or the function of transforming the spatial coordinates of said graphic objects (claim 12), and with the corresponding structure of a GPU including a dedicated processor programmed to execute the transform step of the microcode disclosed in the specification.

b) Tessellation unit

Claim 10 recites “a tessellation unit for tessellating the transformed objects.” Claims 11 and 15 recite a similar limitation. The specification discloses that the function of “tessellating the transformed objects” is performed by a GPU that includes a dedicated processor coupled between the transform unit and a lighting unit, where the dedicated processor is programmed to execute the tessellating steps of the disclosed microcode. Ex. 1001, 6:4–59, 7:10–15, 7:20–24, 12:49–52; Ex. 1003 ¶¶ 108–109. We construe “tessellation unit” as a means plus function limitation with the function of tessellating the transformed objects and with the corresponding structure of a GPU including a dedicated processor coupled between the

transform unit and the lighting unit, where the dedicated processor is programmed to execute the tessellating steps of the disclosed microcode.

c) Lighting unit

Claim 10 recites a “lighting unit comprising means for lighting triangles resulting from said tessellation unit.” Claim 13 recites “a lighting unit . . . for lighting the tessellated transformed objects.” Claim 15 recites “lighting vertices of triangles resultant from said tessellating using said lighting unit.” The specification discloses that the function of “lighting triangles resulting from said tessellation unit,” “lighting the tessellated transformed objects,” and “lighting vertices of triangles resultant from said tessellating” is performed by a GPU that includes a dedicated processor programmed to execute code to light the vertices of the triangles. Ex. 1001, 6:60–65, 7:10–15, 7:24–26, 12:49–52; Ex. 1003 ¶¶ 110–111. We construe “lighting unit” as a means plus function limitation with the function of lighting triangles resulting from said tessellation unit (claim 10), lighting the tessellated transformed objects (claim 13), or lighting vertices of triangles resultant from said tessellating (claim 15), and with the corresponding structure of a GPU that includes a dedicated processor programmed to execute code to light the tessellated objects.

d) Rendering unit

Claim 14 recites “a rendering unit operatively coupled to the lighting unit for rendering the lighted, tessellated, transformed objects.” The specification discloses that the function of rendering the lighted, tessellated, transformed objects is performed by a GPU that includes a dedicated processor programmed to execute the rendering steps of the disclosed microcode. Ex. 1001, 6:65–7:3, 7:10–15, 7:24–26, 12:49–52; Ex. 1003 ¶¶ 112–113. We construe “rendering unit” as a means plus function

limitation with the function of rendering the lighted, tessellated, transformed objects, and with the corresponding structure of a GPU that includes a dedicated processor to execute the rendering steps of the disclosed microcode.

e) Remaining claim terms

No other terms require express construction at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“Because we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy,’ we need not construe [a particular claim limitation] where the construction is not ‘material to the . . . dispute.’” (citation omitted)).

D. Discretion Under 35 U.S.C. § 325(d)

1. Advanced Bionics

Patent Owner asserts that we should exercise our discretion to deny institution of the *inter partes* review under 35 U.S.C. § 325(d). Prelim. Resp. 15–29. For the reasons that follow, we decline to deny institution on that basis.

In evaluating arguments under § 325(d), we use:

[a] two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of [the] first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential); *see also Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first

paragraph) (listing factors to consider in evaluating the applicability of § 325(d)) (“Becton, Dickinson”).

Under the first part of *Advanced Bionics*, we consider factors (a), (b), and (d) of *Becton, Dickinson* in the evaluation of whether the same or substantially the same art or arguments were previously presented to the Office. *Advanced Bionics*, Paper 6 at 10. *Becton, Dickinson* identifies these factors as:

(a) the similarities and material differences between the asserted art and the prior art involved during examination;

(b) the cumulative nature of the asserted art and the prior art evaluated during examination; and

(d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art. *Becton, Dickinson*, Paper 8 at 17–18. If the first part of the *Advanced Bionics* framework is satisfied, we turn to the second part, where we consider *Becton, Dickinson* factors (c), (e), and (f) in the evaluation of whether a petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Becton, Dickinson* identifies these factors as:

(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

(e) whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and

(f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18.

2. *Advanced Bionics Framework, First Part*

The ground asserted by Petitioner involves Foley. Pet. 1. Patent Owner contends that Foley was previously presented to the Office. Prelim. Resp. 22. Petitioner contends that “although [Patent Owner] filed one IDS during prosecution of the ’213 patent²], citing pages 511–527 of Foley, most of the portions relied upon in this Petition were not presented to or considered by the Examiner relative to the challenged claims.” Pet. 78.

We agree with Petitioner. Pages 511–527 of Foley were previously presented to the Office. *See* Ex. 1001, code (56). In contrast, Petitioner relies on pages 17, 279–281, 508, 521, 721, 736–737, 807, 855, 866–871, 873–879, 888, and 890–892 of Foley. *See* Pet. 30–77. Out of all of the pages of Foley cited in the Petition, only one, page 521, was previously presented to the Office. On the record before us, there is no indication that any of the remaining pages of Foley cited in the Petition were presented to, or considered by, the Office. Notably, the IDS disclosure cited just 17 pages out of Foley’s over 1200 pages of content, but did not cite the pages that teach the feature that the Examiner found was patentable over the prior art. *Compare* Ex. 1017, at 177 (In the statement of allowable subject matter, the Examiner concluded that “the prior [art] fails to teach a tessellate unit coupled between the transform unit and the lighting unit.”), *with* Ex. 1007, at 807 (Foley teaches that “tessellation should occur after transformation into a coordinate system in which screen size can be determined” for the benefits of “enabl[ing] tessellation size to be determined adaptively, and limit[ing] the amount of data that is transformed.”); *see also id.* at 866–877. Thus, the

² U.S. Patent No. 7,532,213, which was reissued as the ’534 patent at issue here. *See* Ex. 1001, code (64).

pages of Foley cited in the Petition, with the exception of page 521, were not previously presented to the Office.

Patent Owner contends that even if Petitioner cites to portions of Foley not considered by the Office, the Examiner considered other references that are cumulative to and substantially the same as the portions of Foley cited by Petitioner. Prelim. Resp. 22. In particular, Patent Owner contends that the '534 patent recognizes that pipeline graphics architecture was well-known at the time of invention, and that other references that teach pipeline graphics architecture were considered by the Office. Prelim. Resp. 23–24 (citing Ex. 1001, Fig. 2, 2:42–58; Ex. 1032, Fig. 2b, 5:18–22; Ex. 1033, Fig. 1A, 6:28–31, 21:1–3). We disagree with Patent Owner. Foley's disclosure of a pipeline graphics architecture that teaches the benefits of employing dedicated processors for tessellating after transforming is explicit and, so far as we can tell from the record presented, is not found in any reference previously cited to the Office. *See* Ex. 1007, 807, 866–877. Thus, the same or substantially the same art was not previously presented to the Office.

Patent Owner contends that the Office previously considered the same argument presented by Petitioner. Prelim. Resp. 24–25. According to Patent Owner, during prosecution of the '299 patent³, the Examiner stated that it would have been obvious to modify the '501 patent's⁴ teachings to implement the processing steps of the '501 patent in a GPU, which is the same as Petitioner's argument. *Id.* at 25 (citing Ex. 1017, at 65–67).

³ U.S. Patent No. 7,245,299, which issued from a parent application identified on the face of the '534 patent. *See* Ex. 1001, code (63).

⁴ U.S. Patent No. 6,563,501, which issued from a parent application identified on the face of the '534 patent. *See* Ex. 1001, code (63).

We disagree. During prosecution of the '299 patent, the Examiner stated that “it would have been obvious to one of ordinary skill to substitute the computer readable medium of claim 21 [of the '501 patent] with the graphics processing unit of claims 1–3 and 12–14 [of the pending application].” Ex. 1017, 67. The Examiner, in making this obviousness-type double patenting rejection⁵, did not find a prior art reference that showed a graphics processing unit. Rather, the Examiner attempted to use the graphics processing unit recited in the pending claims as prior art against itself. The Applicant successfully argued against the Examiner’s improper use of the pending claims as prior art by stating that the '501 patent did not disclose the graphics processing unit incorporating the tessellation unit as claimed. *Id.* at 138, 175.

Contrary to Patent Owner’s contention, during prosecution of the '299 patent, the Examiner did not combine the processing steps of the '501 patent with any prior art that teaches a pipeline graphics processing unit, let alone prior art that teaches both a pipeline GPU and that “[t]essellation should occur after transformation” in order to “enable[] tessellation size to be determined adaptively, and [to] limit[] the amount of data that is transformed,” as does Foley. Ex. 1007, at 807. Even Patent Owner has not, at this point, disputed in this proceeding that the combination of Sfarti and Foley as presented in the Petition teaches a tessellation unit coupled between the transform unit and the lighting unit. Therefore, we find that the same or substantially the same arguments were not previously presented to the Office.

⁵ The Examiner did not make a prior art rejection using the '501 patent. *See* Ex. 1017, 65-73.

In sum, we determine that the asserted prior art and arguments are not substantially the same as those previously presented to the Office, and that the first part of the *Advanced Bionics* framework is not met. We do not proceed to the second part. We decline to exercise discretion to deny under 35 U.S.C. § 325(d).

E. Discretionary Denial under 35 U.S.C. § 314(a)

Institution of *inter partes* review is discretionary. *See Harmonic Inc.*, 815 F.3d at 1367 (“[T]he [U.S. Patent and Trademark Office] is permitted, but never compelled, to institute an IPR proceeding.”). Patent Owner urges the Board to exercise discretion to deny institution of *inter partes* review under § 314(a) based on the factors established in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2126495, at 2–3 (PTAB Mar. 20, 2020) (precedential). Prelim. Resp. 50–54.

On June 21, 2022, the Director of the USPTO issued an Interim Procedure for Discretionary Denials in AIA Postgrant Proceedings with Parallel District Court Litigation, *available at* https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (the “Interim Procedure”). The Interim Procedure explains that “[c]onsistent with *Sotera Wireless, Inc.*, the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure 3 (internal footnote omitted) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)). The Interim Procedure explains that a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and duplicative efforts between the district

court and the PTAB [and] allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8.

The defendants in the co-pending litigation, Dell Technologies and Dell Inc. (“Dell”), who are real parties-in-interest in this case, have offered a *Sotera* stipulation agreeing that upon institution, Dell will not pursue any grounds in the co-pending litigation that were raised or reasonably could have been raised in its IPR Petition for the challenged claims. Paper 9, 1; IPR2023-00006, Paper 12. Contemporaneously with the present Decision, we are issuing a decision in IPR2023-00006 instituting review of the ’534 patent on the same ground being instituted here, and we also are joining the two proceedings together for purposes of trial. Thus, Dell’s stipulation has taken effect.

Dell offered the stipulation before our Decision on whether to institute, which is appropriate. *See NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 at 4 (PTAB Sept. 7, 2022) (precedential) (Director’s holding “that the only appropriate time for a petitioner to offer a stipulation related to the *Fintiv* factor 4 analysis is prior to the Board’s decision of whether to institute review”).

Patent Owner argues that the *Sotera* stipulation is not dispositive, because Intel did not offer a *Sotera* stipulation or provide assurance that it will not participate in the co-pending litigation. Paper 10, 1. However, Intel is not a party to the co-pending litigation because Patent Owner has not sued Intel in district court. Therefore, Intel is not obligated to make a *Sotera* stipulation in district court. Further, the guidance under the Interim Procedure does not require a prospective stipulation because *Fintiv* does not apply to potential litigation, it only applies to active litigation. The Interim Procedure explicitly says that “the PTAB will not discretionarily deny

institution in view of parallel district court litigation,” not potential district court litigation, “where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure 3. Given the *Sotera* stipulation in the District Court Litigation by Dell (which is the only party sued by Patent Owner in that litigation), and the guidance under the Interim Procedure, we decline to exercise discretion to deny institution in this proceeding.

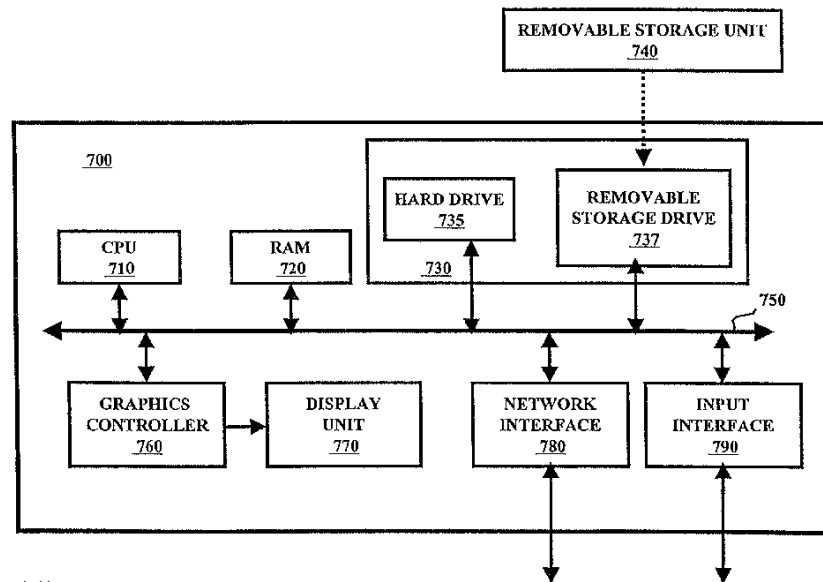
F. Obviousness Ground based on Sfarti and Foley

Petitioner contends that claims 10–20 would have been obvious over the combined teachings of Sfarti and Foley. Pet. 28–77.

1. Overview of Sfarti

Sfarti is the pre-grant publication of the application that led to the ’501 patent. Ex. 1001, code (63). Sfarti discloses a method and system for rendering bicubic surfaces of an object on a computer system. *See* Ex. 1009, codes (54), (57).

Figure 3 is a block diagram of a computer system of Sfarti, and is reproduced below.



Sfarti, Figure 3, showing computer system 100⁶ with CPU 110 and graphics controller 160. *Id.* ¶ 34.

Sfarti describes that graphics controller 160 receives commands and data from CPU 110, and “generates display signals (e.g., in RGB format) to display unit 170. The display signals are generated according to the commands and data received.” *Id.* ¶ 36. Sfarti explains that the “execution of both subdivision [tessellation] and rendering is made possible inside the same graphics controller 160. Alternatively, the subdivision can be executed by the CPU 110 while the rendering is executed by the graphic controller 160.” *Id.* ¶ 41. Sfarti describes its computer systems perform steps of

⁶ As pointed out by Petitioner, the element numbers in Figure 3 are in the 7XX range, rather than the 1XX range used in the portion of the Specification describing the figure. Pet. 29 n. 9. We will also use the Specification’s element numbers, which translate easily to the incorrect element numbers in the figure, as can be seen in the corrected version of Figure 3 in the ’501 patent.

transforming vertices (Step 0), tessellating (Steps 1–4), calculating lighting (Step 5), and rendering (Step 8). *Id.* ¶ 42.

2. Overview of *Foley*

Foley is a reference book on computer graphics that is part of an IBM-sponsored collection of books, called “The Systems Programming Series,” about principles and techniques for various topics. Ex. 1007, ix. The book is designed for course work, but also is a detailed reference book. *Id.*

Within the extensive exploration of computer graphics topics, *Foley* includes a chapter titled “Advanced Raster Graphics Architecture.” *Id.* at 855–922. The chapter examines “the major computations performed by raster systems, and the techniques that can be used to accelerate them,” noting that “[g]raphics systems architecture is a specialized branch of computer architecture.” *Id.* at 855. This includes using “speed-up techniques” of general-purpose computer architecture, such as “pipelining” and “parallelism.” *Id.*

Foley presents a logical model, for implementation in software or hardware, of a rendering pipeline for use in graphics system, in Figure 18.7, reproduced below.

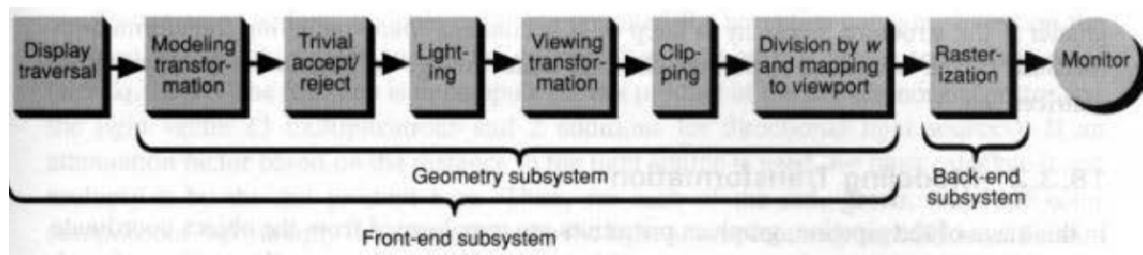


Figure 18.7 shows a block diagram of a graphics pipeline for “Gourand- or Phong-shaded polygons.” *Id.* at 867.

Foley explains that the pipeline of Figure 18.7 “is typical for systems using conventional primitives (lines and polygons) and conventional shading

techniques (constant, Gouraud, or Phong).” *Id.* Foley describes transforming the vertices of graphics primitives from an object-coordinate system to a world-coordinate system, and computing color for each polygon in an illumination model, and the use of parallelization to accelerate rendering. *Id.* at 868, 876. Foley also describes a particular algorithm, the Oslo algorithm, for tessellating. *Id.* at 509–510.

3. *Obviousness over Sfarti and Foley*

Reasons to combine the teachings of Sfarti and Foley

Petitioner contends that Sfarti teaches a graphics processing unit that performs the ordered steps of transforming, tessellating, and lighting. Pet. 36–38 (citing Ex. 1009 ¶ 42). Petitioner contends that Foley teaches a graphics pipeline of dedicated processors where tessellating is performed after transforming. Pet. 37 (citing Ex. 1007, at 807). Petitioner contends that Foley teaches that a benefit of implementing the steps of Sfarti in the graphics pipeline of dedicated processors of Foley is providing more processing power than a single CPU can provide. Pet. 39 (citing Ex. 1007, 873, 874, 877). Dr. Bajaj testifies that concurrent processing from Foley’s hardware pipeline of dedicated processors provides significant performance improvements, for example, “a non-pipelined construction that is divided into n pipelined stages should give a speed-up factor of n, which is the reason to use it.” Ex. 1003 ¶ 147 (quoting Ex. 1008, at 8).

On this record, we agree with Petitioner that a person of ordinary skill would have implemented the steps of transforming, tessellating, and lighting as taught by Sfarti in a graphics pipeline of dedicated processors as taught by Foley to yield the benefits of providing more processing power than a single CPU can provide, and significantly improving performance speed. On this record, we agree with Petitioner that a person of ordinary skill in the art

would have performed tessellating after transforming using the graphics pipeline of dedicated processors of Foley to yield the benefits of adaptively determining tessellation size and limiting the amount of data that needs to be transformed as taught by Foley.

Petitioner contends that the combination of Sfarti and Foley is the use of Foley's known technique of using a graphics pipeline of dedicated processors to improve the graphics controller of Sfarti in the same way, namely, to enhance performance via increased concurrent processing. Pet. 41 (citing *KSR Int'l.*, 550 US 415–21). On this record, we agree with Petitioner, that Foley's "technique of [using a graphics pipeline of dedicated processors] has been used to improve [a graphics processing] device, and a person of ordinary skill would recognize that it would improve [the graphics controller of Sfarti] in the same way," therefore, "using the technique is obvious." *KSR Int'l.*, 550 US at 417.

Petitioner contends that the combination of Sfarti and Foley combines the known prior art elements of Sfarti's graphics processor performing the ordered functions of transforming, tessellating, and lighting, with Foley's known hardware pipelining, according to Foley's known method of assigning each of the ordered functions to its own dedicated processor, and does no more than yield the predictable result of increasing performance speed by concurrently processing the ordered functions of transforming, tessellating, and lighting. Pet. 42 (citing *KSR Int'l.*, 550 US at 415–421). On this record, we agree with Petitioner that performing the known steps of transforming, tessellating, and lighting as taught by Sfarti, using a separate, dedicated processor for executing each step as taught by Foley, does no more than yield the predictable result of increasing performance speed as taught by Foley.

Petitioner contends that a person of ordinary skill would have had a reasonable expectation of success in implementing the steps of Sfarti using the graphics pipeline of dedicated processors of Foley, because pipeline architectures have been a popular approach to building high-performance graphics systems since the 1960s, and pipelining is a speed-up technique used in general purpose computer architecture over the last several decades. Pet. 43 (citing Ex. 1007, 855, 874, 877).

For purposes of this decision, we find Petitioner cites sufficient evidence to support its contention that a person of ordinary skill in the art would have had reason to combine the teachings of Sfarti and Foley.

A central processing unit

Claim 10 recites “a central processing unit.” Petitioner contends that Sfari discloses this limitation in describing central processing unit (CPU) 110. Pet. 43 (citing Ex. 1009, Fig. 3). Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that Sfarti discloses this limitation of claim 10.

A bus operatively connected to said central processing unit

Claim 10 recites “a bus operatively connected to said central processing unit.” Petitioner contends that Sfari discloses this limitation in describing CPU 110 connected to communication path 150, which may contain several buses. Pet. 44 (citing Ex. 1009 ¶ 34, Fig. 3). Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that Sfarti discloses this limitation of claim 10.

a graphics processing unit (GPU) operatively connected to said bus

Claim 10 recites “a graphics processing unit operatively connected to said bus.” Petitioner contends that Sfari discloses this limitation in

describing graphics controller 160 connected to communication path 150, which may contain several buses. Pet. 44 (citing Ex. 1009 ¶ 34, Fig. 3). Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that Sfarti discloses this limitation of claim 10.

Wherein the CPU transmits graphic objects to the GPU via the bus

Claim 10 recites “wherein the central processing unit transmits graphic objects to said graphics processing unit via said bus.” Petitioner contends that Sfarti discloses this limitation in describing that the CPU sends control points which define surfaces representing graphic objects to graphics controller 160, which then renders the image. Pet. 45–47 (citing Ex. 1009 ¶¶ 2, 34, 40–41, 43, Fig. 3). Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that Sfarti discloses this limitation of claim 10.

Wherein the GPU comprises a transform unit

Claim 10 recites “wherein said graphics processing unit comprises a transform unit that transforms the graphic objects into transformed objects.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 47–48. Petitioner contends that Sfarti teaches the function of transforming graphic objects into transformed objects in describing software executed by graphics controller 160 that transforms the 16 control points for each bicubic surface. Pet. 48–49 (citing Ex. 1009 ¶¶ 16, 39–42). Petitioner contends that Foley teaches the structure of the claimed transform unit in describing floating-point processors, or geometry engines (GEs), arranged in a pipeline, where the first GE is programmed to transform vertices and vertex normals. Pet. 49–50 (citing Ex. 1007, 877–879, 890–892, Fig. 18.19). Based on the evidence and arguments currently of record, for

purposes of institution, we find that Petitioner has demonstrated that the combination of Sfarti and Foley teaches this limitation of claim 10.

A tessellation unit

Claim 10 recites “a tessellation unit for tessellating the transformed objects.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 50–51. Petitioner contends that Sfari teaches the function of tessellating transformed objects in describing a subdivision algorithm that generates triangles by connecting neighboring vertices. Pet. 51–55 (citing Ex. 1009 ¶¶ 41–42). Petitioner contends that Foley teaches the structure of the claimed tessellation unit in describing that each stage of an object rendering pipeline is implemented as an individual processor, such that the tessellation stage of Sfarti is performed by a dedicated processor in Foley’s pipeline architecture. Pet. 57 (citing Ex. 1007, 877, 879).

Claim 10 recites that the “tessellation unit” is “operatively coupled between said transform unit and a lighting unit.” Petitioner contends that the combination of Sfarti and Foley teaches each stage of Sfarti’s object rendering process is implemented as a dedicated processor using the pipeline architecture of Foley, such that the dedicated processor for transformation outputs transformed control points which are used by the dedicated processor for tessellation to generate triangles, and the dedicated processor for tessellation provides the triangle data to the dedicated processor for lighting. Pet. 58. Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that the combination of Sfarti and Foley teaches this limitation of claim 10.

A lighting unit

Claim 10 recites “said lighting unit comprising means for lighting triangles resulting from said tessellation unit.” Petitioner contends that the

combination of Sfari and Foley teaches this limitation. Pet. 58–59.

Petitioner contends that Sfari teaches the function of lighting triangles in describing calculating lighting for vertices of the triangles received from the tessellation stage. Pet. 59–60 (citing Ex. 1009 ¶¶ 40–42). Petitioner contends that Foley teaches the structure of the lighting unit in describing a programmable floating-point processor to perform lighting calculations. Pet. 60–61 (citing Ex. 1007, 878). Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that the combination of Sfarti and Foley teaches this limitation of claim 10.

Based on the evidence and arguments currently of record, for purposes of institution, we find that Petitioner has demonstrated that a person of ordinary skill would have reason to combine the teachings of Sfari and Foley and that their combined teachings would have taught or suggested the features recited in claim 10 to an ordinarily skilled artisan. Patent Owner, at this stage, does not set forth arguments for claim 10. On this record, we are persuaded that Petitioner has shown a reasonable likelihood of prevailing on its assertion that claim 10 is unpatentable over Sfari and Foley.

Petitioner sets forth contentions regarding claims 11–20. Pet. 63–77. Patent Owner does not set forth arguments for these claims at this stage. We find Petitioner’s contentions sufficiently persuasive for purposes of institution that claims 11–20 would have been obvious over the combination of Sfari and Foley.

III. CONCLUSION

Based on the arguments presented in the Petition, we conclude that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '534 patent challenged in the Petition. Accordingly, we institute a trial on all claims and all grounds asserted in the Petition. The Board has not made a final determination under 35 U.S.C. § 318(a) with respect to the patentability of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 10–20 of the '534 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '534 patent shall commence on the entry date of this Decision, and notice is hereby given of the institution of a trial.

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Patent RE42,534 E

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