

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION, DELL TECHNOLOGIES INC., and DELL INC.,
Petitioner,

v.

3D SURFACES, LLC,
Patent Owner.

IPR2022-01591¹
Patent RE42,534 E

Before JEFFREY S. SMITH, GEORGE R. HOSKINS, and
ROBERT L. KINDER, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

¹ IPR2023-00006 has been joined with this proceeding. *See* Paper 14.
Accordingly, a copy of this Decision will also be entered into the record of
IPR2023-00006.

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition (Paper 3, “Pet.”) pursuant to 35 U.S.C. §§ 311–319 to institute an *inter partes* review of U.S. Patent No. RE42,534 E (Ex. 1001, “the ’534 patent”), claims 10–20. We issued an Institution Decision (Paper 12, “Inst. Dec.”) instituting the petitioned review.

3D Surfaces, LLC (“Patent Owner”) then filed a Patent Owner Response (Paper 19, “PO Resp.”) to the Petition. Petitioner filed a Reply (Paper 22, “Pet. Reply”) to the Patent Owner Response. Patent Owner filed a Sur-reply (Paper 23, “PO Sur-reply”) to the Reply.

An oral hearing was held on January 16, 2024, for which the transcript was entered into the record (Paper 29, “Tr.”).

We have jurisdiction under 35 U.S.C. § 6(b)(4) and § 318(a). This Decision is a final written decision under 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 as to the patentability of claims 10–20 of the ’534 patent. We determine Petitioner has shown by a preponderance of the evidence that those claims are unpatentable.

II. BACKGROUND

A. *Real Parties-in-Interest and Related Proceedings*

Petitioner identifies itself (i.e., Intel Corporation), as well as Dell Technologies Inc. and Dell Inc., as real parties-in-interest for Petitioner. *See* Pet. 81. Patent Owner identifies itself (i.e., 3D Surfaces, LLC) as the real party-in-interest for Patent Owner. *See* Paper 4, 1.

The parties identify one district court litigation involving the ’534 patent: *3D Surfaces, LLC v. Dell Techs. Inc., et al.*, No. 1:22-cv-00854

(W.D. Tex.) (“the District Court Litigation”). *See* Pet. 81–82; Paper 4, 1 (explaining the District Court Litigation was previously No. 6:21-cv-01107, the case number Petitioner identifies). The Court has stayed the litigation “through the PTAB’s issuance of its final written decision.” *3D Surfaces v. Dell Techs.*, Docket No. 97.

The parties further identify three other IPR proceedings challenging the ’534 patent: IPR2022-01590; IPR2023-00005; and IPR2023-00006. *See* Pet. 81; Paper 4, 1.

B. The ’534 Patent

The ’534 patent is directed to a method and apparatus for rendering bicubic surfaces in real-time on a computer system. *See* Ex. 1001, 1:28–30. Specifically, the patent teaches “a method and apparatus for minimizing the number of computations required for the subdivision of bicubic surfaces into triangles for real-time tessellation.” *Id.* at 4:41–44. Figure 3 of the ’534 patent is reproduced below.

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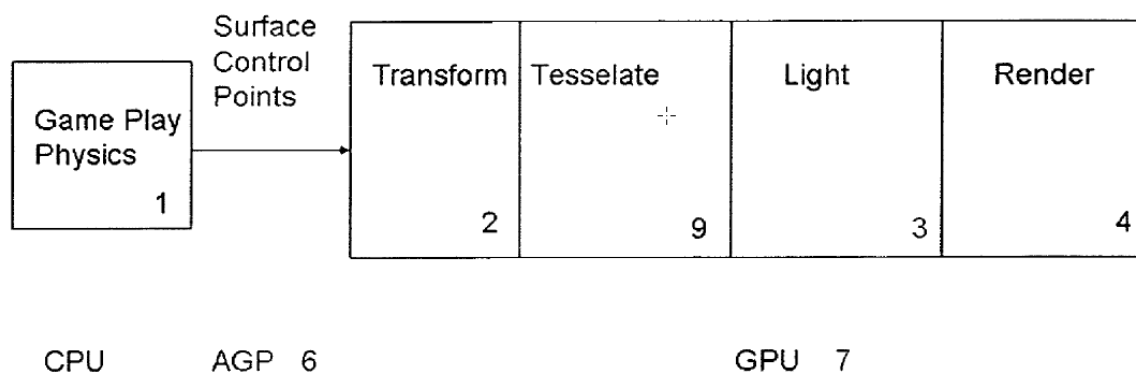


Figure 3

Figure 3 is a block diagram of the graphics system of the '534 patent, which includes CPU 1, AGP bus 6, and Graphics Processing Unit 7, comprised of “transform unit 2, a lighting unit 3, a renderer unit 4, and a tessellate unit 9 coupled between the transform unit 2 and the lighting unit 3 for tessellating both rational and non-rational object surfaces in real-time.” *Id.* at 7:9–14. CPU 1 executes a software application and transmits over the AGP bus 6 control points of the bicubic surfaces, which are transformed by the transform unit 2, and then the surfaces are tessellated into triangles by the tessellate unit 9. *Id.* at 7:15–21.

C. The Challenged Claims of the '534 Patent

Challenged claim 10 of the '534 patent recites:

A system comprising:

a central processing unit;

a bus operatively connected to said central processing unit; and

a graphics processing unit operatively connected to said bus;

wherein the central processing unit transmits graphic objects to said graphics processing unit via said bus; and

wherein said graphics processing unit comprises a transform unit that transforms the graphic objects into transformed objects;

a tessellation unit for tessellating the transformed objects, wherein said tessellation unit is operatively coupled between said transform unit and a lighting unit; and said lighting unit comprising means for lighting triangles resulting from said tessellation unit.

Ex. 1001, 14:48–64.

D. Asserted Prior Art

Petitioner relies principally on the following two prior art references in this proceeding. *See* Pet. 1–2.

Name	Reference	Pub. Date	Exhibit No.
Sfarti ²	US 2002/0033821 A1	Mar. 2002	1009
Foley	James D. Foley et al., <i>Computer Graphics: Principles and Practice, Second Edition</i> (Addison-Wesley Pub. Co., 1990)	Jan. 1991	1007

E. Asserted Ground

Petitioner asserts the following ground of unpatentability for the challenged claims. *See* Pet. 2.

Ground	Claims Challenged	35 U.S.C. §³	References/Basis
1	10–20	103(a)	Sfarti, Foley

F. Testimonial Evidence

Petitioner relies on the testimony of Dr. Chandrajit L. Bajaj, Ph.D. (Exhibits 1003, 1043, and 2007) as a proffered expert witness. Patent Owner relies on the testimony of Mr. Korbin S. Van Dyke (Exhibits 1044 and 2005) as a proffered expert witness.

² The Petition and the Patent Owner Response both refer to this reference as “501-Pub” for reasons which will become clear below. We instead refer to it as “Sfarti” because the solely-named inventor is Adrian Sfarti.

³ The ’534 patent issued in July 2011. *See* Ex. 1001, code (45). Therefore, the first-inventor-to-file provisions of the Leahy-Smith America Invents Act (Pub. L. No. 11229, 125 Stat. 284 (2011)), which took effect in March 2013, do not apply here.

G. Priority Date of the Challenged '534 Patent Claims

The '534 patent was filed as U.S. Patent Application No. 12/767,997 on April 27, 2010. *See* Ex. 1001, codes (21) and (22). The “Related U.S. Application Data” field on the front page of the '534 patent indicates it is a reissue of U.S. Patent No. 7,532,213, which is a continuation of U.S. Patent No. 7,245,299 (“the '299 patent”) filed on Dec. 9, 2003, which is continuation-in-part of U.S. Patent Application No. 10/436,698 (“the '698 Application”), filed on May 12, 2003, which is a continuation-in-part of U.S. Patent No. 6,563,501 (“the '501 patent”), filed on Dec. 11, 2000. *See id.* at codes (63) and (64). The “Related U.S. Application Data” field also lists U.S. Provisional Application No. 60/222,105 (“the '105 provisional”), filed on July 28, 2000. *See id.* at code (60). The Specification of the '534 patent begins with a “CROSS-REFERENCE TO RELATED APPLICATIONS” paragraph, which also lists the '299 patent, the '698 application, the '501 patent, and the '105 provisional. *See id.* at 1:13–24.

Petitioner contends the effective filing date of the challenged '534 patent claims “is no earlier than May 12, 2003,” the filing date of the '698 Application. Paper 2, 4. In particular, according to Petitioner, the challenged '534 patent claims are not entitled to the benefit of the filing date of the '501 patent, for various reasons. *See id.*; Pet. 17–28.

Patent Owner has stipulated that: “If the Board declines to institute the [IPR2022-01590] petition under § 314(a), Patent Owner will not challenge the prior art status of [Sfarti] in [IPR2022-01591, the present proceeding].” Paper 8, 2. In this event, as characterized by Patent Owner, “there is no priority dispute” in the present proceeding. *Id.*

Contemporaneously with the Institution Decision in this proceeding, we also entered a decision in IPR2022-01590 that denied institution in that proceeding under § 314(a) based on Patent Owner’s stipulation. Therefore, we treat Patent Owner’s stipulation as an admission, for the purposes of this proceeding, that Sfarti is prior art to the ’534 patent. *See* Inst. Dec. 6.

III. ANALYSIS OF PETITIONER’S GROUNDS

A. *Statement of Law*

Petitioner bears the burden of proving unpatentability of the challenged claims, and this burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Petitioner must prove unpatentability by a preponderance of the evidence. *See* 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, “would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the claimed subject matter pertains.” *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective indicia of nonobviousness, which have not been introduced in this proceeding. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). “While the sequence of these questions might be reordered in any particular case,” *KSR*, 550 U.S. at 407, the Federal Circuit has explained that an obviousness determination

can be made only after consideration of all of the *Graham* factors. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1360 (Fed. Cir. 2012).

B. Level of Ordinary Skill in the Art

Petitioner contends a person having ordinary skill in the art pertaining to the '534 patent “would have had at least a Bachelor’s degree in computer science, computer engineering, electrical engineering, or a related scientific field, and approximately two years of work experience in computer graphics or, alternatively, two years['] work towards a masters or doctorate degree in these scientific fields.” Pet. 10; Ex. 1003 ¶¶ 96–97. Patent Owner applies Petitioner’s formulation of ordinary skill in the Patent Owner Response. *See* PO Resp. 11; Ex. 2005 ¶ 31.

Based on the record presented, we now find as we did in the Institution Decision that Petitioner’s formulation of the level of ordinary skill in the art is consistent with the level of skill reflected in the '534 patent and the prior art of record, and is not disputed by Patent Owner. *See* Inst. Dec. 7–8. We, therefore, apply Petitioner’s formulation in this Decision.

C. Claim Construction

We interpret the '534 patent claims “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b). This “includ[es] construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

1. The Petition

Petitioner asserts the claim terms “transform unit”, “lighting unit”, “rendering unit”, and “tessellation unit” (“the Unit Terms”) “require construction in this proceeding” because they are means-plus-function limitations per pre-AIA 35 U.S.C. § 112, ¶ 6. Pet. 12–13; Ex. 1003 ¶¶ 101–105. Petitioner then provides corresponding constructions of the Unit Terms. See Pet. 13–16; Ex. 1003 ¶¶ 106–113. Petitioner also discusses Patent Owner’s contentions in the District Court Litigation, where Patent Owner has argued the Unit Terms are *not* means-plus-function limitations. See Pet. 16–17; Ex. 1003 ¶¶ 192–195, 222.

2. The Institution Decision

In the Institution Decision, we agreed with Petitioner that the Unit Terms are means-plus-function limitations subject to § 112, ¶ 6. See Inst. Dec. 9. We further construed each of the Unit Terms to require a GPU including a dedicated processor programmed to execute the transforming / lighting / rendering / tessellating step of the disclosed microcode in the ’534 patent specification. *Id.* at 10–12.

3. The Patent Owner Response

Patent Owner states “Petitioner correctly notes” the parties have disputed in the District Court Litigation whether the Unit Terms are subject to § 112, ¶ 6. PO Resp. 11. “Patent Owner submits that the Board need not make a final determination as to whether the claims are subject to § 112, ¶6 . . . because Petitioner has not met its burden to prove unpatentability of the challenged claims regardless of whether § 112, ¶6 applies.” *Id.* at 12. In particular, according to Patent Owner, Petitioner and Dr. Bajaj have both

agreed that neither Sfarti nor Foley “disclose[s] the allegedly ‘improved architecture’ for GPU hardware” of the ’534 patent claims, wherein “each ‘unit’ [includes] specialized graphics hardware of a GPU (including any associated software) that is used for the recited graphics-processing-related tasks, as opposed to a generic, general-purpose processor.” *Id.* at 12–13 (citing Pet. 23; Ex. 1003 ¶¶ 116–117, 183; Ex. 2005 ¶ 44; Ex. 2007, 36:5–21).

Patent Owner also argues the Institution Decision’s claim construction, in referring to “a GPU including a *dedicated* processor” (emphasis added), “implies each unit may only perform exactly one functionality and, thus, requires the units to be in a separate physical position and order within a GPU.” *Id.* at 13. Patent Owner “disagrees that this is required by the claims,” and contends that a person of ordinary skill in the art “would have recognized that each of the ‘unit’ terms connotes structure that includes specialized graphics hardware (and any associated software) that is configured to perform graphics processing.” *Id.* at 13–14 (citing Ex. 2005 ¶¶ 42–46).

4. *The Petitioner Reply*

In reply, Petitioner asserts the Patent Owner Response does not dispute the Institution Decision’s preliminary determination that the Unit Terms are each means-plus-function limitations subject to § 112, ¶ 6. *See* Pet. Reply 16–17. Petitioner argues we should construe at least the “tessellation unit” limitation because Patent Owner’s arguments place that term in dispute, particularly the structural aspect(s) of that term. *See id.* at 16–17, 24–25 (citing PO Resp. 13).

In that regard, and further concerning all four Unit Terms, Petitioner argues the Institution Decision correctly determined the corresponding structure of the '534 patent is a *dedicated* processor. *See id.* at 17 (section title). In support, Petitioner contends: “The sole structural embodiment in the '534 patent for each ‘*unit*’ term is simply a processor that executes the relevant microcode to perform the unit’s function.” *Id.* at 18 (citing Ex. 1001, 7:21–23, 12:49–52). Further according to Petitioner, “[t]here is nothing, anywhere in the specification, describing this processor as a specialized processor or specialized hardware” as Patent Owner would construe the Unit Terms. *Id.* at 18–21 (citing PO Resp. 13; Ex. 1044, 124:14–125:4, 126:11–19). Petitioner adds that the '534 patent specification in fact “directly contradicts” Patent Owner’s position that each of the Unit Terms “include[s] specialized graphics hardware of a GPU (including any associated software) that is used for the recited graphics-processing-related tasks, **as opposed to** a generic, general-purpose processor,” because it teaches “its microcode can be executed on either a GPU or a CPU.” *Id.* at 20–21 (quoting PO Resp. 13 (emphasis added by Petitioner)) (citing Ex. 1001, 7:40–42).

Petitioner then explains each of the Unit Terms requires a *dedicated* processor in that the claims and the '534 patent specification set forth “a specific order and separate physical positions of the ‘*transform unit*’, ‘*tessellation unit*’, ‘*lighting unit*’ and ‘*rendering unit*.’” *Id.* at 21–22 (citing Ex. 1001, Fig. 3, 4:16–18, 7:5–6). Petitioner further asserts that, during prosecution of the '534 patent, “Applicant stressed this exact physical ordering of the units.” *Id.* (citing Ex. 1017, 137–138, 175).

Further according to Petitioner, each *dedicated* processor “unit is devoted and intended to perform one and only one recited graphics processing function.” *Id.* at 22. Thus, taking the tessellation unit as an example, its processor performs tessellating but not transforming, lighting, or rendering. *See id.* at 22–23. Petitioner asserts Mr. Van Dyke agrees with this understanding. *See id.* (citing Ex. 1044, 137:18–138:8).

5. *The Patent Owner Sur-reply*

Patent Owner replies that “regardless of whether Section 112, paragraph 6 applies, each ‘unit’ term requires *specialized* graphics hardware of a GPU,” as opposed to “a generic processor executing software.” PO Sur-reply 16–17 (emphasis added) (citing PO Resp. 12–13); *id.* at 18–19 (citing Ex. 2005 ¶¶ 44–46; Ex. 2007, 26:5–21; Ex. 1003 ¶ 116). Patent Owner particularly asserts the Unit Terms “are directed to GPU graphics pipeline hardware,” as established by the specification and prosecution history of the ’534 patent. *Id.* at 17–18 (citing Ex. 1001, 3:23–58, 5:25–34, 11:56–60; Ex. 1002, 67, 112–113, 137–139; Ex. 1007, 20).

Patent Owner adds: “In graphics processing, ‘hardware’ is distinct from executing software using a processor, hence Patent Owner’s proposal of ‘specialized hardware,’” despite that the ’534 patent does not use the “specialized” term. *Id.* at 19 (citing Ex. 2005 ¶ 44). Patent Owner explains that “[c]onstruing the term ‘tessellation unit’ to encompass a generic processor executing software, would ignore the additional ‘hardware’ functionality” disclosed in the ’534 patent versus its parent application (i.e., Sfarti). *Id.* at 19–20 (citing Ex. 1001, 2:66–3:2, 5:24–34, 12:49–52; Ex. 1017, 137–139). Further according to Patent Owner, “graphics

‘hardware’ is distinct from ‘software’ that must be executed on a processor.”
Id. at 19 (citing Ex. 2007, 24:9–14; Ex. 1007, 11, 877).

Patent Owner asserts the Patent Owner Response *did* argue, and Mr. Van Dyke *did* testify, that § 112, ¶ 6 does *not* apply to the Unit Terms. *See* PO Sur-reply 20–21 (citing PO Resp. 11–14; Ex. 2005 ¶¶ 42–46). In particular, Patent Owner asserts “specialized hardware of a GPU clearly indicates structure, making § 112, ¶ 6 inapplicable,” but at the same time “the structure for each unit is specialized graphics hardware of a GPU (including any associated software) that is used for the recited-graphics-processing-related tasks” regardless of whether § 112, ¶ 6 applies. *Id.* at 20–21.

In opposition to Petitioner’s “dedicated” processor contentions, Patent Owner argues that word is not found in the ’534 patent specification. PO Sur-reply 21. Patent Owner particularly disagrees that the Unit Terms require a processor that “perform[s] *only* one function” without any “ancillary processing.” *Id.*

6. *Analysis and Determination*

We conclude the Unit Terms are means-plus-function limitations subject to § 112, ¶ 6, and we provide a corresponding construction of each term (sub-section (a)). We also discuss the possible application of a plain and ordinary meaning construction to the Unit Terms, to provide a complete record (sub-section (b)) and to demonstrate that even if the Unit Terms are not means-plus-function limitations, our ultimate determinations would not materially differ.

(a) *Mean-Plus-Function Claim Construction*

On the predicate issue of whether the Unit Terms are means-plus-function limitations subject to § 112, ¶ 6, we conclude that they are. Because the Unit Terms do not use the word “means,” we apply a rebuttable presumption that § 112, ¶ 6 does not apply. *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348–49 (Fed. Cir. 2015) (en banc in relevant part). Nonetheless, as Petitioner argues, the claim term “unit” does not connote any particular structure, and the terms “transform unit”, “lighting unit”, “rendering unit”, and “tessellating unit” recite function without reciting sufficient structure for performing that function.

The “unit” term at issue here is closely akin to the “module” term at issue in *Williamson*, and similarly generic terms such as “element” and “device,” and is, therefore, in the context of the ’534 patent claims and specification, a “nonce” word used “in a manner that is tantamount to using the word ‘means.’” *Williamson*, 792 F.3d at 1350–51; *see also Diebold Nixdorf, Inc. v. Int’l Trade Comm’n*, 899 F.3d 1291, 1298–1301 (Fed. Cir. 2018) (holding the claim term “cheque standby unit” was subject to § 112, ¶ 6, because it failed to “recite *any* structure, much less ‘sufficiently definite structure,’” and the claim recited a function without reciting sufficient structure for performing that function, despite an expert witness’s contrary testimony); *WSOU Invs. LLC v. Google LLC*, No. 2022-1066, 2023 WL 6210607, at *4 (Fed. Cir. Sept. 25, 2023) (stating “the term ‘unit,’ in a vacuum, is defined only by the function it performs, much like terms such as

‘element’ or ‘means’” and “[a] ‘unit’ could be almost anything”).⁴ We therefore agree with Petitioner’s position that the rebuttable presumption against application of § 112, ¶ 6 is overcome in this case, because the Unit Terms are not understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure. *See Williamson*, 792 F.3d at 1349 (“The standard is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure.”).

Patent Owner’s and Mr. Van Dyke’s apparent disagreement with this conclusion is not supported by the ’534 patent disclosures they cite. *See* PO Resp. 12–14 (citing Ex. 2005 ¶¶ 42–46, 49, 66); PO Sur-reply 16–20 (citing Ex. 1001, 2:66–3:2, 5:24–34, 11:56–60; Ex. 2005 ¶¶ 44–46); Ex. 2005 ¶¶ 42–46, 49, 66 (citing Ex. 1001, Fig. 3, 7:19–26). In particular, none of those disclosures equates the claimed “unit[s]” to “specialized” hardware, as Patent Owner vaguely argues. *See* Ex. 1001, Fig. 3, 2:66–3:2, 3:22–58, 5:25–34, 7:16–26, 11:56–60. Instead, the cited disclosures most pertinently state only that “[t]he present invention” of the ’534 patent “utilizes . . . an improved architecture for the computer graphics pipeline hardware,” wherein the improvement constitutes including a tessellation unit in that hardware. *Id.* at 5:25–34, 7:5–15. The cited disclosures do not provide any

⁴ We acknowledge that in *Inventio AG v. ThyssenKrupp Elevator Americas Corp.*, 649 F.3d 1350 (Fed. Cir. 2011), the Court held the claim term “computing unit” connoted sufficiently definite structure to avoid application of § 112, ¶ 6. *See id.* at 1359–60. However, the Court there stated “the presumption flowing from the absence of the term ‘means’ is a strong one that is not readily overcome” (*id.* at 1356), which was expressly overruled by the Court in *Williamson*, 792 F.3d at 1348–49.

further structural details for the “tessellation unit” limitation, or any of the other Unit Terms, to be limited to some sort of “specialized” hardware per Patent Owner’s arguments.

Nor is Patent Owner’s position supported by the prosecution history of the ’299 patent (a parent of the ’534 patent) cited by Patent Owner, for similar reasons. That is, the prosecution history reflects that the claims provide an improved architecture for computer graphics pipeline hardware, but it does not identify any particular structural configuration of the individual units that are included in the hardware. *See* PO Sur-reply 17–18, 20 (citing Ex. 1017, 67, 112–113, 137–139, 172–180).

Finally, during oral argument, Patent Owner’s counsel was asked about how the hardware architecture of the ’299 patent claims differs from or improves upon Sfarti’s disclosure. *See* Tr. 35:21–40:19. In response, Patent Owner’s counsel relied in part on the “microcode” disclosures of the ’299 patent as being a disclosure of structural hardware, differing from software. *See id.* at 38:1–39:18 (citing Ex. 1013, 7:9–19) (“[W]hen you implement something with microcode, microcode is low level instructions that are specific to a piece of hardware” and “burned into hardware.”). Petitioner’s counsel objected to this argument as being “brand-new.” *Id.* at 47:20–48:1. We agree with Petitioner. We have been unable to find the word “microcode” appearing anywhere in the Patent Owner Response. When queried about where this argument was made in the record prior to the hearing, Patent Owner referred to paragraph 45 of Mr. Van Dyke’s declaration. *See* Tr. 53:24–55:5. However, although Mr. Van Dyke does refer to “microcode” there, he does not opine that the “microcode” has a

definite meaning to a person of ordinary skill as specialized hardware. *See* Ex. 2005 ¶ 45.

Therefore, we conclude the Unit Terms are means-plus-function terms. “Construing a means-plus-function claim term is a two-step process.” *Williamson*, 792 F.3d at 1351. We “must first identify the claimed function,” then we “must determine what structure, if any, disclosed in the specification corresponds to the claimed function.” *Id.* In cases involving a special purpose computer-implemented means-plus-function limitation, the Federal Circuit requires “that the specification disclose an algorithm for performing the claimed function.” *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015). “A description of the function in words may ‘disclose, at least to the satisfaction of one of ordinary skill in the art, enough of an algorithm to provide the necessary structure under § 112, ¶ 6.’” *Typhoon Touch Techs., Inc. v. Dell, Inc.*, 659 F.3d 1376, 1385–86 (Fed. Cir. 2011). “The law is clear that patent documents need not include subject matter that is known in the field of the invention and is in the prior art, for patents are written for persons experienced in the field of the invention.” *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1371 (Fed. Cir. 2001).

We apply this two-step framework to each of the Unit Terms, as follows.

(1) *Transform Unit*

Claim 10 recites “a transform unit that transforms the graphic objects into transformed objects.” Claim 15 recites a similar limitation. Claim 12 recites “said transform unit transforms the spatial coordinates of said graphic

objects.” The specification discloses that the function of “transform[ing] the graphic objects into transformed objects” and “transform[ing] the spatial coordinates of said graphic objects” is performed by a graphics processing unit (GPU), including a dedicated processor programmed to execute the transform step of the disclosed microcode. Ex. 1001, 5:63–6:3; 7:10–15, 7:19–20, 12:49–52; Ex. 1003 ¶¶ 106–107. We construe “transform unit” as a means plus function limitation with the function of transforming graphic objects into transformed objects (claims 10 and 15), or the function of transforming the spatial coordinates of said graphic objects (claim 12), and with the corresponding structure of a GPU with computer graphics pipeline hardware including a processor programmed to execute the transforming step of the microcode disclosed in the specification.

The foregoing construction of “transform unit” is identical to the preliminary construction in the Institution Decision, with two exceptions. First, it adds that the corresponding structure is a GPU *with computer graphics pipeline hardware* including a processor. *See* Inst. Dec. 10. We agree with Patent Owner’s contention that the ’534 patent describes such pipeline hardware as being part of “[t]he present invention,” so we include it in our construction. Ex. 1001, 5:25–34.

Second, our construction does not require a *dedicated* processor, which is part of Petitioner’s claim construction. *See* Inst. Dec. 10; Pet. 14–15. As Patent Owner points out, the ’534 patent specification does not include the term “dedicated.” To the extent Petitioner’s “dedicated” term is meant to require that the processor is programmed *solely* to perform the claimed transforming function, to the exclusion of *any* other processing, we

conclude that the claim is open to both a dedicated processor and a non-dedicated processor.

Nonetheless, we agree with Petitioner's position that the transform unit encompasses, at least in some embodiments, a *different* unit from the other three claimed units. This is suggested by the language of claim 10, which refers to each of the units separately. Claim 10 additionally refers to the tessellation unit being "*coupled between* the transform unit and the lighting unit," demonstrating that at least those three units can be different units. Further, Figure 3 of the '534 patent correspondingly illustrates four separate units 2, 9, 3, and 4 within GPU 7. *See* Ex. 1001, Fig. 3, 7:4–15. Thus, although the transform unit may perform functions other than the transforming function, the transform unit in at least some embodiments does not perform the lighting, rendering, or tessellating functions of the other claimed units.

In summary, we construe "transform unit" as a means plus function limitation with the function of transforming graphic objects into transformed objects (claims 10 and 15), or the function of transforming the spatial coordinates of said graphic objects (claim 12), and with the corresponding structure of a GPU with computer graphics pipeline hardware including a processor programmed to execute the transforming step of the microcode disclosed in the '534 patent specification. Further, the transform unit does not perform the lighting, rendering, or tessellating functions of the other claimed units.

(2) *Lighting Unit*

Claim 10 recites a “lighting unit comprising means for lighting triangles resulting from said tessellation unit.” Claim 13 recites “a lighting unit . . . for lighting the tessellated transformed objects.” Claim 15 recites “lighting vertices of triangles resultant from said tessellating using said lighting unit.” The specification discloses that the function of “lighting triangles resulting from said tessellation unit,” “lighting the tessellated transformed objects,” and “lighting vertices of triangles resultant from said tessellating” is performed by a GPU with computer graphics pipeline hardware including a processor programmed to execute code to light the vertices of the triangles. Ex. 1001, 6:60–65, 7:10–15, 7:24–26, 12:49–52; Ex. 1003 ¶¶ 110–111.

For substantially the same reasons discussed above in connection with the transform unit, we construe “lighting unit” as a means plus function limitation with the function of lighting triangles resulting from said tessellation unit (claim 10), lighting the tessellated transformed objects (claim 13), or lighting vertices of triangles resultant from said tessellating (claim 15), and with the corresponding structure of a GPU with computer graphics pipeline hardware including a processor programmed to execute the lighting step of the microcode disclosed in the specification. Moreover, the lighting unit does not perform the transforming, rendering, or tessellating functions of the other claimed units.

(3) *Rendering Unit*

Claim 14 recites “a rendering unit operatively coupled to the lighting unit for rendering the lighted, tessellated, transformed objects.” The

specification discloses that the function of rendering the lighted, tessellated, transformed objects is performed by a GPU with computer graphics pipeline hardware including a processor programmed to execute the rendering steps of the disclosed microcode. Ex. 1001, 6:65–7:3, 7:10–15, 7:24–26, 12:49–52; Ex. 1003 ¶¶ 112–113. For substantially the same reasons discussed above in connection with the transform unit, we construe “rendering unit” as a means plus function limitation with the function of rendering the lighted, tessellated, transformed objects, and with the corresponding structure of a GPU with computer graphics pipeline hardware including a processor programmed to execute the rendering step of the microcode disclosed in the specification. Moreover, the rendering unit does not perform the transforming, lighting, or tessellating functions of the other claimed units.

(4) Tessellation Unit

Claim 10 recites “a tessellation unit for tessellating the transformed objects.” Claims 11 and 15 recite a similar limitation. The specification discloses that the function of “tessellating the transformed objects” is performed by a GPU with computer graphics pipeline hardware including a processor coupled between the transform unit and a lighting unit, where the processor is programmed to execute the tessellating steps of the disclosed microcode. Ex. 1001, 6:4–59, 7:10–15, 7:20–24, 12:49–52; Ex. 1003 ¶¶ 108–109.

For substantially the same reasons discussed above in connection with the transform unit, we construe “tessellation unit” as a means plus function limitation with the function of tessellating the transformed objects, and with the corresponding structure of a GPU with computer graphics pipeline

hardware including a processor coupled between the transform unit and the lighting unit, where the processor is programmed to execute the tessellating step of the microcode disclosed in the specification. Moreover, the tessellation unit does not perform the transforming, lighting, or rendering functions of the other claimed units.

(b) Plain and Ordinary Meaning Claim Construction

As discussed above, Patent Owner has suggested the Unit Terms may not be means-plus-function limitations subject to § 112, ¶ 6, on the basis that a person of ordinary skill in the art would have understood these terms as having a definite meaning as the name for structure. *See supra* Sections III.C.3 and III.C.5 (summarizing Patent Owner’s arguments). That structure, in Patent Owner’s view, is a GPU with specialized computer graphics pipeline hardware (and any associated software) that is used to perform the claimed transforming, lighting, rendering, and tessellating functions. *See id.*

For reasons provided above in Section III.C.6(a), we conclude the Unit Terms are means-plus-function limitations, despite Patent Owner’s foregoing argument. Nonetheless, in order to provide a complete record, we additionally note here that the corresponding structure portion of our means-plus-function construction is the same as Patent Owner’s posited structure, except that our construction does not require “specialized” hardware, because we find the Specification does not disclose specialized hardware for performing the claimed transforming, tessellating, lighting, and rendering functions. Even if Patent Owner is correct that the Unit Terms are not subject to § 112, ¶ 6, we still conclude “specialized” hardware is not

required, for the reasons provided above in Section III.C.6(a). Thus, our analysis of Petitioner’s obviousness ground below would not materially differ, even if we were to apply a plain and ordinary meaning construction to the Unit Terms.

7. *Remaining Claim Terms*

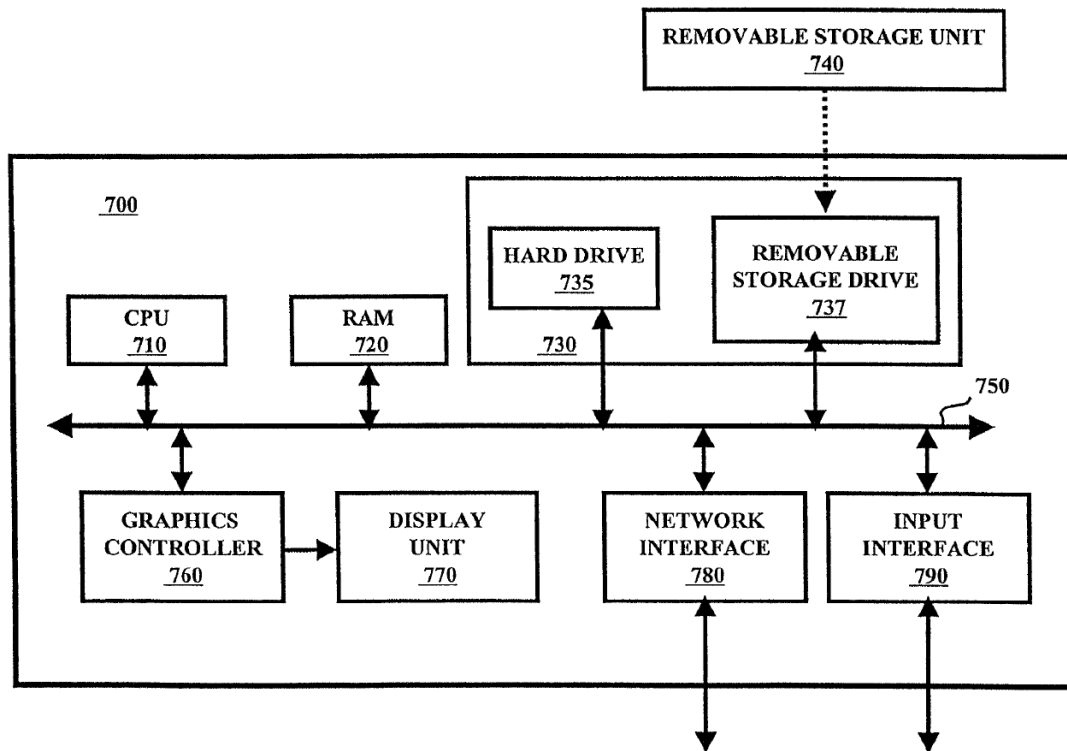
Upon review of the arguments and evidence, we determine no further construction of any claim term is needed. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (per curiam) (claim terms need to be construed “only to the extent necessary to resolve the controversy” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness over Sfarti and Foley*

Petitioner contends that claims 10–20 would have been obvious over the combined teachings of Sfarti and Foley. Pet. 28–77. We conclude a preponderance of the evidence supports Petitioner’s assertions as to all challenged claims. We begin our analysis with brief summaries of Sfarti and Foley, then we address the parties’ contentions as to obviousness.

1. *Overview of Sfarti*

Sfarti is the pre-grant publication of the application that led to the ’501 patent. Ex. 1001, code (63). Sfarti discloses “a method and system for rendering bicubic surfaces of an object on a computer system.” *See* Ex. 1009, codes (54) and (57). Figure 3 is a block diagram of a computer system of Sfarti, and is reproduced below.



Sfarti, Figure 3.

Figure 3 is a block diagram of computer system 100⁵ with CPU 110 and graphics controller 160. *Id.* ¶ 34.

Sfarti indicates graphics controller 160 receives commands and data from CPU 110, and “generates display signals (e.g., in RGB format) to display unit 170 . . . according to the commands and data received.” *Id.* ¶ 36. Sfarti explains the “execution of both subdivision [i.e., tessellation] and rendering is made possible inside the same graphics controller 160,” or alternatively “the subdivision can be executed by the CPU 110 while the

⁵ As Petitioner points out, the element numbers in Figure 3 are in the 7XX range, rather than the 1XX range used in the written description of Sfarti. *See* Pet. 29 n.9. Like Petitioner, we use the written description’s 1XX range of element numbers, which translate easily to the incorrect element numbers in the figure, as can be seen in the corrected version of Figure 3 in the ’501 patent. *See* Ex. 1014, Fig. 3.

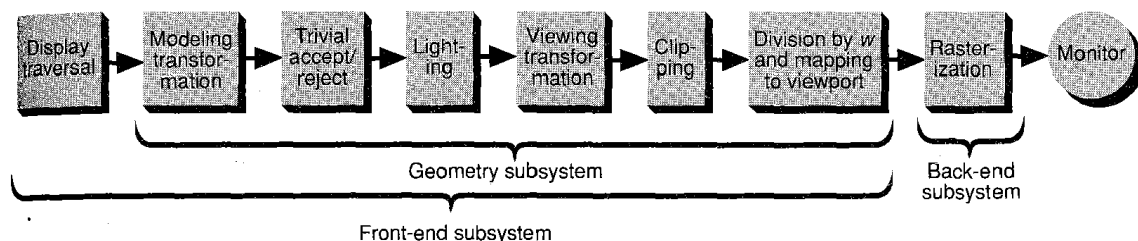
rendering is executed by the graphic controller 160.” *Id.* ¶ 41. Sfarti indicates its computer systems perform steps of transforming vertices (Step 0), tessellating (Steps 1–4), calculating lighting (Step 5), and rendering (Step 8). *Id.* ¶ 42.

2. Overview of *Foley*

Foley is a reference book on computer graphics that is part of an IBM-sponsored collection of books, called “The Systems Programming Series,” about principles and techniques for various topics. Ex. 1007, ix. The book is designed for course work, but is also a detailed reference book. *Id.*

Within the extensive exploration of computer graphics topics, *Foley* includes Chapter 18, entitled “Advanced Raster Graphics Architecture.” *Id.* at 855–922. Chapter 18 examines “the major computations performed by raster systems, and the techniques that can be used to accelerate them,” noting that “[g]raphics systems architecture is a specialized branch of computer architecture.” *Id.* at 855. This includes using “speed-up techniques” of general-purpose computer architecture, such as “pipelining” and “parallelism.” *Id.*

Foley presents a logical model, for implementation in software or hardware, of a rendering pipeline for use in a graphics system, as depicted in Figure 18.7, reproduced below.



Foley, Figure 18.7.

Figure 18.7 shows a block diagram of a “Standard graphics pipeline for Gouraud- or Phong-shaded polygons.” *Id.* at 867. Foley explains that the pipeline of Figure 18.7 “is typical for systems using conventional primitives (lines and polygons) and conventional shading techniques (constant, Gouraud, or Phong).” *Id.* Foley describes transforming the vertices of graphics primitives from an object-coordinate system to a world-coordinate system, and computing color for each polygon in an illumination model, and the use of parallelization to accelerate rendering. *See id.* at 868–869, 876. Foley also describes a particular algorithm, the Oslo algorithm, for tessellating. *See id.* at 509–510.

3. *Claim 10*

Petitioner provides arguments and evidence in support of its contention that claim 10 is unpatentable as having been obvious over Sfarti and Foley. *See* Pet. 34–63; Ex. 1003 ¶¶ 119–195. We first discuss Petitioner’s proffered motivations for combining Sfarti and Foley to practice the invention of claim 10 (sub-section (a)), then we discuss Petitioner’s mapping of claim 10 to the respective disclosures of Sfarti and Foley (sub-sections (b)–(f)). Patent Owner’s opposition to Petitioner’s case for obviousness is based on whether Sfarti and Foley combine to teach the tessellation unit of claim 10 (sub-section (f)).

(a) Reasons to Combine the Teachings of Sfarti and Foley

Petitioner contends Sfarti teaches a GPU that performs the ordered steps of transforming, tessellating, lighting, and rendering. Pet. 36–38 (citing Ex. 1009 ¶ 42). Petitioner contends Foley teaches a graphics pipeline of different processors, in which (as in Sfarti) tessellating may be performed

after transforming. Pet. 37 (citing Ex. 1007, 807). Petitioner contends Foley teaches that a benefit of implementing the steps of Sfarti in the computer graphics pipeline hardware of different processors described in Foley is providing more processing power than a single CPU can provide. Pet. 39 (citing Ex. 1007, 873, 874, 877). Dr. Bajaj testifies that concurrent processing as provided by Foley’s computer graphics pipeline hardware of different processors provides significant performance improvements, for example, “a non-pipelined construction that is divided into n pipelined stages should give a speed-up factor of n, which is the reason to use it.” Ex. 1003 ¶ 147 (quoting Ex. 1008, 8); *see id.* ¶ 146.

Patent Owner does not dispute Petitioner’s foregoing motivation contentions. Instead, Patent Owner’s opposition is directed to whether Sfarti and Foley combine to teach the claimed “tessellation unit . . . coupled between said transform unit and a lighting unit,” as we consider below in sub-section (f). *See, e.g.*, PO Resp. 19–31; PO Sur-reply 5 (noting “Petitioner primarily criticizes Patent Owner for allegedly not responding to Petitioner’s generic, high level ‘motivations to combine,’” and responding only that “[t]his misses the point: even if the references could be combined, the combination nevertheless fails to disclose the claimed tessellation unit”).

We agree with Petitioner that a person of ordinary skill would have implemented Sfarti’s ordered steps of transforming, tessellating, lighting, and rendering in a computer graphics pipeline hardware of different processors as taught by Foley to yield the benefits of providing more processing power than a single CPU can provide, and significantly improving performance speed. *See* Pet. 39–40; Ex. 1003 ¶¶ 134–147; Pet. Reply 4–6; Ex. 1007, 866, 873, 874, 877. We rely on the testimony of

Dr. Bajaj in finding that a person of ordinary skill would have expected significant performance improvements when processing the ordered steps of Sfarti using the concurrent processing of Foley's hardware pipeline.

Ex. 1003 ¶ 147. We rely on the testimony of Dr. Bajaj in finding that a person of ordinary skill would have expected that "a non-pipelined construction that is divided into n pipelined stages should give a speed-up factor of n, which is the reason to use it." Ex. 1003 ¶ 147 (quoting Ex. 1008, 8).

Petitioner also contends the combination of Sfarti and Foley is the use of Foley's known technique of using a graphics pipeline of different processors to improve the graphics controller of Sfarti in the same way, namely, to enhance performance via increased concurrent processing. *See* Pet. 41 (citing *KSR*, 550 U.S. at 415–21); Ex. 1003 ¶ 148; Pet. Reply 5. We agree with Petitioner that Foley's "technique [of using a computer graphics pipeline hardware of different processors] has been used to improve [a graphics processing] device, and a person of ordinary skill would recognize that it would improve [the graphics controller of Sfarti] in the same way," therefore, "using the technique is obvious." *KSR*, 550 U.S. at 417.

Petitioner moreover contends the combination of Sfarti and Foley combines the known prior art elements of Sfarti's graphics processor performing the ordered functions of transforming, tessellating, lighting, and rendering, with Foley's known hardware pipelining, according to Foley's known method of assigning each of the ordered functions to its own processor, and does no more than yield the predictable result of increasing performance speed by concurrently processing the ordered functions of transforming, tessellating, lighting, and rendering. *See* Pet. 42 (citing *KSR*,

550 U.S. at 415–21); Ex. 1003 ¶ 151. We agree with Petitioner that concurrently performing the known steps of transforming, tessellating, lighting, and rendering as taught by Sfarti using a different processor for executing each ordered step as taught by Foley, does no more than yield the predictable result of increasing performance speed as taught by Foley. *See KSR*, 550 U.S. at 416 (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”).

We finally agree with Petitioner that a person of ordinary skill would have had a reasonable expectation of success in implementing the steps of Sfarti using the graphics pipeline of different processors of Foley, because pipeline architectures have been a popular approach to building high-performance graphics systems since the 1960s, and pipelining is a speed-up technique used in general purpose computer architecture over the several decades prior to Foley. Pet. 43 (citing Ex. 1007, 855, 874, 877); Ex. 1003 ¶ 151.

(b) Central Processing Unit

Claim 10 recites “a central processing unit.” Petitioner contends that Sfarti discloses this limitation in describing CPU 110. Pet. 44 (citing Ex. 1009 ¶ 34, Fig. 3).

Patent Owner does not challenge Petitioner’s analysis and evidence directed to the central processing unit of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner’s opposition, directed solely to the tessellation unit limitation).

We find that Petitioner has demonstrated that Sfarti teaches this limitation of claim 10, as summarized above.

(c) Bus

Claim 10 recites “a bus operatively connected to said central processing unit.” Petitioner contends that Sfarti discloses this limitation in describing CPU 110 connected to communication path 150, which may contain several buses. Pet. 44 (citing Ex. 1009 ¶ 34, Fig. 3).

Patent Owner does not challenge Petitioner’s analysis and evidence directed to the bus limitation of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner’s opposition, directed solely to the tessellation unit limitation).

We find that Petitioner has demonstrated that Sfarti teaches this limitation of claim 10, as summarized above.

(d) Graphics Processing Unit

Claim 10 recites “a graphics processing unit operatively connected to said bus.” Petitioner contends that Sfarti discloses this limitation in describing graphics controller 160 connected to communication path 150, which may contain several buses. Pet. 44 (citing Ex. 1009 ¶ 34, Fig. 3).

Patent Owner does not challenge Petitioner’s analysis and evidence directed to the graphics processing unit limitation of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner’s opposition, directed solely to the tessellation unit limitation).

We find that Petitioner has demonstrated that Sfarti teaches this limitation of claim 10, as summarized above.

(e) Wherein the CPU Transmits Graphic Objects to the GPU via the Bus

Claim 10 recites “wherein the central processing unit transmits graphic objects to said graphics processing unit via said bus.” Petitioner contends that Sfarti discloses this limitation in describing that the CPU sends control points which define surfaces representing graphic objects to graphics controller 160, which then renders the image. Pet. 45–47 (citing Ex. 1009 ¶¶ 2, 34, 40–41, 43, Fig. 3).

Patent Owner does not challenge Petitioner’s analysis and evidence directed to the transmission limitation of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner’s opposition, directed solely to the tessellation unit limitation).

We find that Petitioner has demonstrated that Sfarti teaches this limitation of claim 10, as summarized above.

(f) Transform Unit

Claim 10 recites “wherein said graphics processing unit comprises a transform unit that transforms the graphic objects into transformed objects.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 47–48. Petitioner contends that Sfarti teaches the function of transforming graphic objects into transformed objects in describing software executed by graphics controller 160 that transforms the 16 control points for each bicubic surface. Pet. 48–49 (citing Ex. 1009 ¶¶ 16, 39–42). Petitioner contends that Foley teaches the structure of the claimed transform unit in describing floating-point processors, or geometry engines (GEs), arranged in a pipeline, where the first GE is programmed to transform

vertices and vertex normals. Pet. 49–50 (citing Ex. 1007, 877–879, 890–892, Fig. 18, 19).

Patent Owner does not challenge Petitioner’s analysis and evidence directed to the transform unit limitation of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner’s opposition, directed solely to the tessellation unit limitation).

We find that Petitioner has demonstrated that the combination of Sfarti and Foley teaches this limitation of claim 10, as summarized above.

(g) Tessellation Unit

Claim 10 recites “a tessellation unit for tessellating the transformed objects, wherein said tessellation unit is operatively coupled between said transform unit and a lighting unit.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 50–51; Ex. 1003 ¶¶ 168–182. Patent Owner disagrees. *See* PO Resp. 14–31; Ex. 2005 ¶¶ 47–76.

(1) The Petition

Claim 10 recites “a tessellation unit for tessellating the transformed objects.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 50–51. Petitioner contends that Sfarti teaches the function of tessellating transformed objects in describing a subdivision algorithm that generates triangles by connecting neighboring vertices. Pet. 51–55 (citing Ex. 1009 ¶¶ 41–42). Petitioner contends that Foley teaches the structure of the claimed tessellation unit in describing that each stage of an object rendering pipeline is implemented as an individual processor, such that the tessellation stage of Sfarti is performed by an

individual processor in Foley’s pipeline architecture. Pet. 57 (citing Ex. 1007, 877, 879).

Claim 10 recites that the “tessellation unit” is “operatively coupled between said transform unit and a lighting unit.” Petitioner contends that the combination of Sfarti and Foley teaches each stage of Sfarti’s object rendering process is implemented as an individual processor using the pipeline architecture of Foley, such that the individual processor for transformation outputs transformed control points, which are used by the individual processor for tessellation to generate triangles, and the individual processor for tessellation provides the triangle data to the individual processor for lighting. Pet. 57–58.

(2) *The Patent Owner Response*

Patent Owner argues neither Sfarti nor Foley teaches a “graphics processing unit comprising . . . a tessellation unit . . . coupled between said transform unit and a lighting unit” as recited in claim 10. PO Resp. 19–20.

As to Sfarti, Patent Owner argues it does “not describe tessellation as part of a graphics hardware pipeline within a GPU” as claimed, and it was not until the ’299 patent that Dr. Sfarti “describe[s] his new improvement over” the disclosure in Sfarti. *Id.* at 15–17, 26 (citing Ex. 1013, 5:20–5:29; Ex. 1009 ¶¶ 11–12, 31, 36, 41; Ex. 2005 ¶¶ 47–50, 66–67). Patent Owner argues Petitioner and Dr. Bajaj both agree Sfarti “does not disclose the ‘new architecture for a GPU that includes a tessellation unit’” as “claimed in

independent claims 10 and 15 of the '534 patent.” *Id.* at 20, 24 (quoting Pet. 22) (citing Pet. 18; Ex. 1003 ¶¶ 116–117; Ex. 2007, 62:2–8).⁶

Patent Owner also asserts Sfarti teaches tessellation may be implemented using either a CPU or “a graphics controller, the alleged GPU,” but Sfarti “does not teach or suggest the claimed architecture of the GPU including tessellation in any graphics pipeline” and “does not discuss a graphics pipeline.” *Id.* at 24–25 (citing Ex. 1009 ¶¶ 35, 40–41; Ex. 2005 ¶¶ 50, 66–67). Patent Owner argues that during prosecution of the '299 patent, the Examiner withdrew an obviousness-type double patenting rejection in view of the claims of the '501 patent that issued from Sfarti, thereby establishing the '534 patent claims would not have been obvious over Sfarti and knowledge of conventional GPU hardware pipelines. *See id.* at 2, 8–11, 25 (citing Ex. 1017, 112–113, 172–180).

As to Foley, Patent Owner argues neither Petitioner nor Dr. Bajaj “identifies any portion of Foley as teaching a tessellation unit in a GPU, nor do they contend that Foley taught performing tessellation in a GPU at all.” *Id.* at 20. Patent Owner asserts Foley in fact does not disclose the claimed tessellation unit, because Foley discloses only “‘an individual general-purpose processor’ that is not even programmed to perform tessellation” and does not disclose performing “tessellation in a GPU at all.” *Id.* at 21 (citing Ex. 1007, 877; Ex. 2005 ¶¶ 54–56, Ex. 2007, 71:18–23). Patent Owner argues that contrary to Petitioner’s assertion and Dr. Bajaj’s

⁶ The cited passages in the Petition and Dr. Bajaj’s declaration relate to Petitioner’s argument that the '534 patent lacks written description support in Sfarti, and thus cannot claim priority to Sfarti. *See* Pet. 17–23; Ex. 1003 ¶¶ 114–118.

testimony that Foley teaches tessellation after transformation, Foley in fact does not teach tessellation in an object rendering pipeline. *Id.* (citing Pet. 37; Ex. 1003 ¶¶ 60, 139; Ex. 1007, 807; Ex. 2005 ¶¶ 54–57, 59–61, 64; Ex. 2007, 57:14–68:14).

Further according to Patent Owner, even if Foley does teach tessellation in a graphics pipeline, Foley “still does not disclose or suggest performing tessellation *in a GPU* for two reasons.” *Id.* at 22. First, Foley “does not describe any implementation details” for tessellation, so a person of ordinary skill in the art “would not have understood Foley’s disclosure of performing tessellation related to graphics processing, in the abstract, to disclose or suggest doing so in any physical graphics hardware pipeline discussed in a separate chapter of Foley nearly 100 pages later.” *Id.* (citing Ex. 1007, 806–807, 866–873; Ex. 2005 ¶ 62). Second, “even if Foley did disclose tessellation as part of a graphics pipeline (conceptual or not),” still “[a] hardware graphics pipeline is not limited to a GPU and includes other components of a system, for example, the CPU processor.” *Id.* at 22–24 (citing Ex. 2005 ¶¶ 62–64). Patent Owner asserts Dr. Bajaj agrees that a graphics pipeline can include components such as a CPU, and that Foley teaches certain parts of the rendering pipeline are performed by a CPU rather than a GPU. *Id.* at 23–24 (citing Ex. 1007, 867; Ex. 2007, 40:25–41:9, 41:16–43:23, 45:2–7).

As to the combination of Sfarti and Foley, Patent Owner reiterates neither reference in isolation from the other “discloses the improved graphics hardware architecture of the GPU that includes a tessellation unit,” from which Patent Owner concludes that “absent hindsight, it would not have been obvious to modify the teachings of [Sfarti] based on the teachings

of Foley to arrive at the improved graphics architecture of the '534 patent, which includes 'a tessellation unit . . . coupled between said transform unit and a lighting unit.'" *Id.* at 26–27 (citing Ex. 2005 ¶¶ 68–76). Patent Owner particularly asserts here that Foley's disclosure concerning tessellation is limited to *pre*-tessellating primitive shapes such as triangles *off-line*, which is a prior art method improved upon by both Sfarti and the '534 patent by performing tessellation *after* transformation as part of a graphics pipeline in a GPU. *See id.* at 27–29 (citing Ex. 1001, 2:32–34, 2:40–45, 2:50–55; Ex. 1007, 855, 867 (Fig. 18.7), 871–72; Ex. 2005 ¶¶ 64, 69–73). Patent Owner argues that, because Foley employed pre-tessellated objects stored in the database, it would not have made sense for Foley to include a tessellation unit in a GPU. *See id.* at 28–29 (citing Ex. 2005 ¶¶ 71–73).

Patent Owner acknowledges "Petitioner relies on Foley's disclosure of 'multiprocessing' (which can either be pipeline or parallel) as disclosing 'hardware pipelined architecture.'" *Id.* at 29 (quoting Pet. 33–34). Patent Owner nonetheless maintains Foley does not describe multiprocessing in the context of tessellation, or tessellating in a pipelined processor. *See id.* (citing Ex. 1007, 871, 873–874). Patent Owner asserts a person of ordinary skill in the art "would have understood Foley's 'multiprocessing' to be used to perform the graphics processing at the time of the invention, to render pre-tessellated triangles stored in a database." *Id.* at 29–30 (citing Ex. 2005 ¶ 73). Thus, Patent Owner's view is that a person of ordinary skill in the art "would have recognized that there would be no need to speed up any tessellation" in Foley by employing multiprocessing in a graphics pipeline, "because the processing of the tessellation was already complete" using

parallel processing prior to the graphics pipeline. *Id.* at 30 (citing Ex. 1007, 877; Ex. 2005 ¶¶ 73–74).

Returning to Sfarti, Patent Owner asserts Petitioner and Dr. Bajaj “are emphatic” that the graphics architecture of the ’534 patent is not taught in Sfarti. *Id.* at 31 (citing Pet. 18–23; Ex. 1003 ¶¶ 87, 91, 112–116; Ex. 2005 ¶ 75). Patent Owner then reiterates that Sfarti “does not describe a tessellation unit or including tessellation in a graphics hardware pipeline.” *Id.* (citing Ex. 1017, 138; Ex. 1003 ¶ 93; Ex. 2005 ¶¶ 50, 75).

Patent Owner concludes “[n]o reference teaches” the claimed tessellation unit in a GPU, so it would not have been obvious for a person of ordinary skill in the art “to abandon the state of the art at the time of the invention to arrive at the claimed invention with no teaching or motivation to do so.” *Id.* (citing Ex. 2005 ¶ 76).

(3) *The Petitioner Reply*

In reply, Petitioner emphasizes that “[t]he ’534 patent definitively and unambiguously states that the ’534 patent’s alleged ‘invention utilizes [Sfarti’s] method’ which performs the ordered object rendering process of (1) transforming bicubic surfaces, (2) tessellating the transformed surfaces into triangles in real-time, (3) lighting the tessellated triangles, and (4) rendering the tessellated and lighted triangles.” Pet. Reply 1–2 (citing Ex. 1001, 5:9–29; Ex. 1009 ¶¶ 42–43) (footnote omitted). Petitioner asserts neither Patent Owner nor its expert witness Mr. Van Dyke disputes that allegation. *See id.* (citing PO Resp. 9, 16–17; Ex. 1044, 99:3–18). Petitioner contends that, as even applicant admitted during prosecution of the ’299 patent, “the ’299 patent merely presents an allegedly new graphics

hardware pipeline architecture to perform the method” already disclosed by Sfarti, by “insert[ing] a tessellation unit between the transform and lighting units of [Foley’s] existing graphics hardware pipeline.” *Id.* at 2 (citing Ex. 1017, 113, 138; Pet. 20–21; PO Resp. 8, 9, 17).

In particular, Petitioner argues its combination of Sfarti and Foley relies on Sfarti for an object rendering process that performs tessellation between transformation and lighting in a graphics controller, and relies on Foley for its teaching of mapping stages of an object rendering process onto a physical pipeline of processors. *See id.* at 4 (citing Pet. 33–38; Ex. 1003 ¶¶ 134–151; Ex. 1009 ¶¶ 39–42; Ex. 1007, 877). Petitioner contends that Foley provides “a ‘*pipeline processor* contain[ing] a number of *processing elements* (PEs) arranged such that the output of one becomes the input of the next, in pipeline fashion.’” *Id.* at 5 (citing Pet. 30; Ex. 1007, 867, 874 (Fig. 18.9(a)), 877). Thus, as argued by Petitioner, the combination of Sfarti and Foley provides a pipeline of different processors (as shown in Figure 18.9 of Foley) for an object rendering process performed by a GPU (as shown by the algorithm and Figure 3 of Sfarti) such that one processor performs transformation, another tessellation, another lighting, and another rendering. *See id.* at 4–5 (citing Pet. 32–43; Ex. 1003 ¶¶ 134–151).

Petitioner asserts Patent Owner “does not address the combination of Sfarti and Foley presented in the Petition but instead attacks each reference individually,” and “bases its argument on a strawman combination and **not** the combination presented in the Petition.” Pet. Reply 6, 14–15. Petitioner characterizes Patent Owner’s opposition as being that Foley does not teach or suggest performing tessellation in a GPU. *See id.* at 6–7 (citing PO Resp. 21–22). Petitioner responds that “Petitioner’s combination relies on Sfarti,

not Foley, for the teaching of performing tessellation in a GPU,” after transformation and before lighting. *Id.* at 6, 14–15 (citing Pet. 28–30, 34–43, 51–52); *see id.* at 1–2 (citing Ex. 1009 ¶¶ 42–43).

Petitioner moreover argues that even Foley teaches, in some embodiments, tessellating after transformation and before lighting, rather than pre-tessellation, including benefits achieved by doing so. *See* Pet. Reply 6–7 (citing Pet. 37; Ex. 1007, 807; Ex. 1043 ¶¶ 7–9; Ex. 1044, 158:2–7). Petitioner asserts Patent Owner’s witness Mr. Van Dyke misunderstood these teachings in Foley. *See id.* at 7–9 (citing Ex. 1007, 807, 1114; Ex. 1043 ¶¶ 6–14; Ex. 1044, 166:8–21, 167:14–22; Ex. 2005 ¶ 57).

Petitioner further argues Patent Owner “mischaracterizes Foley’s multiprocessing (e.g., pipelining) teachings,” when “arguing that Foley’s hardware pipelines are limited to a computer graphics process using pre-tessellation.” Pet. Reply 9–10 (citing PO Resp. 29–30) (emphasis omitted). According to Petitioner: (1) Foley’s pipeline “performs tessellation after transformation and before lighting,” in one embodiment; (2) Foley’s graphics process performs numerous aspects of graphics processing such as “transformation, lighting, and rendering,” that require significant computing resources; and (3) Foley teaches that “the ‘only way to attain’ the needed performance levels for graphics processing ‘is to perform multiple operations concurrently.’” *Id.* at 9–10 (citing Ex. 1007, 855–856, 866–871, 873–874, 877; Ex. 1043 ¶ 22).

Concerning Sfarti, Petitioner responds to Patent Owner’s argument that “Sfarti does not teach performing tessellation in a GPU pipeline.” Pet. Reply 11 (citing PO Resp. 24–26). Petitioner asserts “Sfarti provides an

ordered object rendering process (a conceptual graphics pipeline) having sequential stages in which tessellation (subdivision) of a bicubic surface is performed in real-time after transformation and before lighting,” as Patent Owner allegedly acknowledges. Pet. Reply 11 (citing Ex. 1009 ¶¶ 42–43; Ex. 1003 ¶¶ 120, 134–143; PO Resp. 1 n.2, 8–9); *see id.* at 12–13. Petitioner also asserts Patent Owner does not dispute Sfarti’s graphics controller is a GPU, as was asserted in the Petition. *See id.* at 11 (citing Pet. 43–47; PO Resp. 16).

Petitioner also disagrees with Patent Owner’s argument that “Sfarti’s GPU cannot be or have a tessellation unit because it is a general-purpose processor.” *Id.* at 11 (citing PO Resp. 24–26). Petitioner argues Patent Owner overlooks Sfarti’s teachings of performing tessellation in a GPU, after transformation and before lighting. *Id.* at 13–14 (citing Ex. 1009 ¶¶ 16–17, 31, 39–43).

Petitioner contends that the Petition, supported by the testimony of Dr. Bajaj, presented four separate reasons why a person of ordinary skill in the art would have been motivated to combine the teachings of Sfarti and Foley. Pet. Reply 14–15 (citing Pet. 34–43; Ex. 1003 ¶¶ 134–151). Petitioner contends that Patent Owner does not address the actual combination presented in the Petition, but instead, “creates its own combination that relies on a graphics process that performs pre-tessellation. *Id.* (citing PO Resp. 26, 28, 30).” Petitioner contends that the Petition’s combination uses the object rendering process disclosed by Sfarti, which removes the need for pre-tessellation by performing tessellation in the GPU after transformation and before lighting. *Id.* at 15 (citing Pet. 28–30, 34–43).

Petitioner finally argues that we should give Mr. Van Dyke’s testimony on behalf of Patent Owner “little or no weight.” *Id.* at 27. Petitioner asserts Mr. Van Dyke admitted during his deposition “that he has no experience with tessellation of curved surfaces — the graphics concept central to the dispute in the case,” and he was unfamiliar with various details of other particular techniques known in the art. *Id.* at 3, 27 (citing Ex. 1001, code (54); Ex. 1044, 54:23–55:3, 57:23–58:25, 175:14–176:10, 177:22–24). Petitioner further asserts Mr. Van Dyke is “admittedly an ‘occasional friend’ of the named Inventor who hand-picked him to act as an expert in this proceeding.” *Id.* (citing Ex. 1044, 15:24–16:10, 18:5–10).

(4) *The Patent Owner Sur-reply*

Patent Owner in reply maintains that Sfarti and Foley do not teach or suggest “splicing the conventional computer graphics hardware pipeline and inserting a tessellation unit into that hardware pipeline,” as recited in claim 10. PO Sur-reply 2, 4. Patent Owner argues Sfarti does not teach such a tessellation unit, as Petitioner and its expert witness Dr. Bajaj concede. *See id.* at 6. Patent Owner reiterates that Foley describes only a conventional graphics pipeline lacking a tessellation unit, like the prior art architecture shown in Figure 2 of the ’534 patent. *See id.* at 3. Patent Owner concludes Petitioner’s case for obviousness therefore fails, because the combination of Sfarti and Foley is missing the tessellation unit claim limitation, and no asserted reference suggests modifying graphics pipeline architecture to include a tessellation unit. *See id.* at 5, 14–16.

According to Patent Owner, Petitioner’s argument that Sfarti teaches “performing tessellation in a GPU” (Pet. Reply 11) “misses the point”

because nothing in Sfarti or Foley “discloses or suggests performing tessellation in [the] graphics pipeline hardware of a GPU.” PO Sur-reply 6. In particular, Patent Owner asserts Sfarti’s disclosure is limited to “tessellation being done in software, executed within either the CPU or the graphics controller (the alleged GPU).” *Id.* at 6–7 (citing PO Resp. 24–25; Ex. 2005 ¶¶ 50, 67).

Turning to Foley, Patent Owner argues “Petitioner’s citations to Foley include portions of two separate chapters separated by nearly 150 pages — chapters 16 and 18.” *Id.* at 8. Patent Owner asserts Foley’s Chapter 16 discloses only “several distinct ‘conceptual’ graphics pipelines . . . none of which include tessellation” or even “GPU pipeline *hardware* at all.” *Id.* at 8–9 (citing Ex. 1007, 807–809; Ex. 1043 ¶¶ 6–13; Ex. 2007, 67:14–71:10). Patent Owner asserts Foley’s Chapter 18 also does not teach or suggest including a tessellation unit in a graphics pipeline hardware, including as part of any “multiprocessing” technique. *Id.* at 9–11 (citing Ex. 1007, 806, 866–867; Ex. 2005 ¶¶ 62, 71–73). Patent Owner asserts Foley suggests only that tessellation occurs *before* the graphics pipeline. *See id.* at 10 (citing Ex. 2005 ¶¶ 71–74).

Patent Owner then addresses Petitioner’s various reply arguments regarding Foley. *See* PO Sur-reply 11–13. First, Patent Owner argues Petitioner fails to explain how Foley discloses performing tessellation in GPU pipeline hardware. *Id.* at 11 (citing Pet. Reply 10). Second, Patent Owner argues Foley’s “standard conceptual process” has nothing to do with tessellation, including tessellation in either a conceptual graphics pipeline or a hardware graphics pipeline. *Id.* at 11–12 (citing Ex. 2007, 40:25–41:9; Pet. Reply 6–7). Third, Patent Owner argues Foley’s concurrent processing

hardware pipeline does not include tessellation. *See id.* at 12 (citing Pet. Reply 9–10). Fourth, Patent Owner argues Foley renders objects that were already tessellated and thus does not need to have a tessellation unit in graphics pipeline hardware. *See id.* at 12–13 (citing Ex. 1007, 855; Pet. Reply 10). Fifth, Patent Owner concedes “Foley does not forbid non-pre-tessellated primitives,” but Patent Owner nonetheless contends Petitioner bears the burden to show Foley discloses tessellation in a graphics pipeline hardware, which has not been met. *Id.* at 13 (citing Ex. 1007, 807; Pet. Reply 10).

Finally concerning the credibility of Mr. Van Dyke’s testimony, Patent Owner argues he “significantly exceeds” the agreed-upon formulation of ordinary skill in the art. PO Sur-reply 22–24 (citing Pet. 12; Ex. 2006, 9–12; Ex. 1044, 69:19–70:3). Concerning Mr. Van Dyke’s deposition testimony, Patent Owner asserts “the claims do not require any particular algorithm for tessellation.” *Id.* at 22. Further: “Petitioner’s attempt to paint Mr. Van Dyke as biased because Mr. Van Dyke referred to Dr. Sfarti as an ‘occasional friend’ is baseless.” *Id.* at 23–24 (citing Ex. 1044, 17:20–18:16, 19:1–18, 20:2–19; Ex. 2005 ¶ 5).

(5) *Analysis and Determination*

We determine Petitioner’s contentions are supported by a preponderance of the evidence. Starting with Sfarti, Dr. Bajaj testifies Sfarti discloses the function of tessellating transformed objects. *See* Ex. 1003 ¶¶ 169–176; Pet. 51–55. Dr. Bajaj further testifies that Sfarti discloses performing tessellation after transformation and before lighting. *See* Ex. 1003 ¶ 183; Pet. 57–58. Turning to Foley, Dr. Bajaj testifies Foley

teaches a computer graphics pipeline hardware for rendering objects, implemented as a series of different processors. *See* Ex. 1003 ¶ 181; Pet. 57.

We credit Dr. Bajaj’s testimony that a person of ordinary skill would have implemented Sfarti’s ordered steps of transforming, tessellating, lighting, and rendering in a graphics pipeline hardware of different processors as taught by Foley, to yield the benefits of providing more processing power than a single CPU can provide, and significantly improving performance speed. *See supra* Section III.D.3(a); Ex. 1003 ¶¶ 134–151; Pet. 34–43. We agree with Petitioner that Foley teaches the structure of the claimed tessellation unit in describing that each stage of an object rendering pipeline is implemented as a different processor, such that the tessellation stage of Sfarti’s ordered steps is performed by a separate processor when using Foley’s pipeline architecture. *See* Ex. 1003 ¶ 181; Pet. 55–57. We also agree that Petitioner’s combination teaches the claimed “tessellation unit coupled between the transform unit and the lighting unit,” because each stage of Sfarti’s object rendering process is implemented on a different processor using the pipeline hardware architecture of Foley, such that the processor that implements the transformation stage would output transformed control points to the processor that implements the tessellation stage, and the processor that implements the tessellation stage would output its data to the processor that implements the lighting stage. *See* Ex. 1003 ¶ 183; Pet. 57–58.

“A person of ordinary skill is also a person of ordinary creativity, not an automaton,” and “in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *KSR*, 550 U.S. at 420–21. That is particularly the case here, where it was known

in Sfarti, which is prior to the '534 patent, for a graphics controller to perform the ordered sequence of steps of transforming control points (*see* Ex. 1009 ¶¶ 41–42 (step 0)), then tessellating the control points into triangles (*see id.* (steps 1–4)), then lighting the triangles (*see id.* (step 5)), and then rendering the triangles (*see id.* (step 8)). *See* Ex. 1003 ¶ 183; *see also* Tr. 31:9–32:17 (Patent Owner’s counsel stating “we’re not disputing the order of [Sfarti]” and “[Sfarti] teaches the order of this graphics processing”), 42:1–3 (same).

Patent Owner’s opposing view that Sfarti does not teach tessellation after transformation and before lighting is not supported by the evidence. *See* Ex. 1009 ¶¶ 41–42; Ex. 1003 ¶ 183. Further, even if Sfarti’s operations were performed by its graphics controller 160 as Patent Owner contends, Petitioner’s combination of Sfarti and Foley calls for the operations to be performed by Foley’s GPU hardware pipeline of different processors. Tessellating after transformation and before lighting does not preclude or otherwise detract from also using Foley’s GPU hardware pipeline of different processors that each execute a different stage of the rendering process, such that one processor performs tessellation after transformation and before lighting, thereby satisfying claim 10.

We disagree with Patent Owner’s arguments and Mr. Van Dyke’s testimony to the contrary. First, the evidence does not support Patent Owner’s position (*see* PO Resp. 24–26) that Sfarti precludes the use of a graphics processor to perform tessellation after transformation and before lighting. Sfarti instead states that its graphics controller 160 may be “implemented using a combination of hardware, software and/or firmware [executing] the software to provide various features of the present

invention.” Ex. 1009 ¶ 39; *see also id.* ¶¶ 40–42 (Sfarti’s object rendering process may be implemented by graphics controller 160). Second, the evidence does not support Patent Owner’s position (*see* PO Resp. 20–24, 29–30) that Foley is limited to a computer graphics process using pre-tessellation or tessellation outside of the GPU. Foley instead states that, in at least some cases, “[t]essellation should occur after transformation” which “enables tessellation size to be determined adaptively,” and after which the “tessellated primitives must be lit.” Ex. 1007, 807.

Moreover, Patent Owner’s overarching position that the Petition is deficient because neither Sfarti nor Foley individually discloses “a tessellation unit for tessellating transformed objects, wherein said tessellation unit is operatively coupled between said transform unit and a lighting unit” as claimed is not persuasive, for at least two reasons. First: “Non-obviousness cannot be established by attacking references individually where the [unpatentability] is based upon the teachings of a combination of references.” *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *see also Fleming v. Cirrus Design Corp.*, 28 F.4th 1214, 1222 (Fed. Cir. 2022) (“That the proposed *combination* of James and POH — rather than one of the individual references — discloses the disputed claim limitations does not defeat the Board’s conclusion of obviousness.”). Here, Petitioner, relying on the testimony of Dr. Bajaj, which we credit, persuasively demonstrates unpatentability by implementing Sfarti’s graphics process of ordered steps on Foley’s graphics hardware pipeline of individual processors, where each of Sfarti’s ordered steps is mapped to an individual processor in Foley’s pipeline, to achieve the performance benefits of concurrent processing as taught by Foley. Pet. 34–43; Ex. 1003 ¶¶ 134–151.

The Federal Circuit’s recent unpublished decision in *Masimo Corp. v. Apple Inc.*, No. 2022-1894, 2024 WL 111647 (Fed. Cir. Jan. 10, 2024), is instructive on this point. There, the Court stated:

[The patent owner] also stresses that no reference teaches or suggests placing louvers over a detector. Essentially, its argument is: because Webster disclosed light-sensitive detectors and light filters (but not louvers specifically), and because Melby disclosed louvers (but not in the context of light-sensitive detectors), the prior art is missing a claim element — and therefore, the claimed invention was not shown to be unpatentable for obviousness. [The patent owner] misunderstands the obviousness inquiry. The question is not whether the prior art disclosed the very thing claimed; it is whether, in light of the prior art, the claimed invention would have nonetheless been *obvious* to a person of ordinary skill in the art as of the relevant date. Contrary to [the patent owner’s] argument, it suffices — as the Board found — “that a person of ordinary skill in the art would have been motivated to combine the prior art in a way such that the combination discloses the claim limitation[.]”

Id. at *3 (citations omitted); *see also* Tr. 12:1–13 (Petitioner’s counsel discussing the *Masimo v. Apple* decision). In our view, Patent Owner in this proceeding misunderstands the obviousness inquiry in the same fashion that the patent owner did in the *Masimo v. Apple* case.

Second, Patent Owner’s overarching contention that the Petition is deficient because neither Sfarti nor Foley individually discloses a computer graphics pipeline hardware including a tessellation unit coupled between a transformation unit and a lighting unit is not persuasive because the contention does not address Petitioner’s reasons why a person of ordinary skill would have combined the teachings of Sfarti and Foley to provide a tessellation unit coupled between a transformation unit and a lighting unit.

We find the Petition and Dr. Bajaj persuasively show multiple reasons why a person of ordinary skill in the art would have implemented each of Sfarti's ordered steps of transforming, tessellating, lighting, and rendering on a corresponding processor in the graphics pipeline of different processors taught by Foley to yield a tessellate unit coupled between a transformation unit and a lighting unit as claimed. *See* Pet. 34–43; Ex. 1003 ¶¶ 134–151.

We reiterate that Petitioner contends, and we agree, that a person of ordinary skill would have been motivated to implement each of Sfarti's ordered steps of transforming, tessellating, lighting, and rendering on a corresponding processor of Foley's graphics pipeline to yield the benefits of providing more processing power than a CPU can provide and significantly improving performance speed as taught by Foley. *See* Pet. 39–40 (citing Ex. 1007, 874, 877; Ex. 1008, 8; Ex. 1003 ¶¶ 143–146). We highlight that Foley explicitly teaches the benefits of employing an individual processor for each stage of a graphics pipeline in disclosing that “the geometry portion of a graphics system can require more processing power than a single CPU can provide,” and that the “only way to attain such performance levels is to perform multiple operations concurrently” such as through a graphics pipeline processor that “contains a number of processing elements (PEs) arranged such that the output of one becomes the input of the next.” Ex. 1007, 873–874 (emphasis omitted). In addition, Dr. Bajaj persuasively testifies that the concurrent processing from a hardware pipeline provides a significant performance improvement, so that “a non-pipelined construction that is divided into n pipelined stages should give a speed-up factor of n , which is the reason to use it.” Ex. 1003 ¶ 147 (citing Ex. 1008, 8).

We agree with Dr. Bajaj in finding that the prior art teaches Petitioner's reason to implement the ordered steps of Sfarti on the graphics pipeline of Foley, namely, to provide more power and increase processing speed. Thus, Patent Owner's contentions that Sfarti alone does not teach "including tessellation in a graphics hardware pipeline at all" (PO Resp. 25–26, 31; Ex. 2005 ¶¶ 50, 67–68, 75), and that "absent hindsight, it would not have been obvious to modify the teachings of [Sfarti] based on the teachings of Foley" to arrive at the claimed "tessellation unit" (PO Resp. 26) do not show a deficiency in Petitioner's motivation for a person of ordinary skill in the art to combine the teachings of Sfarti and Foley, namely, to yield the performance improvements of concurrently processing Sfarti's ordered steps of transforming, tessellating, lighting, and rendering using "a tessellation unit . . . operatively coupled between said transform unit and a lighting unit" as claimed.

As further motivation, Petitioner contends that although Foley does not explicitly show a tessellation stage, Foley teaches performing tessellation after transformation and before lighting. *See* Pet. 34 (citing Ex. 1007, 807); Pet. Reply 6–7. We agree. In this teaching, Foley explains that "[t]essellation should occur after transformation" to yield the benefits of "enabl[ing] tessellation size to be determined adaptively, and limit[ing] the amount of data that is transformed" and that "tessellated primitives must be lit." Ex. 1007, 807. Although Patent Owner contends that Foley does not disclose implementation details of performing tessellation in a graphics hardware pipeline (PO Resp. 22; Ex. 2005 ¶ 62), Patent Owner's contention does not show a deficiency in Foley's reasons for performing tessellation after transformation and before lighting. Rather, Patent Owner seems to

suggest that knowledge of the details needed to implement tessellation in a graphics hardware pipeline was beyond the level of ordinary skill. However, Petitioner and Dr. Bajaj rely on the combined teachings of Sfarti and Foley to show that implementing the ordered steps of Sfarti on the individual processing elements of Foley's graphics pipeline would have been within the level of ordinary skill. *See* Pet. 28–30, 35–38, 43, 51–58; Ex. 1003 ¶¶ 134–151, 168–182. We agree with Petitioner and Dr. Bajaj, that a person of ordinary skill would have been able to implement each of Sfarti's ordered steps of transforming, tessellating, and lighting on a corresponding processing element in Foley's graphics pipeline with a reasonable expectation of success. *See id.*

Similarly, Patent Owner's contention that "Foley makes clear that it only considered its graphics process pipeline . . . after primitives have already been tessellated" so that a person of ordinary skill in the art "would have understood that there is no need for tessellating in the graphics pipeline" (PO Resp. 30; Ex. 2005 ¶ 74) is not persuasive. Again, Patent Owner does not show a deficiency in Foley's reasons for performing tessellating after transforming and before lighting. As Petitioner correctly notes, Sfarti discusses the problems with the prior art methods of pre-tessellating, and, along with Foley, teaches the improved process of adaptive tessellation, which is performed after transformation and before lighting. *See* Pet. Reply 15; Pet. 3–6, 12, 28–30, 34–43; Ex. 1009 ¶¶ 13–17, 31, 42. We credit the testimony of Dr. Bajaj in finding that a person of ordinary skill, in combining Sfarti's ordered steps with Foley's graphics pipeline, would have performed tessellating after transforming in order to overcome the disadvantages of pre-tessellating as taught by Sfarti, to yield the benefits

of “enabl[ing] tessellation size to be determined adaptively, and limit[ing] the amount of data that is transformed” as taught by Foley, and to yield the benefits of adaptively tessellating and rendering images in real time as taught by Sfarti. Ex. 1007, 807; Ex. 1009 ¶¶ 2, 13–17, 31, 42–43; Ex. 1003 ¶¶ 83–84, 137, 139, 156.

In addition to these motivation statements, Petitioner persuasively shows a person of ordinary skill would have recognized Foley’s known technique of using a graphics pipeline of different processors would improve the graphics controller of Sfarti in the same way, namely, to increase performance via increased concurrent processing. *See* Pet. 38–39; Ex. 1003 ¶ 148; Ex. 1007, 873–874; Pet. Reply 5; *KSR*, 550 U.S. at 417 (“[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its application is beyond his or her skill.”). Petitioner also persuasively shows that combining the known prior art elements of Sfarti’s ordered functions of transforming, tessellating, lighting, and rendering with Foley’s known graphics pipeline according to Foley’s known method of assigning each of the ordered functions to its own separate processor does no more than yield the predictable result of increasing performance speed by concurrently processing the ordered stages of transforming, tessellating, lighting, and rendering. Pet. 39–40 (citing Ex. 1003 ¶¶ 132–149; Ex. 1007, 855, 874, 877; Ex. 1009 ¶ 39); *KSR*, 550 U.S. at 416 (“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”).

Patent Owner, in contrast, emphasizes that Foley alone does not disclose a GPU that includes a tessellation unit (*see* PO Resp. 20–24; Ex.

2005 ¶¶ 54–57, 59–64) and that Sfarti alone does not disclose a GPU that includes a tessellation unit (PO Resp. 24–26; Ex. 2005 ¶¶ 50, 65–68, 75). Patent Owner then contends “it would not have been obvious to include a tessellation unit in a GPU in view of Foley” (PO Resp. 30) and that “it also would not have been obvious to implement the tessellation unit in view of the teaching of [Sfarti]” (*id.* at 31). However, in reaching this conclusion, Patent Owner does not persuasively address the Petition’s reasons for performing each of Sfarti’s ordered steps of transforming, tessellating, lighting, and rendering on a corresponding processor of Foley’s graphics pipeline. *See* Pet. 34–43. In particular, Patent Owner’s contention does not address Petitioner’s contention that the combination of Sfarti and Foley would have resulted in the claimed “tessellation unit for tessellating the transformed objects, wherein said tessellation unit is operatively coupled between said transform unit and a lighting unit.” *See* Pet. 50–58.

We credit the testimony of Dr. Bajaj in finding that the Petition and supporting evidence persuasively provides multiple reasons for a person of ordinary skill to combine Sfarti and Foley as discussed above. We further credit the testimony of Dr. Bajaj in finding that the Petition and supporting evidence persuasively shows that the combination of Sfarti and Foley teaches the claimed “tessellation unit” in showing that Sfarti’s tessellation stage occurs after the transformation stage and before the lighting stage, that each stage of Foley’s graphics pipeline can be implemented as an individual programmable processor, and that a person of ordinary skill in the art would have implemented each stage of Sfarti’s graphics rendering process on a corresponding individual processor of Foley’s graphics pipeline to achieve the benefits of increased performance from concurrent processing. *See* Pet.

57–58 (citing Ex. 1003 ¶¶ 181, 183; Ex. 1007, 877, 879; Ex. 1009 ¶¶ 39, 41–42).

Patent Owner contends that Petitioner attempts to shift its burden of persuasion on to Patent Owner in arguing that Sfarti does not prohibit implanting a tessellation unit in its own processor. *See* PO Sur-reply 3, 7. We disagree. Petitioner’s arguments are directed to satisfying its burden to show obviousness by explaining how and why a person of ordinary skill would have modified Sfarti’s graphics controller based on Foley’s teachings. Such arguments directed to the obviousness inquiry help articulate Petitioner’s explanation of why a person of ordinary skill in the art would have been motivated to modify Sfarti’s graphics controller to implement the stages of Sfarti’s rendering process using Foley’s individual processors in a graphics hardware pipeline, and why such person would have had a reasonable expectation of success in doing so. This modification from a single processor to a pipeline of processors would have been made to provide more processing power than a single CPU can provide for the very purpose of compensating for limitations of Sfarti’s graphics controller, as discussed above. In other words, Petitioner’s modification results in improving Sfarti’s graphics controller for executing Sfarti’s rendering process. Similarly, Petitioner’s arguments and the supporting testimony of Dr. Bajaj regarding the teachings of Sfarti’s rendering process, which includes the ordered stages of transforming, tessellating, and lighting, and Foley’s graphics pipeline, which includes an individual processor for each stage of the rendering process, show that a person of ordinary skill in the art would have had a reasonable expectation of success in using Foley’s

graphics pipeline as the graphics controller of Sfarti to execute Sfarti's rendering process. Ex. 1003 ¶¶ 134–151, 168–182.

Finally, we acknowledge that during prosecution of the parent '299 patent, the Examiner withdrew a rejection based on an obviousness-type double patenting over Sfarti. We disagree, however, with Patent Owner's position that this conclusively establishes that claim 10 cannot have been obvious over Sfarti and other reference(s), such as Foley, as asserted by Petitioner. PO Resp. 10–11; PO Sur-reply 2–3. In particular, we disagree with Patent Owner's contention that “by withdrawing the obviousness-type double patenting rejection over the '501 patent claims, the Examiner determined the '299 claims would not have been obvious in view of the '501 patent claims and the general graphics pipeline teachings.” PO Resp. 10; *see id.* at 25. The Examiner, when making the obviousness-type double patenting rejection, did not apply a prior art reference that taught “general graphics pipeline teachings” as alleged by Patent Owner. Rather, the Examiner found that

claims 1–3 and 12–14 describe graphics processing units which contain instructions for subdivision and claim 21 [of the '501 patent] describes a computer readable medium contains program instructions or subdivision. However, it would have been obvious to one of ordinary skill to substitute the computer readable medium of claim 21 with the graphics processing unit of claims 1–3 and 12–14.

Ex. 1017, 67. Thus, the Examiner improperly attempted to use the graphics processing unit recited in then-pending claim 1 of the application that became the '299 patent as prior art against itself. The applicant successfully argued against the Examiner's improper use of the pending claim as prior art against the same pending claim by stating that the '501 patent did not

disclose the graphics processing unit incorporating the tessellation unit as claimed. *See id.* at 138, 175.

Contrary to Patent Owner’s contention, during prosecution of the ’299 patent, the Examiner did not combine the processing steps of the ’501 patent with any prior art that teaches a graphics pipeline of processing units, let alone prior art that teaches both a pipeline GPU and that “[t]essellation should occur after transformation” in order to “enable[] tessellation size to be determined adaptively, and [to] limit[] the amount of data that is transformed,” as does Foley. Ex. 1007, 807. We find that during prosecution of the ’299 patent, the Examiner did not determine that performing the ordered steps of Sfarti on a graphics pipeline, such as the pipeline GPU taught by Foley, would not have been obvious.

We find that Petitioner has demonstrated that the combination of Sfarti and Foley teaches this limitation of claim 10, as summarized above.

(h) Lighting Unit

Claim 10 recites “said lighting unit comprising means for lighting triangles resulting from said tessellation unit.” Petitioner contends that the combination of Sfarti and Foley teaches this limitation. Pet. 58–59. Petitioner contends that Sfarti teaches the function of lighting triangles in describing calculating lighting for vertices of the triangles received from the tessellation stage. Pet. 59–60 (citing Ex. 1009 ¶¶ 40–42). Petitioner contends that Foley teaches the structure of the lighting unit in describing a programmable floating-point processor to perform lighting calculations. Pet. 60–61 (citing Ex. 1007, 877).

Patent Owner does not challenge Petitioner's analysis and evidence directed to the lighting unit limitation of claim 10. *See, e.g.*, PO Resp. 19–31 (Patent Owner's opposition, directed solely to the tessellation unit limitation).

(i) Conclusion as to Claim 10

For the reasons discussed above, we conclude claim 10 of the '534 patent is unpatentable as having been obvious over Sfarti and Foley.

4. Claims 11–20

Petitioner provides arguments and evidence in support of contending claims 11–20 are unpatentable as having been obvious over Sfarti and Foley. *See* Pet. 63–81; Ex. 1003 ¶¶ 196–233. Patent Owner does not oppose Petitioner's contentions as to these claims, apart from arguments we have already considered above in relation to claim 10. *See* PO Resp. 14–31. For the reasons provided above in Section III.D.3 in the context of claim 10, we conclude Patent Owner's arguments are unavailing. We further adopt Petitioner's additional analysis for the obviousness of claims 11–20 as our own in this Decision, and we accordingly conclude Petitioner has demonstrated by a preponderance of the evidence that those claims are unpatentable as having been obvious over Sfarti and Foley.

IV. SUMMARY OF CONCLUSIONS

In summary, we determine a preponderance of the evidence establishes claims 10–20 of the '534 patent are unpatentable, as shown in the following table:⁷

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
10–20	103(a)	Sfarti, Foley	10–20	
Overall Outcome			10–20	

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 10–20 of the '534 patent have been proven by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

⁷ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

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