

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

Zentian Limited
Patent Owner.

Case IPR2023-00033
Patent No. 7,587,319

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I. Introduction	1
II. Background of the ’319 Patent	3
III. Person of ordinary skill in the art	4
IV. Claim construction	4
V. The Board should deny institution under Fintiv	4
A. Fintiv factors 1-5 favor denial of institution	5
B. Fintiv factor 6 requires a “compelling” challenge, which the Petition does not present	7
VI. The Petition fails to demonstrate obviousness as to the combined requirements of limitations 46(b) and (d)	8
A. Limitations 46(b) and (d) together recite a novel design that the ’319 patent distinguished from two prior, known architectures	8
B. The Petition’s theory as to limitations 46(b) and (d) relies on three references that do not teach the ’377 patent’s claimed architecture	11
C. The Petition’s combination theory lacks a motivation, and is the product of improper hindsight bias, not “common sense”	17
VII. Conclusion	26

EXHIBIT LIST

Exhibit No.	Description
2001	<i>Intentionally Left Blank</i>
2002	Declaration of DeLiang Wang, Ph.D., in support of Patent Owner's Preliminary Response
2003	Defendant Apple's Preliminary Invalidity Contentions
2004	W.D. Tex. Scheduling Order

I. Introduction

Limitations 46(b) and (d) of the '319 patent together require multiple groups of processors with each group of processors connected to one of multiple lexical memories, with each lexical memory containing part of the lexical data, and all of the lexical memories combined containing all of the complete lexical data.

To meet those requirements, the Petition proposes to combine three references—Thelen, Bailey, and Chen. But the Petition's combination relies on numerous elements that are never taught in Thelen, Bailey, or Chen, and for which the Petition provides no motivation. In particular, whereas Thelen teaches using one alleged processor per recognition model or preferably one processor for *multiple* recognition models, the Petition asserts that Thelen would have been modified to use *multiple* alleged processors for one recognition model. And while Thelen and Bailey both teach storing *all* of their lexical data in their lexical memories, the Petition asserts—without reason—that the ordinary artisan would have only stored *part* of the lexical data in the memories of the combination. Finally, whereas Thelen and Bailey only teach lexical processor-to-lexical memory architectures of the types expressly distinguished on the face of the '319 patent, the Petition proposes to modify Thelen and Bailey in view of Chen, which has nothing to say about speech recognition system design at all.

To fill the gaps, the Petition falls back on the assertion that moving from the actual teachings of Thelen, Bailey, and Chen to the requirements of the challenged claims would have been merely a “common sense extension” of the prior art. The Federal Circuit, however, has repeatedly foreclosed reliance on allegations of “common sense” to fill gaps in the prior art teachings. *FanDuel, Inc. v. Interactive Games LLC*, 966 F.3d 1334, 1344 (Fed. Cir. 2020) (rejecting petition’s argument that adding a look-up table to the prior art design would have been an “obvious design choice”); *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017) (“Absent some articulated rationale, a finding that a combination of prior art would have been ‘common sense’ or ‘intuitive’ is no different than merely stating the combination ‘would have been obvious.’”); *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (“[R]eferences to ‘common sense’ . . . cannot be used as a wholesale substitute for reasoned analysis and evidentiary support. . . .”); *In re Stepan Co.*, 868 F.3d 1342, 1346 (Fed. Cir. 2017).

Thus, as this Preliminary Response demonstrates, the Petition does not present a reasonable likelihood of success, and falls well short of the much more stringent “high likelihood” of success that the Board should apply here in view of *Fintiv* and recent precedents.

II. Background of the '319 Patent

U.S. Patent 7,587,319, titled “Speech recognition using parallel processors,” is directed to an improved speech recognition circuit that “uses parallel processors for processing the input speech data in parallel.” Ex. 1001, 1:4-6. The '319 patent teaches multiple processors “arranged in groups or clusters,” with each group or cluster of processors connected to one of several “partial lexical memories” that “contains part of the lexical data.” Ex. 1001, 2:64-3:3. “Each lexical tree processor is operative to process the speech parameters using a partial lexical memory and the controller controls each lexical tree processor to process a lexical tree corresponding to partial lexical data in a corresponding partial lexical memory.” Ex. 1001, 3:3-7. The '319 patent further teaches that the invention “provides a circuit in which speech recognition processing is performed in parallel by groups of processors operating in parallel in which each group accesses a common memory of lexical data.” Ex. 1001, 3:44-47.

III. Person of ordinary skill in the art

For purposes of this Preliminary Response, Patent Owner does not dispute the Petition's proposed level of skill for a person of skill in the art ("POSA"), because the level of skill in the art is not necessary for addressing any disputes between the parties.

IV. Claim construction

The Petition does not propose any particular claim constructions and raises no claim construction issues.

Patent Owner's arguments in this Preliminary Response are based on the plain and ordinary meaning of the words of the claims themselves in view of the associated teachings of the specification. However, to the extent the Board views Patent Owner's arguments as resting on claim construction positions, the bases for such positions are set forth in the corresponding argument sections below.

V. The Board should deny institution under *Fintiv*

Whereas *inter partes* review was created "to establish a more efficient and streamlined patent system that will improve patent quality and limit unnecessary and counterproductive litigation costs," "[p]arallel district court and AIA proceedings involving the same parties and invalidity challenges can increase, rather than limit, litigation costs." USPTO Memorandum, Interim Procedure for

Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (“Guidance Memo”) (June 21, 2022), at 1.

In considering whether to institute an *inter partes* review proceeding where there is a parallel district court litigation, the Board considers the following six factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential):

1. Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. Proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. Investment in the parallel proceeding by the court and the parties;
4. Overlap between issues raised in the petition and in the parallel proceeding;
5. Whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. Other circumstances that impact the Board’s exercise of discretion, including the merits.

A. *Fintiv* factors 1-5 favor denial of institution

Factor 1: The patent at issue in this IPR is the subject of pending litigation in *Zentian Ltd. v. Apple, Inc.*, C.A. No. 6:22-cv-00122-ADA (W.D. Tex.). No stay has

been granted, and neither party has sought a stay to the extent this proceeding is instituted.

Factors 3 and 5: The parties in the district court case are the same as the parties in this proceeding. That case has continued to proceed since the Petition in this proceeding was filed, and will continue to proceed. The parties have exchanged proposed claim constructions, have completed claim construction briefing, and are awaiting a *Markman* hearing. Preliminary infringement and invalidity contentions have also been exchanged. Fact discovery will commence on March 24, 2023, and the parties are completing discovery on Apple's pending motion to transfer to the Northern District of California.

Factor 4: Apple's preliminary invalidity contentions in the district court case rely on Thelen, Bailey, Chen, Huang, and Jiang, which are all at issue in this IPR. *Compare* Pet. 6 with Ex. 2011 at 18, 19.

Factor 2: A trial date has tentatively been set for April 22, 2024, and will more definitively be set after the *Markman* hearing. Ex. 2012 at 5. By contrast, the Board's Institution Decision in this proceeding is not due until June 15, 2023, placing the Board's projected final written decision date at June 15, 2024—several months after the tentative trial date in the district court proceeding. Accordingly, there is a high likelihood that a final written decision in this *inter partes* review

would come later than a decision in the district court litigation, and that the Board's decision would merely address the same prior art and issues raised in the district court.

Accordingly, *Fintiv* factors 1-5 favor discretionary denial.

B. *Fintiv* factor 6 requires a “compelling” challenge, which the Petition does not present

Because *Fintiv* factors 1-5 favor discretionary denial, the Board must consider whether the Petition presents “compelling merits.” *Commscope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4 (Feb. 27, 2023) (precedential).

“The compelling merits standard is a higher standard than the standard for institution set by statute.” *Id.* at 3. To meet the “compelling merits” standard, the Petition must demonstrate that it is “***highly likely*** that the petitioner would prevail with respect to at least one challenged claim.” *Id.* at 3-4 (emphasis added).

As this Preliminary Response demonstrates, the Petition fails to demonstrate even a reasonable likelihood of success, much less the “high likelihood” of success standard that the Board should apply in view of *Fintiv* and *Commscope*.

VI. The Petition fails to demonstrate obviousness as to the combined requirements of limitations 46(b) and (d)

A. Limitations 46(b) and (d) together recite a novel design that the '319 patent distinguished from two prior, known architectures

The Petition challenges a sole independent claim, claim 46. Limitation 46(b) recites “a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data.” Limitation 46(b) thus requires (1) multiple lexical memories; (2) with each lexical memory containing “part” of the “complete lexical data,” and (3) the lexical memories together containing “complete lexical data for word recognition.” Ex. 2002 ¶ 23.

Limitation 46(d) further recites: “said [plurality of] processors being arranged in groups of processors, each group of processors being connected to a lexical memory.” Limitation 46(d) thus requires (1) multiple processors; (2) arranged in groups of processors; (3) with multiple groups each containing said multiple processors; and (4) with each group of multiple processors being connected to a lexical memory. Ex. 2002 ¶ 24.

Together, limitations 46(b) and 46(d) thus require an architecture with multiple groups of processors, each group containing a plurality of processors, and each group respectively connected to one of multiple lexical memories, with each

lexical memory containing part of the complete lexical data, and all of the lexical memories combined containing all of the complete lexical data. Ex. 2002 ¶ 25.

The specification of the '319 patent describes that same architecture, explaining:

“[T]he present invention provides a circuit in which speech recognition processing is performed in parallel by groups of processors operating in parallel ***in which each group accesses a common memory of lexical data.*** . . . Each processor within a group can access the same lexical data as any other processor in the group. The controller can thus control the parallel processing of input speech parameters in a more flexible manner. For example, it allows more than one processor to process input speech parameters using the same lexical data in a lexical memory. This is because the lexical data is segmented into domains which are accessible by multiple processors.” Ex. 1001, 3:44-58 (emphasis added).

Figure 2 of the patent, annotated below, further illustrates that architecture by showing two groups of lexical tree processors, with each group containing multiple processors 1-*k*, and each group of processors connected to a dedicated “acoustic model memory,” such that there are at least two acoustic model memories for at least two groups of processors. Ex. 2002 ¶ 26, Ex. 1001, Fig. 2 (annotated).

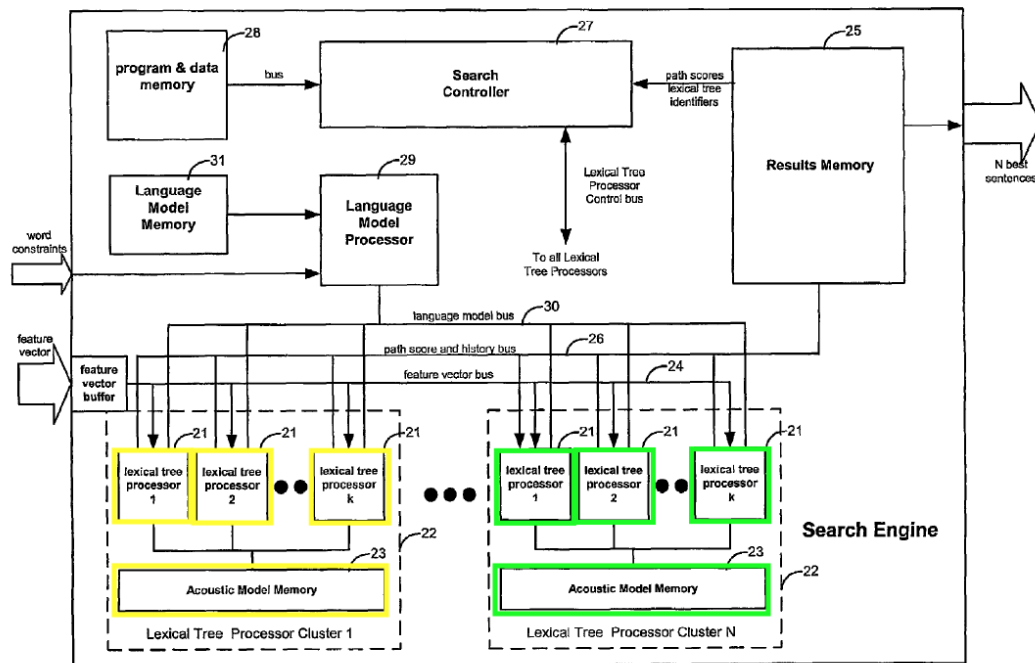


Fig 2

Moreover, the '319 patent expressly distinguishes its novel architecture from two prior known alternative designs, which the patent describes as less advantageous. Ex. 2002 ¶ 27. In particular, the '319 patent teaches that: “By providing a plurality of processors in a group with a common memory, flexibility in the processing is provided without being bandwidth limited by the interface to the memory **that would occur if only a single memory were used for all processors**. The arrangement is more flexible than the parallel processing arrangement **in which each processor only has access to its own local memory** and requires fewer memory interfaces (i.e. chip pins).” Ex. 1001, 3:50-58; Ex. 2002 ¶ 27. The patent thus distinguishes its design from (1) a

one-memory-to-*all*-processors design, which it describes as bandwidth limited in the processor to memory interface; and (2) a one-memory-to-*one*-processor design, which would require more memory interfaces and would be less flexible. Ex. 2002 ¶ 27.

B. The Petition's theory as to limitations 46(b) and (d) relies on three references that do not teach the '377 patent's claimed architecture

To meet the processor to memory architecture of the challenged claims, the Petition relies on the combination of Thelen, Bailey, and Chen. Pet. 23-33, 38-46.

The Petition admits, however, that Thelen's recognizers 1-3 (which the Petition maps as the claimed plurality of processors) all access a *single* memory storage 340. Pet at 24, 30. This is readily illustrated in Thelen's Figure 3, where a single storage 340 serves each of the processors labeled as Rec 1, Rec 2, Rec 3, and Testing Recognizer, and where the single storage 340 contains all of the "models" 341-348. Ex. 1030, Fig. 3 (Petition's annotations); Ex. 2002 ¶ 29.

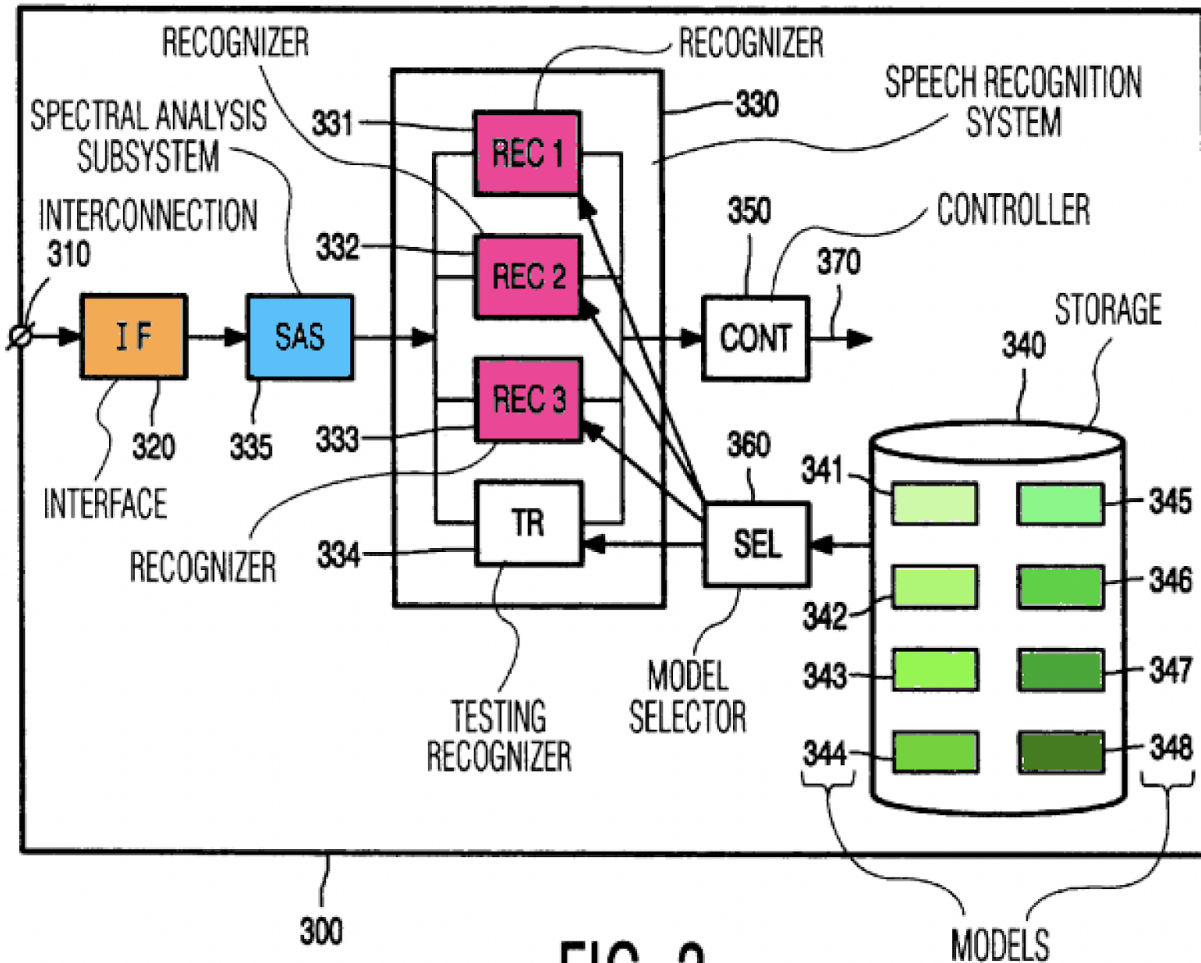
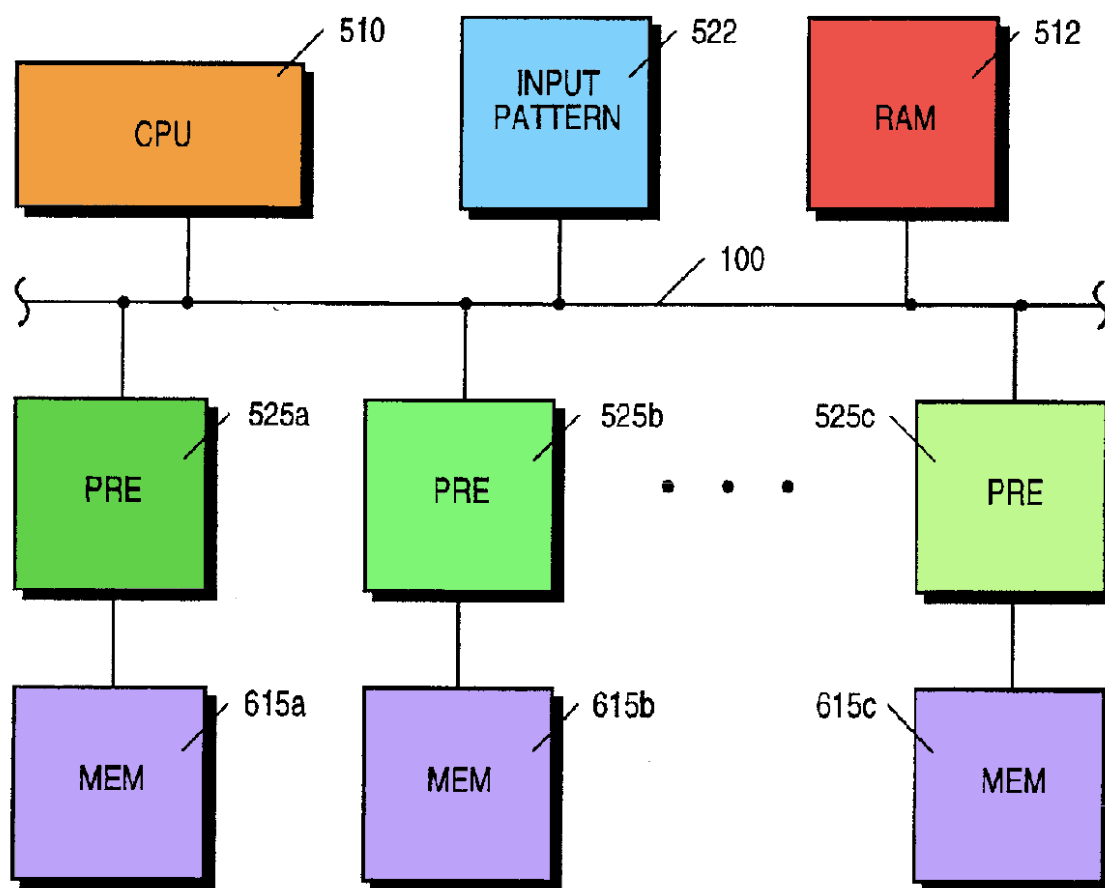


FIG. 3

As Thelen's Fig 3 illustrates, Thelen neither teaches limitation 46(b) nor 46(d), much less the two limitations combined. Ex. 2002 ¶¶31, 32 . With respect to limitation 46(b), Thelen does not teach multiple lexical memories, with each lexical memory containing "part" of the complete lexical data, and the lexical memories together containing "complete lexical data for word recognition." Ex. 2002 ¶ 31. Instead, Thelen teaches the one-memory-to-*all*-processors design that

the '319 patent expressly distinguished and innovated beyond. Ex. 2002 ¶ 31. With respect to limitation 46(d), Thelen does not teach a plurality of processors “arranged in groups of processors, each group of processors being connected to a lexical memory.” Ex. 2002 ¶ 32. Rather, Thelen teaches individual “recognizers,” which are never arranged in groups, and which are all connected to a single complete storage memory 340, rather than one of several lexical memories containing partial lexical data, as the claims require. Ex. 2002 ¶ 32.

To fill Thelen's gap, the Petition first looks to two embodiments from Bailey—the embodiments of Bailey's Figures 3A and 3B. Pet. 30-33, 36-38. But Bailey's two processor-to-memory architectures likewise fail to meet the requirements of limitations 46(b) and (d). Ex. 2002 ¶ 35, 36. Rather, both of Bailey's designs are exactly the ones the '319 patent distinguished and innovated beyond. Ex. 2002 ¶ 35, 36. In the embodiment of Bailey's Fig. 3A (below), each individual processor (labeled Pre) is connected to its own dedicated memory (labeled mem) such that there is one processor to one memory. Ex. 2002 ¶ 34.



Ex. 1031, Fig. 3 (Petition's annotated version). As Bailey states, "each PR engine 525a-525c [is] interfaced with its own *private memory* 615a-615c." Ex. 1031, 11:1-3 (emphasis added); Ex. 2002 ¶ 35. The embodiment of Bailey's Fig. 3A is thus the one-memory-to-*one*-processor design distinguished by the '319 patent. Ex. 2002 ¶ 35. Accordingly, while Bailey's Fig. 3A teaches a "plurality" of memories, it certainly does not teach the memory architecture of the '319 patent, but rather teaches the prior art design that the '319 patent innovated beyond. Ex. 2002 ¶ 35.

The design of Bailey's Figure 3B, by contrast, is identical to the other design distinguished by the '319 patent. Bailey's Figure 3B illustrates a design in which *all* of the processors PRE are connected to a *single* memory MEM 615. Ex. 2002 ¶ 36; Ex. 1031, Fig. 3B, 11:1-4.

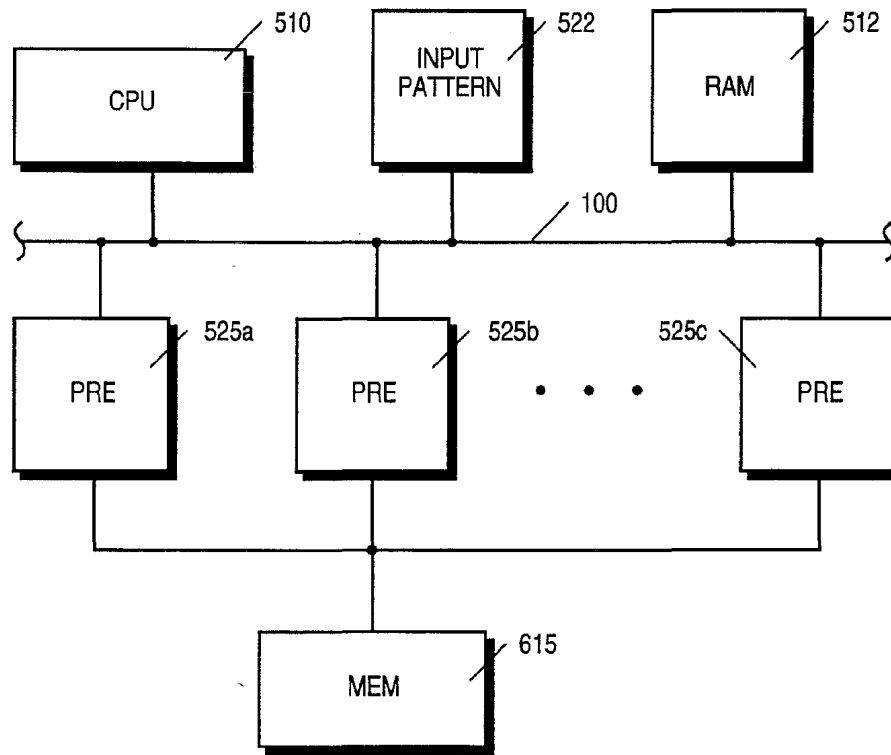


FIG. 3B

The design of Bailey's Figure 3B is thus identical to Thelen's, *i.e.*, one in which "only a single memory [is] used for all processors," as distinguished by the '319 patent. Ex. 2002 ¶ 37. As the '319 patent explained, the design of Thelen and Bailey's Fig. 3B is inferior to the '319 patent's innovative claimed architecture

because it is bandwidth limited. Ex. 1001, 3:44-58; Ex. 2002 ¶ 38. Thus, while Bailey's Fig. 3B (like Thelen) teaches connecting a plurality of processors to *one* memory, Bailey's certainly does not teach the design of the challenged claims. Ex. 2002 ¶ 38. Rather, in Bailey's Fig 3B there are not multiple *groups* of processors, each group containing multiple processors, and each group of processors connected to a lexical memory that contains a portion of the overall lexical data, with the lexical memories combined containing all of the lexical data. Ex. 2002 ¶ 38.

Thus, neither of Bailey's two embodiments teaches the claimed innovative processor to memory architecture of the challenged claims. Instead, Bailey (like Thelen) only teaches the same prior art design the patent expressly innovated beyond. Ex. 2002 ¶ 35, 37, 39.

Implicitly recognizing those shortcomings, the Petition next turns to Chen for the disclosure of multiple clusters of processors, each cluster containing multiple processors connected to a cluster shared memory. Pet. at 38-40. But Chen is not a reference in the field of art of speech recognition. Ex. 2002 ¶ 41. Rather, Chen teaches a general computer architecture design that has nothing to say about the design of speech recognition systems. Ex. 2002 ¶ 41. In particular, Chen provides no teachings regarding "lexical memories," much less "lexical memories containing in combination complete lexical data for word recognition," with "each

lexical memory containing part of said complete lexical data.” Ex. 2002 ¶ 41; *see also* Pet. 38-40 (admitting Chen does not teach lexical memories or lexical data). Chen thus also does not teach the claimed design of limitations 46(b) and (d). Ex. 2002 ¶ 41.

Accordingly, none of Thelen, Bailey, or Chen teaches the processor-to-memory design of limitations 46(b) and (d). Ex. 2002 ¶ 41.

C. The Petition’s combination theory lacks a motivation, and is the product of improper hindsight bias, not “common sense”

Because the Petition has no teaching in the prior art that it can rely upon to demonstrate that the claimed speech recognition system of limitations 46(b) and (d) was known, the Petition relies on a series of modifications to each of Thelen, Bailey, *and* Chen to arrive at what the Petition calls “*a common sense extension*” of the actual teachings of those three references. Pet. 44 (emphasis added).

The Petition’s convoluted and entirely contrived combination theory proceeds as follows:

- (1) Thelen’s recognizers are modified to be in “groups,” Pet. 40;
- (2) Each “group” of recognizers consists of *multiple* recognizers for the *same* subject matter context, e.g., multiple recognizers for “sports,” and multiple recognizers for “health,” etc., Pet. 42-43;

(3) Each newly created “group” of Thelen’s recognizers is connected to a dedicated shared memory, such that there are multiple dedicated shared memories in total, Pet. 40;

(4) Each of the dedicated shared group memories is a lexical memory, Pet. 40;

(5) Each dedicated shared group memory only stores the recognition model for the same specific “context” as the recognizers in the group, Pet. 42-43; and

(6) The shared group memories together contain complete lexical data, Pet. 40, 43.

Each and every aspect of the above theory, however, relies on an arrangement that is nowhere taught in *any* of Thelen, Bailey, or Chen. Ex. 2002 ¶ 43.

First, Thelen does not teach “groups” of multiple recognizers for the *same* subject matter, as the Petition’s steps (1) and (2) above require. Ex. 2002 ¶ 44. Rather, Thelen teaches an embodiment in which “the number of recognition models corresponds to the number of recognizers; each recognizer being associated with an exclusive recognition model in a fixed one-to-one relationship.” Ex. 1030, 7:43-46, 7:30-33. In this embodiment, there is only *one* recognizer for each subject matter, not multiple recognizers per subject matter, as the Petition’s theory

requires. Ex. 2002 ¶ 44. Alternatively, Thelen teaches a “preferred” embodiment in which “the system comprises *more models than active recognizers*[.]” Ex. 1030, 7:47-48 (emphasis added). In this “preferred” embodiment, there is only *one* recognizer for *multiple* subject matters, not multiple recognizers for one subject matter, as the Petition’s theory requires. Ex. 2002 ¶ 45. Thus, Thelen’s preferred embodiment teaches the *opposite* of what the Petition’s theory requires, *i.e.*, an architecture in which multiple recognition models are grouped to *one* processor, rather than multiple processors being grouped to one recognition model. Ex. 2002 ¶ 45.

Second, as demonstrated earlier, none of Thelen, Bailey, or Chen teaches a design in which multiple groups of speech recognition processors, with multiple processors per group, are each connected to one dedicated lexical memory per group, as steps (3) and (4) of the Petition’s theory (above) require. Ex. 2002 ¶ 46. Rather, Thelen and Bailey merely teach the prior art designs the ’319 patent expressly distinguished, and Chen provides no teachings regarding speech recognition or lexical memories at all. Ex. 2002 ¶ 41, 46.

Third, none of Thelen, Bailey, or Chen teaches storing one recognition model per lexical memory, with multiple lexical memories combined storing all recognition models, as steps (5) and (6) of the Petition’s theory (above) require. Ex.

2002 ¶ 47. Rather, Thelen teaches storing all recognition models in one storage memory 340. Ex. 2002 ¶ 47. With respect to the embodiment of Fig. 3B, Bailey also teaches storing all of its lexical data in a single storage memory. Ex. 2002 ¶ 47. As for the embodiment of Fig. 3A, Bailey also teaches storing **all** of its lexical data in each of the dedicated private memories, such that each memory contains **all** of the lexical data, not **part** of the lexical data. Ex. 1031, 13:12-13 (describing “the private memory 615 which holds **all** the prototype patterns.”) (emphasis added); 11:22-23 (“Each PR engine contains its own library of prototype patterns 615*a* to 615*c* respectively.”); Ex. 2002 ¶ 47. Bailey never teaches that the private memories in Fig. 3A contain portions of the overall lexical data. And Chen teaches nothing regarding lexical memories or lexical data at all. Ex. 2002 ¶ 47.

Accordingly, each aspect of the Petition’s combination theory relies on arrangements and modifications that are nowhere taught or suggested by any of Thelen, Bailey, or Chen. Ex. 2002 ¶ 48.

Given that reality, it is particularly crucial for the Petition to provide “a reason **why**” the ordinary artisan, at the time of the ’319 patent, would have been motivated to undertake the numerous modifications the Petition’s theory requires in the precise manner necessary to arrive at the requirements of limitations 46(b) and (d). *In re Nuvasive*, 842 F.3d 1376, 1381-82 (Fed. Cir. 2016) (requiring evidence

and articulation of “a *reason why* a PHOSITA would combine the prior art references.”) (emphasis original); *PersonalWeb Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 991 (Fed. Cir. 2017); *In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1333-34 (Fed. Cir. 2016); *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1364-67 (Fed. Cir. 2015); *ActiveVideo Networks v. Verizon*, 694 F.3d 1312, 1328 (Fed. Cir. 2012); *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1164 (Fed. Cir. 2006) (internal citations and quotations omitted).

The Petition, however, falls far short of demonstrating a motivation to combine Thelen, Bailey, and Chen in the manner necessary to arrive at the design of limitations 46(b) and (d). Ex. 2002 ¶ 49-51. Instead, the Petition merely relies on three conclusory jargons: “common sense extension,” Pet. 44, “yield predictable results,” Pet. 44, and greater “efficiency.” Pet. 41, 42, 44.

But as the Federal Circuit has held, a petition cannot rely on conclusory jargon to overcome a gap between the teachings of the prior art and the design of the claimed invention. *FanDuel, Inc. v. Interactive Games LLC*, 966 F.3d 1334, 1344 (Fed. Cir. 2020) (rejecting petition’s argument that adding a look-up table to the prior art design would have been an “obvious design choice”); *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017) (“Absent some articulated rationale, a finding that a combination of prior art would have been ‘common sense’ or ‘intuitive’ is no

different than merely stating the combination ‘would have been obvious.’”); *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016) (“[R]eferences to ‘common sense’ . . . cannot be used as a wholesale substitute for reasoned analysis and evidentiary support. . . .”); *In re Stepan Co.*, 868 F.3d 1342, 1346 (Fed. Cir. 2017).

And as the Federal Circuit has particularly held, when a petition falls back on “common sense . . . to supply a missing limitation,” the Board must conduct a “searching” inquiry as to whether the petition provides a sufficiently “reasoned basis for resort to common sense[.]” *Arendi*, 832 F.3d at 1363. The Petition provides no such “reasoned basis” here.

Moreover, even the Petition’s “common sense extension” allegation depends on ascribing teachings to the prior art references ***that those references do not teach***. Pet. 44, Ex. 2002 ¶ 49. Thus, while the Petition again implies that Thelen teaches multiple recognizers per recognition model, Pet. 44, Thelen itself contains no such teaching, and indeed teaches the ***opposite*** with respect to its preferred embodiment. Ex. 1030, 7:43-46, 7:30-33 (one recognizer per model); Ex. 1030, 7:47-48 (one recognizer per multiple models is preferred); Ex. 2002 ¶ 45. And while the Petition implies that Bailey teaches multiple groups of processors with each group of processors connected to one of multiple lexical memories, Pet. 44,

Bailey also teaches no such thing. Ex. 2002 ¶ 34-39. Rather, it teaches one memory to one processor or one memory to *all* processors. Ex. 2002 ¶ 34-39. Importantly, the Petition cites to *no reference* for the concept of storing *partial* lexical data in each of multiple lexical memories, such that the lexical memories combined store all the lexical data. Ex. 2002 ¶ 47.

Accordingly, the Petition fails to demonstrate that an ordinary artisan would have expected the combination to “yield predictable results.” Ex. 2002 ¶ 50. To the contrary, the ordinary artisan would not have found it “predictable” to rearrange and modify multiple prior art references to arrive at a design that was never taught in any of those references. Ex. 2002 ¶ 50.

Finally, the Petition’s repeated allegation that its proposed combination would have improved “efficiency” is not evidence of a motivation to combine. The Federal Circuit has expressly rejected the “generic” motivation of improved efficiency, explaining that such an alleged motivation “bears no relation to any specific combination of prior art elements” and “fails to explain why a person of ordinary skill would have combined elements from specific references *in the way the claimed invention does.*” *ActiveVideo*, 694 F.3d at 1328 (emphasis original). Here, as in *ActiveVideo*, the Petition and its expert merely state that the proposed combination would have been more “efficient,” but provide no reasoned analysis

of the countervailing costs and tradeoffs of the modification, and no explanation as to why any such “efficiency” benefits would have motivated the combination in light of the tradeoffs. Ex. 2002 ¶ 51. For instance, the Petition ignores that its proposed modification would have required far more hardware—in terms of processors and memories—than what either Thelen or Bailey teaches, and that this would have necessarily come at significant additional cost and complexity. Ex. 2002 ¶ 51. The Petition’s entirely conclusory “efficiency” rationale thus fails to meet the Federal Circuit’s requirement of weighing both the alleged benefits and costs of the proposed modification. *Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n. 8 (“the benefits, both lost and gained, should be weighed against one another”); *id.* at 1349 (“Motivation to combine requires” what is “on balance, desirable,” in view of the “[t]rade-offs.”). Instead, the Petition states a meaningless and “generic” alleged benefit—“efficiency”—without any consideration of the very real associated costs. That is not evidence of a motivation to combine.

Moreover, the Petition entirely ignores and fails to address that *Thelen itself* teaches that in its preferred embodiment, there should only be *one* recognizer per *multiple* recognition models—the exact opposite of the Petition’s proposed modification. Ex. 2002 ¶ 45.

Furthermore, as Dr. Wang explains, the Petition's wholesale rearrangement of Thelen, Bailey, and Chen beyond the teachings of those references to arrive at the design of the challenged claims goes well beyond the level of *ordinary* skill in the art. Ex. 2002 ¶ 52.

As the Supreme Court explained in *KSR*, the ordinary artisan is a person of *ordinary* creativity. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 421 (2007) ("A person of ordinary skill is also a person of ordinary creativity"). Just as a person of "*ordinary* skill" is "not an automaton," *id.*, the person of ordinary skill is also not a person of above-average creativity in the field of art. *Id.* The line between invention and obviousness is thus not whether *any person could* have arrived at the design of the challenged claims at the time. Rather, it is whether a person of *ordinary* creativity *would have been motivated* to do so with a reasonable expectation of success. *Id.*

In the Petition's combination, the artisan would have required the motivation, insight, and skill to (1) dedicate *multiple* recognizers to each of Thelen's recognition models, creating multiple groups each containing multiple recognizers, contrary to Thelen's own teachings; (2) associate each group of recognizers with a dedicated memory in a manner never taught by Thelen or Bailey; (3) ensure that each dedicated memory contained part of the lexical data,

contrary to Bailey and Thelen's teachings; and (4) ensure that the sum of the dedicated memories together contained the complete lexical data, which was also never taught in Thelen or Bailey. Ex. 2002 ¶ 52.

As Dr. Wang explains, that series of choices and reconfigurations goes well beyond obviousness, and would not have been the work of *ordinary* creativity. Ex. 2002 ¶ 52. The Petition simply identifies no logical path or motivation or prior knowledge in the art that would have led the ordinary artisan, using ordinary creativity, to start from Thelen, Bailey, and Chen and arrive at the design of limitations 46(b) and (d). Ex. 2002 ¶ 52.

Accordingly, the Petition is not reasonably likely to prevail, much less highly likely to prevail.

VII. Conclusion

For the reasons above, the Board should decline to institute the Petition.

Respectfully submitted,

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Date: March 15, 2023

CERTIFICATION OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned **PATENT OWNER'S PRELIMINARY RESPONSE** specified in 37 C.F.R. § 42.24 have 4,940 words, in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24(b)(1). This word count was prepared using Microsoft Word 365.

/Peter C Knops/

Peter C Knops

Counsel for Patent Owner

Date: March 15, 2023

CERTIFICATION OF SERVICE

The undersigned hereby certifies that the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** was served electronically via e-mail on March 15, 2023, on the following counsel of record for Petitioner:

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