

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

ZENTIAN LTD.,

Plaintiff,

v.

APPLE INC.,

Defendant.

Case No. 6:22-cv-00122-ADA

JURY TRIAL DEMANDED

DEFENDANT APPLE INC.’S INVALIDITY CONTENTIONS

I. INTRODUCTION

Pursuant to the September 23, 2022 Scheduling Order (Dkt. 37), Defendant Apple Inc. (“Apple”) provides these Preliminary Invalidity Contentions to Plaintiff Zentian Ltd. (“Zentian”) for the following Asserted Patents¹ and Asserted Claims identified as asserted in Zentian’s Preliminary Infringement Contentions dated September 1, 2022 (“Infringement Contentions”):

- U.S. Patent No. 7,979,277 (’277 patent): claims 1, 4, 5, 7, 9, 10, 12, 14–16
- U.S. Patent No. 7,587,319 (’319 patent): claims 46–51, 53, 54, 58, 59, 64, 67
- U.S. Patent No. 10,971,140 (’140 patent): claims 1–6
- U.S. Patent No. 10,062,377 (’377 patent): claims 1–6
- U.S. Patent No. 10,839,789 (’789 patent): claims 1, 2, 4, 6–14, 16–18, 20–29, 35, 37–39, 42–45

These Invalidity Contentions use the term “POSITA” to refer to a person having ordinary

¹ The Asserted Patents are governed by the pre-AIA statutory framework as the applications were filed before March 16, 2013

skill in the art to which the claimed inventions pertain.

Apple reserves the right to rely on arguments made in the invalidity contentions of Amazon.com Services LLC and Amazon Web Services, Inc. in the related case of *Zentian v. Amazon.com Services LLC*, No. 6:22-cv-00123-ADA (W.D. Tex.). Apple's Invalidity Contentions and Amazon's Invalidity Contentions are collectively referred to herein as "Defendants' Invalidity Contentions."

II. PRIORITY DATE OF THE ASSERTED PATENTS AND CLAIMS

Zentian asserts that the '319 and '140 patents are each entitled to a priority date of no later than February 4, 2002 because they claim priority to a UK application (GB 0202546.8) filed on February 4, 2002.

Zentian further asserts that the '277, '377, and '789 patents are each entitled to a priority date of no later than September 14, 2004 because they claim priority to a UK application (GB 0420464.0) filed on September 14, 2004.

It is Zentian's burden to show entitlement to its asserted priority dates, and Zentian has failed to meet that burden. As described below, elements of the Asserted Claims lack written description and enablement support, and those Asserted Claims therefore cannot claim priority to earlier applications listed on the Asserted Patents.

III. LEGAL STANDARDS

A. Invalidity Under 35 U.S.C. § 101

To be patentable subject matter under § 101, a claim must be directed to one of four eligible subject matter categories: "new and useful process, machine, manufacture, or composition of matter." 35 U.S.C. § 101. "Claims that fall within one of the four subject matter categories may nevertheless be ineligible if they encompass laws of nature, physical phenomena, or abstract ideas." *Digitech Image Techs., LLC v. Elecs. For Imaging, Inc.*, 758 F.3d 1344, 1350

(Fed. Cir. 2014) (citing *Diamond*). The Supreme Court established a two-step test for deciding the subject matter eligibility of claims under § 101. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347, 2355 (2014). First, the claims must be analyzed to determine whether they are drawn to one of the statutory exceptions. *Id.* Claims that invoke generic computer components instead of reciting specific improvements in computer capabilities are abstract under this first step. *See English, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335-36 (Fed. Cir. 2016). Second, the elements of the claims must be viewed both individually and as an ordered combination to see if there is an “inventive concept.” *Id.* at 1336. The mere fact that a claim recites or implies that an abstract idea is implemented using a general-purpose computer does not supply an inventive concept necessary to satisfy § 101. *See Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1355 (Fed. Cir. 2016); *Alice*, 134 S. Ct. at 2357-59.

The Asserted Claims discussed below under the headings for each Asserted Patent are directed to ineligible subject matter under 35 U.S.C. § 101 and applicable case law.²

B. Invalidity Under 35 U.S.C. § 112

Section 112, ¶ 2 includes a definiteness requirement: “[T]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.” 35 U.S.C. § 112, ¶ 2 (pre-AIA). “[A] patent is invalid for indefiniteness if its claims, read in light of the patent’s specification and prosecution

² *See, e.g., Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208 (2014); *SAP America, Inc. v. InvestPic, LLC*, 898 F.3d 1161 (Fed. Cir. 2018); *Intellectual Ventures I LLC v. Capital One Fin. Corp.*, 850 F.3d 1332 (Fed. Cir. 2017); *Intellectual Ventures I LLC v. Erie Indemnity Co.*, 850 F.3d 1315 (Fed. Cir. 2017); *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350 (Fed. Cir. 2016); *Intellectual Ventures I LLC v. Capital One Bank (USA)*, 792 F.3d 1363 (Fed. Cir. 2015); *OIP Techs., Inc. v. Amazon.com, Inc.*, 788 F.3d 1359 (Fed. Cir. 2015); *Content Extraction & Transmission LLC v. Wells Fargo Bank, Nat’l Ass’n*, 776 F.3d 1343 (Fed. Cir. 2014).

history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014).

IPXL Holdings, LLC v. Amazon.com, Inc., 430 F.3d 1377 (Fed. Cir. 2005) held that a claim is indefinite if it is unclear whether infringement occurs when one creates a system that allows a user to perform a method or whether infringement occurs when the user actually uses the system that performs the method.

Section 112 further includes an enablement requirement: “The specification shall contain a written description . . . of the manner and process of making and using [the invention] in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.” 35 U.S.C. § 112, ¶ 1. To satisfy the enablement requirement, the disclosure “must teach those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’”

Genentech, Inc. v. Novo Nordisk A/S, 108 F.3d 1361, 1365 (Fed. Cir. 1997); *MagSil Corp. v. Hitachi Glob. Storage Techs., Inc.*, 687 F.3d 1377, 1380 (Fed. Cir. 2012); *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008). If a specification teaches away from a substantial portion of the claim or does not enable the full scope of the claim, there is no enablement. *AK Steel Corp. v. Sollac*, 344 F.3d 1234 (Fed. Cir. 2003); *see also MagSil Corp.*, 687 F.3d at 1383-84 (Fed. Cir. 2012).

Section 112 further includes a written description requirement: “The specification shall contain a written description of the invention” 35 U.S.C. § 112, ¶ 1. “To satisfy the written description requirement, a patent applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention.” *ICU Medical Inc. v. Alaris Medical Systems, Inc.*, 558 F.3d 1368, 1377 (Fed. Cir. 2009) (internal

quotation marks and citations omitted); *see also Synthes USA, LLC v. Spinal Kinetics, Inc.*, 734 F.3d 1332, 1340 (Fed. Cir. 2013). “The test [for written description support] requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.” *Ariad Pharmaceuticals, Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc).

The specification must describe the claimed invention in sufficient detail so that a POSITA can recognize what is claimed. “The appearance of mere indistinct words in a specification or a claim, even an original claim, does not necessarily satisfy that requirement.” *University of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 923 (Fed. Cir. 2004) (internal quotation marks and citations omitted).

The grounds identified below both individually and collectively render the Asserted Claims invalid under the statutory requirements of § 112. By identifying certain claim language below, Apple does not imply that such language is entitled to any patentable weight when comparing the claim as a whole to the prior art. Apple’s identifications are made based on Apple’s present understanding of the Asserted Claims and Zentian’s apparent interpretation of these claims as reflected in its Infringement Contentions. Apple reserves the right to amend these identifications, including in response to claim constructions and claim interpretations that would render claim limitations not enabled, lacking in written description, or indefinite. To the extent a claim element is contained within an element identified below or encompass an element identified below, that claim element also renders the claim invalid under 35 U.S.C. § 112.

C. Obviousness and Motivation to Combine

No showing of a specific motivation to combine prior art is required to combine the

references disclosed herein and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. *See Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1058 (Fed. Cir. 2016); *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1344 (Fed. Cir. 2017); *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit’s “rigid” application of the teaching, suggestion, or motivation to combine test, and instead applying an “expansive and flexible” approach). Indeed, the Supreme Court held that a POSITA is “a person of ordinary creativity, not an automaton” and “in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *KSR*, 550 U.S. at 420-21. Nevertheless, in addition to the information contained under the headings for each Asserted Patent and elsewhere in these contentions, Apple hereby identifies motivations and reasons to combine.

One or more combinations of the prior art references identified herein would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. *See Apple*, 839 F.3d at 1077; *Intercontinental Great Brands*, 869 F.3d at 1344. In addition, it would have been obvious to try combining the prior art references identified herein because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. *See ACCO Brands Corp. v. Fellowes, Inc.*, 813 F.3d 1361, 1367 (Fed. Cir. 2016); *Sanofi-Aventis Deutschland GmbH v. Glenmark Pharms. Inc., USA*, 748 F.3d 1354, 1360 (Fed. Cir. 2014);

Bayer Pharma AG v. Watson Labs., Inc., 874 F.3d 1316, 1329 (Fed. Cir. 2017); *KSR*, 550 U.S. at 420-21. Further, the combinations of the prior art references identified herein and in the claim charts would have been obvious because the combinations represent known potential options with a reasonable expectation of success. See *InTouch Techs., Inc. v. VGo Comms., Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014).

Additional evidence that there would have been a motivation to combine the prior art references identified herein includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged inventions; and the background knowledge that would have been possessed by a POSITA. See *Arctic Cat Inc. v. Bombardier Rec. Prod. Inc.*, 876 F.3d 1350, 1359 (Fed. Cir. 2017); *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1344 (Fed. Cir. 2017); *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016); *Norgren Inc. v. Int'l Trade Comm'n*, 699 F.3d 1317, 1322-23 (Fed. Cir. 2012).

The motivation to combine the teachings of the prior art references disclosed herein is also found in the references themselves and in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of POSITAs; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had

a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces. See above legal background regarding obviousness combinations and MPEP § 2143.

Thus, to the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

IV. '277 PATENT

A. Prior Art References

Apple identifies the following prior art now known to Apple to anticipate or render obvious the Asserted Claims of the '277 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, either expressly or inherently as understood by a POSITA.

1. Prior Art Publications

- U.S. Patent App. Pub. No. 2002/0049582 (“Baumgartner”). See Ex. A-01.
- U.S. Patent No. 5,699,456 (“Brown”). See Ex. A-02.
- U.S. Patent No. 6,374,219 (“Jiang”). See Ex. A-03.
- U.S. Patent No. 6,879,954 (“Nguyen”). See Ex. A-04.
- Mosur K. Ravishankar, *Efficient Algorithms for Speech Recognition* (May 15, 1996) (“Ravishankar”). See Ex. A-05.
- U.S. Patent No. 5,819,222 (“Smyth”). See Ex. A-06.
- S. Yoshizawa et al., *A Low-Power VLSI Design of an HMM Based Speech Recognition System*, The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002, II-489-92 (2002) (“Yoshizawa 1”). See Ex. A-07.
- U.S. Patent No. 6,490,559 (“Budde”). See Ex. A-10.
- CN1503220 (“Jiang 220”). See Ex. A-11

- Rajeev Krishna et al., *Architectural Optimizations for LowPower, RealTime Speech Recognition*, Int’l. Conf. on Compilers, Architectures & Sythesis for Embedded Systems (CASES) (Oct. 30-Nov. 2, 2003) (“Krishna”). *See* Ex. A-12.
- Int’l. Patent Pub. No. WO2000/060577 (“Lund”). *See* Ex. A-13.
- Binu Mathew et al., *A Low-Power Accelerator for the SPHINX 3 Speech Recognition System*, Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES 2003, 210-19 (Oct. 30, 2003) (“Mathew”). *See* Ex. A-14.
- S. Melnikoff et al., *Speech Recognition on an FPGA Using Discrete and Continuous Hidden Markov Models*, 12th International Conference on Field Programmable Logic and Applications (2002) (“Melnikoff”). *See* Ex. A-15.
- S. Melnikoff et al., *Performing Speech Recognition on Multiple Parallel Files Using Continuous Hidden Markov Models on an FPGA* (“Melnikoff II”). *See* Ex. A-16.
- P. Stogiannos et al., *A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition Using Hidden Markov Models*, Journal of VLSI Signal Processing Systems (2000) (“Stogiannos”). *See* Ex. A-17.
- Anton Stolzle et al., *Integrated Circuits for a Real-Time Large-Vocabulary Continuous Speech Recognition System*, IEEE Journal of Solid-State Circuits, Vol. 26, No. 1 (Jan. 1991) (“Stolzle”). *See* Ex. A-18.
- “Telecommunications Applications with the TMS320C5x DSPs,” Texas Instruments Inc. (1994) (“TMS320C”). *See* Ex. A-19.
- U.S. Patent No. 6,070,140 (“Tran”). *See* Ex. A-20.
- S. Yoshizawa et al., *A High-Speed HMM VLSI Module With Block Parallel Processing*, Electronics and Communications in Japan, Vol. 87, No. 5 (2004) (“Yoshizawa II”). *See* Ex. A-21.

Apple additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below. Apple’s investigation into prior art patent and publication references remains ongoing, and Apple reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Apple reserves the right to supplement as further prior art is identified through investigation or discovery.

2. Prior Art Systems

The following systems are prior art to the Asserted Claims of the '277 patent under at least 35 U.S.C. §§ 102(a), (b) and/or (g), because they were either (1) in public use or on sale in the United States no later than the priority date of the Asserted Claims or (2) reduced to practice in the United States no later than the priority date of the Asserted Claims without being abandoned, suppressed, or concealed. Apple also identifies and relies on prior art systems discussed in the prior art publications listed in the preceding section. Apple reserves the right to rely on other sources of evidence identified as discovery and Apple's investigation progresses.

- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to SPHINX-II. *See* Ex. A-08.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Texas Instruments TMS320C System ("TMS320C System"). *See* Ex. A-22.

3. Obviousness Prior Art

A POSITA would have known that any of the references identified above would have rendered the Asserted Claims obvious, alone or in combination. Additionally, Apple identifies the following prior art now known to Apple that, in combination with the foregoing patents, publications, and systems, render obvious the Asserted claims under 35 U.S.C. § 103, either expressly or inherently as understood by a POSITA, for at least the reasons stated in Section III.C. An invalidity claim chart for these prior art obviousness references is provided in Exhibit A-09.

- U.S. Patent No. 6,374,219 ("Jiang")
- U.S. Patent Application Publication No. 2002/0049582 ("Baumgartner")
- U.S. Patent No. 5,819,222 ("Smyth")
- U.S. Patent No. 5,699,456 to Brown ("Brown")

- International Publication No. WO 99/41684 (“Kazeroonian”)
- U.S. Patent No. 4,567,606 (“Vensko”)

B. The Asserted Claims Would Have Been Obvious in View of the Prior Art

To the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. Nevertheless, Apple provides the following examples of how and why a POSITA would have combined the references above.

The speech recognition circuits and methods claimed in the ’277 patent utilize a front end to generate a feature vector, a calculating circuit to indicate the similarity between the feature vector and predetermined acoustic states, and a search stage to identify words within a lexical tree. ’277 patent, 3:51–4:18, 10:35-61, 11:65–12:10. The claimed speech recognition circuits and methods also pipeline data from the front end to the calculating circuit to the search stage. ’277 patent, 4:8-18.

As discussed in the attached claim charts, Jiang alone or in combination with Baumgartner teaches or renders obvious the functionalities of an “audio front end,” a “calculating circuit,” and a “search stage” as claimed. The figures of Jiang do not expressly show the functionalities of the claimed “audio front end” and “search stage” implemented using a “first processor,” and the functionality of the claimed “calculating circuit” implemented using a “second processor,” as recited in claim of the ’277 patent. Baumgartner, however, teaches a

similar front end and search stage as Jiang's but provided on a first processor, and a similar calculating circuit as Jiang's but provided on a second processor. *Compare* '277 patent, Fig. 21 *with* Baumgartner, Fig. 19; *see* Ex. A-01, limitation 1.e.

A POSITA would have found it obvious and been motivated to modify Jiang, such that Jiang's mapped audio front end and search stage were implemented using a first processor, as taught by Baumgartner, and Jiang's mapped calculating circuit was implemented using a second processor, as taught by Baumgartner. Jiang teaches its speech recognition system may be "practiced with other computer system configurations, including ... multi-processor systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, main-frame computers, and the like." Jiang, 4:60-65. Thus, a POSITA would have understood Jiang contemplated modifications to its hardware architecture, including using two processors. Jiang already teaches that the mapped audio front end, i.e., the feature extraction module, may be a processor, and that the mapped search stage, i.e., tree search engine performing tree searching, is a dedicated processor. Jiang, 6:32-36, 6:39-42.

Given that a POSITA would have understood Jiang's disclosures to contemplate various hardware architectures, a POSITA looking to design a speech recognition system at the time of the '277 Patent would have looked to additional sources—leading a POSITA to Baumgartner. Baumgartner explains "[s]peech recognition ... is currently a computationally intensive task," that "it would be beneficial to reduce the load on the processors of the system when the system performs speech recognition," and "a need exists for techniques to reduce the computational load of a processor during speech recognition." Baumgartner, [0003]-[0006]. A POSITA would have recognized Baumgartner's "invention provides Speech Label Accelerators (SLAs), ... speeds processing during the labeling stage of a speech recognizer[,] and frees one or more processors

from performing labeling.” Baumgartner, [0007]. A POSITA would have further understood that Baumgartner’s hardware architecture—utilizing an accelerator for expensive calculations—provides an efficient solution to the computational load issues identified by the prior art. Baumgartner at [0200]–[0205].

A POSITA would have had a reasonable expectation of success implementing the distance calculation on a second processor without undue experimentation at least because Baumgartner expressly illustrated its feasibility. Additionally, the use of accelerators, such as Baumgartner’s SLA, or co-processors—sometimes called math-processors—was a well-known technique to offload computation tasks in general, prior to the ’277 Patent. The determination of whether to use an accelerator for computationally expensive tasks—as opposed to using a sole processor for the entire system—would have been a simple design choice well within the skill set of a POSITA. Given the widespread use of accelerators at the time, a POSITA would have been able to implement an accelerator into a speech recognition system without undue experimentation. The same analysis would apply to other references that expressly teach utilizing different hardware to perform distance calculation and other speech recognition tasks.

To the extent one or more references do not explicitly or inherently disclose pipelining, a POSITA would have been motivated and found it obvious to modify the Jiang-Baumgartner system to pipeline data according to Brown’s teachings. A POSITA would have understood and found obvious that pipelining data offered numerous well-known advantages including greater overall throughput of the processor, improved performance, decreased cost, and simplified programming. Utilizing the well-known pipelining technique would have improved the Jiang-Baumgartner system in the same way as Brown’s speech recognition system.

Claim 4 of the ’277 patent additionally requires that the first processor supports

multithreaded operation. Multithreading was well known in the art, and Kazeroonian teaches an automated real-time system for processing audio-video data including speech recognition functionality and expressly teaches using multi-threaded operations for pipelined processing. Kazeroonian, Abstract, 13:33-14:1, 17:30–18:5, 19:9-11, Fig. 2. Additionally, Kazeroonian teaches “different processor threads are assigned to different stages of processing.” Kazeroonian, 19:9-11. A POSITA would have been motivated and found it obvious to modify the Jiang-Baumgartner-Brown system to utilize a multi-threaded operation for the claimed “first processor” to run the claimed “search stage” and “front end” as separate threads. Kazeroonian expressly motivates the combination, to provide high throughput, high segmentation speed, and a result only moments after the data is input. Yet further, such a modification would have advantageously “improve[d] performance by judicious assignment of various tasks (stages) to separate threads,” as expressly taught by Kazeroonian. Kazeroonian, 18:3-5.

Claim 9 of the '277 patent describes “interrupt” functionality. A POSITA would have been motivated and found it obvious to further modify the Jiang-Baumgartner-Brown system to include Vensko’s interrupt functionality. *See* Vensko, 6:29-33, 6:48-51, 10:10-19. For example, Baumgartner already contemplates the use of an interrupt in Baumgartner’s SLA. Baumgartner, [0179]-[0180]. A POSITA would have further understood that pipelined systems process system stages concurrently—for example the claimed “audio front end,” “calculating circuit,” and “search stage.” *See* Brown, 3:32-48. Therefore, modifying Jiang’s system such that the second processor performing distance calculation is ready to receive a next feature vector for processing is a routine and obvious modification for obtaining efficient processing.

Claim 10 of the '277 patent recites signaling to the search stage. Because Vensko’s interrupt functionality on the template processor signals that results are ready for transfer in a

pipelined system, in the modified Jiang-Baumgartner-Brown-Vensko system, it would have been obvious for the accelerator (i.e., the component with the calculated distances) to signal the search stage (i.e., the component that next uses the calculated distances) when distances for a new frame are available. Further, Jiang teaches tree search engine 74 accesses information stored in memory 72. Jiang, 7:31-34.

The above descriptions of possible combinations are exemplary and not limiting. It would have been obvious to combine any of the references that teach the individual limitations of the '277 patent following a similar analysis.

C. Invalidity Under 35 U.S.C. § 101

The Asserted Claims of the '277 patent are directed to patent-ineligible subject matter under 35 U.S.C. § 101. Claims 1, 14, 15, and 16 of the '277 patent (and all claims that depend from them) are directed to the abstract idea of calculating data (e.g., feature vectors and distances) and using that data in a known field. Courts have acknowledged that performing calculations such as statistics is a patent-ineligible, abstract idea. *See, e.g., OIP Technologies, Inc. v. Amazon.com, Inc.*, 788 F.3d 1359, 1363-64 (Fed. Cir. 2015).

The elements recited in the claims of the '277 patent are well understood, routine, and conventional and thus do not provide an “inventive concept.” For example, audio front ends, distance calculations with acoustic models, search software, and using multiple processors, and pipelining were all well understood, routine, and conventional at the time of the application for the '277 patent.

The elements recited in the dependent claims were also well understood, routine, and conventional. These elements include, without limitation, multi-threading, feature vectors comprising spectral components, interrupt signals, signaling within software, and digital audio signals.

The specification of the '277 patent (and the references cited therein) support the contention that the elements discussed in the preceding paragraphs were well understood, routine, and conventional. Apple incorporates by reference the prior art cited in the Ex. A charts, which provide further evidence that the above elements were well understood, routine, and conventional.

D. Invalidity Under 35 U.S.C. § 112

1. Lack of Enablement and Written Description Under U.S.C. § 112 ¶1

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 1 because the specification and original patent application fail to provide an enabling disclosure of and written description support for at least the following limitations:

- "a search stage for using said calculated distances to identify words within a lexical tree, the lexical tree comprising a model of words" (claim 1, 14)
- "using a search stage to identify words within a lexical tree using said calculated distances, the lexical tree comprising a model of words" (claim 15)
- "code for controlling the processor to identify words within a lexical tree using said calculated distances, the lexical tree comprising a model of words" (claim 16)
- "autonomously calculate" (claim 5)

2. Indefiniteness Under 35 U.S.C. § 112 ¶2

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 2 because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history. Additionally, certain claim language

below is indefinite under § 112 ¶ 2 due to mixing method and apparatus classes. *See IPXL*, 430 F.3d at 1384.

- “calculating distances indicating the similarity between a feature vector and a plurality of predetermined acoustic states of an acoustic model” (claim 1)
- “using said calculated distances to identify words within a lexical tree” (claims 1, 14)
- “wherein said audio front end and said search stage are implemented using a first processor, and said calculating circuit is implemented using a second processor” (claim 1)
- “A speech recognition circuit as claimed in claim 1, wherein the first processor supports multi-threaded operation, and runs the search stage and front ends as separate threads.” (claim 4)
- “front ends” (claim 4)
- “the said calculating circuit is configured to autonomously calculate distances for every acoustic state defined by the acoustic model” (claim 5)
- “the speech accelerator” (claim 9)
- “the accelerator” (claim 10)
- “the accelerator signals to the search stage when the distances for a new frame are available in a result memory” (claim 10)
- “A non-transitory storage medium storing processor implementable code . . . wherein data is pipelined by the processor” (claim 16)

V. '319 PATENT

A. Prior Art References

Apple identifies the following prior art now known to Apple to anticipate or render obvious the Asserted Claims of the '319 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, either expressly or inherently as understood by a POSITA.

1. Prior Art Publications

- T. S. Anantharaman and R. Bisiani. A Hardware Accelerator for Speech Recognition Algorithms, SIGARCH Comput. Archit. News 14, 2, 216–223 (May 1986) (“Anantharaman”). *See* Ex. B-01.

- U.S. Patent No. 5,459,798 (“Bailey”). *See* Ex. B-02.
- U.S. Patent No. 6,374,219 (“Jiang”). *See* Ex. B-03.
- U.S. Patent No. 6,526,380 (“Thelen”). *See* Ex. B-04.
- J.M. Fernandez et al., *A Flexible VLSI-Based Hardware System for Medium-Large-Vocabulary Real-Time Speech Recognition* (1994) (“Fernandez”). *See* Ex. B-07.
- Hsiao-Wuen Hon, *A Survey of Hardware Architectures Designed for Speech Recognition* (Aug. 9, 1991) (“Hon”). *See* Ex. B-08.
- Int’l. Patent Pub. No. WO2000/060577 (“Lund”). *See* Ex. B-09.
- S. Melnikoff et al., *Performing Speech Recognition on Multiple Parallel Files Using Continuous Hidden Markov Models on an FPGA* (“Melnikoff II”). *See* Ex. B-10.
- P. Stogiannos et al., *A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition Using Hidden Markov Models*, *Journal of VLSI Signal Processing Systems* (2000) (“Stogiannos”). *See* Ex. B-11.
- “Telecommunications Applications with the TMS320C5x DSPs,” Texas Instruments Inc. (1994) (“TMS320C”). *See* Ex. B-12.
- U.S. Patent No. 6,070,140 (“Tran”). *See* Ex. B-13.
- F.L. Vargas et al., *A FPGA-based Viterbi Algorithm Implementation for Speech Recognition Systems* (“Vargas”). *See* Ex. B-14.

Apple additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below. Apple’s investigation into prior art patent and publication references remains ongoing, and Apple reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Apple reserves the right to supplement as further prior art is identified through investigation or discovery.

2. Prior Art Systems

The following systems are prior art to the Asserted Claims of the ’319 patent under at least 35 U.S.C. §§ 102(a), (b) and/or (g), because they were either (1) in public use or on sale in

the United States no later than the priority date of the Asserted Claims or (2) reduced to practice in the United States no later than the priority date of the Asserted Claims without being abandoned, suppressed, or concealed. Apple also identifies and relies on prior art systems discussed in the prior art publications listed in the preceding section. Apple reserves the right to rely on other sources of evidence identified as discovery and Apple's investigation progresses.

- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to SPHINX-II. *See* Ex. B-05.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Texas Instruments TMS320C System ("TMS320C System"). *See* Ex. B-15.

3. Obviousness Prior Art

A POSITA would have known that any of the references identified above would have rendered the Asserted Claims obvious, alone or in combination. Additionally, Apple identifies the following prior art now known to Apple that, in combination with the foregoing patents, publications, and systems, render obvious the Asserted claims under 35 U.S.C. § 103, either expressly or inherently as understood by a POSITA, for at least the reasons stated in Section III.C. An invalidity claim chart for these prior art obviousness references is provided in Exhibit B-06.

- U.S. Patent No. 5,428,803 ("Chen")
- Rajeev Dujari, *Parallel Viterbi Speech Algorithm for Speech Recognition* (Feb. 1992) ("Dujari")
- U.S. Patent No. 6,076,056 ("Huang")
- U.S. Patent Application Publication No. US 2001/0053974 A1 ("Lucke")
- Mosur K. Ravishankar, *Efficient Algorithms for Speech Recognition* (May 15, 1996) ("Ravishankar").
- U.S. Patent No. 5,983,180 ("Robinson").

B. The Asserted Claims Would Have Been Obvious in View of the Prior Art

To the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. Nevertheless, Apple provides the following examples of how and why a POSITA would have combined the references above.

The '319 Patent claims a speech recognition circuit utilizing clustered processors to perform speech recognition using an acoustic model stored in memory. '319 Patent, 1:4-6, 4:53-5:13, Fig. 2. The claimed circuit comprises a plurality of processors connected in parallel to an input buffer, wherein the plurality of processors are controlled by a control processor and access a plurality of lexical memories. '319 Patent, 3:8-16, 3:29-43. Independent claim 46 generally recites five elements: an input buffer, a plurality of lexical memories, a plurality of grouped processors, a control processor, and a results memory.

Thelen teaches a speech recognition circuit that uses a plurality of processors, controlled by a controller 350, to recognize analyzed incoming speech using a plurality of recognition models, wherein each of the "recognition models" is targeted to a "specific part of the huge vocabulary" of the system. Thelen, 1:53-2:16, 7:30-49. Each of Thelen's recognition models are described as "having [its] own processing resources," such as separate processors or processing units in a parallel operating processor. Thelen, 2:30-33, 7:17-23. Moreover, Thelen teaches that each recognition model is characterized by a Hidden Markov Model (HMM) generated from training data. Thelen, 5:29-42. Thelen also teaches a language model processor for use in

recognizing words and groups of words.

Bailey teaches a similar speech recognition circuit that leverages a plurality of pattern recognition engine processors 525a-c, each operating in parallel using its own private memory, to process incoming speech from an input buffer and store the results in a results memory. *See* Bailey, 10:18-11:37, Fig. 3A; 3:60-4:1, 42:54-57, 43:7-47. A POSITA would have recognized that input buffers like those disclosed in Bailey were well-known and widely used prior to the '319 Patent as a simple, operable structure for providing a data signal from one component of a circuit (in this case, Thelen's spectral analysis subsystem 110) to another (Thelen's plurality of processors), leading to a reasonable expectation of success for combining the teachings of Thelen and Bailey.

Moreover, storing the recognition models of Thelen in memories 615a-c of Bailey teaches "a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data." A POSITA would have recognized Bailey's memory architecture would have combined naturally with the plurality of parallel "recognition engines" taught by Thelen and furthered its expressly-stated goal of operating in "real-time." Thelen, 2:30-37, 7:26-29.

In related art, Chen teaches a "parallel processing architecture for connecting together an extendible number of clusters of multiple numbers of processors to create a high performance parallel processing computer system." Chen, 5:9-13.

The speech recognition circuit of Thelen+Bailey modified to utilize Chen's architecture of a plurality of grouped processors renders obvious every limitation of the Asserted Claims of the '319 patent. For example, processors of PR 525a-c taught by Bailey process speech parameters using recognition models comprising lexical data as taught by Thelen stored in said

lexical memories 615a-c (modified, pursuant to Chen, to each be shared cluster memories 104a-d of the groups of clustered processors).

A POSITA would have found it obvious and been motivated to combine Chen's cluster of processors with shared memory with Thelen+Bailey's speech recognition circuit to improve speech recognition performance. Prior to the priority date of the '319 Patent, connecting a plurality of processors in parallel was a well-known technique to increase the processing power available to a computing circuit while without becoming extremely expensive. It was also well-known that speech recognition was a computationally-intensive task. Well before the priority date of the '319 Patent, clusters of processors were used to recognize speech. Combining Chen's cluster of processors with Thelen and Bailey's speech recognition circuitry would have been the use of a known technique to improve a similar device in the same way.

In related art, Huang teaches a "conventional technique for further reducing the magnitude of computation required for speech recognition" using a prefix tree that "represents the lexicon of the speech recognition system as a tree structure wherein all of the words likely to be encountered by the system are represented in the tree structure." Huang, 2:31-37. Thus, Huang's "lexicon of all words" organized in a "prefix tree" teaches lexical data stored as at least one "lexical tree data structure" comprising a "model of words." Huang, 2:31-58.

A POSITA would have been motivated by Huang's express statement of "reducing the magnitude of computation required for speech recognition" to modify Thelen's HMM lexicon 134 into a lexical tree data structure, requiring only reprogramming of data stored in memory, performable by a POSITA without undue experimentation. Storing lexical data in a lexical tree data structure was a well-known prior to the '319 Patent of improving computational efficiency in an HMM searching speech recognition circuit.

Huang also teaches building a monophone model of words during a training phase, which are represented in the lexical tree data structures stored in lexical memory and subsequently used for speech recognition. Huang, 7:15-54, 8:16-20, 11:64-12:46. A POSITA would have been motivated to store the lexical tree data structure as a monophone (an “n phone”) model of words to minimize the amount memory required for storing the trees. Furthermore, Huang teaches context dependent phone models of words.

In related art, Jiang teaches a speech recognition circuit using an HMM acoustic model to generate a score for an audio sample, used to determine a most likely word or set of words. A POSITA would have found it obvious and been motivated to combine Chen’s cluster of processors with shared memory with Jiang’s speech recognition circuit. The combination of the disclosures of Jiang and Chen would have constituted use of a known technique (e.g., Chen’s clustering of processors with memory) to improve a similar device (Jiang’s multiprocessor speech recognition circuit) in the same way.

The above descriptions of possible combinations are exemplary and not limiting. It would have been obvious to combine any of the references that teach the individual limitations of the ’319 patent following a similar analysis.

C. Invalidity Under 35 U.S.C. § 101

The Asserted Claims of the ’319 patent are directed to patent-ineligible subject matter under 35 U.S.C. § 101. Claim 46 of the ’319 patent (and all claims that depend from it) are directed to the abstract idea of processing data parameters. Courts have acknowledged that performing data processing, even limited to a particular field, is a patent-ineligible, abstract idea. *See, e.g., Elec. Power Grp. LLC v. Alston S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016).

The elements recited in the claims of the ’319 patent are well understood, routine, and conventional and thus do not provide an “inventive concept.” For example, buffer memory,

lexical data, parallel processing, control processors, and memory storing results were well understood, routine, and conventional at the time of the application for the '319 patent.

The elements recited in the dependent claims were also well understood, routine, and conventional. These elements include, without limitation: lexical trees, feature vectors, n phone models of words, mono phone models of words, word recognition, language model processing, word scoring, comparisons between speech parameters and lexical data, pipelining, pruning, input buffering, Hidden Markov Models, and the Viterbi search algorithm.

The specification of the '319 patent (and the references cited therein) support the contention that the elements discussed in the preceding paragraphs were well understood, routine, and conventional. Apple incorporates by reference the prior art cited in the Ex. B charts, which provide further evidence that the above elements were well understood, routine, and conventional.

D. Invalidity Under 35 U.S.C. § 112

1. Lack of Enablement and Written Description Under U.S.C. § 112 ¶1

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 1 because the specification and original patent application fail to provide an enabling disclosure of and written description support for at least the following limitations:

- “a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data” (claim 46)
- “each lexical memory stores lexical data as at least one lexical tree data structure, each lexical tree data structure comprises a model of words having common prefix components, and an initial component of each lexical tree data structure is unique” (claim 47)

- “each lexical memory stores said lexical tree data structure as an n phone model of words, where n is an integer, and said components comprise n phones” (claim 48)
- “each lexical memory stores said lexical tree data structure as a mono phone model of words, and said lexical tree processors use said mono phone models to generate context dependant phone models of words dynamically for use in processing the speech parameters” (claim 49)
- “modifying the processing results at a word recognition event” (claim 51)

2. Indefiniteness Under 35 U.S.C. § 112 ¶2

Based on Apple’s present understanding of the Asserted Claims and Zentian’s apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 2 because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history. Additionally, certain claim language below is indefinite under § 112 ¶ 2 due to mixing method and apparatus classes. *See IPXL*, 430 F.3d at 1384.

- “an input buffer receiving processed speech parameters” (claim 46)
- “a plurality of lexical memories containing in combination complete lexical data” (claim 46)
- “complete lexical data for word recognition” (claim 46)
- “a control processor controlling each processor to process said speech parameters using partial lexical data read from a respective said lexical memory” (claim 46)
- “a results memory storing the results” (claim 46)
- “a including language model processor” (claim 51)
- “a said processor” (claim 51)
- “modifying the processing results at a word recognition event” (claim 51)

VI. '140 PATENT

A. Prior Art References

Apple identifies the following prior art now known to Apple to anticipate or render obvious the Asserted Claims of the '140 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, either expressly or inherently as understood by a POSITA.

1. Prior Art Publications

- T. S. Anantharaman and R. Bisiani. A Hardware Accelerator for Speech Recognition Algorithms, SIGARCH Comput. Archit. News 14, 2, 216–223 (May 1986) (“Anantharaman”). *See* Ex. C-01.
- U.S. Patent No. 6,374,219 (“Jiang”). *See* Ex. C-02.
- Georges Quenot et al., *A Dynamic Time Warp VLSI Processor for Continuous Speech Recognition*, ICASSP '86. IEEE International Conference on Acoustics, Speech, and Signal Processing, 1549-1552 (1986) (“Quenot”). *See* Ex. C-03.
- U.S. Patent No. 5,983,180 (“Robinson”). *See* Ex. C-04.
- U.S. Patent No. 5,036,539 (“Wrench”). *See* Ex. C-05.
- S. Yoshizawa et al., *A Low-Power VLSI Design of an HMM Based Speech Recognition System*, The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002, II-489-92 (2002) (“Yoshizawa 1”). *See* Ex. C-06.
- Int'l. Patent Pub. No. WO2000/060577 (“Lund”). *See* Ex. C-09.
- “Telecommunications Applications with the TMS320C5x DSPs,” Texas Instruments Inc. (1994) (“TMS320C”). *See* Ex. C-10.
- U.S. Patent No. 6,070,140 (“Tran”). *See* Ex. C-11.
- A FPGA-based Viterbi Algorithm Implementation for Speech Recognition Systems (“Vargas”). *See* Ex. C-12.
- U.S. Patent No. 6,292,779 (“Wilson”). *See* Ex. C-13.

Apple additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below. Apple's investigation into prior art patent and publication references remains ongoing, and Apple reserves the right to identify

and rely on additional patent or publication references that are identified through further investigation or discovery. Apple reserves the right to supplement as further prior art is identified through investigation or discovery.

2. Prior Art Systems

The following systems are prior art to the Asserted Claims of the '140 patent under at least 35 U.S.C. §§ 102(a), (b) and/or (g), because they were either (1) in public use or on sale in the United States no later than the priority date of the Asserted Claims or (2) reduced to practice in the United States no later than the priority date of the Asserted Claims without being abandoned, suppressed, or concealed. Apple also identifies and relies on prior art systems discussed in the prior art publications listed in the preceding section. Apple reserves the right to rely on other sources of evidence identified as discovery and Apple's investigation progresses.

- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to SPHINX-II. *See* Ex. C-07.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Texas Instruments TMS320C System ("TMS320C System"). *See* Ex. C-14.

3. Obviousness Prior Art

A POSITA would have known that any of the references identified above would have rendered the Asserted Claims obvious, alone or in combination. Additionally, Apple identifies the following prior art now known to Apple that, in combination with the foregoing patents, publications, and systems, render obvious the Asserted claims under 35 U.S.C. § 103, either expressly or inherently as understood by a POSITA, for at least the reasons stated in Section III.C. An invalidity claim chart for these prior art obviousness references is provided in Exhibit C-08.

- U.S. Patent No. 5,428,803 ("Chen")

- US Appl. No. 2001/0053974 (“Lucke”)
- U.S. Patent No. 6,526,380 (“Thelen”)

B. The Asserted Claims Would Have Been Obvious in View of the Prior Art

To the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. Nevertheless, Apple provides the following examples of how and why a POSITA would have combined the references above.

The ’140 Patent claims a speech recognition circuit utilizing clustered processors to perform speech recognition using an acoustic model stored in memory. ’140 Patent, 1:18-20, 5:6-29, Fig. 2. The claimed circuit generates an initial score for an audio sample, used to determine which possible word determinations should be “pruned” from its search. ’140 Patent, 6:21-35, 8:59-9:4.

Jiang and Chen are analogous art to the ’140 Patent, and a POSITA would have been familiar with both references. A POSITA would have found it obvious and been motivated to combine Chen’s cluster of processors with shared memory with Jiang’s speech recognition circuit using an HMM acoustic model to generate scores, as taught by Jiang. Computing platforms providing processors in a cluster was extremely well-known in the art prior to the ’140 Patent, as taught by Chen and numerous other references. Prior to the priority date of the ’140 Patent, connecting a plurality of processors in parallel was a well-known technique to increase the processing power available to a computing circuit without becoming expensive to produce. It was

also well-known that speech recognition was a computationally-intensive task, requiring expensive, sophisticated processors (for the time) if performed in real-time on a solitary, single-core processor. Well before the priority date of the '140 Patent, clusters of processors were used to recognize speech.

The combination of the disclosures of Jiang and Chen would have constituted use of a known technique (e.g., Chen's clustering of processors with memory) to improve a similar device (Jiang's multiprocessor speech recognition circuit) in the same way. A POSITA would have recognized utilizing a clustered processor architecture with shared memory would have enabled the speech recognition circuit to efficiently process branches of the lexical tree in parallel. A POSITA would have understood a cluster of processors, as described in Chen, was usable and desirable in a speech recognition system with multiple processors, such as Jiang's circuit, and would have been a low-cost, simple-to-implement improvement. Specifically, a POSITA would have recognized that the increased computing resources provided by Chen's cluster of processors would have increased the speed of the system, enabling a reduced cost system that recognized speech at a faster rate and/or higher level of accuracy.

There would have been a reasonable expectation of success for adding Chen's clusters to Jiang's system because Chen and Jiang each contemplates a hardware architecture using multiple, vector-based signal processors; therefore, the more efficient processing architecture of Chen would have been simply substituted for Jiang's architecture to achieve a compatible improvement in processing speed and power. Given the ubiquitous use of pluralities of processors in speech recognition circuits, a POSITA would have had a reasonable expectation of success, without undue experimentation, in modifying Jiang's circuit to use Chen's clusters of processors.

A POSITA, having read the disclosure of Lucke, would have recognized that the circuit taught by Jiang in view of Chen, which is already expressly configured to cease processing particular branches of a lexical tree based on a low initial score, would have appropriately been configured to continue processing for branches of the lexical tree having a sufficiently high initial score. Lucke, 0027-0029, 0081-0082. Such a functionality would have been the natural, expected algorithm for lexical tree-based speech recognition systems of the time performing pruning. A POSITA would have recognized that processing would need to continue for branches with a sufficiently high score for the system to determine a final speech recognition result, leading to a reasonable expectation of success for the combination of Jiang, Chen, and Lucke. *Id.*

A POSITA, having read Robinson, would have been motivated to perform the feature vector probability computations already taught by Jiang using the Gaussian mixture model technique taught by Robinson to improve the similar circuit of Jiang+Chen in the same way. Gaussian mixture models were one of “several parametric models used to approximate” the probability computation known at the time of the ’140 Patent, and thus would have been obvious for a POSITA to try. Using the Gaussian mixture model would have only required programming hardware already present in the circuit of Jiang+Chen that would have been within the skill of a POSITA without undue experimentation, leading to a reasonable likelihood of success for the combination.

Wrench, a similar multiprocessor speech recognition circuit, teaches initiating speech recognition processing in at least a subset of processors via a search controller via its “master processor,” which acts as an executive to its plurality of speech recognition processors. Wrench, 4:40-58, 5:6-24, 6:38-7:32, Fig. 2. The master processor’s software includes an “initialization” program module that “performs the various tasks initializing the [speech recognition subsystem]

parameters.” Wrench, 6:40-50, 2:44-58. A POSITA would have recognized, therefore, that Wrench’s master processor teaches a controller coupled to a plurality of processors that “initiates speech recognition processing in at least a subset of processors,” as claimed.

The above descriptions of possible combinations are exemplary and not limiting. It would have been obvious to combine any of the references that teach the individual limitations of the ’140 patent following a similar analysis.

C. Invalidity Under 35 U.S.C. § 101

The Asserted Claims of the ’140 patent are directed to patent-ineligible subject matter under 35 U.S.C. § 101. Claim 1 of the ’140 patent (and all claims that depend from claim 1) are directed to the abstract idea of computing a probability. Courts have acknowledged that performing computations such as statistics is a patent-ineligible, abstract idea. *See, e.g., OIP Technologies, Inc. v. Amazon.com, Inc.*, 788 F.3d 1359, 1363-64 (Fed. Cir. 2015). Moreover, claim 1 of the ’140 patent does not even specify what sort of probability is being calculated.

The elements recited in the claims of the ’140 patent are well understood, routine, and conventional and thus do not provide an “inventive concept.” For example, clusters of processors, acoustic models, memory, and pruning (i.e., using scoring to determine whether to continue processing audio data) well understood, routine, and conventional at the time of the application for the ’140 patent. The arguments Zentian made in prosecution to avoid a written description rejection for claim 1 support this position.

The elements recited in the dependent claims were also well understood, routine, and conventional. These elements include, without limitation:

- state transitions to a model of states,
- Hidden Markov Models,

- Gaussian mixture models,
- feature vectors,
- buffers, and
- control mechanisms for other processors.

The specification of the '140 patent (and the references cited therein) support the contention that the elements discussed in the preceding paragraphs were well understood, routine, and conventional. Apple incorporates by reference the prior art cited in the Ex. C charts, which provide further evidence that the above elements were well understood, routine, and conventional.

D. Invalidity Under 35 U.S.C. § 112

1. Lack of Enablement and Written Description Under U.S.C. § 112 ¶1

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 1 because the specification and original patent application fail to provide an enabling disclosure of and written description support for at least the following limitations:

- “the speech recognition circuit is configured to generate an initial score for an audio sample; and the initial score is used to determine whether to continue processing to determine a final score via processing a larger amount of model data than that was processed to generate the initial score”

2. Indefiniteness Under 35 U.S.C. § 112 ¶2

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 2 because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the

claims in light of the specification and prosecution history.

- “compute a probability using the acoustic model data” (claim 1)
- “A speech recognition circuit . . . wherein . . . the initial score is used” (claim 1)
- “model of states” (claim 2)

VII. ’377 PATENT

A. Prior Art References

Apple identifies the following prior art now known to Apple to anticipate or render obvious the Asserted Claims of the ’377 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, either expressly or inherently as understood by a POSITA.

1. Prior Art Publications

- U.S. Patent No. 5,699,456 (“Brown”). *See* Ex. D-01.
- U.S. Patent No. 6,374,219 (“Jiang”). *See* Ex. D-02.
- U.S. Patent No. 6,879,954 (“Nguyen”). *See* Ex. D-03.
- Mosur K. Ravishankar, *Efficient Algorithms for Speech Recognition* (May 15, 1996) (“Ravishankar”). *See* Ex. D-04.
- U.S. Patent No. 5,819,222 (“Smyth”). *See* Ex. D-05.
- U.S. Patent No. 6,490,559 (“Budde”). *See* Ex. D-08.
- CN1503220 (“Jiang 220”). *See* Ex. D-09.
- Jer Min Jou et al., *An Efficient VLSI Architecture for HMM-Based Speech Recognition* (2001) (“Jou”). *See* Ex. D-10.
- Int’l. Patent Pub. No. WO2000/060577 (“Lund”). *See* Ex. D-11.
- S. Melnikoff et al., *Speech Recognition on an FPGA Using Discrete and Continuous Hidden Markov Models*, 12th International Conference on Field Programmable Logic and Applications (2002) (“Melnikoff”). *See* Ex. D-12.
- S. Melnikoff et al., *Performing Speech Recognition on Multiple Parallel Files Using Continuous Hidden Markov Models on an FPGA* (“Melnikoff II”). *See* Ex. D-13.

- P. Stogiannos et al., A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition Using Hidden Markov Models, Journal of VLSI Signal Processing Systems (2000) (“Stogiannos”). *See* Ex. D-14.
- “Telecommunications Applications with the TMS320C5x DSPs,” Texas Instruments Inc. (1994) (“TMS320C”). *See* Ex. D-15.
- U.S. Patent No. 6,070,140 (“Tran”). *See* Ex. D-16.

Apple additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below. Apple’s investigation into prior art patent and publication references remains ongoing, and Apple reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Apple reserves the right to supplement as further prior art is identified through investigation or discovery.

2. Prior Art Systems

The following systems are prior art to the Asserted Claims of the ’377 patent under at least 35 U.S.C. §§ 102(a), (b) and/or (g), because they were either (1) in public use or on sale in the United States no later than the priority date of the Asserted Claims or (2) reduced to practice in the United States no later than the priority date of the Asserted Claims without being abandoned, suppressed, or concealed. Apple also identifies and relies on prior art systems discussed in the prior art publications listed in the preceding section. Apple reserves the right to rely on other sources of evidence identified as discovery and Apple’s investigation progresses.

- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to SPHINX-II. *See* Ex. D-06.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Texas Instruments TMS320C System (“TMS320C System”). *See* Ex. D-17.

3. Obviousness Prior Art

A POSITA would have known that any of the references identified above would have

rendered the Asserted Claims obvious, alone or in combination. Additionally, Apple identifies the following prior art now known to Apple that, in combination with the foregoing patents, publications, and systems, render obvious the Asserted claims under 35 U.S.C. § 103, either expressly or inherently as understood by a POSITA, for at least the reasons stated in Section III.C. An invalidity claim chart for these prior art obviousness references is provided in Exhibit D-07.

- U.S. Patent App. No. 2002/0049582 (“Baumgartner”)
- U.S. Patent No. 6,959,376 (“Boike”)
- U.S. Patent No. 6,374,219 (“Jiang”)
- U.S. Patent No. 5,819,222 (“Smyth”)

B. The Asserted Claims Would Have Been Obvious in View of the Prior Art

To the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. Nevertheless, Apple provides the following examples of how and why a POSITA would have combined the references above.

The '377 patent generally claims a speech recognition system that uses multiple programmable devices to perform different calculations in the recognition process. '377 patent, 5:63–6:6, 6:20-33. These steps include feature extraction, distance calculations, and search.

As discussed in the attached claim charts, Jiang alone or in combination with Smyth

teaches or renders obvious calculating feature vectors from a digital audio stream, calculating distances between a feature vector and states in an acoustic model, and identifying words in a digital audio stream, as claimed. The figures of Jiang do not expressly show the functionalities of the claimed feature vector extraction, distance calculation, and search implemented using three separate programmable devices as recited in claim 1 of the '377 patent. Smyth, however, teaches using separate processors to perform feature extraction, distance calculation, and search.

A POSITA would have found it obvious and been motivated to modify Jiang's tree search engine 74 to include a second processor, as taught by Smyth, or to otherwise perform Jiang's distance calculation using a processor distinct from the tree search engine's processor. In the modified Jiang, the speech recognition system includes a processor programmed to perform the distance calculation taught by Jiang, in addition to Jiang's tree search engine 74 programmed to perform word identification.

Jiang already teaches that its invention "may be practiced with other computer system configurations," including "microprocessor-based or programmable consumer electronics." Jiang notes its CPU 21, which includes tree search engine, "may include one or more processors." Jiang, 6:39-42. In fact, Jiang refers to distinct processors for performing distinct speech recognition functionality repeatedly, indicating to a POSITA that Jiang envisions dedicated processors for performing specific speech recognition functionality. *See, e.g.*, Jiang, 6:53-57 (stating feature extraction module 66 is a "conventional array processor"), 7:19-21 (stating silence detection module 68 "can either be implemented on the same, or a different processor as that used to implement the feature extraction module 66").

Both Jiang and Baumgartner also teach that calculating the distances or probability is a computationally-intensive processing task. Jiang, 2:19-24; Baumgartner, [0003], [0005], [0007].

By modifying Jiang's tree search engine to comprise two dedicated processors, e.g., DSPs, with one processor/DSP performing the computationally-intensive distance calculation, the overall speech recognition process achieves both accuracy and speed.

Jiang suggests to a POSITA that the hardware and software architecture and configuration for performing the described functionality is amenable to design and use considerations. Jiang, 4:60–5:3. Jiang discusses that “those skilled in the art will appreciate that the invention may be practiced with other computer system configurations.” By employing distinct processors, including microprocessors such as DSPs as taught by Smyth, to perform the various speech recognition steps, each DSP can be a dedicated processor, as urged by Jiang. Jiang, 6:39-42. Providing discrete processors for feature extraction, distance calculation, and searching allows for segmentation of higher-load processing. The result of distinct processors is a faster, more efficient, and more accurate speech recognition process, which is a goal of speech recognition.. Although modifying Jiang to include three processors instead of two processors (66 and 74) arguably adds cost, Jiang's own teachings discussing the multiplicity of possible computer configuration indicates to a POSITA that Jiang is not concerned with cost alone. Moreover, the cost for a separate DSP or processor for performing distance calculation would be minimal relative to the efficiency and accuracy gain. *Id.*

In the modified Jiang, the processor 341 of Smyth is added to the Jiang speech recognition system to perform Jiang's distance calculation. As the Jiang prefix tree is traversed, the tree search engine receives scores otherwise computed by the added processor for distance calculation. This relieves the tree search engine (to the extent it is a single processor) from performing both the distance calculation and tree search for word identification. Instead, the tree search engine's processor need only receive the computed scores for each node associated with a

phoneme branch, leaving the tree search engine's processor to perform the word identification.

Moreover, to the extent not already taught or rendered obvious in the Jiang-Smyth combination, it would have been obvious to modify Jiang's extractor 66 and tree search engine 74 to comprise DSPs, as taught by Smyth, such that the Jiang speech recognition system comprised three separate distinct DSPs for performing the respective functionality of feature vector extraction, distance calculation (i.e., computing probability scores of phonemes in an HMM), and word search identification.

Modifying Jiang to include DSPs for performing the disclosed functionality would have been met with a reasonable expectation of success, given that DSPs for performing speech recognition, such as the Motorola DSP56000 and others, were known and allowed for "higher integration." Moreover, incorporation of multiple DSPs for performing specific functionality of speech recognition would have yielded the predictable result of flexibility in design and integration with other devices, such as Jiang's consumer electronics. *Id.* For example, a DSP is well suited for the mathematical computations required in computing a probability or score that a given HMM produced a given observed feature vector, as taught by Jiang.

The above descriptions of possible combinations are exemplary and not limiting. It would have been obvious to combine any of the references that teach the individual limitations of the '377 patent following a similar analysis.

C. Invalidity Under 35 U.S.C. § 101

The Asserted Claims of the '377 patent are directed to patent-ineligible subject matter under 35 U.S.C. § 101. Claim 1 of the '377 patent (and all claims that depend from it) are directed to the abstract idea of calculating data (e.g., feature vectors and distances) and using that data in a known field. Courts have acknowledged that performing calculations such as statistics is a patent-ineligible, abstract idea. *See, e.g., OIP Technologies, Inc. v. Amazon.com, Inc.*, 788

F.3d 1359, 1363-64 (Fed. Cir. 2015).

The elements recited in the claims of the '377 patent are well understood, routine, and conventional and thus do not provide an “inventive concept.” For example, feature vectors from digital audio, distance calculations with acoustic models, word searches and identification, Hidden Markov Models, neural networks, and lexical trees were all well understood, routine, and conventional at the time of the application for the '377 patent.

The elements recited in the dependent claims were also well understood, routine, and conventional. These elements include, without limitation, pipelining speech recognition tasks, uni-processing, multiprocessing, and placing distinct circuits on a single integrated circuit.

The specification of the '377 patent (and the references cited therein) support the contention that the elements discussed in the preceding paragraphs were well understood, routine, and conventional. Apple incorporates by reference the prior art cited in the Ex. D charts, which provide further evidence that the above elements were well understood, routine, and conventional.

D. Invalidity Under 35 U.S.C. § 112

1. Lack of Enablement and Written Description Under U.S.C. § 112 ¶1

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 1 because the specification and original patent application fail to provide an enabling disclosure of and written description support for at least the following limitations:

- “a search stage for using the calculated distances to identify words within a lexical tree, the lexical tree comprising a model of words” (claim 1)
- “physically distinct processing circuit[s]” (claims 3-5)

2. Indefiniteness Under 35 U.S.C. § 112 ¶2

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 2 because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history.

- “a second programmable device programmed to calculate distances indicating the similarity between a feature vector and a plurality of acoustic states of an acoustic model” (claim 1)
- “the time period taken for identification of spoken words” (claim 2)
- “the time period taken for said second programmable device to calculate one or more distances” (claim 2)
- “physically distinct processing circuit[s]” (claims 3-5)
- “one physical uni-processor or multi-processor” (claims 5-6)

VIII. '789 PATENT

A. Prior Art References

Apple identifies the following prior art now known to Apple to anticipate or render obvious the Asserted Claims of the '789 patent under at least 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, either expressly or inherently as understood by a POSITA.

1. Prior Art Publications

- U.S. Patent No. 6,629,073 (“Hon”). *See* Ex. E-01.
- H. Ishizuka et al., *A Microprocessor for Speech Recognition*, ICASSP '83. IEEE International Conference on Acoustics, Speech, and Signal Processing, 503-506 (1983) (“Ishizuka”). *See* Ex. E-02.
- Binu K. Matthew et al., *A Gaussian Probability Accelerator for Sphinx 3* (July 22, 2003) (“Mathew 2”). *See* Ex. E-03.
- U.S. Patent No. 6,832,194 (“Mozer”). *See* Ex. E-04.

- U.S. Patent No. 6,879,954 (“Nguyen”). *See* Ex. E-05.
- U.S. Patent No. 6,230,128 (“Smyth”). *See* Ex. E-06.
- U.S. Patent App. No. 2004/039573 (“Vasilache”). *See* Ex. E-07.
- U.S. Patent No. 6,490,559 (“Budde”). *See* Ex. E-10.
- CN1503220 (“Jiang 220”). *See* Ex. E-11.
- R. Krishna et al., Architectural Optimizations for LowPower, RealTime Speech Recognition (“Krishna”). *See* Ex. E-12
- Int’l. Patent Pub. No. WO2000/060577 (“Lund”). *See* Ex. E-13.
- Binu Mathew et al., *A Low-Power Accelerator for the SPHINX 3 Speech Recognition System*, Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES 2003, 210-19 (Oct. 30, 2003) (“Mathew”). *See* Ex. E-14.
- S. Melnikoff et al., Speech Recognition on an FPGA Using Discrete and Continuous Hidden Markov Models, 12th International Conference on Field Programmable Logic and Applications (2002) (“Melnikoff”). *See* Ex. E-15.
- S. Melnikoff et al., Performing Speech Recognition on Multiple Parallel Files Using Continuous Hidden Markov Models on an FPGA (“Melnikoff II”). *See* Ex. E-16.
- A VLSI Implementation of Pdf Computations in HMM Based Speech Recognition by Pihl et al. (“Pihl”). *See* Ex. E-17.
- P. Stogiannos et al., A Configurable Logic Based Architecture for Real-Time Continuous Speech Recognition Using Hidden Markov Models, Journal of VLSI Signal Processing Systems (2000) (“Stogiannos”). *See* Ex. E-18.
- “Telecommunications Applications with the TMS320C5x DSPs,” Texas Instruments Inc. (1994) (“TMS320C”). *See* Ex. E-19.
- U.S. Patent No. 6,070,140 (“Tran”). *See* Ex. E-20.
- S. Yoshizawa et al., *A Low-Power VLSI Design of an HMM Based Speech Recognition System*, The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002, II-489-92 (2002) (“Yoshizawa I”). *See* Ex. E-21.
- S. Yoshizawa et al., A High-Speed HMM VLSI module with block parallel processing (“Yoshizawa II”). *See* Ex. E-22.

Apple additionally identifies and relies on patent or publication references that describe

or are otherwise related to the prior art systems identified below. Apple's investigation into prior art patent and publication references remains ongoing, and Apple reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Apple reserves the right to supplement as further prior art is identified through investigation or discovery.

2. Prior Art Systems

The following systems are prior art to the Asserted Claims of the '789 patent under at least 35 U.S.C. §§ 102(a), (b) and/or (g), because they were either (1) in public use or on sale in the United States no later than the priority date of the Asserted Claims or (2) reduced to practice in the United States no later than the priority date of the Asserted Claims without being abandoned, suppressed, or concealed. Apple also identifies and relies on prior art systems discussed in the prior art publications listed in the preceding section. Apple reserves the right to rely on other sources of evidence identified as discovery and Apple's investigation progresses.

- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the OKI MSM6679 Voice Recognition Processor. *See* Ex. E-08.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to SPHINX-II. *See* Ex. E-09.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Sensory RSC family of microcontrollers (RSC-164, RSC-200/264T, RSC-300/364) *See* Ex. E-09.
- Products, components, systems, and methods invented, designed, developed, reduced to practice, and/or in public use or on sale related to the Texas Instruments TMS320C System ("TMS320C System"). *See* Ex. E-23.

3. Obviousness Prior Art

A POSITA would have known that any of the references identified above would have rendered the Asserted Claims obvious, alone or in combination. Additionally, Apple identifies

the following prior art now known to Apple that, in combination with the foregoing patents, publications, and systems, render obvious the Asserted claims under 35 U.S.C. § 103, either expressly or inherently as understood by a POSITA, for at least the reasons stated in Section III.C. An invalidity claim chart for these prior art obviousness references is provided in Exhibit E-09.

- U.S. Patent No. 5,774,859 (“Houser”)
- U.S. Patent No. 4,567,606 (“Vensko”)
- U.S. Patent App. Pub. 2002/0091826 (“Comeau”)
- U.S. Patent No. 6,959,376 (“Boike”)
- U.S. Patent No. 7,171,358 (“Whittaker”)
- U.S. Patent No. 7,478,041 (“Ichikawa”)
- U.S. Patent No. 7,587,318 (“Seshadri”)
- U.S. Patent App. Pub. 2003/0012347 (“Steinbiss”)
- SPHINX-II System
- Sensory RSC family of microcontrollers (RSC-164, RSC-200/264T, RSC-300/364)

B. The Asserted Claims Would Have Been Obvious in View of the Prior Art

To the extent one or more of the references do not explicitly or inherently disclose any claim limitation, that reference combined with one or more other primary references or obviousness references would have rendered the Asserted Claims obvious.

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. Nevertheless, Apple provides the following examples of how and why a POSITA

would have combined the references above.

The claims of the '789 patent recite an acoustic coprocessor containing a “calculating apparatus” for calculating distances between a feature vector and acoustic states of an acoustic model, along with a first interface for receiving the feature vector and a second interface for providing the calculated distances as output. Some of the dependent claims further recite a CPU that executes software to perform a speech recognition word search. Other dependent claims recite well known electronic hardware such as a processor, a serial bus, and different types of memory, among other things.

As discussed in the attached claim charts, Smyth alone or in combination with Mozer teaches or renders obvious the claimed “calculating apparatus,” acoustic model memory, first and second interfaces, and result memory limitations, among others. Mozer teaches a single integrated circuit on which a vector processor 423 (i.e., calculating apparatus) and memory 460 (i.e., acoustic model memory) are fabricated. Mozer, 7:53-58. A POSITA would have been motivated and found it obvious to modify Smyth to fabricate classifying processor 341 and state memory 342 of classifier 34 on a single integrated circuit according to Mozer’s teachings. Indeed, Mozer itself teaches that providing a recognition peripheral system on one integrated circuit provides advantages. Mozer, 9:16-18 (“However, the embodiments described herein are illustrative of the advantages of providing a recognition peripheral system on one integrated circuit[.]”). For example, Mozer teaches “embodiments of the present invention have the advantage of allowing the system designer to offload burdensome vector processing operations associated with audio recognition from the programmable processing unit to the audio recognition peripheral during the execution of the audio recognition algorithm.” Mozer, 10:46-52. A POSITA would have understood and found obvious that when modifying Smyth

according to Mozer's teachings to fabricate a calculating apparatus and acoustic model memory on a single integrated circuit, the modified Smyth would have likewise captured such advantages. Among other things, Mozer also teaches the use of a serial bus to transfer information, using a neural network to calculate distances, and an acoustic model memory with a plurality of storage locations within an SRAM, as claimed.

Nguyen teaches additional details regarding distance calculations with an acoustic model. Among other things, Nguyen teaches utilizing an acoustic model for which Gaussian data serves as the basis of said acoustic model. Nguyen teaches that each "Hidden Markov Model includes a collection of probabilities associated with the states themselves and transition amongst the states. Because probability values associated with each state may be more complex than a single value could represent, some systems will represent probability in terms of a Gaussian distribution." Nguyen, 2:49-54. A POSITA would have found it obvious and been motivated to modify Smyth's acoustic model to represent probability in terms of a Gaussian distribution as taught by Nguyen. Nguyen provides express motivations, including "probability values associated with each state may be more complex than a single value could represent," and to "provide a more robust model[.]" Nguyen, 2:49-67. A POSITA would have been motivated to modify Smyth to capture such advantages.

Nguyen also teaches a system including a CPU in which a time period for the speech recognition word search overlaps a time period for the acoustic coprocessor to calculate the distance in response to receiving the second feature vector. A POSITA would have found it obvious and been motivated to modify Smyth's speech recognition system to operate using the contemporaneous processing taught in Nguyen. Nguyen teaches performing the similarity computation (i.e., the distance calculation) for a group of acoustic feature vectors reduces the

number of I/O operations required to load and unload each acoustic model. Nguyen, 3:57-60; A POSITA also would have been motivated to modify Smyth's multiple processors/DSPs to use Nguyen's contemporaneous distance calculation step and searching step to advantageously increase system performance. Smyth itself teaches an embodiment with one DSP for performing distance calculations (i.e., classifying processor 341 implemented as a DSP) and another processor/DSP for performing speech recognition (i.e., parsing processor 351).

Other limitations of the '789 patent recite well known electronic hardware. For example, it should have been obvious to utilize flash memory to store acoustic model data as taught in Houser. It also would have been obvious to generate an interrupt in response to a completion of calculation of a set of distances as taught in Vensko. *See Vensko*, 6:29-33, 10:10-19. Using Vensko's teachings would have advantageously allowed Smyth's acoustic coprocessor to be capable of generating an interrupt to inform sequencer 35 that calculation of a set of distances is completed. Vensko also teaches a DMA controller to transfer data between processors. A POSITA would have been motivated and found it obvious to modify Smyth to include a DMA controller for copying distances from a result memory to a buffer memory. Indeed, it was well known in the art that DMA controllers were used to access and copy data from one memory to another, with Vensko as one example. Moreover, a POSITA would have understood that a DMA controller would have been capable of copying distances in a plurality of sequential bursts.

Comeau teaches a coprocessor capable of setting one or more bits in a status register to values that indicate the completion of a task. The Smyth combination as modified by Comeau teaches or renders obvious an acoustic processor capable of setting one or more bits in a status register to values that indicate the completion of calculation of a set of distances. Such a modification would have advantageously allowed the modified Smyth to provide a "flexible

mechanism for status information to be shared with the host [processor] 40.” Comeau, [0201].

Although Smyth does not expressly teach that the acoustic coprocessor and the at least one processor are fabricated on a single integrated circuit, this would have been an obvious design choice. Moreover, Boike teaches a “system-on-a-chip (SoC) integrated circuit 10 containing multiple digital signal processors (DSPs).” Boike, 2:52-54. A POSITA would have found it obvious and been motivated to modify Smyth to include distinct processing circuits on a single IC, as taught by Boike. Boike alone expressly motivates the combination, informing a POSITA that it would have reduced space and costs and conserved power to form multiple DSPs on a single IC. Boike, 1:19-42.

Whittaker teaches additional details of acoustic modeling, including the use of parameters represented with integer data. A POSITA would have been motivated and found it obvious to modify the Smyth combination to utilize an acoustic model including parameters represented with integer data, as taught by Whittaker. Such a modification would have advantageously “obtain[ed] an 86% reduction in the size of the language model with no increase in the word error rate,” per Whittaker’s teachings. Whittaker, 2:30-32.

The remaining asserted claims of the ’789 patent recite features of obvious operating environments for the claimed acoustic coprocessor. Ichikawa teaches a speech recognition system with a voice input microphone array constituted of a plurality of microphones. A POSITA would have been motivated and found it obvious to modify Smyth to use a plurality of microphones to advantageously eliminate noise, per Ichikawa’s teachings. Seshadri teaches a “speech recognition system of the invention can be configured on at least but not limited to a laptop computer[.]” Seshadri, 3:60-65. Seshadri also teaches implementing speech recognition system on a mobile phone, a game console, (i.e., an electronic entertainment product), and a

variety of other settings. Steinbiss, moreover, expressly teaches an appliance comprising a speech recognition system. All of these would have been obvious operating environments for a speech recognition system.

The above descriptions of possible combinations are exemplary and not limiting. It would have been obvious to combine any of the references that teach the individual limitations of the '789 patent following a similar analysis.

C. Invalidity Under 35 U.S.C. § 101

The Asserted Claims of the '789 patent are directed to patent-ineligible subject matter under 35 U.S.C. § 101. Claims 1 and 10 of the '789 patent (and all claims that depend from them) are directed to the abstract idea of receiving data, performing calculations on that data and sending that data to a destination. Courts have acknowledged that performing data processing, even limited to a particular field, is a patent-ineligible, abstract idea. *See, e.g., Elec. Power Grp. LLC v. Alston S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016).

The elements recited in the claims of the '789 patent are well understood, routine, and conventional and thus do not provide an “inventive concept.” For example, interfaces, feature vectors, distance calculations with acoustic models, and memory were all well understood, routine, and conventional at the time of the application for the '789 patent.

The elements recited in the dependent claims were also well understood, routine, and conventional. These elements include, without limitation, integrated circuits, Gaussian parameters and probability distributions, flash memory, serial buses, “results” memory, neural networks, CPUs, SRAM, status registers, DMA, and burst copying.

The specification of the '789 patent (and the references cited therein) support the contention that the elements discussed in the preceding paragraphs were well understood, routine, and conventional. Apple incorporates by reference the prior art cited in the Ex. E charts

which provide further evidence that the above elements were well understood, routine, and conventional.

D. Invalidity Under 35 U.S.C. § 112

1. Lack of Enablement and Written Description Under U.S.C. § 112 ¶1

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 1 because the specification and original patent application fail to provide an enabling disclosure of and written description support for at least the following limitations:

- “autonomously calculate[s/ing]” (claim 6, 17)

2. Indefiniteness Under 35 U.S.C. § 112 ¶2

Based on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions, the Asserted Claims may fail to satisfy the requirements of § 112, ¶ 2 because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history.

- “data associated with an audio signal” (claim 1)
- “autonomously calculate[s/ing]” (claim 6, 17)
- “associated acoustic state” (claim 6-7)
- “generating an interrupt” (claim 22)
- “sequential bursts” (claim 27)
- “the buffer memory” (claim 39)
- “An electronic entertainment product comprising the speech recognition system of claim 39.” (claim 44)

- “An appliance comprising the speech recognition system of claim 39.” (claim 45)

IX. UNENFORCEABILITY

During prosecution of all five of the Asserted Patents, Zentian claimed small entity status with the U.S. Patent & Trademark Office. On information and belief, Zentian was actively trying to license its technology to large companies while prosecuting the Asserted Patents. To the extent that Zentian successfully licensed its technology any company that did not qualify for small entity status, Zentian committed fraud upon the Patent Office, and its patents are unenforceable. *See* 37 C.F.R. § 1.27(h). Apple’s investigation is ongoing, and Apple reserves the right to supplement these contentions based on discovery.

X. DOCUMENT PRODUCTION ACCOMPANYING PRELIMINARY INVALIDITY CONTENTIONS

Apple is producing and/or making available for inspection documents under a separate letter.

Apple reserves the right to produce and rely on additional documents relating to their products in view of, for example, additional information revealed during discovery regarding Zentian’s allegations and/or amendments to the Infringement Contentions.

XI. OTHER RESERVATIONS AND EXPLANATIONS

These Preliminary Invalidity Contentions and accompanying document productions are preliminary and subject to further revision as follows. Nothing in these contentions constitutes an admission concerning the priority date, conception date, or date of reduction to practice of the Asserted Claims. Apple reserves the right to modify or supplement these Preliminary Invalidity Contentions, including in response to any positions taken or information disclosed regarding the priority date, conception date, or date of reduction to practice of the Asserted Claims.

For prior art patents and prior art publications identified in these Preliminary Invalidity Contentions, Apple reserves the right to rely on the public use, offer for sale, sale, and/or actual products embodying the methods and systems described therein uncovered during discovery. Apple also reserves the right to rely on any related patents and patent applications, foreign patent counterparts and foreign patent applications of U.S. patents identified in these Preliminary Invalidity Contentions, and U.S. counterparts of foreign patents and foreign patent applications identified in these Preliminary Invalidity Contentions.

The Court has not yet construed any of the terms in the Asserted Patents. Accordingly, Apple's Preliminary Invalidity Contentions are based in part on Apple's present understanding of the Asserted Claims and Zentian's apparent interpretation of these claims as reflected in its Infringement Contentions. By including prior art that anticipates or renders obvious claims based on Zentian's apparent claim interpretations, Apple is not agreeing that Zentian's claim interpretations are correct.

The accompanying invalidity claim charts provide examples of prior art that discloses, either expressly or inherently, every limitation of certain claims and/or teachings, suggestions and motivations through which a POSITA at the time of the alleged invention would have considered the limitations obvious in view of the state of the art at the time, the differences between the claimed invention and the state of the art, and the foreseeability from a technical perspective and/or marketing and/or natural and expected evolution of the art. Where Apple cites to a particular figure in a reference, the citation should be understood to encompass the caption and description of the figure and any text relating to the figure. Conversely, where Apple cites to particular text referring to a figure, the citation should be understood to include the

figure as well. As discovery progresses and the scope and focus of the liability issues become clearer, Apple may rely on uncited portions of the prior art.

Apple reserves the right to revise their ultimate contentions concerning the invalidity of the Asserted Claims, which may change depending on discovery taken in the case, the Court's construction of the Asserted Claims, any findings as to the priority date of the Asserted Claims, and/or positions that Zentian or expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Apple may rely on Zentian's or any inventor's admissions concerning the scope of prior art relevant to the Asserted Patents; the patent prosecution histories for the Asserted Patents; any deposition testimony of the named inventors on the Asserted Patents; and the papers filed and any evidence submitted by Zentian in connection with this litigation. For example, Apple reserves the right to assert that the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event that Apple obtains evidence that the named inventors did not invent (either alone or in conjunction with others) the subject matter claimed in the Asserted Patents. Should Apple obtain such evidence, it will provide the name(s) of the person(s) from whom and the circumstances under which the claimed invention or any part of it was derived.

Prior art not included in this disclosure, whether known or not known to Apple, may become relevant. In particular, Apple is currently unaware of the extent, if any, to which Zentian will contend that limitations of the Asserted Patents are not disclosed in the prior art identified by Apple. To the extent such an issue arises, Apple reserves the right to identify other references that would render obvious the allegedly missing limitation(s) of the disclosed device or method. Further, because discovery has yet to begin and because Apple has not yet completed its search for or analysis of relevant prior art, Apple reserves the right to revise, amend, and/or supplement

the information provided herein, including identifying, charting, and relying on additional references, should Apple's further search and analysis yield additional information or references, consistent with the Federal Rules of Civil Procedure.

Additionally, because third-party discovery has not yet begun, Apple reserves the right to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g), and/or § 103, located during the course of such discovery or further investigation, and to assert invalidity under 35 U.S.C. §§ 102(c), (d), or (f), to the extent that such discovery or investigation yields information forming the basis for such invalidity. For example, Apple expects to issue subpoenas to, and receive information from, third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed above and/or additional prior art. These third parties include, without limitation, the authors, inventors, vendors, or assignees of the references listed in these disclosures.

Apple further reserves the right to modify or add additional contentions under the procedures set forth in the Court's Order Governing Procedures, which permits amendments in Final Invalidity Contentions.

Apple further reserves the right to modify or add additional contentions in the event that Zentian provides amended infringement contentions and to the extent the Court orders or allows Zentian to amend its infringement contentions. For example, Apple reserves the right to modify or add additional contentions in response to Zentian's amended or Final Infringement Contentions.

Apple also reserves the right to argue that various portions of the Asserted Claims, such as an intended use or result, printed matter that is not functionally or structurally related to the physical substrate holding the printed matter, non-functional descriptive material, and certain

preamble language, are entitled to no patentable weight. Mapping of a portion of an Asserted Claim to a prior art reference does not represent that such portion of the claim is entitled to patentable weight when comparing the claimed subject matter to the prior art.

Zentian's Infringement Contentions do not provide any detailed contentions based on the doctrine of equivalents. Accordingly, Apple contends that Zentian should be precluded from asserting infringement under the doctrine of equivalents. If, however, Zentian provides additional information and is permitted to rely on the doctrine of equivalents, Apple reserves the right to amend and supplement these Preliminary Invalidity Contentions as appropriate

Pursuant to the operative Scheduling Order and in light of Zentian's Infringement Contentions and accompanying claim charts, Apple lists in these Preliminary Invalidity Contentions the prior art now known that Apple contends anticipates or renders obvious the Asserted Claims. Although Apple has identified at least one disclosure of a limitation for each prior art reference, each and every disclosure of the same limitation in the same reference is not necessarily identified. In an effort to focus the issues, Apple's citations are only representative portions of an identified reference, even where a reference may contain additional support for a particular claim limitation. POSITAs generally read an item of prior art as a whole and in the context of other publications and literature. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such persons would rely on other information within the reference, along with other publications and their general scientific knowledge. Apple may rely on uncited portions of the prior art references and on other publications and expert testimony to provide context, and as aids to understanding and interpreting the portions that are cited.

Apple incorporates in these Preliminary Invalidity Contentions, in full, all prior art references cited in the Asserted Patents and their prosecution histories and any applicable post-grant proceedings, including *inter partes* reviews (currently pending or otherwise).

Subject to Apple's reservation of rights, Apple identifies each item of prior art that anticipates and/or renders obvious the Asserted Claims. The patents/applications, publications, and systems identified are also relevant to show the state of the art and reasons and motivations for making improvements, additions, and combinations.

Apple also contends that the Asserted Patents are invalid in view of public knowledge and uses and/or offers for sale or sales of products and services that are under 35 U.S.C. § 102(a) and/or 35 U.S.C. § 102(b) and/or prior inventions made in this country by other inventors who had not abandoned, suppressed, or concealed them under 35 U.S.C. § 102(g).

Apple also reserves the right to rely on any system, public knowledge or use embodying or otherwise incorporating any of the prior art disclosed herein alone or in combination. Apple further reserves the right to rely on any other documents or references describing any such system, knowledge, or use.

Dated: October 27, 2022

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CERTIFICATE OF SERVICE

I hereby certify that on October 27, 2022 a copy of the foregoing **DEFENDANT APPLE INC.'S INVALIDITY CONTENTIONS** was served by secure file transfer upon the following:

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