

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

ZENTIAN LIMITED,
Patent Owner.

IPR2023-00033
Patent 7,587,319 B2

Before KEVIN F. TURNER, JEFFREY S. SMITH, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

OGDEN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Petitioner Apple Inc. (“Apple”) filed a Petition (Paper 1, “Pet.”) under 35 U.S.C. §§ 311–319 requesting *inter partes* review of claims 46–51, 53, 54, 58, 59, 64, and 67 of U.S. Patent No. 7,587,319 B2 (Ex. 1001, “the ’319 patent”). Patent Owner Zentian Limited (“Zentian”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).¹

Under the authority delegated to us by the Director under 37 C.F.R. § 42.4(a), we may institute an *inter partes* review when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see also* 37 C.F.R. § 42.108(c) (2022). Applying that standard, we institute an *inter partes* review of all the challenged claims of the ’319 patent for the reasons explained below. This is a preliminary decision, and we will base our final written decision on the full trial record.

II. BACKGROUND

A. THE ’319 PATENT (EX. 1001)

The ’319 patent describes “a speech recognition circuit which uses parallel processors for processing the input speech data in parallel.” Ex. 1001, 1:4–6. The processors analyze models of words having common

¹ Each party alleges that it is the sole real party in interest, and this is not contested on the preliminary record. *See* Pet. 77; Paper 4, 1.

prefix components, and store lexical data in a lexical memory. *Id.* at code (57). The processors are arranged in clusters, each with its own “partial lexical memory” for storing part of the lexical data. *See id.* at 2:64–3:7.

Figure 2, reproduced below, is a schematic diagram of the speech-recognition circuit.

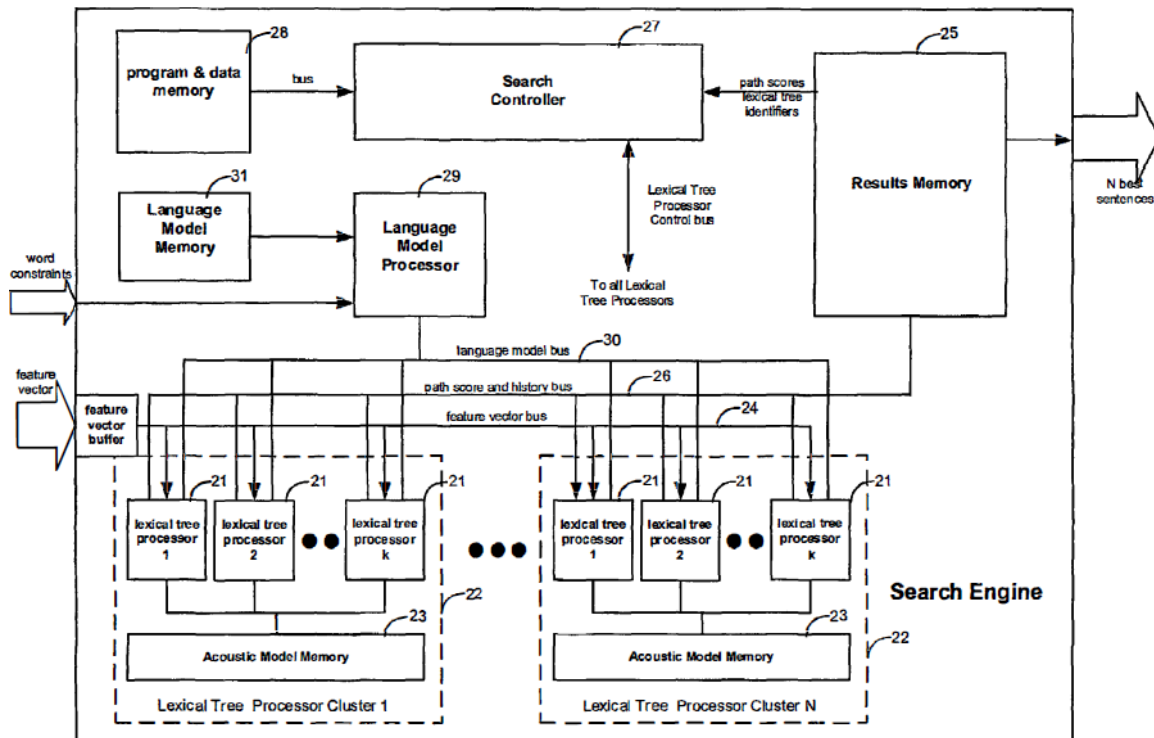


Fig 2

As shown above in Figure 2, there is a feature vector buffer (middle left) for receiving a set of speech data as feature vectors. *See Ex. 1001, 4:55–57.* Clusters 22 (of which there are N), each having k lexical tree processors 21 (and thus $N \times k$ total processors) read the feature vectors from feature vector bus 26, process the feature vectors, and store the resulting lexical data in an acoustic model memory (23) that is part of each cluster. *Id.* at 4:65–5:13.

B. CHALLENGED CLAIMS AND GROUNDS

Claim 46, the sole challenged independent claim, is as follows:

46. A speech recognition circuit comprising:

- [a] an input buffer receiving processed speech parameters;
- [b] a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data;
- [c] a plurality of processors connected in parallel to said input buffer for processing the speech parameters in parallel,
- [d] said processors being arranged in groups of processors, each group of processors being connected to a lexical memory;
- [e] a control processor controlling each processor to process said speech parameters using partial lexical data read from a respective said lexical memory; and
- [f] a results memory storing the results of the processing of the speech parameters from said processors.

Ex. 1001, 15:55–16:2 (Apple’s reference numbers added).

Apple argues four grounds for *inter partes* review, as summarized in the following table:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
46, 50, 54, 64, 67	103(a) ²	Thelen, ³ Bailey, ⁴ Chen ⁵
47–49	103(a)	Thelen, Bailey, Chen, Huang ⁶
53, 58, 59	103(a)	Thelen, Bailey, Chen, Jiang ⁷
51	103(a)	Thelen, Bailey, Chen, Katz ⁸

Pet. 6.

C. DECLARATORY TESTIMONY

Apple submits a declaration by Christopher Schmandt. Ex. 1003.
Zentian likewise submits a declaration by Dr. DeLiang Wang. Ex. 2002.

D. RELATED PROCEEDINGS

As related matters, the parties identify *Zentian Ltd. v. Apple Inc.*, No. 6:22-cv-00122-ADA (W.D. Tex. filed Feb. 2, 2022) (“parallel district court proceeding”) and *Zentian Ltd. v. Amazon.com*, No. 6:22-cv-00123-ADA

² 35 U.S.C. § 103(a) (2006), *amended* by Leahy–Smith America Invents Act, Pub. L. No. 112-29 § 103, sec. (n)(1), 125 Stat. 284, 287, 293 (2011) (effective Mar. 16, 2013). This version of § 103 applies because the ’319 patent issued from an international application filed on February 4, 2003, which is before the effective date of the AIA amendments. *See* Ex. 1001, code (22).

³ Thelen et al., US 6,526,380 B1 (issued Feb. 25, 2003) (Ex. 1030).

⁴ Bailey et al., US 5,459,798 (issued Oct. 17, 1995) (Ex. 1031).

⁵ Chen et al., US 5,428,803 (issued June 27, 1995) (Ex. 1005).

⁶ Huang et al., US 6,076,056 (issued June 13, 2000) (Ex. 1034).

⁷ Jiang, US 6,374,219 B1 (issued Apr. 16, 2002) (Ex. 1004).

⁸ Katz, US 4,831,550 (issued May 16, 1989) (Ex. 1035).

(W.D. Tex. filed Feb. 2, 2022), as well as co-pending inter partes review proceedings IPR2023-00034 to -00037. Pet. 77; Paper 4, 1.

III. DISCRETIONARY GROUND FOR DENYING INSTITUTION

In light of the parallel district court proceeding that also challenges claims of the '319 patent, Zentian contends that we should deny institution based on our discretion under 35 U.S.C. § 314(a). Prelim. Resp. 4–7.

Institution of inter partes review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016); *see also* 35 U.S.C. § 314(a). The Board has held that the advanced state of a parallel district court action is a factor weighing in favor of denying a petition under § 314(a). *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential); Patent Trial and Appeal Board, Consolidated Trial Practice Guide, 58 & n.2 (Nov. 2019), <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>. (“Trial Practice Guide”).

In *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential), the Board explained that “cases addressing earlier trial dates as a basis for denial under *NHK Spring* have sought to balance considerations such as system efficiency, fairness, and patent quality.” *Fintiv*, Paper 11 at 5. *Fintiv* sets forth six non-exclusive factors for determining “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Id.* at 6. The Director of the USPTO has also issued interim guidance to the Board on applying these factors. *See* Katherine K. Vidal, Interim Procedure for Discretionary Denials in AIA Post-Grant

Proceedings with Parallel District Court Litigation (June 21, 2022) 9, https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Interim Procedure”).

The Interim Procedure explains that “[c]onsistent with *Sotera Wireless, Inc.*, the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure 3 (footnote omitted) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)). The Interim Procedure explains that such a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB . . . and allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8.

After Zentian submitted its Preliminary Response, Apple requested authorization to submit a *Sotera*-type stipulation, which we authorized on April 14, 2023. *See* Paper 9, 1. Apple stipulated as follows: “If the instant IPR is instituted, Petitioner will not pursue in the parallel district court proceeding the same grounds as in the Petition or any grounds that could have reasonably been raised in the pending Petition.” *Id.* This is the type of broad stipulation contemplated in the Interim Procedure, and in light of this stipulation, we decline to exercise our discretion to deny institution under § 314(a).

IV. GROUNDS OF THE PETITION

For the reasons below, we determine that Apple has demonstrated a reasonable likelihood that it would prevail in showing that at least one of claims 46–51, 53, 54, 58, 59, 64, and 67 of the '319 patent is unpatentable under the grounds of the Petition. Before analyzing these grounds in detail, we address two matters that will underlie our analysis: the level of ordinary skill in the art and the construction we will apply to the claim terms.

A. LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Relying on Mr. Schmandt’s testimony, Apple argues that a person of ordinary skill in the art would have had “a master’s degree in computer engineering, computer science, electrical engineering, or a related field, with at least two years of experience in the field of speech recognition, or a bachelor’s degree in the same fields with at least four years of experience in the field of speech recognition.” Pet. 5 (citing Ex. 1003 ¶¶ 24–26).

At this stage, Zentian does not dispute Apple’s proposed level of ordinary skill in the art. Prelim. Resp. 4. Because Apple’s articulation of that level of skill is uncontested, supported by testimonial evidence, and appears consistent with the types of problems and solutions in the ’319 patent, we adopt it for this decision.

B. CLAIM CONSTRUCTION

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2022). This generally includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.* The ordinary and customary meaning of a claim term “is its meaning to the ordinary artisan after reading the entire patent,” and “as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313, 1321.

Apple states that it “applies the plain and ordinary meaning of all claim terms,” and does not propose any explicit constructions. *See* Pet. 7. Likewise, Zentian does not propose any explicit constructions at this stage. *See* Prelim. Resp. 4.

We do not find it necessary to explicitly construe any terms for this decision. To the extent that we need to interpret claim language, we address that language below in the context of the prior art. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the

extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

C. OBVIOUSNESS OF CLAIM 46 BASED ON THELEN, BAILEY, AND CHEN

First, Apple first argues that claim 46 is unpatentable under § 103(a) as obvious over Thelen in view of Bailey and Chen. Pet. 9–54.

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are “such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). When a ground in a petition is based on a combination of references, we consider “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *Id.* at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

We base our obviousness inquiry on factual considerations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) any objective indicia of obviousness or non-obviousness that may be in evidence. *See Graham*, 383 U.S. at 17–18.

Considering these factors,⁹ we determine that Apple has shown a reasonable likelihood that claim 46 is unpatentable as obvious over Thelen

⁹ Because neither party argues that there are objective indicia of obviousness or non-obviousness at this stage, this does not factor into our decision.

in view of Bailey and Chen. We begin our analysis with a brief overview of the prior art, and then we address the parties' contentions with respect to the challenged claims.

1. *Thelen*

Thelen describes “[a] huge vocabulary speech recognition system for recognizing a sequence of spoken words.” Ex. 1030, code (57). Figure 3, reproduced below, is a block diagram of this system:

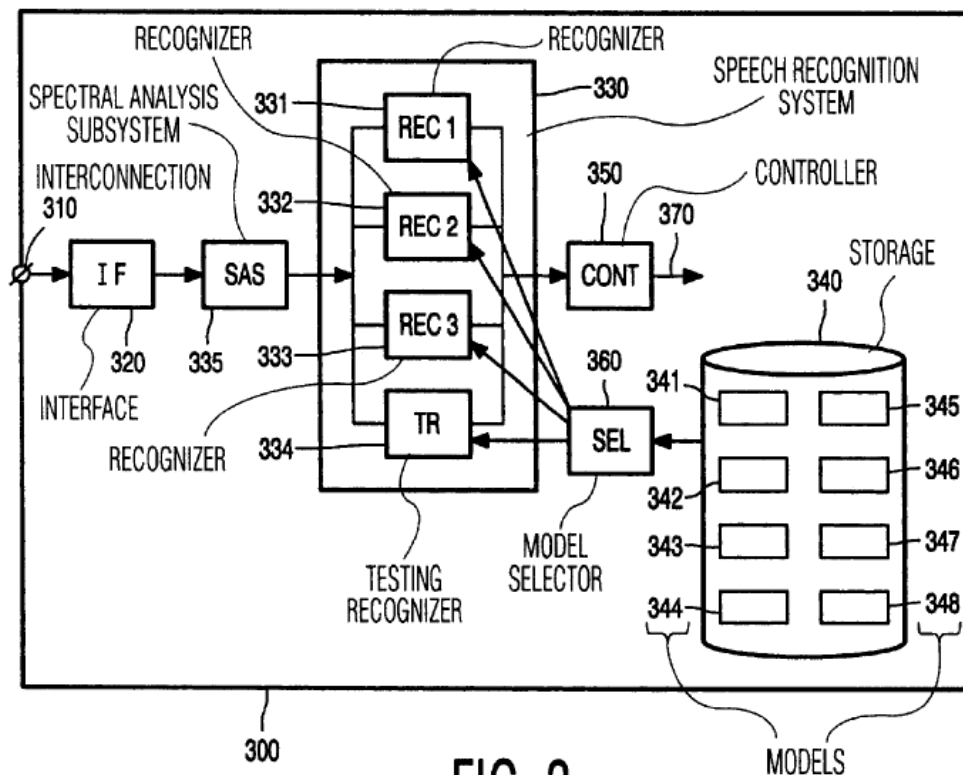


FIG. 3

The above figure depicts standalone system 300 with interconnection 310 and interface 320 for receiving a user's speech signal from, for example, a microphone or recording. Ex. 1030, 6:47–63. Spectral analysis subsystem (SAS) 335 processes the digital speech signal to produce a feature vector, which is fed to recognition system 330. *Id.* at 4:30–33, 6:63–66, 7:2–6.

Recognition system 330 “comprises a plurality of large vocabulary speech recognizers [331, 332, and 333], each being associated with a respective, different large vocabulary recognition model” that can be loaded from storage 340. *Id.* at 1:56–61, 6:66, 7:5–7, 7:34–35. “The recognizers may use the same algorithm, where the difference lies in the models being used, such as the vocabulary and the language model.” *Id.* at 7:7–9. “The recognizers operate in ‘parallel,’ in the sense that they independently recognize the same speech input at almost the same moment. This can be realized by using separate resources for each of the recognizers, such as a separate processor.” *Id.* at 7:17–21.

2. *Bailey*

Bailey describes a pattern-recognition system, useful for voice recognition, that “includes a specially optimized multiprocessing hardware unit capable of performing, in parallel, a multitude of steps required for pattern recognition procedures.” Ex. 1031, 5:27–34. Figure 3A, reproduced below, is a block diagram depicting one embodiment of this system:

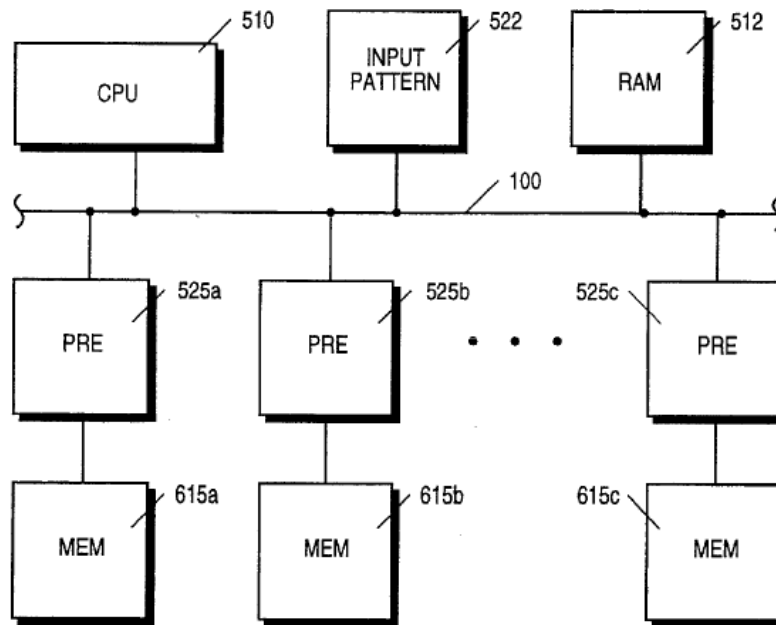


FIG. 3A

As shown in the figure above, the pattern-recognition system includes CPU 510, memory 512, and input pattern block 522 coupled to host communication bus 100. Ex. 1031, 11:11–14. Input pattern block 522 obtains a voice sample from a microphone. *Id.* at 11:17–20. Also connected to bus 100 are a “number of [pattern recognition] engines, 525a to 525c, each independently coupled to . . . bus 100.” *Id.* at 11:20–22. Each of pattern recognition engines 525a–525c is also “interfaced with its own private memory 615a–615c. *Id.* at 11:1–3. Alternatively, pattern recognition engines 525a–525c may share a common memory. *Id.* at 11:3–4, Fig. 3B.

3. *Chen*

Chen is directed to “parallel processing computer systems for performing multiple-instruction-multiple-data (MIMD) parallel processing.” Ex. 1005, 1:29–31. Chen organizes the MIMD multiprocessors into four or more physically separable clusters, and can use either a shared memory

model or a distributed memory model, depending on the application. *Id.* at 1:32–43. Figure 4, reproduced below, is a block diagram of Chen’s system:

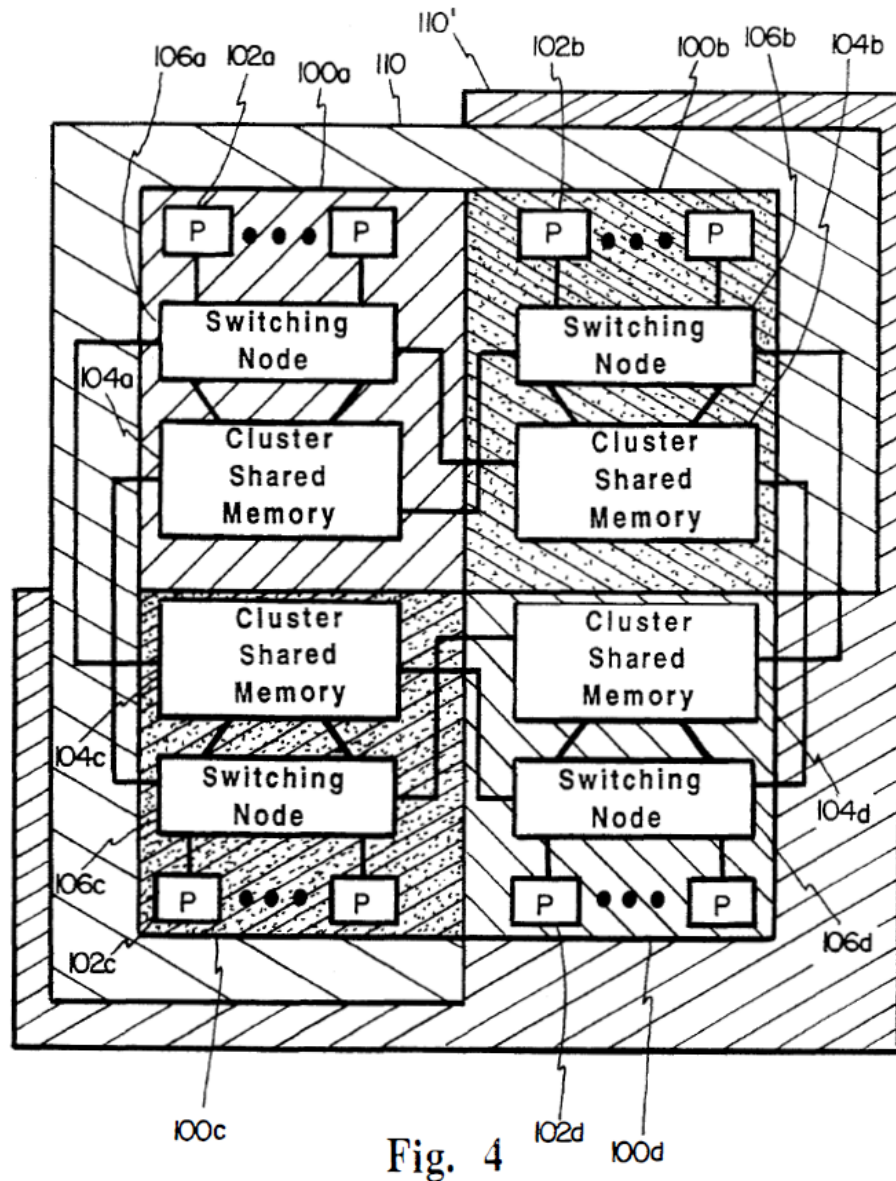


Fig. 4

The above figure depicts four clusters 100a–d, each with processors 102a–d and cluster shared memory 104a–d, where the clusters may be connected together in various shared or distributed memory configurations. Ex. 1005, 9:20–56. In particular, “[a] true shared memory model with symmetrical

access to a common shared memory 104a is provided for all processors 102a in cluster 100a.” *Id.* at 9:46–48.

4. *Preamble and Limitations 46(a) and 46(c)*

The preamble of claim 46 and limitation 46(a) recite “[a] speech recognition circuit comprising: an input buffer receiving processed speech parameters.” Ex. 1001, 15:55–56.

“To the extent the preamble is limiting,” Apple contends that Thelen “teaches or at least renders obvious a speech recognition circuit, as claimed” because it “teaches a speech recognition apparatus including a microphone, A/D converter, and processors.” Pet. 9–11 (citing Ex. 1030, code (57), 1:5–12, 2:30–37, 6:46–66, 7:20–26, Fig. 3; Ex. 1003 ¶¶ 68–69).

For limitation 46(a), Apple contends that Thelen’s recognition system 330 receives “observation vectors” from spectral analysis subsystem 335 which correspond to the recited “processed speech parameters.” *See* Pet. 12–16 (citing Ex. 1030, 4:29–43, 4:66–5:2, 6:53–7:7, 7:17–29, Figs. 1, 3; Ex. 1003 ¶¶ 70–75). Apple concedes that “*Thelen* does not expressly recite an ‘input buffer’” that received the processed speech parameters, but according to Apple, Bailey’s RAM 512 would constitute the recited buffer. Pet. 17. In particular, Apple points to Bailey’s teaching that an “unknown input *pattern* may be *temporarily stored* in memory array 512” which, Apple contends, would suggest to a person of ordinary skill in the art that RAM 512 is acting as an input buffer. Pet. 19 (quoting Ex. 1031, 11:16–17) (citing Ex. 1003 ¶ 72). According to Apple, there would have been motivation to incorporate Bailey’s input buffer into Thelen’s system because such input “[b]uffers were well-known, inexpensive, and easy-to-implement solutions to improve system efficiency.” Pet. 21 (citing Ex. 1003 ¶ 74).

Limitation 46(c) recites “a plurality of processors connected in parallel to said input buffer for processing the speech parameters in parallel.” Ex. 1001, 15:60–61. Apple identifies the recited processors with Thelen’s recognizers 331–333 and argues that they are designed to process the speech input in parallel, and that in the Thelen–Bailey combination they would be connected to the input buffer. *See* Pet. 33–38 (citing Ex. 1030, 2:30–37, 2:38–40, 7:2–7, 7:6–9, 7:17–23, 7:26–29, Figs. 2, 3; Ex. 1031, 3:60–4:1, 9:36–41, 11:9–29, 13:25–51, 14:15–29, Figs. 2, 3A; Ex. 1003 ¶¶ 81–82).

Zentian does not contest these arguments at this stage. *See generally* Prelim. Resp. Because the preliminary evidence suggests that Thelen teaches a speech recognition circuit (*see, e.g.*, Ex. 1030, Fig. 3 (system 300), 6:46–49 (stating that system 300 “preferably is implemented on a computer, such as a PC”)), we need not decide whether the preamble is limiting. Also, at this stage we find Apple’s arguments sufficiently persuasive that a person of ordinary skill in the art would have had reason to use an input buffer, such as that exemplified in Bailey, to improve efficiency in processing a speech input, and that Thelen’s recognizers 331–333 would be connected to that input buffer to process the input in parallel.

5. *Limitations 46(b) and 46(d)*

Limitation 46(b) recites “a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data.” Ex. 1001, 15:57–59. Limitation 46(d) requires “said processors being arranged in groups of processors, each group of processors being connected to a lexical memory.” *Id.* at 15:62–64.

According to Apple, Thelen describes dividing a huge vocabulary (corresponding to the “complete lexical data for word recognition”) into separate recognition models, each of which contains only part of the complete lexical data. *See* Pet. 23–30 (citing Ex. 1030, code (57), 1:5–12, 1:53–2:33, 5:14–45, 5:49–52, 6:12–39, 7:17–23, 7:30–52, 8:1–5, 8:54–59, Figs. 1, 3; Ex. 1003 ¶¶ 76–78).

Apple concedes that Thelen “does not expressly teach that each of its recognition models and associated lexicons (the mapped ‘parts’ of said complete lexical data) are stored in a plurality of lexical memories.” Pet. 30–31. But Apple argues that Thelen “envision[s] each recognizer (including its processing resources, such as processors and memory) may be associated with an exclusive recognition model in a ‘fixed one-to-one relationship.’” Pet. 31 (citing Ex. 1030, 2:30–33, 7:42–49; Ex. 1003 ¶ 78). Apple also points to Bailey’s Figure 3A embodiment, in which each parallel processor explicitly has its own memory. Pet. 30–32 (citing Ex. 1031, code (57), 1:16–20, 2:62–66, 10:18–11:44, 13:25–51, Fig. 3A; Ex. 1003 ¶ 79).

As to the requirement in limitation 46(d) that processors are arranged in groups, with each group connected to a lexical memory, Apple relies, in part, on Bailey’s Figure 3B embodiment, in which all processors share a single memory, as a suggestion “to group a plurality of processors together and connect[them] to a lexical memory.” Pet. 32–33 (citing Ex. 1031, 11:1–4, Fig. 3B). However, Apple relies primarily on Chen for limitation 46(d). *See* Pet. 38–46.

Apple argues that Chen teaches clusters 100a–d, each comprising multiple processors 102a–d and shared memory 104a–d. Pet. 38–40 (citing Ex. 1005, 5:9–17, 6:17–21, 9:5–43, 10:14–35, Figs. 4, 5A, 6A–B; Ex. 1003

¶ 83). Apple concedes that Chen “does not specifically teach a ‘lexical’ memory,” but proposes a modification of the Thelen–Bailey combination in which “each group of processors (embodied in recognizers) includes a memory, where the memory is a *lexical* memory as already taught by *Thelen–Bailey*.” Pet. 40. According to Apple, a person of ordinary skill in the art would have made this combination “for the purpose of associating the generic and specific contexts (e.g., all sports contexts) together in a group for efficient word recognition” which would “store all similar contexts on a lexical memory connected to the group of recognizers directed to those contexts.” Pet. 40–41 (citing Ex. 1030, 7:17–58, 8:1–3, 8:6–8, 8:54–9:32; Ex. 1031, Figs. 3A–B; Ex. 1003 ¶¶ 80, 84–85).

Apple contends that Thelen already teaches dividing lexical data into a hierarchy of topics, and where multiple processors are assigned to each such topic, it would have been a logical extension that each such processor would have access to a shared memory “to facilitate more efficient control and processing.” Pet. 42–44 (citing Ex. 1005, code (57); Ex. 1030, 7:30–34, 8:54–56, 8:62–9:11, Fig. 4; Ex. 1003 ¶ 84). In other words, “[i]t would have been a common[-]sense extension of *Thelen*’s grouped, hierarchical recognition models to similarly group the recognizers (per *Chen*), where each recognizer is associated with a recognition model (per *Thelen*), and each group of recognizers (and associated processors) is connected to a lexical memory, per *Bailey*.” Pet. 44 (citing Ex. 1003 ¶ 84). According to Apple, this grouping “would have yielded the predictable result of consolidating speech recognition for a particular context within a particular group of recognition processors” and “would have more efficiently allowed

for sharing of lexical data common to each of the recognition models.” *Id.* (citing Ex. 1003 ¶ 84).

Apple also contends that grouping the processors with shared memory in this way “would have yielded the predictable result of reducing the time required to recognize a user’s speech, desirably speeding the system’s response.” Pet. 44 (citing Ex. 1003 ¶ 85). Apple argues that Thelen recognizes the importance, in real-time speech processing, “that no significant delay occurs’ between a word being received in the system and recognizing the word,” and would have “simply substituted” Chen’s “more efficient processing architecture” for the Thelen–Bailey recognizers. Pet. 44–45 (quoting Ex. 1030, 7:27) (citing Ex. 1030, 7:20–26; Ex. 1003 ¶ 85). According to Apple, there would have been a reasonable expectation of success in making this substitution because it “would have only required arrangement of well-known memory components and relocation of lexical data already present in *Thelen*.” Pet. 45–46 (citing Ex. 1003 ¶ 85).

In response, Zentian argues that the ’319 patent distinguishes its claimed invention from prior art where (1) “only a single memory were used for all processors” (like Thelen or Bailey’s Figure 3B) or (2) “each processor only has access to its own local memory” (like Bailey’s Figure 3A). Prelim. Resp. 10–11 (emphasis omitted) (citing Ex. 1001, 3:50–58; Ex. 2002 ¶ 27). Zentian contends that “Thelen neither teaches limitation 46(b) nor 46(d), must less the two limitations combined” because Thelen’s processors are “never arranged in groups.” *Id.* at 11–13 (citing Ex. 1030, Fig. 3; Ex. 2002 ¶¶ 29, 31–32). And according to Zentian, “Bailey’s two processor-to-memory architectures likewise fail to meet the requirements of limitations 46(b) and (d)” because Bailey’s Figure 3A and 3B embodiments are the

same as the two designs that the '319 patent distinguishes. *Id.* at 13–16 (citing Ex. 1001, 3:44–58; Ex. 1031, 11:1–4, Figs. 3A–B; Ex. 2002 ¶¶ 34–39); *see also id.* at 18–19 (citing Ex. 1030, 7:30–33, 7:43–48; Ex. 2002 ¶¶ 41, 44–46).

Zentian also contends that “Chen is not a reference in the field of art of speech recognition,” and thus “has nothing to say about the design of speech recognition systems.” Prelim. Resp. 16–17 (citing Ex. 2002 ¶ 41). And according to Zentian, neither Thelen, Bailey, nor Chen teaches the arrangement that Apple relies upon for limitations 46(b) and 46(d). *Id.* at 17–20 (citing Ex. 1030, 7:30–33, 7:43–48; Ex. 1031, 11:22–23, 13:12–13; Ex. 2002 ¶¶ 41, 43–48).

As to the proposed motivation to combine, Zentian argues that Apple has failed to explain *why* a person of ordinary skill in the art “would have been motivated to undertake the numerous modifications the Petition’s theory requires in the precise manner necessary to arrive at the requirements of limitations 46(b) and (d).” Prelim. Resp. 20–21. Instead, according to Zentian, Apple merely relies on appeals to “common sense,” “predictable results,” and “efficiency,” which are insufficient to articulate a basis for obviousness. *Id.* at 21–22 (citing Pet. 41–42, 44); *see also id.* at 23–24 (citing Ex. 2002 ¶ 51) (arguing that Apple ignores that its proposed modification “would have required far more hardware—in terms of processors and memories—than what either Thelen or Bailey teaches, and that this would have necessarily come at significant additional cost and complexity”).

Zentian next argues that Thelen teaches away from grouping processors by teaching in its preferred embodiment that “there should only

be one recognizer per multiple recognition models—the exact opposite of the Petition’s proposed modification.” Prelim. Resp. 24 (citing Ex. 2002 ¶ 45); *see also id.* at 22–23 (citing Ex. 1030, 7:30–33, 7:43–46; Ex. 2002 ¶¶ 34–39, 45, 47, 50).

Finally, relying on testimony by Dr. Wang, Zentian argues that the technical skill required for Apple’s proposed combination would have been beyond the level of ordinary skill in the art. Prelim. Resp. 25–26 (citing Ex. 2002 ¶ 52). Zentian contends that the modification would have required, contrary to the teachings of Thelen and Bailey, (1) grouping processors, (2) associating each group with a dedicated memory, (3) ensuring that the dedicated memory contained part of the lexical data, and (4) ensuring that the sum of the dedicated memories together contained the complete lexical data. *Id.* (citing Ex. 2002 ¶ 52).

We find that Apple has presented a sufficiently persuasive and particular argument, at this stage, that a person of ordinary skill in the art would have had reason to combine Thelen, Bailey, and Chen as outlined in the Petition. Although Zentian correctly points out that neither Thelen, Bailey, or Chen, alone, teaches every aspect of limitations 46(b) and (d), that is not the requirement for showing obviousness. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (“The test for obviousness is not . . . that the claimed invention must be expressly suggested in any one or all of the references.”). Nor does it matter that the ’319 patent distinguishes some of the prior art embodiments that Apple relies on for its combination, because Apple’s arguments in the Petition rely on a *combination* of prior art features, not the uncombined features or Thelen, Bailey, or Chen alone.

We also disagree with Zentian’s implication that Chen is a non-analogous reference. The ’319 patent “describes a parallel processing computing platform utilizing clustered processors.” Pet. 8 (citing Ex. 1001, 3:13–24, 5:6–36, Fig. 2; Ex. 1005, 5:9–17, 9:5–43; Ex. 1003 ¶ 64). Chen teaches “a unified parallel processing architecture for connecting together an extendible number of clusters for multiple numbers of processors to create a high[-]performance parallel processing computer system.” Ex. 1005, 5:9–13. At this stage, the preliminary evidence suggests that Chen’s teachings in this regard would have been reasonably pertinent to the particular problem with which the inventor is involved, which includes the use of parallel processing to speed up searches performed in a speech recognition system. *See, e.g.*, Ex. 1001, 1:13–15, 1:30–32, 1:44–46; *see In re Clay*, 966 F.2d 656, 659 (Fed. Cir. 1992) (“A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor’s endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor’s attention in considering his problem.”).

We also disagree with Zentian that Apple has failed, at this stage, to sufficiently articulate a reason why a person of ordinary skill in the art would have made the proposed combination of Thelen, Bailey, and Chen. Although Apple contends that its proposed combination would have been a predictable, efficient, and a common-sense extension to the prior art, Apple also provides a supporting rationale for these contentions. For example, we find it reasonable, at this stage, that a person of skill in the art would have considered Chen’s architecture desirable as a substitution for that of the Thelen–Bailey combination because, at the very least, it leverages the power

of multiple processors available for use within each of Thelen's recognition contexts. *See* Ex. 1003 ¶ 84.

We recognize that Thelen teaches a preferred embodiment in which “the system comprises more models than active recognizers.” Ex. 1030, 7:47–48. But presenting this embodiment as a preference does not constitute teaching away. *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) (“A reference does not teach away . . . if it merely expresses a general preference for an alternative invention but does not ‘criticize, discredit, or otherwise discourage’ investigation into the invention claimed.” (quoting *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004))). In any event, even under Thelen's preferred embodiment, each processor is associated with only a subset of the system's complete lexical data, and the same rationale would apply for providing each processor with dedicated memory, in this case to hold the plurality of recognition models associated with each processor.

Finally, at this stage we find Mr. Schmandt's testimony that the proposed modification would have been within the ordinary skill in the art more credible than Dr. Wang's somewhat more conclusory testimony to the contrary. *See* Ex. 1003 ¶ 84; Ex. 2002 ¶ 52. We note that, at this preliminary stage, the parties agree that the level of ordinary skill in the art would have included a master's degree in a field such as computer engineering with specific experience in speech recognition. *See* Ex. 1003 ¶ 23; Ex. 2002 ¶ 14. The preliminary evidence suggests that such a person would have had the necessary education and background to be able to modify Thelen based on the teachings of Bailey and Chen.

For the above reasons, we find that Apple has sufficiently shown, at this stage, that limitations 46(b) and (d) would have been obvious over the combination of Thelen, Bailey, and Chen.

6. *Limitation 46(e) and 46(f)*

Limitation 46(e) recites “a control processor controlling each processor to process said speech parameters using partial lexical data read from a respective said lexical memory.” Ex. 1001, 15:65–67.

Apple associates the recited control processor with Thelen’s “model selector 360 in combination with controller 350,” and also Bailey’s CPU 510. Pet. 46–49 (citing Ex. 1030, 7:50–61, 7:63–8:1, 8:36–41, 9:8–10, 10:20–24, Fig. 3; Ex. 1031, 9:5–39, 11:4–8, 11:23–34, 11:59–64, 12:12–25, 13:5–23, Figs. 3A–B; Ex. 1003 ¶¶ 86–87). Apple contends that it would have been obvious to modify the Thelen–Bailey–Chen system to include Bailey’s CPU 510 for controlling the processors because it was well-known in the art to use a master processor to control a group of other processors. Pet. 50 (citing Ex. 1032, 12:2–11; Ex. 1003 ¶¶ 86–88).

Limitation 46(f) recites “a results memory storing the results of the processing of the speech parameters from said processors.” Ex. 1001, 16:1–2.

Apple identifies the recited results memory with Bailey’s RAM 512, and argues that a person of ordinary skill in the art would have been motivated to add such a results memory to Thelen because of a recognized need “to report outcomes of the comparisons.” Pet. 51–54 (citing Ex. 1030, 7:50–58; Ex. 1031, 11:23–34, 11:42–59, 12:2–11, 12:41–61, Fig. 4; Ex. 1003 ¶¶ 89–91).

Zentian does not contest these arguments at this stage. *See generally* Prelim. Resp. We find Apple’s arguments sufficiently persuasive for the reasons outlined in the Petition.

For all the above reasons, we find Apple’s arguments sufficiently persuasive at this stage that claim 46 is unpatentable under § 103(a) as obvious over the combination of Thelen, Bailey, and Chen.

D. OTHER CLAIMS

Claims 47–51, 53, 54, 58, 59, 64, and 67 depend directly or indirectly from claim 46. *See* Ex. 1001, 16:3–28, 16:34–41, 16:56–62, 17:12–14, 17:22–25. Zentian does not contest Apple’s specific arguments for any of these claims at this stage. *See generally* Prelim. Resp.

Because Apple has shown a reasonable likelihood of prevailing with respect to claim 46, we will institute on all claims and all grounds raised in the Petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1364 (Fed. Cir. 2019) (“[I]f the Board institutes an IPR, it must . . . address all grounds of unpatentability raised by the petitioner.”).

V. CONCLUSION

For the reasons above, Apple has shown that there is a reasonable likelihood it would prevail with respect to at least one of the claims challenged in the Petition. Thus, we institute trial on all asserted grounds and all challenged claims.

VI. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 46–51, 53, 54, 58, 59, 64, and 67 of the '319 patent is instituted with respect to all the grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, *inter partes* review of the '319 patent commences on the entry date of this Order, and the Board hereby gives notice of the institution of a trial.

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Patent 7,587,319 B2

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