

Inter Partes Review U.S. Patent No. 7,587,319

Oral Argument, March 11, 2024

Apple Inc. v. Zentian Limited
Case No. IPR2023-00033

Petitioner's Demonstrative Exhibits – Not Evidence

Petitioner's DX-I

Claim 46 and Proposed Ground I

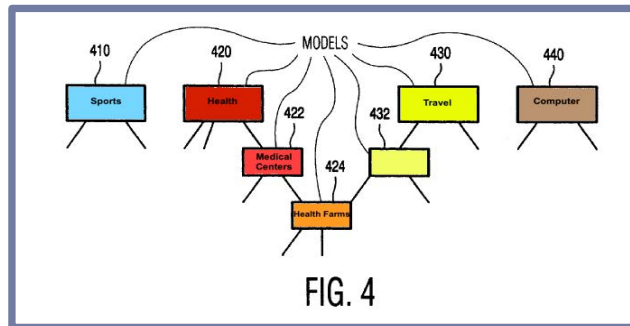
- ▶ Ground I: Claims 46, 50, 54, 64, and 67
 - ▶ **Thelen** (Ex. 1030) in view of **Bailey** (Ex. 1031) and **Chen** (Ex. 1005)

Claim 46:

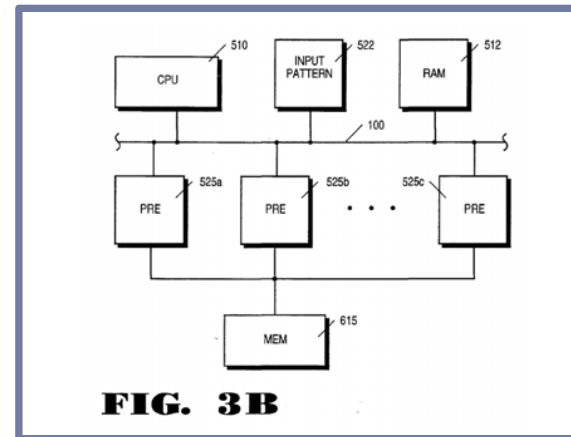
Claim Designation	Claim Language
Claim 46(Pre)	A speech recognition circuit comprising:
Claim 46(a)	an input buffer receiving processed speech parameters;
Claim 46(b)	a plurality of lexical memories containing in combination complete lexical data for word recognition, each lexical memory containing part of said complete lexical data;
Claim 46(c)	a plurality of processors connected in parallel to said input buffer for processing the speech parameters in parallel,
Claim 46(d)	said processors being arranged in groups of processors, each group of processors being connected to a lexical memory;
Claim 46(e)	a control processor controlling each processor to process said speech parameters using partial lexical data read from a respective said lexical memory; and
Claim 46(f)	a results memory storing the results of the processing of the speech parameters from said processors.

The Petition's Mapped Combination

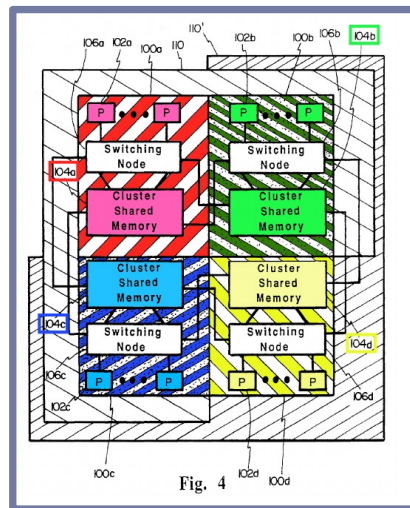
Thelen: Speech recognizers organized hierarchically



Bailey: Multiple recognizers sharing a memory



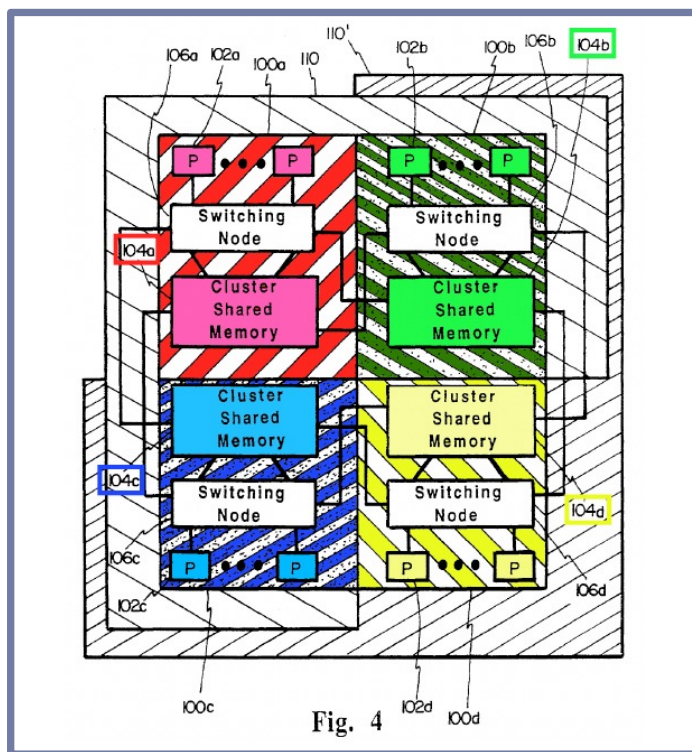
Chen:
Clustered
processors
with a
shared
memory



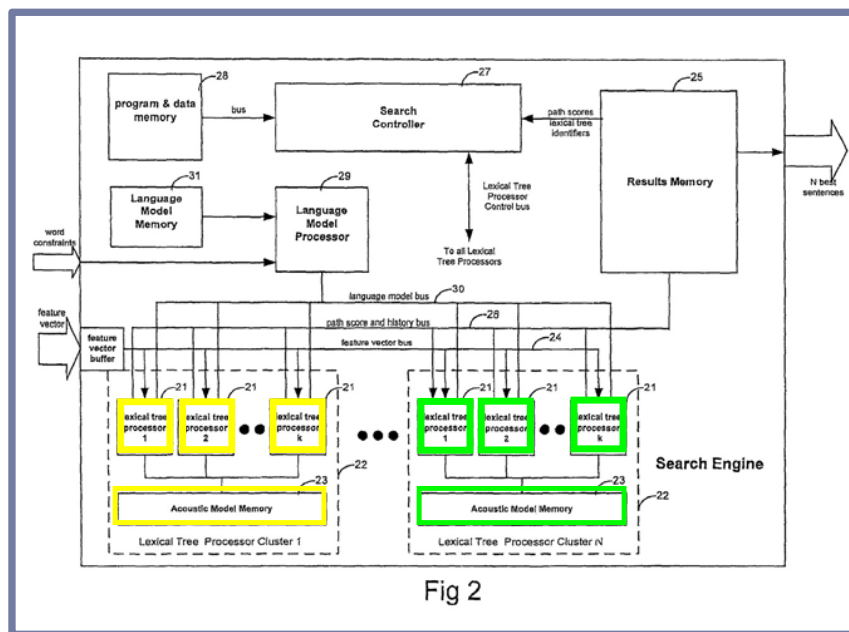
RESULT:

**Storing context-related
acoustic models efficiently
in shared lexical memory**

Chen's Clustered Processors Compared to '319 Patent



Chen (Ex. 1004), Fig. 4



'319 Patent (Ex.1001), Fig. 2

Motivations to Combine

► Benefits

Reduced
Duplication of
Lexical Data

Lower Financial
Cost of the
System

Increased
Processing Power
for a Given Cost

Less Memory
Required to
Operate

Zentian's Unclaimed and Undescribed Implementation Details

- ▶ **Memory Collisions**  **NO DISCLOSURE**
- ▶ **Task Sharing**  **NO DISCLOSURE**
- ▶ **Messaging Strategy**  **NO DISCLOSURE**
- ▶ **Bandwidth and Latency Issues**



**Single Sentence
of Disclosure:**

By providing a plurality of processors in a group with a common memory, flexibility in the processing is provided without being bandwidth limited by the interface to the memory that would occur if only a single memory were used for all processors.

'319 Patent, 3:50-54

'319 Patent's Discussion of Memory Access

Each processor within a group can access the same lexical data as any other processor in the group. The controller can thus control the parallel processing of input speech parameters in a more flexible manner. For example, it allows more than one processor to process input speech parameters using the same lexical data in a lexical memory.

'319 Patent, 3:58-63

Zentian's “Obstacles”: Alleged Memory Collisions

► **Chen Teaches:**

“Equally applicable to any type of parallel processing computer system”

Pet. Reply, 9, *citing*
Chen, 11:33-41

Inter-cluster memory access “does not have to sacrifice performance for the increased interconnection...provided by an extended shared memory model”

Pet. Reply, 16,
citing Chen, 5:3-41

Commercially
available
processors

Pet. Reply, 9, *citing*
Chen, 10:14-35

Tradeoffs between
parallel processing
performance and
memory access

Pet. Reply, 16, *citing*
Chen, 5:47-53

Techniques for addressing
memory collisions

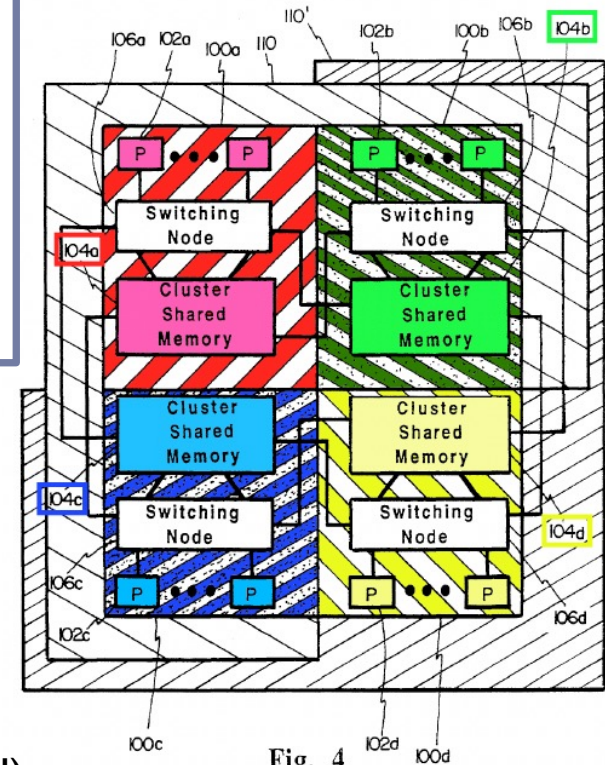
Pet. Reply, 15, *citing*
Chen, 14:39–18:42

Zentian's "Obstacles": Alleged Reprogramming Effort

► **Chen's Shared Memory Model**

Thus, in the mapped combination, there are multiple, clustered processors, with each cluster of processors sharing a single memory. This architecture is a shared memory model per *Chen's* definition and does not require any significant reprogramming effort. *Chen*, 5:20-25 (“[a] shared memory model can be used with programs that can be executed in the cluster shared memory of a single cluster”).

Pet. Reply, 22



Chen, Fig. 4 (Annotated)

Fig. 4

Level of Skill of a POSITA

► The Parties Agree:

D. Level of Skill of a POSITA

A POSITA at the time of the '319 Patent would have had a master's degree in computer engineering, computer science, electrical engineering, or a related field, with at least two years of experience in the field of speech recognition, or a bachelor's degree in the same fields with at least four years of experience in the field of speech recognition. Additional education or experience might substitute for the above requirements. *Dec.*, 24-26.¹

Pet., 5

Level of Skill of a POSITA – No Disputes

▶ Zentian DOES NOT:

▶ Dispute the Level of Skill

Q. Okay. Do you dispute that this is a correct level of skill for the 140 and the 319 patents?

A. I do not.

Anderson Depo.Tr., 9:10-12

▶ Provide an Alternative Level of Skill

III. Person of ordinary skill in the art

This Response addresses the Petition's deficiencies by assuming the Petition's proffered definition of the person of ordinary skill in the art.

POR, 5

▶ Argue that Mr. Schmandt Does Not Meet the Level of Skill

A. I'm saying that the petitioner put forth a person of ordinary skill in the art definition. It was reasonable. Somebody with experience in speech recognition. I believe somebody with those particular backgrounds could implement the patents at issue, and so those are the ones that I used.

Anderson Depo.Tr., 12:1-6