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571-272-7822

Paper 16
Entered: May 15, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00072
Patent RE38,806 E

Before MINN CHUNG, JULIA HEANEY, and SHELDON M. McGEE, *Administrative Patent Judges*.

Opinion of the Board by CHUNG, *Administrative Patent Judge*.

Opinion concurring by McGEE, *Administrative Patent Judge*.

CHUNG, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, and 32 (the "challenged claims") of U.S. Patent No. RE38,806 E (Ex. 1001, "the '806 patent"). Katana Silicon Technologies LLC ("Patent Owner") timely filed a Preliminary Response. Paper 6 ("Prelim. Resp."). Pursuant to our authorization (Ex. 3001), the parties filed briefs further addressing claim construction of "adhesion layer." Paper 13 ("Reply"); Paper 15 ("Sur-reply").

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review is authorized when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." After considering the information presented in the Petition, Preliminary Response, Reply, and Sur-reply, we determine that the information presented establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review of all challenged claims of the '806 patent, based on all grounds raised in the Petition.

II. BACKGROUND

A. Related Matters

According to the parties, the '806 patent is the subject of the following district court litigation: *Katana Silicon Techs. LLC v. Micron Tech., Inc.*, 1:22-cv-00282 (D. Idaho). Paper 5, 1; Pet. 2.

The '806 patent is one of several patents owned by Patent Owner that are challenged by Petitioner in various petitions for *inter partes* review, including in IPR2023-00071, IPR2023-00073, and IPR2023-00105.

B. Real Party-in-Interest

Petitioner identifies itself, Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC as the real parties-in-interest. Pet. 2. Patent Owner identifies itself as the sole real party-in-interest. Paper 5, 1.

C. The '806 Patent

The '806 patent describes a miniaturized semiconductor device having a chip size package (CSP) that includes multiple semiconductor chips stacked vertically inside the package (in an arrangement called a stacked package structure). Ex. 1001, 1:15–20, 1:53–65, 2:63–65.

Figure 14(a) of the '806 patent is reproduced below.

FIG.14(a)

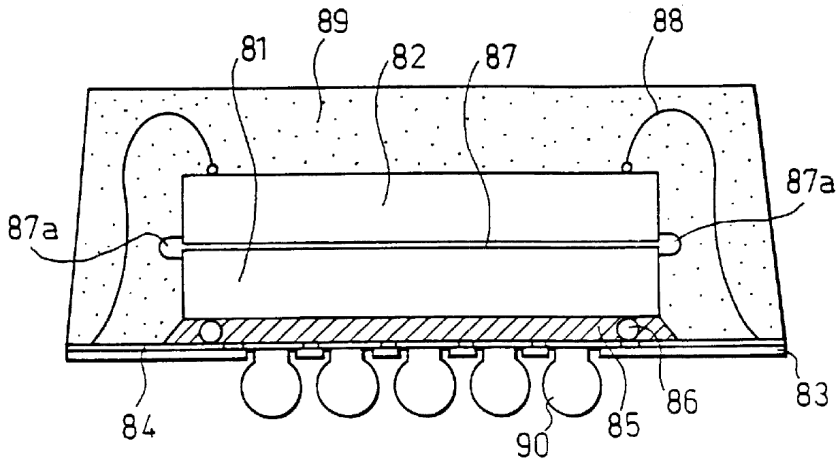


Figure 14(a) shows a cross-sectional view of a conventional semiconductor device having a stacked package structure. *Id.* at 6:24–26.

The '806 patent describes that in a conventional semiconductor device where multiple semiconductor chips are stacked and laminated, two different

methods are used to bond the laminated semiconductor chips to each other in a stacked package—"an adhesive agent (paste) potting method" and "a method using a thermo-compression sheet." *Id.* at 2:16–21. According to the '806 patent, in the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent may spread and overflow beyond the outer edge of the semiconductor chips, as illustrated in Figure 14(a) (showing adhesive agent 87 between semiconductor chips 81 and 82 overflowing beyond the edges of the chips). *Id.* at 2:23–29. Such overflown adhesive agent may come in contact with wires in the package or the electropad of the semiconductor chips. *Id.* at 2:30–42. The '806 patent describes that "[o]n the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82 . . . causing problems such as separation of the semiconductor chip 82 from the semiconductor chip 81." *Id.* at 2:44–48.

According to the '806 patent, the conventional method using a thermo-compression sheet for bonding semiconductor chips during packaging also has shortcomings. *Id.* at 2:49–56, 4:12–21. In the conventional method, the thermo-compression sheet is disposed on the surface of a first semiconductor chip, and then a second semiconductor chip is adhered to the thermo-compression sheet. *Id.* at 9:46–50. The '806 patent describes that in the conventional thermo-compression sheet method, the thermo-compression sheet must have the same size as semiconductor chip 82 and must be placed accurately at a specific location on semiconductor chip 81. *Id.* at 2:49–53. "In addition, the semiconductor chip 82 must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet." *Id.* at 2:53–56.

The '806 patent purports to avoid these problems or complications in the conventional method by forming an adhesion layer "in advance" on a back surface of a wafer when the semiconductor chips are in a "wafer state" during the semiconductor fabrication process before the wafer is cut or diced to produce individual chips. *Id.* at 4:18–63. Specifically, the '806 patent describes

> [a] method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:
>
> (a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;
>
> (b) producing separate first semiconductor chips from the first wafer by dicing;
>
> (c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;
>
> (d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;
>
> (e) producing separate second semiconductor chips from the second wafer by dicing;
>
> (f) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;
>
> (g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;
>
> (h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and
>
> (i) sealing the first and semiconductor chips and the wires.

Id. at 4:25–47.

According to the '806 patent, "[w]ith the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface *in advance when being in the wafer state*," "the adhesive agent does not overflow the space between

the first and second semiconductor chips" and "the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip." *Id.* at 4:48–61 (emphasis added).

The '806 patent describes two embodiments. *Id.* at 6:30–12:67. In both embodiments, a thermo-compression sheet is adhered or affixed to the back surface of a wafer to form an adhesion layer "in advance" before the wafer is cut or diced to produce individual pieces of semiconductor chips with an adhesion layer, which are then stacked and bonded to each other in a multi-chip semiconductor device package. *Id.* at 9:17–50, 12:32–44.

Figure 1 of the '806 patent is reproduced below.

FIG.1

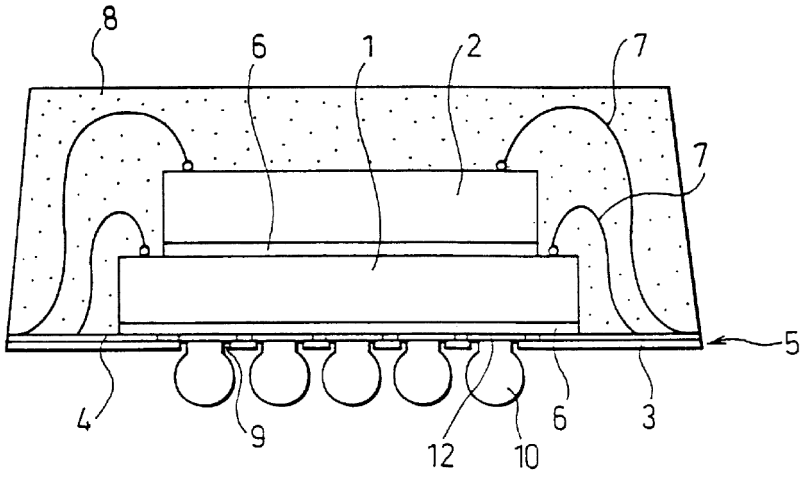


Figure 1 shows a cross-sectional view of a semiconductor device in accordance with the first embodiment of the '806 patent. *Id.* at 5:36–38.

As shown in Figure 1, in a semiconductor device of the first embodiment, "a first semiconductor chip 1 and a second semiconductor chip 2 are laminated . . . on a circuit board 5 including an insulating

substrate 3 and a wiring layer 4 mounted on the insulating substrate 3." *Id.* at 6:37–40, Fig. 1. The '806 patent refers to the surface (front surface) of a semiconductor chip on which a circuit element is formed as a "circuit formed surface" and the surface of the opposite side of the chip as a "back surface." *Id.* at 6:42–45. In the first embodiment depicted in Figure 1, semiconductor chip 1 is disposed with its back surface facing insulating substrate 3. *Id.* at 6:46–47, Fig. 1. "The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6." *Id.* at 6:47–51.

The '806 patent describes that "[w]hen the first semiconductor chip 1 is in a wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips 1." *Id.* at 9:17–21. Similarly, "[w]hen the second semiconductor chip 2 is in the wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce separate pieces of second semiconductor chips 2." *Id.* at 9:31–35.

According to the '806 patent,

> By affixing the thermo-compression sheet 6 to the back surface of the second semiconductor chip 2 in advance, accurate positioning is necessary only when mounting the second semiconductor chip 2 on the first semiconductor chip 1. Therefore, since one step requiring accurate positioning is omitted in the process for manufacturing the semiconductor device in accordance with the present embodiment, this manufacturing process is simplified compared with the conventional process in which the thermo-compression sheet 6 is disposed on the circuit formed surface of the first

> semiconductor chip 1, and then the second semiconductor chip 2 is adhered to the thermo-compression sheet 6.

Id. at 9:38–49.

Figure 10 of the '806 patent is reproduced below.

FIG.10

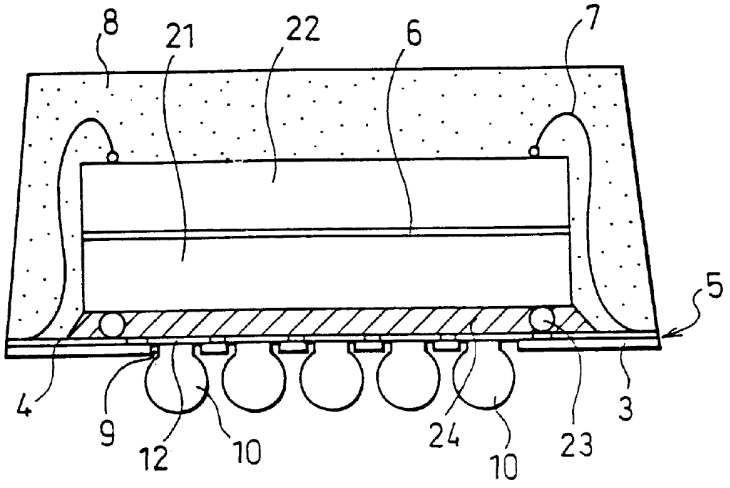


Figure 10 shows a cross-sectional view of a semiconductor device arranged in accordance with the second embodiment of the '806 patent. *Id.* at 6:6–8, 11:17–18.

As shown in Figure 10, circuit board 5 includes insulating substrate 3, and wiring layer 4 formed on the insulating substrate. *Id.* at 11:21–23. In the second embodiment, "a first semiconductor chip 21 is mounted on a circuit board 5 with its circuit formed surface facing the circuit board 5, i.e., facing down" (*id.* at 11:19–21) and "[a] second semiconductor chip 22 is mounted on the back surface of the first semiconductor chip 21 through a thermo-compression sheet 6" (*id.* at 11:23–25). In this arrangement, the back surface of second semiconductor chip 22 faces the back surface of first semiconductor chip 21. *Id.* at 11:25–27. "Namely, the back surfaces of the

first semiconductor chip 21 and the second semiconductor chip 22 are adhered to each other through the thermo-compression sheet 6." *Id.* at 11:27–29.

The '806 patent describes that "[w]hen the second semiconductor chip 22 is in a state of wafer, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips 22." *Id.* at 12:32–36. According to the '806 patent, "[l]ike the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet 6 to the back surface of the second semiconductor chip 22 in advance." *Id.* at 12:39–44.

D. Illustrative Claims

Of the challenged claims, claims 1, 2, 23, 24, and 30 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below.

> 1. A semiconductor device including a stacked package structure and a chip size package structure, comprising:
>
> an insulating substrate including a wiring layer having electrode sections;
>
> a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first adhesion layer;
>
> a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer; and
>
> each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first and

> second semiconductor chips and the wire being sealed with a resin.

Ex. 1001, 13:45–63.

E. Prior Art and Declaration Evidence

Petitioner cites the following references in its challenge to patentability:

U.S. Patent No. 4,821,944, issued Apr. 18, 1989 (Ex. 1007, "Tsumura");

U.S. Patent No. 5,323,060, issued June 21, 1994 (Ex. 1004, "Fogal");

U.S. Patent No. 7,166,495 B2, filed Feb. 20, 1996 (Ex. 1005, "Ball");

International Publication WO 1996/13066, published May 2, 1996 (Ex. 1003, "Mostafazadeh"); and

U.S. Patent No. 6,682,954 B1, filed Jan. 31, 1997 (Ex. 1009, "Ma");

U.S. Patent No. 6,014,586, filed Feb. 27, 1997 (Ex. 1008, "Weinberg"); and

U.S. Patent No. 5,790,384, filed June 26, 1997 (Ex. 1006, "Ahmad").

Petitioner also relies on additional patents listed in the Table of Exhibits, including U.S. Patent No. 4,688,075 (Ex. 1030, "Phy"), U.S. Patent No. 5,411,921 (Ex. 1031, "Negoro"), U.S. Patent No. 5,762,744 (Ex. 1032, "Shibata"), U.S. Patent No. 5,110,388 (Ex. 1033, "Komiyama"), and U.S. Patent No. 6,007,920 (Ex. 1034, "Umehara"). Pet. vi, 4.

Petitioner supports its challenge with a declaration from Jeffrey C. Suhling, Ph.D. (Ex. 1002, "Suhling Declaration"). Patent Owner has submitted a declaration from Peter Elenius (Ex. 2001, "Elenius Declaration") in support of Patent Owner's Preliminary Response.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 5–6).

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1, 2, 12, 13, 23, 24, 30	103(a)[1]	Ball, Fogal, Mostafazadeh, Knowledge of a Skilled Artisan
6, 7, 9, 10, 25, 26	103(a)	Ball, Fogal, Mostafazadeh, Ahmad, Knowledge of a Skilled Artisan
14, 15	103(a)	Ball, Fogal, Mostafazadeh, Weinberg, Knowledge of a Skilled Artisan
16–19	103(a)	Ball, Fogal, Mostafazadeh, Ma, Knowledge of a Skilled Artisan
32	103(a)	Ball, Fogal, Mostafazadeh, Tsumura, Knowledge of a Skilled Artisan

III. ANALYSIS

A. Multiple Petitions

Petitioner has filed petitions in this proceeding and in IPR2023-00071, challenging different claims of the '806 patent. *See* Pet. 2. Petitioner contends that two petitions are necessary because the '806 patent includes "numerous claims (33 in total) spanning six columns of text and 2,700+

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the '806 patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

words" and because "the numerous (8) independent claims recite two very different interconnection techniques for stacked multichip modules." *Id.* Petitioner represents that

> The current Petition challenges independent claims 1, 2, 23, 24, and 30 in addition to dependent claims 6-7, 9-10, 12-13, 14-19, 25-26, and 32—all of which recite a wire bond interconnection technique. The first Petition (IPR 2023-00071) seeks cancellation of independent claims 3, 27, and 31 in addition to dependent claims 4-5, 8, 11, 20-22, 28, 29, and 33—all of which recite using a combination of flip-chip and wire bond interconnection techniques for stacked multichip modules.

Id. at 2–3. Petitioner further states that "each claim is challenged only once." *Id.* at 3.

Patent Owner does not dispute Petitioner's contentions that two petitions are necessary. *See generally* Prelim. Resp.

On the present record, we see no reason to exercise our discretion to deny institution of either petition on the basis of Petitioner filing two petitions to address the large number of claims included in the '806 patent. *See* Patent Trial and Appeal Board Consolidated Trial Practice Guide, 59–60 (Nov. 2019)[2] (in determining whether multiple petitions are necessary, the Board may consider petitioner's explanations regarding "the differences between the petitions, why the issues addressed by the differences are material, and why the Board should exercise its discretion to institute additional petitions if it identifies one petition that satisfies petitioner's burden under 35 U.S.C. § 314(a).").

[2] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the relevant time is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical "person of ordinary skill in the art," from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct "presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan." *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Citing testimony from Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art at the priority date of the '806 patent would have had

> i) a bachelor-level degree in electrical engineering, mechanical engineering, material science, or a related subject and five or more years of experience working in the field of semiconductor packaging; ii) a Master's-level degree in mechanical engineering, electrical engineering, material science, or a related field, and at least 1-3 years of experience in the design/development of semiconductor packages; or iii) a Ph.D.-level degree in mechanical engineering, material science, electrical engineering, or a related field, and at least some experience in the area of semiconductor packaging.

Pet. 17–18 (citing Ex. 1002 ¶¶ 28–32). Petitioner further states that "[a]dditional education may substitute for professional experience, and significant work experience may substitute for formal education." *Id.* at 18.

Patent Owner's declarant, Mr. Elenius, states that a person of ordinary skill in the art would have had "a bachelor's degree in electrical, mechanical or materials engineering and two to three years of experience in the design or development of semiconductor manufacturing, or the equivalent." Ex. 2001 ¶ 32. Mr. Elenius further states that "[a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education." *Id.*

Although the proposals for the level of skill in the art by the parties' declarants have differences in wording, we do not find the proposals to be materially different. For purposes of this Decision, we find no meaningful differences between the parties' respective definitions that would materially alter the outcome of this Decision. Thus, although we do not find the parties' proposals for the level of skill in the art to be materially different, for purposes of this Decision, based on our review of the '806 patent, the types of problems and solutions described in the '806 patent, and cited prior art, we adopt and apply Petitioner's definition of the level of ordinary skill in the art.

C. Claim Construction

In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2022). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the effective filing date of the patent application and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look

principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that a person of ordinary skill in the art reading the '806 patent would understand the claim term "electrode section" recited in the challenged claims to mean "electrical terminals, usually called bond pads, that are part of the substrate's wiring layer." Pet. 16–17 (citing Ex. 1002 ¶¶ 103–107). At this time, Patent Owner does not dispute Petitioner's proposed construction of "electrode section." *See generally* Prelim. Resp. For purposes of this Decision, we need not construe the term "electrode section" because the parties do not identify any material issue that would turn on the construction. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only terms that are in controversy need to be construed, and "only to the extent necessary to resolve the controversy"); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

Patent Owner contends that the term "adhesion layer" recited in the challenged independent claims should be construed to mean "a pre-formed layer that is adhered." Prelim. Resp. 13–15. Patent Owner argues that Ball, Fogal, and Mostafazadeh do not teach "adhesion layer" under Patent Owner's proposed construction of the term. *See, e.g.*, *id.* at 16–24. Although Patent Owner's argument raises an issue of claim construction, we need not expressly construe "adhesion layer" for purposes of this Decision because, as discussed in Section III.D.5 below, Petitioner shows sufficiently

that the asserted combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan teaches or suggests "adhesion layer" even under Patent Owner's proposed claim construction. *See Vivid Techs.*, 200 F.3d at 803.

No other claim terms need to be construed expressly for purposes of this Decision.

D. Asserted Obviousness over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

Petitioner asserts that claims 1, 2, 12, 13, 23, 24, and 30 are unpatentable under § 103 over Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Pet. 29–60. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 16–36. Based on the record presented and for the reasons discussed below, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level

of skill in the art; and (4) where in evidence, so-called secondary considerations.[3] *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")); *see Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that "some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]")).

"Whether prior art invalidates a patent claim as obvious is determined from the perspective of one of ordinary skill in the art." *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1374 (Fed. Cir. 2011). Further, "the assessment of a claim's patentability is inextricably tied to a skilled artisan's knowledge and skill level." *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Permissible uses of general knowledge of one having ordinary skill under § 103 include providing a motivation to combine and supplying a claim limitation, if supported by evidence of record. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1363 (Fed. Cir. 2013); *see also Qualcomm*, 24 F.4th at 1376 (permissible uses of

[3] The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

what a skilled artisan would have known at the time of the invention include "furnishing a motivation to combine" and "supplying a missing claim limitation" (citing *Randall Mfg.*, 733 F.3d at 1363; *Koninklijke Philips*, 948 F.3d at 1337–38)).

We analyze the asserted ground based on obviousness with the principles identified above in mind.

2. Overview of Ball (Ex. 1005)

Ball describes a multi-chip semiconductor device in which semiconductor chips (called dies) are vertically stacked on top of one another using a combination of face-down (flip-chip) or face-up (wire bond) assembly arrangements. Ex. 1005, Abstract, 1:8–12, 2:16–20. According to Ball, "flip-chip attachment" refers to a method of attaching a semiconductor chip (die) to a substrate in which "the die is inverted so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate (such as a printed circuit board)." *Id.* at 1:28–32.

Figure 1 of Ball is reproduced below.

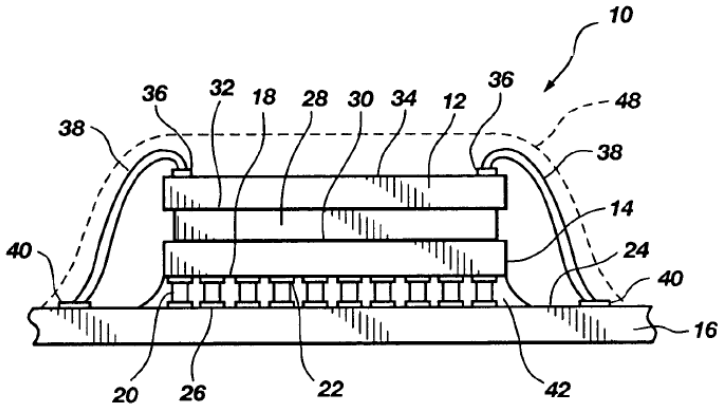


Fig. 1

Figure 1 shows a side plan view of an exemplary multi-die assembly of Ball with a flip-chip vertical stacking arrangement. *Id.* at 4:58–59, 5:1–18.

Ball describes that assembly 10 of Figure 1 comprises upper die 12, opposing lower die 14, and substrate 16. *Id.* at 5:2–3. Ball further describes that

> Fabrication of the assembly 10 comprises providing the lower die 14 having a face surface 18 with at least one flip chip electric connection 20 (such as a C4 solder bump connection, conductive polymer bump or pin connection, these and other alternatives being known in the art, by way of example) extending from a bond pad or other terminal 22 on the lower die face surface 18. The flip chip electric connections 20 extend to a surface 24 of the substrate 16 in such a manner that the flip chip electric connections 20 physically (mechanically) attach to, and make electrical contact with, lead ends, trace ends, terminals or other electrical contact elements 26 in or on the surface 24 of the substrate 16.

and that "back side 32 of the upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over a lower die back side 30." *Id.* at 5:6–20. "An adhesive requiring a curing step, such as an epoxy, is preferred, although many adhesives known in the art are suitable." *Id.* at 5:20–22.

3. Overview of Fogal (Ex. 1004)

Fogal describes multichip modules with a wire bond stacked chip assembly arrangement. Ex. 1004, Abstract.

Figure 1 of Fogal is reproduced below.

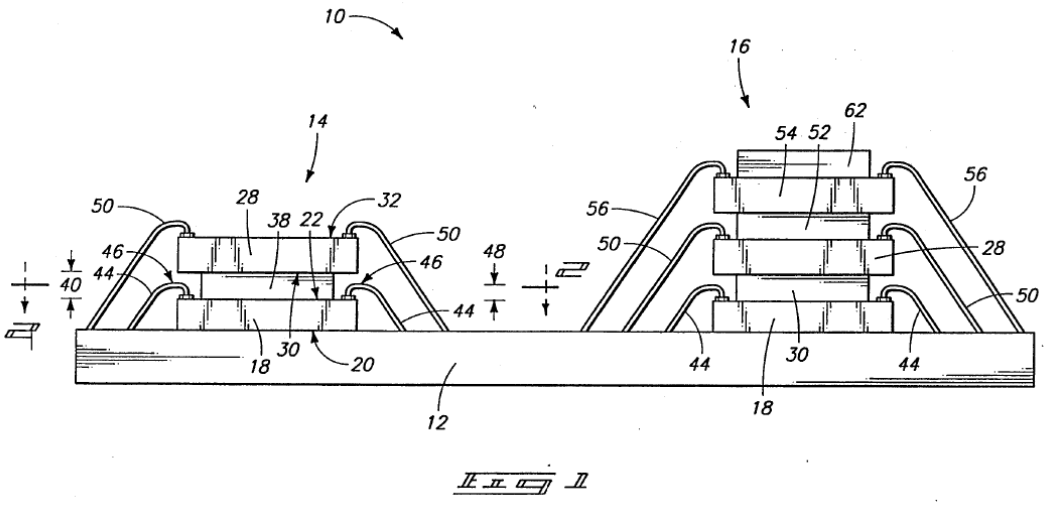


Figure 1 shows a side elevational view of an exemplary multichip module of Fogal. *Id.* at 1:45–46.

As illustrated in Figure 1, Fogal describes that base face 20 is adhered to substrate 12 by means of an adhesive, such as "epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc." *Id.* at 2:38–41. According to Fogal, bonding face 22 includes bonding pads 26 that connect first chip 18 to substrate 12 via bonding wires 44. *Id.* at 2:41–43, 2:55–63. Second chip 28 includes bonding pads 36 that connect second chip 28 to substrate 12 via bonding wires 50. *Id.* at 2:49–66.

Fogal further describes that adhesive layer 38 is interposed between and connects bonding face 22 of first chip 18 and base face 30 of second chip 28. *Id.* at 2:49–54. According to Fogal, "[e]xample materials for adhesive 38 include epoxies and tape" and "[m]ost preferred is a thermoplastic tape." *Id.* at 2:67–68.

4. Overview of Mostafazadeh (Ex. 1003)

Mostafazadeh describes a method of forming an adhesive coating on a semiconductor wafer surface. Ex. 1003, Abstract. The adhesive coating is dried, and the semiconductor wafer is diced to form several integrated circuit dies, each having an integrated circuit and an adhesive layer. *Id.*

According to Mostafazadeh, "[g]luing and taping are conventional techniques" to attach an individual die (a fabricated integrated circuit chip) to a structure (e.g., a connection substrate) during packaging of the individual chips. *Id.* at 1:22–25. Mostafazadeh states that a disadvantage of the conventional processes applying glue on an individual die during packaging is that the glue "tends to interfere with connections to the attached die by *jutting up around the die's edges*." *Id.* at 2:18–20 (emphasis added). Mostafazadeh purports to avoid this shortcoming in the conventional glue technique by applying, before a semiconductor wafer is diced to form individual dies, an adhesive coating to the entire surface of the semiconductor wafer "as opposed to an individual support surface or an individual die[,] as is common in the conventional processes." *Id.* at 8:2–5.

Mostafazadeh also discloses that "[w]hen taping is contemplated[,] the tape is typically applied . . . to the back surface of a semiconductor wafer prior to dicing." *Id.* at 2:22–23. Mostafazadeh states, however, that "tape has the drawback of being relatively expensive." *Id.* at 2:24–25.

Mostafazadeh states that "[i]n view of the forgoing, an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly and *does not jut around the edges of the die* would be advantageous." *Id.* at 2:27–29 (emphasis added).

Figure 2 of Mostafazadeh is reproduced below.

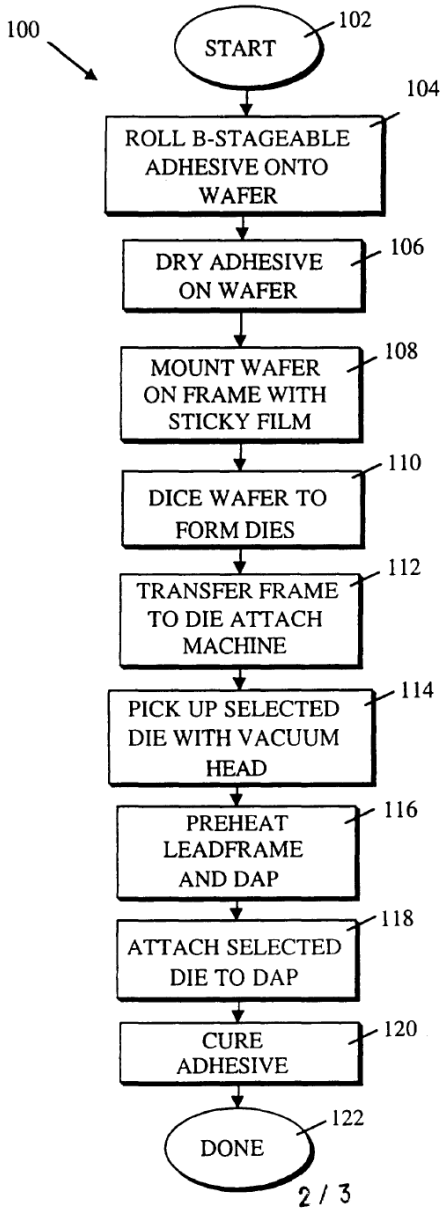


Figure 2 is a flowchart illustrating Mostafazadeh's exemplary method of attaching an integrated circuit[4] die to a support surface. *Id.* at 4:15–16.

The process of Mostafazadeh's Figure 2 begins with step 102 in which a multiplicity of integrated circuits are fabricated on a semiconductor

[4] Mostafazadeh refers to an integrated circuit as "IC." Ex. 1003, 9:20.

wafer. *Id.* at 5:22–23. Mostafazadeh describes that after fabrication of the ICs on the semiconductor wafer, an adhesive is then rolled onto a mounting surface (i.e., the surface opposite to the IC formed surface) of the wafer "to form an adhesive coating thereon in a rolling step 104." *Id.* at 5:23–25. According to Mostafazadeh, the disclosed process "insures that an adhesive coating . . . is formed over the entire wafer surface." *Id.* at 6:29–7:1. Mostafazadeh further describes that "in some embodiments, the adhesive may be a B-stageable epoxy." *Id.* at 3:22–23.

Mostafazadeh describes that "[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid." *Id.* at 6:3–4. But "once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106," which "turns the adhesive coating into a *hard surface*" if "the adhesive is good B-stageable epoxy." *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as "hardened").

The wafer is then cut or diced into a multiplicity of dies or IC chips in dicing step 110. *Id.* at 7:29–8:1. After the dicing step, each die has an integrated circuit and an adhesive layer that includes the dried adhesive coating. *Id.* at 8:1–2. The result of dicing the semiconductor wafer in step 110 to form several integrated circuit dies 174 is shown in Figure 5c. *Id.* at 8:5–6.

Figure 5c of Mostafazadeh is reproduced below.

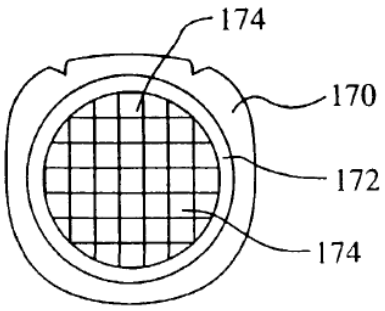


Fig. 5c

Figure 5c is a top view illustrating the result of dicing step 110 of Figure 2 forming a multiplicity of integrated circuit dies. *Id.* at 5:7–8.

According to Mostafazadeh, as the result of applying adhesive to a wafer, drying the coating to form a hardened layer, and dicing the wafer to the chip size, the adhesive layer on each individual chip is "*exactly the same size* as the mounting surface of the die." *Id.* at 9:15–16 (emphasis added). Thus, "when the die is attached to its supporting surface" during packaging of individual chips, "the adhesive *does not extend beyond* a mounting surface of *the die*." *Id.* at 9:16–18 (emphases added).

Figure 6a of Mostafazadeh is reproduced below.

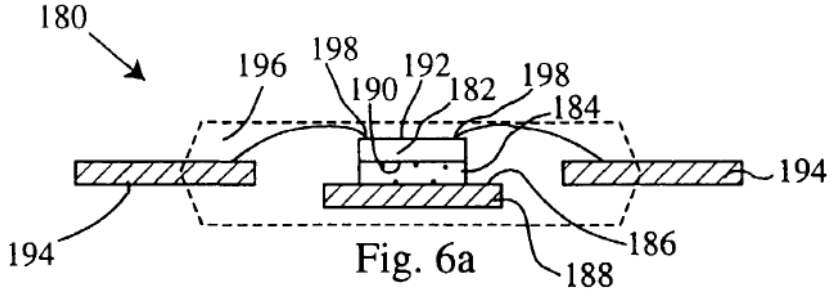


Fig. 6a

Figure 6a is a diagrammatic cross sectional side view of an exemplary packaged integrated circuit with a die attached to a support surface by an adhesive layer. *Id.* at 5:10–12.

As shown in Figure 6a, in packaged integrated circuit 180, die 182 is attached to its support surface 188 via adhesive layer 184. *Id.* at 10:4–5. "The *adhesive layer 184* covers an entire mounting surface 190 of the selected integrated circuit die 182 and *does not extend beyond a boundary* of the mounting *surface 190*." *Id.* at 10:6–8 (emphases added). Mostafazadeh further describes that "more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)." *Id.* at 11:16–18.

5. Independent Claim 1 as Obvious over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

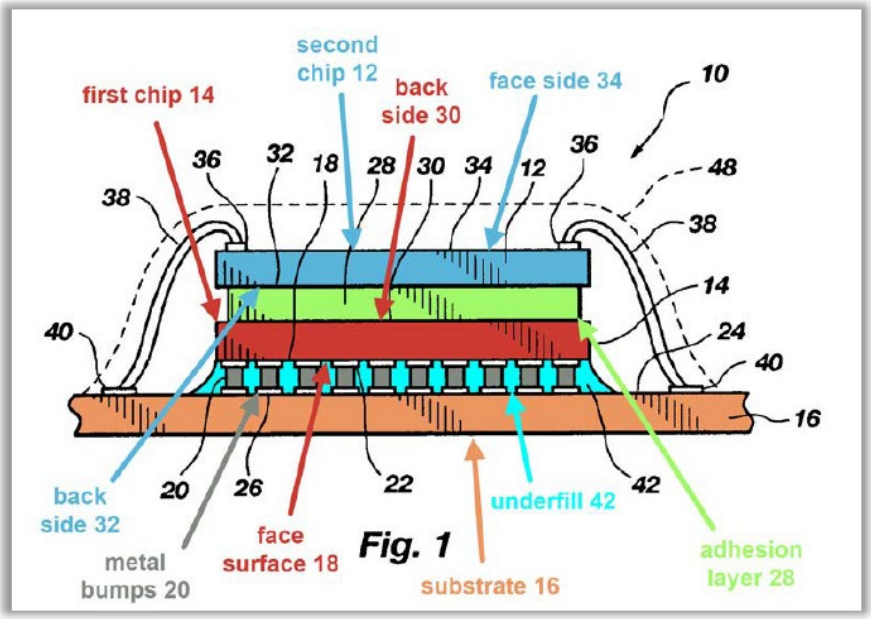
Petitioner contends that the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan teaches or suggests all elements of claim 1 and that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh with the knowledge of a skilled artisan to arrive at the subject matter recited in claim 1. Pet. 29–50. At this stage of the proceeding, Patent Owner contests Petitioner's showings only on the limitations of claim 1 reciting "adhesion layer" and the reasons to combine the references. Prelim. Resp. 16–36.

a. Petitioner's Assertions

In its proposed combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan, Petitioner relies on Ball and Fogal as teaching all of the elements of claim 1, except for the limitations reciting "adhesion layer," for which Petitioner further relies on Mostafazadeh and the knowledge of one of ordinary skill in the art. Pet. 33–50.

Specifically, Petitioner asserts that Ball and Fogal teach or suggest all elements of claim 1 relating to the assembly of a stacked package arrangement of semiconductor chips in a semiconductor device. Pet. 33–50.

Figure 1 of Ball as annotated by Petitioner is reproduced below.



Pet. 37. Annotated Figure 1 of Ball reproduced above, illustrates Petitioner's alleged identification in Ball of the structural arrangement of a semiconductor device recited in claim 1. *Id.* at 18–19, 33–50.

Petitioner contends that Ball's Figure 1 discloses stacked die multichip module 10 (the recited "semiconductor device") comprising upper die 12 (the claimed "second semiconductor chip") and opposing lower die 14 (the claimed "first semiconductor chip"). Pet. 19 (citing Ex. 1005, 4:58–59, 5:3–6, Fig. 1). Petitioner further asserts that Ball's Figure 1 discloses "[a] semiconductor device including a stacked package structure and a chip size package structure," as recited in the preamble of claim 1, because "Ball is directed to a 'stacked package structure' where dies are

vertically stacked on top of one another in either a face-down (flip chip) or face-up (chip-on-board) configuration." *Id.* at 33 (citing Ex. 1005, Title, Abstract, 1:8–12, 2:16–20, 3:33–37, 3:41–42, claim 1).

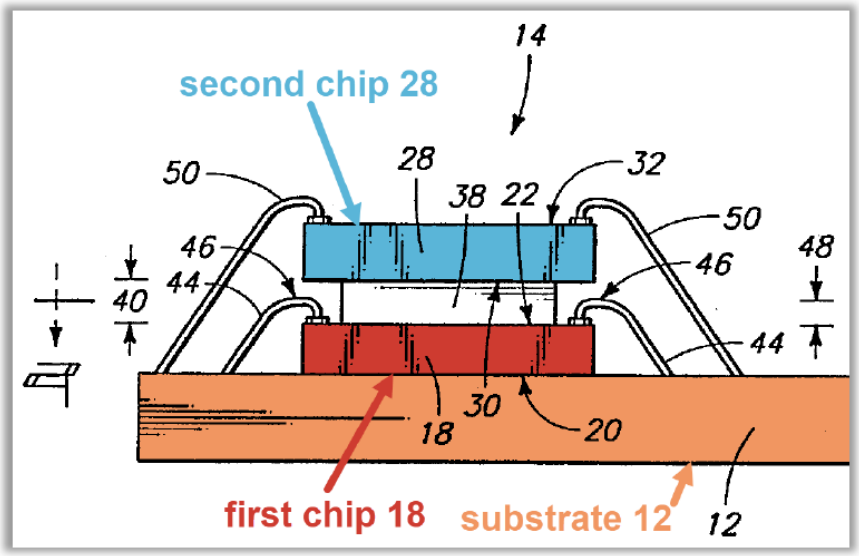
Petitioner next asserts that substrate 16 shown in Ball's Figure 1 teaches "an insulating substrate" recited in claim 1 because Ball describes substrate 16 as "insulating." Pet. 37 (citing Ex. 1005, 5:37–40; Ex. 1002 ¶¶ 243–250). Additionally, Petitioner contends that "lead end or trace end patterns 26 aligned with the bump connections 22 on the front surface 18 of lower die 14" assembled on top surface 24 of substrate 16, as depicted in Ball's Figure 1, teach the recited "wiring layer." *Id.* at 35 (citing Ex. 1005, 3:51–53, 5:12–18, Fig. 1).

Petitioner also asserts that Ball describes terminals 26 and 40 (the claimed "electrode sections") are used to electrically connect first die 14 to the substrate's wiring layer, as part of the wiring layer located on top of substrate 16. Pet. 36–37 (citing Ex. 1005, 5:51–55). In addition, Petitioner contends that "[t]erminals 40 are the claimed 'electrode sections' that are part of the wiring layer on substrate 16 for wire bonding the upper chip 12 to the substrate 16." *Id.* at 36.

Petitioner argues that Ball, therefore, teaches or suggests "an insulating substrate including a wiring layer having electrode sections," as recited in claim 1. Pet. 35–37 (citing Ex. 1002 ¶¶ 243–250).

Next, addressing limitations "a first semiconductor chip . . . mounted on said wiring layer" and "a second semiconductor chip . . . mounted on a circuit-formed front surface of said first semiconductor," Petitioner relies on the combination of Ball and Fogal.

Figure 1 of Fogal as annotated by Petitioner is reproduced below.



Fogal - Figure 1

Pet. 39. Annotated Figure 1 of Fogal reproduced above, illustrates Petitioner's alleged identification in Fogal of the structural arrangement of a semiconductor device recited in claim 1.

Petitioner asserts that Figure 1 of Fogal discloses multichip stack 14 (the recited "semiconductor device") comprised of first chip 18 (the claimed "first semiconductor chip") adhered to substrate 12 and second chip 28 (the claimed "second semiconductor chip") adhered to the top of first chip 18. Pet. 38 (citing Ex. 1004, 1:46–47, 2:31–36, Fig. 1). Petitioner further argues that Fogal's Figure 1 discloses that opposed base 30 of second chip 28 faces bonding face 22 of first chip 18—in other words, "the backside of second chip is adhered to the front surface (surface with semiconductor circuitry and bond pads) of the first chip." *Id.* at 45–46 (citing Ex. 1004, 2:44–54, 2:63–66, Fig. 1).

Petitioner argues that a person of ordinary skill in the art would have understood that

> Ball's lower die having an adhesive backside could be used in two ways including: (1) mounting the first chip's adhesive backside directly to a substrate in a face-up orientation, or (2) mounting the first chip using flip-chip bump interconnections so that a second chip is mounted to the first chip's adhesive backside.

Pet. 39. Petitioner further argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball and Fogal to "attach the first chip's adhesive backside to the wiring layer on the substrate and build the multichip module from there, understanding that using the face-up orientation and wire bond interconnection techniques provides additional options for designing multichip modules." *Id.* at 39–40 (citing Ex. 1002 ¶¶ 251–261).

Next, Petitioner asserts that Ball and Fogal teach "each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire," as recited in claim 1, because "Ball's Figure 1 explicitly shows the bond pads 36 of the second chip connected by wire 38 to electrode sections 40" and "Fogal's Figure 1 also shows second chip 28 wire bonded to substrate 12 through wires 50." Pet. 47 (citing Ex. 1005, 5:23–27, Fig. 1; Ex. 1004, 2:63–66, Fig. 1).

Petitioner further contends that Ball teaches or suggests "said first and second semiconductor chips and the wire being sealed with a resin," as recited in claim 1, because Ball discloses sealing or encapsulating the stacked chips and wires. Pet. 48. To support its contention, Petitioner cites Ball's disclosure that "[a]n encapsulant is generally used to cover the bond wires and metal tape leads to prevent contamination." *Id.* (citing Ex. 1005, 4:5–10). According to Petitioner, the terms "encapsulation" and "sealing"

are used interchangeably in the semiconductor industry. *Id.* at 50 (citing Ex. 1002 ¶¶ 265–275).

Finally, addressing the limitations reciting "a first semiconductor chip having a first adhesion layer adhered to its back surface" and "a second semiconductor chip having a second adhesion layer adhered to its back surface," Petitioner asserts that Fogal teaches the recited "adhesion layer" that is "adhered to" the back surface of the semiconductor chips because Fogal discloses that "an adhesive, such as epoxy, thermoplastic materials, *tape, tape coated with thermoplastic materials*, etc.," is adhered to base face 20 of chip 18 (the claimed "first semiconductor chip") and that "adhesive layer 38 is interposed between . . . first chip bonding face 22 and second chip base face 30." Pet. 38 (emphasis added) (citing Ex. 1004, 2:36–41), 40 (citing Ex. 1004, 2:28–43), 45–46 (citing Ex. 1004, 2:49–54).

Petitioner further asserts that Fogal teaches "said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer," as recited in claim 1, because Fogal discloses that "the backside of second chip is adhered to the front surface (surface with semiconductor circuitry and bond pads) of the first chip through an adhesion layer." Pet. 46 (citing Ex. 1004, 2:49–54).

Petitioner further argues that claim 1 "simply requires a first chip '*having a first adhesion layer adhered to its back surface*' and is not limited—in any way—as to when or how the adhesive is applied." Pet. 42. Nonetheless, Petitioner contends that, to the extent it is required to show that "the first semiconductor chip must have a *pre-applied adhesive backside*," Mostafazadeh discloses a wafer-level fabrication process that results in pre-applied adhesive backsides on individual chips (*id.* (emphasis added)),

which was also well-within the knowledge of a skilled artisan at the time of the invention of the '806 patent (*id.* at 42–43).

Petitioner asserts that "by 1998, the idea of forming an adhesive *thin film* on the backside of a wafer was decades old and was used by industry leaders like Fairchild Semiconductor and National Semiconductor as early as 1983." Pet. 42–43 (emphasis added). Petitioner contends that "Mostafazadeh is just one example of the many patents that teaches this process." *Id.* at 43.

Referencing Figure 2 of Mostafazadeh (reproduced above in Section III.D.4), Petitioner asserts that Mostafazadeh discloses a process in which a multiplicity of integrated circuits are fabricated on a semiconductor wafer and "an adhesive is then rolled onto a mounting surface of the wafer to form an adhesive coating." Pet. 43 (citing Ex. 1003, 6:8–24, Fig. 2). Petitioner further asserts that in Mostafazadeh's process, the adhesive coating is then dried and the wafer is cut into a "**multiplicity of dies**," "**producing individual pieces of dies having 'an integrated circuit and an adhesive layer.**'" *Id.* at 43–44 (citing Ex. 1003, 7:28–8:6, Fig. 5c).

Citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have understood "how to apply adhesive to the backside of a wafer to produce individual chips, like those used in Ball and Fogal, having circuitry on one side and a pre-applied adhesive on the other." *Id.* at 44 (citing Ex. 1002 ¶¶ 251–261).

Addressing the reasons to combine Ball, Fogal, and Mostafazadeh, Petitioner asserts that all three references are in the same field of semiconductor devices, and more specifically, multichip modules. Pet. 29. Petitioner further explains that Ball and Fogal solve the same problem:

producing higher performance, lower cost, and smaller semiconductor packages, whereas Mostafazadeh provides a process that makes vertically stacking chips more efficient. *Id.* at 29–30 (citing Ex. 1005, 2:26–31; Ex. 1004, 1:22–31; Ex. 1003, 1:13–30). Petitioner argues, therefore, a person of ordinary skill in the art would have looked to these references to design a smaller, cheaper, and denser multichip module. *Id.* at 30.

As discussed above, Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Ball's teaching of advanced stacking orientations for semiconductor chips with Fogal's teaching of mounting chips in a face-up orientation because the combination would provide "additional creative options . . . for configuring high-density multichip modules." Pet. 30–31; *see also id.* at 39–40 (citing Ex. 1002 ¶¶ 251–261).

Citing the testimony of Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art would have combined Ball and Fogal with Mostafazadeh because Ball and Fogal teach vertically stacking chips and Mostafazadeh teaches a method for producing individual chips with adhesive back surfaces that would simplify the stacking processes in Ball and Fogal. *Id.* at 31 (citing Ex. 1002 ¶¶ 55–57).

As discussed above, Petitioner asserts that the process of applying thin films to the backsides of wafers to create chips with adhesive backsides for mounting to substrates "was well-within the knowledge of a skilled artisan, and was nothing more than a common-sense fabrication step." Pet. 32 (citing Ex. 1002 ¶¶ 62–69). Petitioner argues that "Mostafazadeh is just one example of the many patents that teaches this process." *Id.* at 43.

Petitioner argues that Mostafazadeh explicitly recommends using its adhesive process to efficiently build multichip modules. Pet. 32 (citing Ex. 1003, 11:16–18 ("In addition, more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)."")). Petitioner asserts, therefore, a person of ordinary skill in the art would have been motivated to combine the teachings of Mostafazadeh, Ball, and Fogal, with a reasonable expectation of success, to utilize Mostafazadeh's process resulting in hundreds of individual chips with adhesive backsides for use in building the vertical chip stacks and multichip modules described in Ball and Fogal because using chips with adhesive backsides would make building multichip modules more efficient. *Id.* at 32–33 (citing Ex. 1002 ¶¶ 230–239).

Petitioner further contends that, given Mostafazadeh's express teaching of using semiconductor chips produced by its wafer-level process to build multichip modules, a person of ordinary skill in the art would have been motivated to combine, with a reasonable expectation of success, Mostafazadeh's adhesive application process resulting in hundreds of chips with adhesive backsides with Ball's teaching of mounting chips in a multichip module and Fogal's teaching of mounting the lower chip's backside on the substrate in a face-up orientation. Pet. 33 (citing Ex. 1002 ¶¶ 230–239).

b. Patent Owner's Arguments and Our Analysis

At this stage of the proceeding, Patent Owner contests Petitioner's showings only on the limitations of claim 1 reciting "adhesion layer" and the

reasons to combine the references. Prelim. Resp. 16–36. We address each of Patent Owner's arguments in turn.

First, Patent Owner asserts that the claim term "adhesion layer" recited in claim 1 should be construed to mean "a pre-formed layer that is adhered." Prelim. Resp. 13–15. According to Patent Owner, the '806 patent distinguishes a liquid or semi-liquid viscous adhesive agent from a solid sheet. *Id.* at 14 (citing Ex. 1001, 2:23–58, Fig. 14(b)). Petitioner disagrees and argues that the term "adhesion layer" should be accorded its plain and ordinary meaning. Reply 3. Petitioner argues that, to the extent express construction of this term is necessary, the plain and ordinary meaning of "adhesion layer" is "a layer that adheres" in view of the '806 patent's intrinsic record. *Id.*

Addressing Petitioner's reliance on Fogal as teaching the "adhesion layer" recited in claim 1, Patent Owner contends that Fogal does not disclose "some sort of solid sheet that is adhered to the back surface of a semiconductor chip," as allegedly required under Patent Owner's proposed construction of the term "adhesion layer." Prelim. Resp. 18. Citing the testimony of Mr. Elenius, Patent Owner asserts that "[t]he adhesives taught by Fogal, such as *epoxy*, are of the conventional structure and one of the very problems the '806 patent sought to solve." *Id.* (emphasis added) (citing Ex. 2001 ¶ 73).

As discussed above, Petitioner relies on Fogal's disclosure of "an adhesive, such as epoxy, thermoplastic materials, *tape, tape coated with thermoplastic materials*, etc.," as teaching the "adhesion layer" recited in claim 1. Pet. 38 (emphasis added) (citing Ex. 1004, 2:36–41), 40 (citing Ex. 1004, 2:28–43). Fogal further discloses that "[e]xample materials for

adhesive 38 include epoxies and *tape*" and that "*[m]ost preferred* is a *thermoplastic tape*." Ex. 1004, 2:67–68 (emphases added).

Patent Owner's argument is unavailing because Patent Owner focuses only on epoxy described in Fogal and does not address Petitioner's reliance on Fogal's disclosures of "tape, tape coated with thermoplastic materials" or "thermoplastic tape" as teaching the recited "adhesion layer."

Patent Owner further asserts that although "Fogal teaches a tape and a tape coated with thermoplastic materials," "[a person of ordinary skill in the art] reading this entire sentence would understand *the tape to be an adhesive to adhere things, not a pre-formed layer that is adhered*." Prelim. Resp. 21 & n.2 (emphasis added) (citing Ex. 1004, 2:36–41; Ex. 2001 ¶ 68). We are not persuaded by Patent Owner's argument because Patent Owner does not explain why a tape or thermoplastic tape is not "a pre-formed layer that is adhered."

In his Declaration, Mr. Elenius likewise does not explain why a tape or thermoplastic tape is not a "a pre-formed layer that is adhered." Mr. Elenius states that "[a]s to the 'tape' and 'tape coated with thermoplastic materials' disclosed by Fogal, I would understand when reading this entire sentence that *the tape is an adhesive to adhere things, not a pre-formed layer that is adhered*," but does not explain the basis for his understanding or provide any supporting evidence for his testimony. Ex. 2001 ¶ 68 (emphasis added). Thus, Mr. Elenius's testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (expert testimony that "merely repeats,

verbatim, the conclusory assertion for which it is offered to support [and] does not cite to any additional supporting evidence or provide any technical reasoning to support [the] statement . . . is entitled to little weight") (precedential); *see also Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997) (nothing requires a fact finder to credit the inadequately explained testimony of an expert).

Patent Owner further contends that "a [person of ordinary skill in the art] would recognize that the method of Fogal would likely result in the very adhesive overflow problem the '806 patent seeks to solve." Prelim. Resp. 24 (citing Ex. 2001 ¶ 73).

In his Declaration, Mr. Elenius states that "Fogal falls into the category of conventional structure described by the '806 patent" because "[m]ore often than not, the method of Fogal results in the very adhesive overflow problem the '806 patent seeks to solve," where "the adhesive will overflow to exceed the boundaries of the entire bottom surface of a chip." Ex. 2001 ¶ 73. Mr. Elenius, however, does not cite any supporting evidence for his statements. *See id.* Thus, Mr. Elenius's testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65.

Further, as discussed below, Patent Owner's argument and Mr. Elenius's testimony are contrary to the express disclosures of Fogal.

Figure 1 of Fogal is reproduced below.

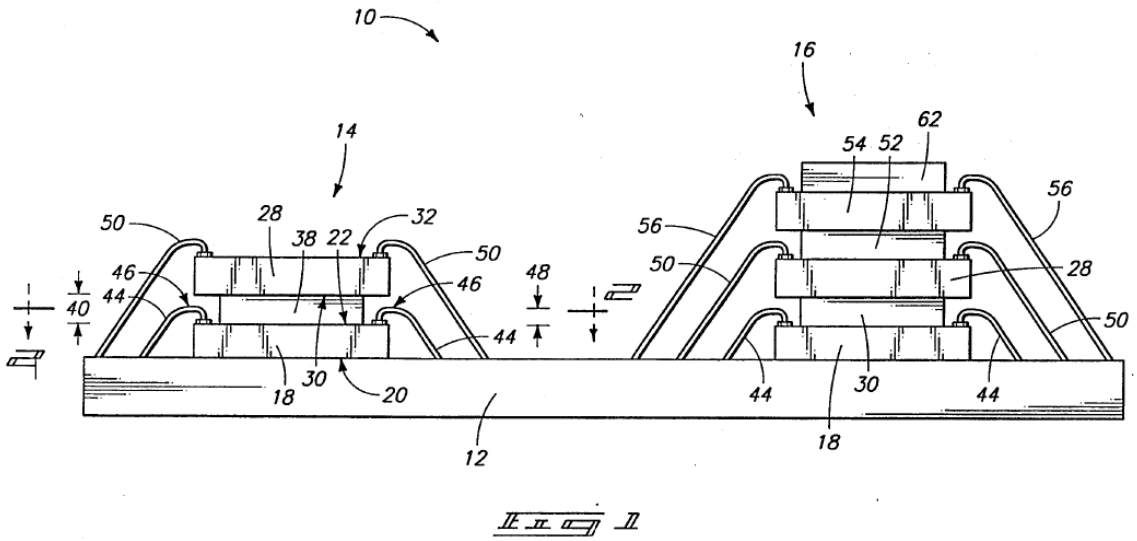


Figure 1 shows a side elevational view of an exemplary multichip module of Fogal. Ex. 1004, 1:45–46.

As discussed above, Petitioner relies on Fogal's disclosure of "adhesive layer 38 . . . interposed between . . . first chip bonding face 22 and second chip base face 30" as teaching the recited "adhesion layer" that is "adhered to" the back surface of the second semiconductor chip, where the second semiconductor chip is mounted on the front surface of the first semiconductor chip "through the second adhesion layer." Pet. 45–46 (citing Ex. 1004, 2:49–54). As shown in Figure 1 of Fogal reproduced above, Fogal explicitly discloses that adhesive layer 38 *remains within* the boundaries of first chip 18 and second chip 28 when second chip 28 is mounted on first chip 18 through adhesive layer 38. Ex. 1004, Fig. 1.

Neither Patent Owner nor Mr. Elenius explains why, contrary to the express disclosure of Fogal, Fogal's adhesive layer 38 using a tape or thermoplastic tape would *overflow beyond* the boundaries of the chips during mounting of the chips in a multichip package. Thus, Patent Owner's

argument is unpersuasive because it is contrary to the express disclosure of Fogal.

Next, Patent Owner asserts that Fogal does not teach "a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed," as recited in claim 1, because "a reference *must show* that an adhesion layer extends to cover the *entire* portion of back surface of the first semiconductor chip where a circuit is not formed." Prelim. Resp. 19–20 (emphases added) (citing Ex. 1001, 6:48–51, Fig. 1). Patent Owner similarly argues that Fogal does not teach "a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed," as recited in claim 1, because Fogal does not disclose "an adhesion layer that covers the *entire* back surface of the second chip where a circuit is not formed." *Id.* at 26 (emphasis added).

Claim 1, however, does not recite "a first adhesion layer adhered to [the first semiconductor chip's] *entire* back surface where a circuit is not formed" or "a second adhesion layer adhered to [the second semiconductor chip's] *entire* back surface where a circuit is not formed."

The cited portion of the '806 patent states "[t]he second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that *its back surface* is adhered to the thermo-compression sheet 6." Ex. 1001, 6:48–51 (emphasis added). Thus, there is no description in the cited portion that the adhesion layer is adhered to the entire back surface of the second semiconductor chip. As to Figure 1 of the '806 patent cited by Patent Owner, although Figure 1 appears to show that thermo-compression sheet 6 is approximately the size of second semiconductor 2,

the '806 patent states that Figure 1 describes "the first embodiment of the present invention." *Id.* at 5:36–38.

A particular embodiment appearing in the written description is generally not incorporated into a claim if the claim language is broader than the embodiment. *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (citation omitted). Further, "it is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Epos Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014). Thus, based on the current record, to the extent there is disclosure in the Patent Owner-cited portions of the Specification indicating that the thermo-compression sheet covers the entire back surface of the semiconductor chips, such disclosure does not limit claim 1 to the feature described in the Specification but not recited in the claim.

Lastly, addressing the limitations reciting "a wiring layer having electrode sections" and "each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire," Patent Owner contends that Fogal does not teach "each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire," because "for Fogal to disclose the limitation, it must have a wiring layer in its substrate 12 for the bond wires to connect to" and "Petitioner has provided no evidence that such a wiring layer with an electrode section is present in Fogal." Prelim. Resp. 28.

Patent Owner's argument does not undermine Petitioner's showing because Petitioner relies on Ball as teaching "a wiring layer having electrode

sections" and further relies on the combination of Ball and Fogal as teaching "each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire," as recited in claim 1. Pet. 35–37 (citing Ex. 1005, 3:51–53, 5:12–18, 5:51–55, Fig. 1), 46–47 (citing Ex. 1005, 5:23–27, Fig. 1; Ex. 1004, 2:63–66, Fig. 1). A finding of obviousness cannot be overcome "by attacking references individually where the rejection is based upon the teachings of a combination of references." *Bradium Techs. LLC v. Iancu*, 923 F.3d 1032, 1050 (Fed. Cir. 2019) (quoting *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986)).

As discussed above, Petitioner argues that claim 1 "simply requires that the first semiconductor chip has '*an adhesion layer adhered to its back surface*' and is not limited—in any way—as to when or how the adhesive is applied." Pet. 42. Nonetheless, Petitioner contends that if it is required to show that "the first semiconductor chip must have a *pre-applied adhesive backside*," Mostafazadeh discloses a wafer-level fabrication process that results in pre-applied adhesive backsides on individual chips (*id.* (emphasis added)), which was also well-within the knowledge of a skilled artisan at the time of the invention of the '806 patent (*id.* at 42–43).

Considering the claim language of claim 1 as a whole, *see Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999) ("Proper claim construction . . . demands interpretation of the entire claim in context, not a single element in isolation."), we agree with Petitioner that claim 1 does *not* recite *when* or *how* the "adhesion layer" is "adhered to [the first semiconductor chip's] back surface."

Patent Owner appears to argue that the "first semiconductor chip" with "an adhesion layer adhered to its back surface," as recited in claim 1,

must have been created "in advance," e.g., by a wafer-level fabrication process, *before* the chip is mounted in the recited semiconductor device. Patent Owner argues that the patentee recognized that applying a paste or thermo-compression sheet on individual chips during packaging (i.e., mounting of the chips during packaging) caused the "overflow" and "gap" problems. Sur-reply 2 (citing Ex. 1001, 2:16–24, 2:44–46). According to Patent Owner, "the patentee further recognized that merely switching to a pre-formed solid sheet alone would not solve the problem" because using a thermo-compression sheet on an individual chip for mounting during packaging "results in the same problem as using an adhesive due to the inability to place the chip accurately on the thermo-compression sheet." *Id.* at 2–3 (citing Ex. 1001, 2:49–56). Thus, Patent Owner argues that the '806 patent proposes a two-fold solution: "Use a preformed solid sheet ***and*** attach that sheet to the back surface of the wafer first" during the wafer fabrication process "before cutting and placing the chip" in a multichip package. *Id.* at 3 (underlined emphases added). Patent Owner asserts, therefore, "a first semiconductor chip having . . . an adhesion layer adhered to its back surface," as recited in claim 1, must have a pre-formed adhesion layer adhered to its back surface "in advance" before mounting the chip in a multichip package, such as a solid thermo-compression sheet applied to the backside of wafer during wafer-level fabrication processing before the chips are produced by dicing. Prelim. Resp. 13–14; Sur-reply 2–3.

We note, however, that claim 1 does not recite a "wafer," placing "an adhesion layer on a back surface of a wafer," or producing semiconductor chips by dicing or cutting the wafer. *See* Ex. 1001, 13:45–63. Nor does the claim recite any limitations indicating when or how an "adhesion layer" is

"adhered to [the first semiconductor chip's] back surface." Thus, at least based on the claim language, claim 1 does not require the recited semiconductor chips with an adhesion layer to have been produced "in advance" before the chips are mounted in the recited semiconductor device.

Nonetheless, for purposes of this Decision, we need not and do not decide whether claim 1 is limited as Patent Owner contends because, as discussed below, Petitioner shows sufficiently that the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan teaches or suggests all elements of claim 1 even under Patent Owner's proposed claim construction.

Patent Owner does not dispute that Mostafazadeh discloses a wafer-level fabrication process that results in creating individual chips with adhesive backsides "in advance" before the chips are created and subsequently used for mounting in a package. Patent Owner asserts instead that Mostafazadeh's wafer-level fabrication process does not teach an "adhesion layer" as recited in claim 1 because "Mostafazadeh discloses an adhesive that is rolled onto a semiconductor wafer 160 using a roller 150 to form an adhesive coating 164." Prelim. Resp. 18–19 (citing Ex. 1003, 3:7–8, 6:25–29, Fig. 4a). Patent Owner argues that "[a] roll coated epoxy is not a layer that is adhered" and, therefore, does not teach an "adhesion layer" under Patent Owner's claim construction. *Id.* at 19 (citing Ex. 2001 ¶¶ 56, 68).

As discussed above, however, Petitioner persuasively relies on Fogal's disclosure of tape or thermoplastic tape as teaching the recited "adhesion layer" that is "adhered." Pet. 38, 46. In addition, as Patent Owner acknowledges, Mostafazadeh expressly contemplates applying tape to the

back surface of a semiconductor wafer prior to dicing. Ex. 1003, 2:22–23 ("When *taping is contemplated*[,] the tape is typically applied . . . to the back surface of a semiconductor wafer prior to dicing.") (emphasis added); Prelim. Resp. 32 (citing Ex. 1003, 2:22–29). In other words, Mostafazadeh discloses that in its wafer-level fabrication process, an adhesive tape may be applied on the back surface of a wafer instead of applying epoxy and drying it to form an adhesive layer. Thus, Mostafazadeh also provides an express motivation to combine the teachings of Fogal and Mostafazadeh to utilize adhesive tapes or thermoplastic tapes in Mostafazadeh's process.

Additionally, Petitioner further relies on Phy, Negoro, Shibata, Komiyama, and Umehara for their teachings of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet on a wafer's backside to form an adhesive layer, as part of the general knowledge of a skilled artisan in the asserted ground of obviousness over Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Pet. 32 (citing Ex. 1002 ¶¶ 62–69), 42–43. For example, in the cited paragraphs of his Declaration, Dr. Suhling discusses Shibata as follows:

> In a third example, U.S. Patent No. 5,762,744 ("Shibata")—another Rohm Co. Ltd. patent, with a priority date of 1991—teaches that to save processing steps, *a preform layer of expandable film is applied to the backside of a wafer*. The wafer is diced and when the chips are picked up from the expandable tape, the preformed material remains adhered onto the bottom of each chip allowing the chip to be die-bonded onto a leadframe.

Ex. 1002 ¶ 65 (emphasis added) (citing Ex. 1032, 1:38–55). Dr. Suhling further explains that Komiyama teaches adhering a tape to a wafer backside, dicing and mounting the chip to a leadframe via the adhesive on its backside:

> In accordance with another aspect of the invention there is provided a method for using the above-mentioned adhesive tape, which method comprises the steps of **adhering a semiconductor wafer to said adhesive tape, dicing said wafer into chips together with the adhesive layer of said adhesive tape**, irradiating the adhesive layer of said tape with an energy beam, **picking up the chips together with pieces of the diced adhesive layer adhered thereto from said base sheet, placing the chips on a leadframe so that the respective pieces of the adhesive layer may come in contact with said leadframe, and causing the pieces of the diced adhesive layer to again develop tackiness by heating thereby securely mounting the chips on said leadframe**.
>
> In the method according to the invention, the adhesive tape according to the invention serves as a dicing tape for holding the wafer in position during the dicing step. Each piece of the diced and cured adhesive layer, that is attached to each chip and capable of being tackified by heating, provides an adhesive for securely mounting the chip on the leadframe in the die-bonding step.

Id. ¶ 66 (citing Ex. 1033, 2:16–29).

Dr. Suhling also discusses Umehara at length. According to Dr. Suhling, Umehara explains problems encountered by conventional techniques using adhesives as:

> In the die bonding step, the picked up IC chips are fixed on IC chip mount zones (simply, mount zones) of a leadframe by means of an IC chip bonding adhesive such as an epoxy adhesive, a polyimide adhesive or a silver paste which is fed in the form of a viscous liquid to form an adhesive coat on the mount zones, followed by being subjected to the wire bonding step and resin mold step, thereby obtaining a semiconductor device. **However, when the size of each of the IC chips is very small, it is difficult to uniformly apply an appropriate amount of adhesive with the use of the above liquid adhesive, so that the adhesive outflows the IC chips. On the other hand, when the size of each of the IC chips is very large, the use of the above**

> **liquid adhesive has encountered the problems such that the amount of the adhesive is short to thereby disenable bonding which ensures a satisfactory bonding strength**.

Ex. 1002 ¶ 67 (underlined emphases added) (citing Ex. 1034, 1:45–2:4).

Dr. Suhling explains that, to solve this problem, Umehara describes:

> A film adhesive of a polyimide type resin having excellent heat resistance has been proposed for use in the bonding of IC chips to the leadframe. Further, it has been proposed to employ a dicing sheet comprising a substrate film and, detachably laminated thereto, such an adhesive for bonding of IC chips, which dicing sheet can simultaneously be used in dicing and die bonding. In the first process for producing a semiconductor device according to the present invention, initially, the bonding sheet 10 is fixed on a dicing apparatus by means of the ring frame 5, **and a thermocompression bonding of one side of a silicon wafer 6 is conducted to the polyimide adhesive layer 4 of the bonding sheet 10.** The thermocompression bonding is conducted under the above conditions. **Subsequently, the above silicon wafer 6 is cut into IC chips by the use of cutting means such as a dicing saw (refer to FIG. 4).** The cutting depth is determined taking into account the thickness of the silicon wafer 6, the polyimide adhesive layer 4, the processing film for polyimide type resin 3 and the dicing saw wear. Thereafter, the bonding sheet 10 is expanded so that the IC chip spacings are enlarged to thereby facilitate the pickup of IC chips, as shown in FIG. 5. The pickup of IC chips enables peeling from the processing film for polyimide type resin 3 the IC chips in the state of having the cut polyimide adhesive layer sticking thereto on their backs. That is, the adhesive strength between the IC chips and the polyimide adhesive layer is greater than that between the polyimide adhesive layer and the processing film for polyimide type resin, so that the IC chips can be peeled in the state of having the polyimide adhesive layer sticking thereto on their one sides from the processing film for polyimide type resin.
> . . . .
>
> **The resultant IC chips having the polyimide adhesive layer sticking thereto are placed on a leadframe in a manner such**

that the polyimide adhesive layer is interposed between the IC chips and the leadframe.

Id. ¶ 68 (citing Ex. 1034, 7:3–27, 7:46–50).[5] Dr. Suhling opines that "[t]hese examples demonstrate that the idea of applying an adhesive layer to the backside of a wafer for various purposes was well-known in the state of the art and well within the knowledge of a [person of ordinary skill in the art]." Ex. 1002 ¶¶ 129–130. As discussed above, citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have known how to apply these techniques well-known to a skilled artisan to the teachings of Ball, Fogal, and Mostafazadeh. Pet. 44; Ex. 1002 ¶¶ 258, 260.

In view of Petitioner's argument and the evidence presented, we interpret the Petition as relying on Phy, Negoro, Shibata, Komiyama, and Umehara for their teachings of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet on a wafer's backside to form an adhesive layer, as part of the general knowledge of a skilled artisan in the asserted ground of obviousness over Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. *See Koninklijke Philips*, 948 F.3d at 1338 (finding that the Board properly determined that the challenged claims would have been obvious over SMIL 1.0 "in light of the general knowledge

[5] In other words, Umehara, like the '806 patent, recognized the "overflow" and "gap" problems of the conventional method in which "the adhesive outflows the IC chips" during packaging. *See* Ex. 1034, 1:45–2:4; Ex. 1001, 2:16–24, 2:44–46; Sur-reply 2 (citing Ex. 1001, 2:16–24, 2:44–46). Also, like the '806 patent, Umehara discloses an improved method that solves this problem by affixing a thermo-compression bonding sheet to a backside of a wafer "in advance" and dicing the wafer to produce IC chips with an adhesive layer. *See* Ex. 1034, 7:3–27, 7:46–50; Sur-reply 3.

of a skilled artisan" when "the Board relied on expert evidence, which was corroborated by Hua, in concluding that pipelining was not only in the prior art, but also within the general knowledge of a skilled artisan"); *see also Lone Star Silicon Innovations LLC v. Iancu*, 809 F. App'x 773, 777 (Fed. Cir. 2020) (finding that the petitioner properly relied on additional references in an asserted ground of obviousness over Watatani and Tanaka when "the additional references were being relied on exclusively for their teachings about what was well-known in the art") (nonprecedential).

As discussed above, Mostafazadeh expressly contemplates applying tape to the back surface of a semiconductor wafer prior to dicing. Ex. 1003, 2:22–23. In view of this disclosure in Mostafazadeh, we alternatively interpret Petitioner's citation to Phy, Negoro, Shibata, Komiyama, and Umehara as providing evidence of what a person of ordinary skill in the art would have understood Mostafazadeh's disclosure of using tape to teach. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1372–73 (Fed. Cir. 2019). That is, a person of ordinary skill in the art reading Mostafazadeh would have known that Mostafazadeh's taping method may be implemented using the well-known techniques of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet to the back surface of a semiconductor wafer prior to dicing, as described in detail in Phy, Negoro, Shibata, Komiyama, and Umehara. Under these circumstances, Petitioner need not "demonstrate a sufficient motivation to combine the . . . references," i.e., a motivation to combine Ball, Fogal, and Mostafazadeh with Phy, Negoro, Shibata, Komiyama, and Umehara. *See Realtime Data*, 912 F.3d at 1373.

Patent Owner argues that Mostafazadeh teaches away from using an adhesive tape in the proposed combination because Mostafazadeh states that

tape has the drawback of being expensive. Prelim. Resp. 32 (citing Ex. 1003, 2:22–25; Ex. 2001 ¶ 93). Although Mostafazadeh states "tape has the drawback of being *relatively expensive*" (Ex. 1003, 2:24–25 (emphasis added)), economic costs do not necessarily counsel against a beneficial combination or modification, unless there was some technological incompatibility that prevented the combination or a significant technical challenge that would teach away from the combination. *See Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1013 (Fed. Cir. 1983) ("[T]he fact that the two disclosed apparatus would not be combined by businessmen *for economic reasons* is not the same as saying that it could not be done because skilled persons in the art felt that there was some technological incompatibility that prevented their combination. Only the latter fact is telling on the issue of nonobviousness." (emphasis added)). In addition, "the teaching away inquiry does not focus on whether a person of ordinary skill in the art would have merely favored one disclosed option over another disclosed option." *Bayer Pharma AG v. Watson Lab'ys, Inc.*, 874 F.3d 1316, 1327 (Fed. Cir. 2017). "In assessing whether prior art teaches away, that better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes." *Id.* (quotation marks omitted) (citation omitted). "When there are only two possible formulations and both are known in the art at the time, the fact that there may be reasons a skilled artisan would prefer one over the other does not amount to a teaching away from the lesser preferred but still *workable option*." *Id.* (emphasis added).

Citing the testimony of Mr. Elenius, Patent Owner further contends that "a tape cannot be coated on using the Mostafazadeh's fabrication

method." Prelim. Resp. 32 (citing Ex. 2001 ¶ 93). In the cited paragraph of his Declaration, Mr. Elenius states that "a tape cannot be coated on using the Mostafazadeh's fabrication method," but does not explain why or provide any supporting evidence for his testimony. Ex. 2001 ¶ 93. Thus, Mr. Elenius's testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65; *Xerox*, Paper 9 at 15.

At this stage of the proceeding, based on the current record, we determine that Mostafazadeh's statement that "tape has the drawback of being relatively expensive" is not likely to amount to teaching away, absent a persuasive showing of some technological incompatibility or a significant technical challenge in using an adhesive tape, film, thermoplastic tape, or thermo-compression sheet in the wafer-level fabrication process of Mostafazadeh. The parties are invited to brief this issue further during trial.

Patent Owner further asserts that a person of ordinary skill in the art would not have been motivated to combine Ball, Fogal, and Mostafazadeh with a reasonable expectation of success because "the combination would not result in a functioning semiconductor device." Prelim. Resp. 29.

First, Patent Owner argues that the proposed combination of Mostafazadeh with Fogal fails "because the resulting structure would deform and even short-circuit the bond wires extending from the substrate to the top surface of the first (lower) semiconductor chip." Prelim. Resp. 29 (citing Ex. 2001 ¶ 90). To illustrate its argument, Patent Owner presents an annotated figure illustrating the purported combined multichip structure of Mostafazadeh with Fogal. *Id.* at 30.

Patent Owner's argument is unavailing because, as discussed above, Petitioner relies on Fogal and Ball, not Mostafazadeh, as teaching the claim

elements relating to the assembly of a semiconductor device with a stacked package arrangement of semiconductor chips. Pet. 33–42, 44–50.

In addition, to the extent Patent Owner's argument is premised on physical incorporation of Mostafazadeh's structure into Fogal's multichip structure, we disagree with Patent Owner because "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference . . . . Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) (*quoting In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Next, Patent Owner argues that the combination of Ball, Fogal, and Mostafazadeh would fail "because all three references teach an adhesive, which when applied to the back surface of the semiconductor chip and mounted . . . could overflow." Prelim. Resp. 31.

Patent Owner's argument does not undermine Petitioner's showing because, as discussed above, Petitioner persuasively relies on Fogal's disclosure of tape or thermoplastic tape as teaching the recited "adhesion layer" that is "adhered." Pet. 38, 46.

In addition, Petitioner also relies on Phy, Negoro, Shibata, Komiyama, and Umehara for their teachings of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet on a wafer's backside as part of the general knowledge of a skilled artisan in the asserted ground of obviousness over Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Pet. 32 (citing Ex. 1002 ¶¶ 62–69), 42–43.

Moreover, Patent Owner's argument is unavailing because it is contrary to the express disclosures of Mostafazadeh. For instance, Dr. Suhling testifies that a person of ordinary skill in the art would have known that using individual chips with adhesive backsides created by Mostafazadeh's process would have been beneficial because the adhesive layer on the chips "does not '*jut around the edges of the die*.'"[6] Ex. 1002 ¶ 132 (citing Ex. 1003, 2:26–28). As set forth below, Petitioner further argues persuasively that this feature of Mostafazadeh is similar to the purported improvement over conventional technique described in the '806 patent—to avoid overflowing of adhesive beyond the edges of the chips.

> [L]ike the '806 patent, Mostafazadeh describes its inventive process as "an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly ***and does not jut around the edges of the die***[.]" (*Compare* Mostafazadeh at 2:27-29 (describing "an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly") *with* the '806 patent at 4:8-10 (describing the need to avoid "a situation where the excessively applied adhesive agent overflows the space between the first and second semiconductor chips."); *see also* (Mostafazadeh at 2:27-29, 3:29-4:1 ("The adhesive layer material substantially does not extend beyond the mounting area boundary."), 9:15-18, 10:6-8.)

Pet. 22–23 (underlined emphases added); *see also* Ex. 1002 ¶ 114.

As discussed above in Section III.D.4, in Mostafazadeh's process, although "[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid" (Ex. 1003, 6:3–4), "once

[6] The verb "jut" means "to (cause to) stick out, especially above or past the edge or surface of something." Cambridge English Dictionary, https://dictionary.cambridge.org/us/dictionary/english/jut. Ex. 3003, 1.

the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106," which "turns the adhesive coating into a *hard surface*" if "the adhesive is good B-stageable epoxy." *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as "hardened"). Thus, according to Mostafazadeh, "when the die is attached to its supporting surface" during packaging of individual chips, "the adhesive *does not extend beyond* a mounting surface of *the die*." *Id.* at 9:16–18 (emphases added). In other words, Mostafazadeh expressly discloses that its process results in creating individual semiconductor chips with a solidified adhesive layer that does *not* extend or overflow beyond the edges of the chips during packaging.

Thus, Patent Owner's argument directed to Mostafazadeh is not persuasive because it is contrary to express disclosures of Mostafazadeh.

Patent Owner also asserts that "Mostafazadeh did not recognize, foresee, or try to solve the problem of adhesive overflow to cover the bond pads." Prelim. Resp. 33.

Contrary to Patent Owner's assertion, Mostafazadeh states that a disadvantage of the conventional processes applying glue on an individual die during packaging is that the glue "tends to interfere with connections to the attached die by *jutting up around the die's edges*." Ex. 1003, 2:18–20 (emphasis added). Mostafazadeh further states that "[i]n view of the forgoing, an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly and *does not jut around the edges of the die* would be advantageous." *Id.* at 2:27–29 (emphasis added). Thus, Patent Owner's argument is unavailing because it is contrary to express disclosures of Mostafazadeh.

Patent Owner further asserts that in Mostafazadeh "the die attach pad that the chip is to be mounted to," i.e., the substrate or supporting structure of a semiconductor package, is pre-heated just before the die is attached, which "*could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads." Prelim. Resp. 32–33 (emphasis added) (citing Ex. 1003, 9:10–13; Ex. 2001 ¶ 94). In the cited paragraph of his Declaration, Mr. Elenius states that

> Mostafazadeh teaches a method of mounting that requires pre-heating and flash heating immediately prior to and during mounting, *possibly* causing overflow and covering of the bond pads. Mostafazadeh explains, the die attach pad that the chip is to be mounted to should be pre-heated or flash heated just before the epoxy-covered die is attached. In one embodiment that uses a B-stage adhesive, this heating will cause "the B-stageable adhesive dried in step 106 [to] reflow to form a stronger bond between the integrated circuit die and a die attach pad during the attachment step 118." This reflowing *could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads.

Ex. 2001 ¶ 94 (emphases added) (citing Ex. 1003, 9:10–13). In the next paragraph following that cited by Patent Owner and Mr. Elenius, however, Mostafazadeh discloses that "when *the die is attached* to its supporting surface *the adhesive does not extend beyond a mounting surface of the die*." Ex. 1003, 9:16–18 (emphases added). Neither Patent Owner nor Mr. Elenius addresses this express disclosure of Mostafazadeh that appears contrary to Patent Owner's assertions, nor do they explain adequately why the solidified adhesive layer of Mostafazadeh nonetheless "*could* cause the adhesive used to overflow past the edge of the chip." Thus, based on the current record, we find Patent Owner's argument and Mr. Elenius's testimony to be

unpersuasive because they are at best speculative and contrary to the express disclosure of Mostafazadeh.

Lastly, Patent Owner contends that a person of ordinary skill in the art would have expected the combination of Ball, Fogal, and Mostafazadeh to fail because "Mostafazadeh did not contemplate multi-chip stacking and the accompanying multiple step chip-to-substrate and chip-to-chip mounting." Prelim. Resp. 33 (citing Ex. 2001 ¶ 97). In the cited paragraph of his Declaration, Mr. Elenius opines

> The statement in Mostafazadeh that its process can be used when "more than one integrated circuit die [is] packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)" appears to be mere speculation. At the time of Mostafazadeh's filing MCPs and MCMs were most commonly planar structures versus stacked semiconductor chip structures.

Ex. 2001 ¶ 97. Mr. Elenius, however, does not explain the basis for his testimony or cite supporting evidence. Thus, Mr. Elenius's testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65.

In his Declaration, Dr. Suhling testifies that given the express teachings in Mostafazadeh about using its adhesive process to efficiently build multichip modules such as MCPs or MCMs, a person of ordinary skill in the art would have been motivated to combine the teachings of Mostafazadeh and Ball, with a reasonable expectation of success, to utilize Mostafazadeh's process resulting in hundreds of individual chips with adhesive backsides for use in building the vertical chip stacks and multichip modules described in Ball. Ex. 1002 ¶ 134 (citing Ex. 1003, 11:16–18); Pet. 32. Dr. Suhling further explains that MCPs or MCMs—which are "3-D packaged" devices with vertically stacked IC chips—were known in the art

well before 1998. Ex. 1002 ¶¶ 58–61 (discussing vertically stacked 3-D package devices described in various prior art references (citing Ex. 1025, 220; Ex. 1027, 110; Ex. 1028, Fig. 4A; Ex. 1029, 110, Fig. 3)). Based on the current record, we find Dr. Suhling's testimony credible and supported by the evidence Dr. Suhling cites.

c. Conclusion as to Claim 1 as Obvious over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

Based on the current record and for the foregoing reasons, we determine, for purposes of this Decision, that Petitioner has shown sufficiently that the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan teaches or suggests all elements of claim 1. We also find, for purposes of this Decision, Petitioner has provided sufficient explanation and evidence to show that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh with the knowledge of a skilled artisan, as proposed by Petitioner, with a reasonable expectation of success.

Accordingly, based on the current record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claim 1 under 35 U.S.C. § 103 as obvious over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan.

6. Independent Claims 2, 23, 24, and 30 as Obvious over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

Independent claims 1 and 2 recite substantially similar limitations, except that claim 2 recites "a first semiconductor chip having a paste applied to its back surface." *Compare* Ex. 1001, 13:45–63, *with id.* at 13:64–14:13. Independent claims 23, 24, and 30 also recite limitations that are similar to

those in claim 1, except that claims 23, 24, and 30 recite "forming" an "adhesion layer on a back surface of a wafer" and producing semiconductor chips "by dicing" or "by dicing the wafer." *See* Ex. 1001, 16:29–17:7, 17:58–18:16.

For independent claims 2, 23, 24, and 30, Petitioner cites to and relies on its analysis regarding Petitioner's application of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan to claim 1. Pet. 51–52, 54–60. Patent Owner similarly addresses independent claims 1, 2, 23, 24, and 30 together, raising the same arguments directed to all five independent claims. Prelim. Resp. 17–36.

Based on the current record and for the reasons discussed above with respect to claim 1, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to independent claims 2, 23, 24, and 30 under 35 U.S.C. § 103 as obvious over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan.

7. Dependent Claims 12 and 13 as Obvious over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

Claim 12 depends from claim 1 and claim 13 depends from claim 12. Petitioner asserts that Fogal teaches or suggests the additionally recited limitations of claims 12 and 13. Pet. 52–53. Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 12 and 13 is taught in Fogal, which we find sufficiently persuasive on the current record and at this stage of the proceeding. *Id.*

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to independent claim 1 discussed above. *See* Prelim. Resp. 16–36.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 12 and 13 as unpatentable under § 103 over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan.

E. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Ahmad, and the Knowledge of a Skilled Artisan

Claim 6 depends from claim 1 and claim 9 depends from claim 6. Claim 7 depends from claim 2 and claim 10 depends from claim 7. Claim 25 depends from claim 23 and claim 26 depends from claim 24.

Petitioner asserts that claims 6, 7, 9, 10, 25, and 26 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, Ahmad, and the knowledge of a skilled artisan. Pet. 60–66.

Ahmad discloses a semiconductor chip package comprising vertically-stacked dies on top of a substrate. Ex. 1006, Abstract, 3:62–63. Ahmad describes fabricating interposers 60 from a material that has the same, or substantially the same, thermal coefficient of expansion as die 20 and die 30. *Id.* at 4:65–5:3.

Petitioner explains that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, Mostafazadeh, Ahmad, with the knowledge of a skilled artisan because Ahmad relates to semiconductor devices and specifically teaches vertically stacking semiconductor chips on top of one another to create multichip modules. Pet. 60 (citing Ex. 1006, 1:5–7, 3:11–27). According to Petitioner, Ahmad also solves the same problem as Ball, Fogal, and Mostafazadeh—producing higher performance, lower cost, and smaller semiconductor packages. *Id.* (citing Ex. 1004, 1:14–21; Ex. 1005, 2:26–31; Ex. 1003, 2:27–29; Ex. 1006, 1:62–67; Ex. 1002

¶ 314). Petitioner asserts that Ahmad teaches using an interposer as a support member when stacking a larger chip on top of a smaller one and that this arrangement of chips (i.e., a bigger chip on top of a smaller chip) allows for more efficient wiring configurations. *Id.* at 61 (citing Ex. 1006, Fig. 2, 2:1–34, 4:40–49, 5:8–25; Ex. 1002 ¶¶ 313–316).

Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 6, 7, 9, 10, 25, and 26 is taught in Ahmad, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 61–66.

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to independent claims 1, 2, 23, and 24 discussed above. *See* Prelim. Resp. 36–37.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 6, 7, 9, 10, 25, and 26 as unpatentable under § 103 over the combination of Ball, Fogal, Mostafazadeh, Ahmad, and the knowledge of a skilled artisan.

F. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Weinberg, and the Knowledge of a Skilled Artisan

In this asserted ground of obviousness, Petitioner adds the teachings of Weinberg to the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan and challenges dependent claims 14 and 15 as obvious over the combination of Ball, Fogal, Mostafazadeh, Weinberg and the knowledge of a skilled artisan. Pet. 67–70.

Claim 14 depends from claim 12 and claim 15 depends from claim 13. As discussed above in Section III.D.7, Petitioner has shown a reasonable

likelihood of prevailing with respect to its challenge to claims 12 and 13 as unpatentable under § 103 over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Petitioner contends that Weinberg teaches or suggests the additional limitations recited in dependent claims 14 and 15. Pet. 68–70.

Weinberg describes a semiconductor package having vertically integrated components placed on a substrate surface and "configured to increase packaging density of the components." Ex. 1008, Abstract.

Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 14 and 15 is taught in Weinberg, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 68–70.

Petitioner also explains that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan further with Weinberg because Weinberg is directed to a method of increasing packaging density of a vertically-stacked electronic package by wire bonding the chips in the stack to the substrate surface using a unique layout that minimizes the amount of space required, thereby resulting in a smaller footprint. Pet. 67–68. Citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have recognized that the disclosures of Ball and Fogal, both of which disclose wire bonding to a substrate surface, would benefit from the innovative technique of Weinberg. *Id.* at 68 (citing Ex. 1002 ¶ 329). Petitioner asserts, therefore, a person of ordinary skill in the art would have been motivated to combine, with a reasonable expectation of success, Weinberg's teaching of "optimiz[ing] use of substrate surface area by

combining vertically-stacked chips with a unique substrate conductive layout" with the vertically-stacked packages of Ball and Fogal. *Id.* (citing Ex. 1008, 3:29–34; Ex. 1002 ¶¶ 327–330).

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to independent claims 1 and 2 discussed above. *See* Prelim. Resp. 37.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 14 and 15 as unpatentable under § 103 over the combination of Ball, Fogal, Mostafazadeh, Weinberg, and the knowledge of a skilled artisan.

G. Asserted Obviousness over Ball, Mostafazadeh, Ma, and the Knowledge of a Skilled Artisan

Claims 16 and 18 depend from claim 12 and claims 17 and 19 depend from claim 13. As discussed above in Section III.D.7, Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 12 and 13 as unpatentable under § 103 over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Petitioner contends that Ma teaches or suggests the additional limitations recited in dependent claims 16–19. Pet. 72–75.

Ma describes mounting a patch die on the top surface of a primary die in a semiconductor package "to achieve an upgrade, modify chip operating parameters[,] or remedy a design or fabrication problem" of the primary die. Ex. 1009, Abstract, 1:14–19, 4:18–25. Petitioner provides detailed analysis showing where it contends each additional limitation of dependent

claims 16–19 is taught in Ma, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 72–75.

Petitioner explains that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan further with Ma because "Ma is directed to a method of upgrading, modifying, and/or remediating chips contained in semiconductor packages like the ones described in Ball and Fogal." Pet. 71 (citing Ex. 1009, 1:12–19). Petitioner also explains that a person of ordinary skill in the art would have understood that Ma's teachings would be useful if the packages disclosed in Ball or Fogal needed to be upgraded, modified, or fixed. *Id.* (citing Ex. 1009, 4:5–8).

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to independent claims 1 and 2 discussed above. *See* Prelim. Resp. 37.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 16–19 as unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Ma, and the knowledge of a skilled artisan.

H. Asserted Obviousness over Ball, Mostafazadeh, Tsumura, and the Knowledge of a Skilled Artisan

In this asserted ground of obviousness, Petitioner adds the teachings of Tsumura to the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan and challenges claim 32 as obvious over the combination of Ball, Fogal, Mostafazadeh, Tsumura, and the knowledge of a skilled artisan. Pet. 75–79.

Claim 32 depends from claim 30. Petitioner contends that Tsumura teaches or suggests the limitations additionally recited in dependent claim 32. Pet. 76–79. Tsumura describes a thermo-compression bonding method for bonding a wire onto a material such as an aluminum electrode of a semiconductor chip. Ex. 1007, Abstract, 2:28–30. Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claim 32 is taught in Tsumura, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 76–79. Petitioner also explains that a person of ordinary skill in the art would have looked to Tsumura for details on how to wire-bond the various components in the multichip modules of Ball and Fogal. *Id.* at 76. Petitioner explains persuasively that a person of ordinary skill in the art would have been motivated to combine Tsumura with the combination of Ball, Fogal, and Mostafazadeh, and the knowledge of a skilled artisan because Tsumura provides an efficient, straightforward, wire-bonding technique that complements the wire-bonding steps already used in Ball, Fogal, and Mostafazadeh and known in the art. *Id.* (citing Ex. 1002 ¶¶ 345–347).

Patent Owner does not respond specifically to Petitioner's challenge to claim 32 beyond Patent Owner's arguments advanced with respect to independent claim 30 discussed above. *See* Prelim. Resp. 38.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claim 32 as unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Tsumura, and the knowledge of a skilled artisan.

IV. CONCLUSION

For the foregoing reasons, taking into account the arguments and evidence presented in Preliminary Response, Reply, and Sur-reply, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in proving that at least one challenged claim of the '806 patent is unpatentable. Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

At this stage of the proceeding, we have not made a final determination as to the patentability of any of the challenged claims. Our final determination will be based on the record as fully developed during trial.

V. ORDER

In consideration of the foregoing, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is hereby instituted as to claims 1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, and 32 of the '806 patent on all grounds presented in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, commencing on the entry date of this Decision.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES, LLC,
Patent Owner.

IPR2023-00072
Patent RE38,806 E

Before MINN CHUNG, JULIA HEANEY, and SHELDON M. McGEE, *Administrative Patent Judges*.

McGEE, *Administrative Patent Judge*, concurring.

I concur with the majority's decision to institute trial in this proceeding. Although, in my view, the current record supports Patent Owner's claim construction of the phrase "adhesion layer" as "a pre-formed layer that is adhered," Petitioner relies on prior art in this proceeding that is

different than that relied on in IPR2023-00071 and IPR2023-00073.[7] Specifically, Petitioner cites to Fogal's "adhesive, such as . . . tape [and] tape coated with thermoplastic materials" to evince the claimed adhesion layer. Pet. 38, 42.

Like the majority, I am unpersuaded by Patent Owner's arguments at this preliminary stage that Fogal's tape does not constitute the claimed "adhesion layer." Namely, Patent Owner has not persuasively argued how Fogal's tape is not "a pre-formed layer that is adhered" consistent with Patent Owner's claim construction. Prelim. Resp. 17–18; Ex. 2001 ¶ 68. Rather, Patent Owner focuses on Fogal's epoxy adhesive. Prelim. Resp. 18.

Unlike the majority, however, I am disinclined at this point in the proceeding to consult Mostafazadeh's disclosure regarding the conventional use of tapes because Petitioner does not appear to expressly rely on that teaching to evince the claimed adhesion layer. Maj. Op. at 42–43, 47 (citing Mostafazadeh, 2:22–23). Moreover, to the extent that the majority opinion relies on Mostafazadeh's disclosure of a rollable liquid or semi-liquid adhesive that is cured to constitute the claimed "adhesion layer," I respectfully do not join in that analysis here for the reasons I provided in my dissenting opinions in each of IPR2023–00071 and IPR2023-00073. *See,* e.g., Maj. Op. at 15–16 ("Petitioner shows sufficiently that the asserted

[7] In those IPRs, I dissented from the majority view that Petitioner's proffered arguments and evidence—particularly with respect to Mostafazadeh—are sufficient to demonstrate a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. My dissenting opinions focused on what I perceive to be sufficient distinction in the '806 patent and family member '879 patent between an "adhesion layer" recited in the claims and an "adhesive agent" such as liquid or semi-liquid adhesives, e.g., an epoxy.

combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan teaches or suggests 'adhesion layer' even under Patent Owner's proposed claim construction"); *id.* at 22–23, 50–54 (discussing details of Mostafazadeh's process of rolling a fluid-based adhesive onto a surface, then drying the adhesive).

In any event, I agree with the majority that we need not construe the phrase "adhesion layer" for purposes of institution here because even adopting Patent Owner's construction, Fogal appears to disclose the claimed "adhesion layer."

Thus, because Petitioner has established a reasonable likelihood of prevailing with respect to at least one claim, I concur with my colleagues' decision to institute trial in this proceeding.

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