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Paper 42
Entered: May 13, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00072
Patent RE38,806 E

Before ELIZABETH M. ROESEL, JULIA HEANEY, and SHELDON M. McGEE, *Administrative Patent Judges*.

HEANEY, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, and 32 (the "challenged claims") of U.S. Patent No. RE38,806 E (Ex. 1001, "the '806 patent"). We instituted this *inter partes* review as to all challenged claims. Paper 16 ("Dec. on Inst.").

Katana Silicon Technologies LLC ("Patent Owner") filed a Patent Owner Response (Paper 29, "PO Resp."); Petitioner filed a Reply to the Patent Owner Response (Paper 30, "Pet. Reply"); and Patent Owner filed a Sur-reply (Paper 31, "PO Sur-reply"). Petitioner filed the Declaration of Jeffrey C. Suhling, Ph.D (Ex. 1002) in support of the Petition. Patent Owner filed the Declaration of Peter Elenius in support of its Response (Ex. 2014). The parties also filed transcripts of the depositions of Dr. Suhling (Ex. 2012) and Mr. Elenius (Ex. 1037).

Petitioner moved to exclude four exhibits submitted by Patent Owner (Paper 35, "Mot. Exclude"). Patent Owner responded (Paper 36, "Opp. Mot.").

An oral hearing was held on February 15, 2024, and a transcript of the hearing is included in the record. Paper 41 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, and 32 of the '806 patent. For the reasons discussed below, we hold that Petitioner has demonstrated by a preponderance of the evidence that these claims are not patentable.

A. Real Parties-in-Interest

Petitioner identifies Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC as the real parties-in-interest. Pet. 2. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

A. Related Proceedings

According to the parties, the '806 patent is the subject of the following district court litigation: *Katana Silicon Techs. LLC v. Micron Tech., Inc.*, 1:22-cv-00282 (D. Idaho). Paper 5, 1; Pet. 2.

The '806 patent is one of several patents owned by Patent Owner that are challenged by Petitioner in various petitions for *inter partes* review, including in IPR2023-00072, IPR2023-00073, and IPR2023-00105.

B. The '806 patent

The '806 patent describes a miniaturized semiconductor device having a chip size package (CSP) that includes multiple semiconductor chips stacked vertically inside the package (in an arrangement called a stacked package structure). Ex. 1001, 1:15–20, 1:53–65, 2:63–65.

Figure 14(a) of the '806 patent is reproduced below.

FIG.14(a)

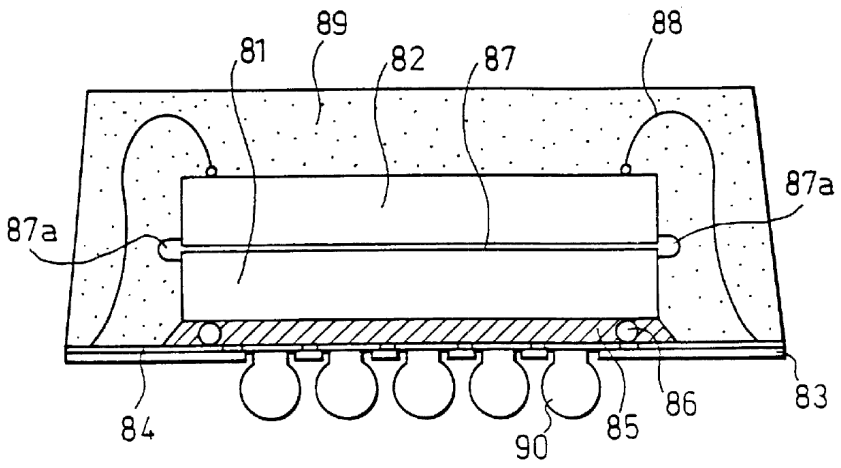


Figure 14(a) shows a cross-sectional view of a conventional semiconductor device having a stacked package structure. *Id.* at 6:24–26.

The '806 patent describes that in a conventional semiconductor device where multiple semiconductor chips are stacked and laminated, two different methods are used to bond the laminated semiconductor chips to each other in a stacked package—"an adhesive agent (paste) potting method" and "a method using a thermo-compression sheet." *Id.* at 2:16–21. According to the '806 patent, in the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent may spread and overflow beyond the outer edge of the semiconductor chips, as illustrated in Figure 14(a) (showing adhesive agent 87 between semiconductor chips 81 and 82 overflowing beyond the edges of the chips). *Id.* at 2:23–29. Such overflown adhesive agent may come in contact with wires in the package or the electropad of the semiconductor chips. *Id.* at 2:30–42. The '806 patent describes that "[o]n the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82 . . . causing problems such as separation of the semiconductor chip 82 from the

semiconductor chip 81." *Id.* at 2:44–48.

According to the '806 patent, the conventional method using a thermo-compression sheet for bonding semiconductor chips during packaging also has shortcomings. *Id.* at 2:49–56, 4:12–21. In the conventional method, the thermo-compression sheet is disposed on the surface of a first semiconductor chip, and then a second semiconductor chip is adhered to the thermo-compression sheet. *Id.* at 9:46–50. The '806 patent describes that in the conventional thermo-compression sheet method, the thermo-compression sheet must have the same size as semiconductor chip 82 and must be placed accurately at a specific location on semiconductor chip 81. *Id.* at 2:49–53. "In addition, the semiconductor chip 82 must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet." *Id.* at 2:53–56.

The '806 patent purports to avoid these problems or complications in the conventional method by forming an adhesion layer "in advance" on a back surface of a wafer when the semiconductor chips are in a "wafer state" during the semiconductor fabrication process before the wafer is cut or diced to produce individual chips. *Id.* at 4:18–63. Specifically, the '806 patent describes

> [a] method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:
>
> (a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;
>
> (b) producing separate first semiconductor chips from the first wafer by dicing;
>
> (c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;

(d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;
(e) producing separate second semiconductor chips from the second wafer by dicing;
(f) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;
(g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;
(h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and
(i) sealing the first and semiconductor chips and the wires.

Id. at 4:25–47.

According to the '806 patent, "[w]ith the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface *in advance when being in the wafer state*," "the adhesive agent does not overflow the space between the first and second semiconductor chips" and "the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip." *Id.* at 4:48–61 (emphasis added).

The '806 patent describes two embodiments. *Id.* at 6:30–12:67. In both embodiments, a thermo-compression sheet is adhered or affixed to the back surface of a wafer to form an adhesion layer "in advance" before the wafer is cut or diced to produce individual pieces of semiconductor chips with an adhesion layer, which are then stacked and bonded to each other in a multi-chip semiconductor device package. *Id.* at 9:17–50, 12:32–44.

Figure 1 of the '806 patent is reproduced below.

FIG.1

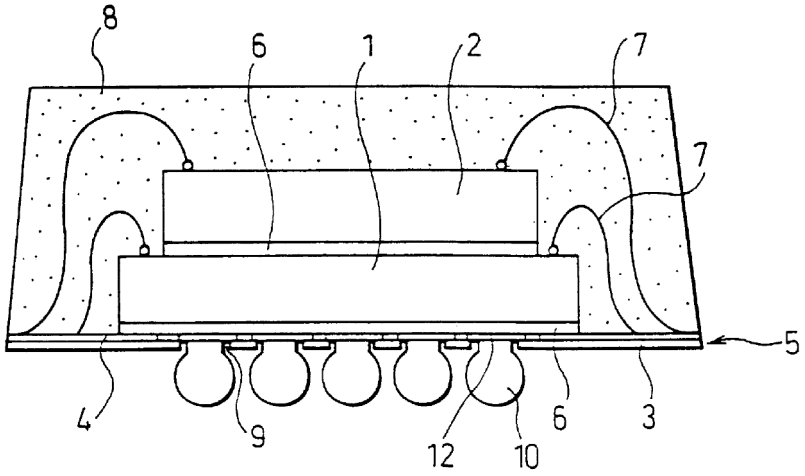


Figure 1 shows a cross-sectional view of a semiconductor device in accordance with the first embodiment of the '806 patent. *Id.* at 5:36–38.

As shown in Figure 1, in a semiconductor device of the first embodiment, "a first semiconductor chip 1 and a second semiconductor chip 2 are laminated . . . on a circuit board 5 including an insulating substrate 3 and a wiring layer 4 mounted on the insulating substrate 3." *Id.* at 6:37–40, Fig. 1. The '806 patent refers to the surface (front surface) of a semiconductor chip on which a circuit element is formed as a "circuit formed surface" and the surface of the opposite side of the chip as a "back surface." *Id.* at 6:42–45. In the first embodiment depicted in Figure 1, semiconductor chip 1 is disposed with its back surface facing insulating substrate 3. *Id.* at 6:46–47, Fig. 1. "The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6." *Id.* at 6:47–51.

The '806 patent describes that "[w]hen the first semiconductor chip 1 is in a wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips 1." *Id.* at 9:17–21. Similarly, "[w]hen the second semiconductor chip 2 is in the wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce separate pieces of second semiconductor chips 2." *Id.* at 9:31–35.

According to the '806 patent,

> By affixing the thermo-compression sheet 6 to the back surface of the second semiconductor chip 2 in advance, accurate positioning is necessary only when mounting the second semiconductor chip 2 on the first semiconductor chip 1. Therefore, since one step requiring accurate positioning is omitted in the process for manufacturing the semiconductor device in accordance with the present embodiment, this manufacturing process is simplified compared with the conventional process in which the thermo-compression sheet 6 is disposed on the circuit formed surface of the first semiconductor chip 1, and then the second semiconductor chip 2 is adhered to the thermo-compression sheet 6.

Id. at 9:38–49.

Figure 10 of the '806 patent is reproduced below.

FIG.10

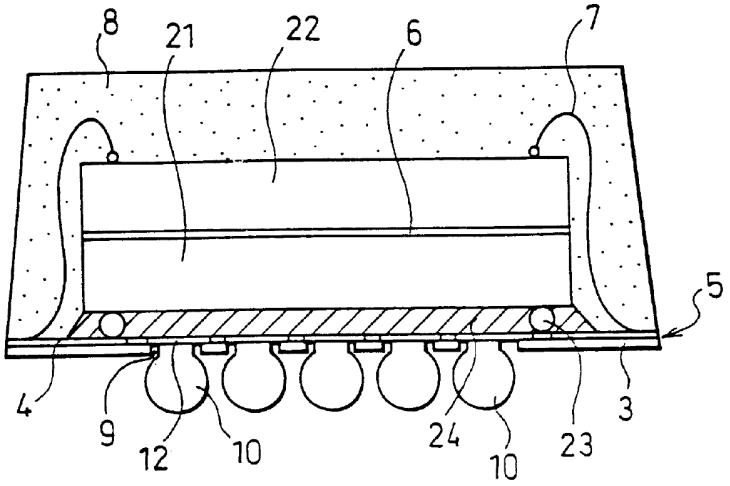


Figure 10 shows a cross-sectional view of a semiconductor device arranged in accordance with the second embodiment of the '806 patent. *Id.* at 6:6–8, 11:17–18.

As shown in Figure 10, circuit board 5 includes insulating substrate 3, and wiring layer 4 formed on the insulating substrate. *Id.* at 11:21–23. In the second embodiment, "a first semiconductor chip 21 is mounted on a circuit board 5 with its circuit formed surface facing the circuit board 5, i.e., facing down" (*id.* at 11:19–21) and "[a] second semiconductor chip 22 is mounted on the back surface of the first semiconductor chip 21 through a thermo-compression sheet 6" (*id.* at 11:23–25). In this arrangement, the back surface of second semiconductor chip 22 faces the back surface of first semiconductor chip 21. *Id.* at 11:25–27. "Namely, the back surfaces of the first semiconductor chip 21 and the second semiconductor chip 22 are adhered to each other through the thermo-compression sheet 6." *Id.* at 11:27–29.

The '806 patent describes that "[w]hen the second semiconductor chip 22 is in a state of wafer, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips 22." *Id.* at 12:32–36. According to the '806 patent, "[l]ike the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet 6 to the back surface of the second semiconductor chip 22 in advance." *Id.* at 12:39–44.

C. Illustrative Claim

Of the challenged claims, claims 1, 2, 23, 24, and 30 are independent. Claims 1 is illustrative of the challenged claims and is reproduced below,[1] with numbering added to each element as set forth in the Petition.

> 1. A semiconductor device including a stacked package structure and a chip size package structure, comprising:
>
> [1a] an insulating substrate including a wiring layer having electrode sections;
>
> [1b] a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first adhesion layer; and
>
> [1c] a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said second semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer;
>
> [1d] each of said first and second semiconductor chips being wire-bonded to the electrode section with a wire, said first

[1] We omit the bracketed term "[insulating]" which appears twice in claim 1.

and second semiconductor chips and the wire being sealed with a resin.

Ex. 1001, 13:44–66.

D. Instituted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1, 2, 12, 13, 23, 24, 30	103(a)[2]	Ball,[3] Fogal,[4] Mostafazadeh[5]
6, 7, 9, 10, 25, 26	103(a)	Ball, Fogal, Mostafazadeh, Ahmad[6]
14, 15	103(a)	Ball, Fogal, Mostafazadeh, Weinberg[7]
16–19	103(a)	Ball, Fogal, Mostafazadeh, Ma[8]
32	103(a)	Ball, Fogal, Mostafazadeh, Tsumura[9]

[2] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the '806 patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

[3] U.S. Patent No. 7,166,495 to Ball, issued Jan. 23, 2007 (Ex. 1005).

[4] U.S. Patent No. 5,323,060 to Fogal, issued June 21, 1994 (Ex. 1004).

[5] Int. Pub. WO1996/13066 by Mostafazadeh et al., published May 2, 1996 (Ex. 1003).

[6] U.S. Patent No. 5,790,384 to Ahmad et al., issued Aug. 4, 1998 (Ex. 1006).

[7] U.S. Patent No. 6,014,586 to Weinberg, issued Jan. 11, 2000 (Ex. 1008)

[8] U.S. Patent No. 6,682,954 to Ma, issued Jan. 27, 2004 (Ex. 1009)

[9] U.S. Patent No. 4,821,944 to Tsumura, issued Apr. 18, 1989 (Ex. 1007).

II. ANALYSIS

A. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.[10] *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")); *see Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that "some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]")).

[10] The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

"Whether prior art invalidates a patent claim as obvious is determined from the perspective of one of ordinary skill in the art." *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1374 (Fed. Cir. 2011). Further, "the assessment of a claim's patentability is inextricably tied to a skilled artisan's knowledge and skill level." *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Permissible uses of general knowledge of one having ordinary skill under § 103 include providing a motivation to combine and supplying a claim limitation, if supported by evidence of record. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1363 (Fed. Cir. 2013); *see also Qualcomm*, 24 F.4th at 1376 (permissible uses of what a skilled artisan would have known at the time of the invention include "furnishing a motivation to combine" and "supplying a missing claim limitation" (citing *Randall Mfg.*, 733 F.3d at 1363; *Koninklijke Philips*, 948 F.3d at 1337–38)).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include the "(1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.,* 707 F.2d 1376, 1381–82 (Fed.

Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id*

Citing testimony from Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art at the priority date of the '806 patent would have had

> i) a bachelor-level degree in electrical engineering, mechanical engineering, material science, or a related subject and five or more years of experience working in the field of semiconductor packaging; ii) a Master's-level degree in mechanical engineering, electrical engineering, material science, or a related field, and at least 1-3 years of experience in the design/development of semiconductor packages; or iii) a Ph.D.-level degree in mechanical engineering, material science, electrical engineering, or a related field, and at least some experience in the area of semiconductor packaging.

Pet. 17–18 (citing Ex. 1002 ¶¶ 28–32). Petitioner further states that "[a]dditional education may substitute for professional experience, and significant work experience may substitute for formal education." *Id.* at 18.

Patent Owner's declarant, Mr. Elenius, states that a person of ordinary skill in the art would have had "a bachelor's degree in electrical, mechanical or materials engineering and two to three years of experience in the design or development of semiconductor manufacturing, or the equivalent." Ex. 2014 ¶ 32. Mr. Elenius further states that "[a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education." *Id.*

Although the proposals for the level of skill in the art by the parties' declarants have differences in wording, we find no meaningful differences between the parties' respective definitions that would materially alter the outcome of this Decision. Nevertheless, based on our review of the '806 patent, the types of problems and solutions described in the '806 patent, and

cited prior art, we adopt and apply Petitioner's definition of the level of ordinary skill in the art.

C. Claim Construction

We apply the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2022). Under that standard, claim terms "are generally given their ordinary and customary meaning" as understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In our Decision on Institution, we determined that we did not need to explicitly construe any claim terms, including the terms "electrode section" for which Petitioner sought construction, and "adhesion layer" for which Patent Owner sought construction. Dec. on Inst. 14–16; *see Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating "we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). During trial, Patent Owner continued to seek construction of the term "adhesion layer," while Petitioner argued that the term does not necessarily require construction. *See* PO Resp. 21–25; PO Sur-reply 2–10; Pet. Reply 3.

On the complete record, we determine construction of "adhesion layer" is necessary to resolve the controversy.

"adhesion layer"

In the table below, we set forth Petitioner's and Patent Owner's positions on the term "adhesion layer," and our construction after considering the entire record.

Petitioner	Patent Owner	PTAB
ordinary meaning, i.e., a layer that adheres	a pre-formed layer that is adhered	a layer that adheres

Patent Owner argues an "adhesion layer" means "a pre-formed layer that is adhered." PO Resp. 21. According to Patent Owner, an "adhesion layer" is "a pre-formed layer like a solid sheet, as opposed to an adhesive agent, an adhesive, or an adhesive layer that is completely or partially comprised of a liquid or a viscous semi-liquid." *Id.* at 22. Petitioner opposes Patent Owner's construction and argues "adhesion layer" should be given its ordinary meaning, i.e., a layer that adheres. Pet. Reply 4–5.

On the fully developed record, we find that Petitioner's construction, "a layer that adheres," is more strongly supported by the evidence than Patent Owner's construction, "a pre-formed layer that is adhered."

Our analysis begins with the claim language. The term "adhesion layer" appears in each of the '806 patent's independent claims, which include both method and device claims. *See, e.g.*, Ex. 1001, 13:44–63 (claim 1 directed to a "semiconductor device"); *id.* at 17:58–18:17 (claim 30 directed to a "method of manufacturing a semiconductor device"). Claim 1 recites "a first semiconductor chip having a first *adhesion layer* adhered to its back surface" and "a second semiconductor chip having a second

adhesion layer adhered to its back surface." *Id.* at 13:49–51, 13:54–56 (emphasis added). Claim 30 recites the steps of "forming a first insulating *adhesion layer* on a back surface of a first wafer" and "forming a second insulating *adhesion layer* on a back surface of a second wafer." *Id.* at 17:60–62, 18:3–5 (emphases added). In the absence of contrary evidence, we must assume that the term "adhesion layer" has the same meaning in all claims of the '806 patent. *In re Varma*, 816 F.3d 1352, 1363 (Fed. Cir. 2016) ("the principle that the same phrase in different claims of the same patent should have the same meaning is a strong one, overcome only if 'it is clear' that the same phrase has different meanings in different claims," quoting *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)). The language of claim 30 and similarly worded claims of the '806 patent suggests strongly that an "adhesion layer" may be formed *in situ* on the back surface of a wafer and need not be pre-formed, as argued by Patent Owner. The testimony of Patent Owner's expert Mr. Elenius supports this interpretation. *See* Ex. 2014 ¶¶ 43, 50 (testifying that a person of ordinary skill in the art "would recognize that there are multiple methods of forming an 'adhesion layer' on the back surface of the semiconductor chip" and that "[p]astes and other adhesives, adhesive agents, adhesive layers or other material that are dispensed onto a substrate or chip back *are formed into a layer over time as they harden through curing*." (emphasis added)). Thus, the language of claims 30 and 31 does not support Patent Owner's construction that the "adhesion layer" must be a pre-formed layer that is adhered. *Cf.* PO Resp. 21–25 (arguing for that construction).

Patent Owner points to nothing in the claim language supporting its contention that an adhesion layer must be "pre-formed" as a solid sheet

before it is adhered to the back surface of a wafer. Patent Owner nevertheless attempts to support its construction that an "adhesion layer" is "a fully formed layer in advance." PO Resp. 23. Specifically, Patent Owner argues that the phrase "adhesion layer" and the term "paste (an adhesive)" are distinct, referencing claim 2's recitation of "a first semiconductor chip having a paste applied to its back surface" and "a second semiconductor chip having a second adhesion layer adhered to its back surface." *Id.*, Ex. 1001, 14:1–7. Patent Owner argues that claim 2 "evidences that the patentee did not intend an adhesion layer to be an adhesive such as an epoxy paste or other substance that can flow during manufacture." PO Resp. 23. We disagree. The "second adhesion layer" implies the existence of a first adhesion layer, and the only other reference in claim 2 to adhering is "a first semiconductor chip having a paste applied to its back surface." Ex. 1001, 14:1–2. Therefore, claim 2 supports Petitioner's position that an "adhesion layer" can be made from an adhesive agent such as paste. *See* Pet. Reply 8 (arguing that "the use of paste to attach the bottom/first chip to the substrate does not limit the type of 'adhesion layer' used to stack or mount the second chip to the first chip"). When asked about this possible construction of claim 2 at oral hearing, Patent Owner's counsel responded that inclusion of the word "second" was a drafting error. Tr. 43:23–24, 44:13–14. We do not find this explanation credible, particularly where the '806 patent is a reissue patent, and language in other claims was corrected, such as claim 24, which was amended to remove the language "second insulating" preceding "adhesion layer." Ex. 1001, 16:64.

We next turn to the Specification. The term "adhesion layer" appears multiple times in the "summary of the invention" in contexts similar to the

claims. Ex. 1001, 2:61–5:30. Analogous to our finding about claim 30, we find that disclosure of the step "forming a first insulating adhesion layer on a back surface of a first wafer" (*id.* at 4:27–29) suggests that an "adhesion layer" may be formed *in situ* on the back surface of a wafer and need not be pre-formed, as argued by Patent Owner. *See, e.g.,* PO Resp. 24 (arguing that an "adhesion layer" is "already formed and then adhered to the entire back surface of a semiconductor chip.").

The summary of the invention supports a finding that an "adhesion layer" may be formed from an adhesive agent. Ex. 1001, 4:25–63 (describing a first manufacturing method); *id.* at 4:64–5:30 (describing a second manufacturing method). The '806 patent discloses a method of manufacturing a semiconductor device, including steps of forming an adhesion layer "on a back surface" of a wafer. *Id.* at 4:25–47 (steps (a) and (d)); *id.* at 4:64–5:14 (step (c)). In that method, the *adhesion layer* is adhered to the back surface of a semiconductor chip in advance when the chip is in the wafer state. *Id.* at 4:48–54, 5:15–21. According to the '806 patent, this method has several advantages, including that "*the adhesive agent* does not overflow the space between the first and second semiconductor chips." *Id.* at 4:57–62, 5:24–29 (emphasis added).

We find it significant that the '806 patent refers to "the adhesive agent" with respect to "the above manufacturing method" (*id.*), while the enumerated method steps include forming an adhesion layer, without expressly mentioning an "adhesive agent." *Id.* at 4:25–47, 4:64–5:14. Importantly, the '806 patent does not say that an "adhesive agent" is not used in the method. Rather, the '806 patent uses language that implies that an "adhesive agent" may indeed be present, and that it "does not overflow

the space between the first and second semiconductor chips." *Id.* at 4:57–59, 5:24–26. Moreover, we observe that no other reference to adhesion or adhesives is mentioned with respect to that manufacturing method. *Id.* at 4:25–5:30. Thus, we find that the '806 patent discloses a direct relationship between "the adhesive agent" and the formation of an "adhesion layer" in the manufacturing method disclosed in the preceding paragraphs. *Id.* at 4:27–29, 4:35–37, 4:57–59, 5:4–5, 5:24–26. In other words, the antecedent for "the adhesive agent" is the "adhesion layer" in the preceding paragraphs describing the method steps. *Id.* The reference to an "adhesive agent" in conjunction with an "adhesive layer" in the summary of the invention strongly supports our finding that an adhesion layer, as recited in the claims, may be formed from an adhesive agent. *Id.*; *see* Pet. Reply 4–5 (relying on this portion of the Specification as support for Petitioner's claim construction).

Furthermore, when describing the semiconductor device structure, the summary of the invention uses the phrase, "in the case of using [a/the] thermo-compression sheet" immediately after discussing "a situation in which the excessively applied adhesive agent overflows the space between the first and second semiconductor chips." Ex. 1001, 3:25–38, 4:4–18. We agree with Petitioner (Pet. Reply 5–6) that the phrase, "in the case of using [a/the] thermo-compression sheet," implies that an adhesion layer can be formed using *either* a thermo-compression sheet or an adhesive agent, so long as the adhesion layer is adhered to the back surface of the semiconductor chip. Ex. 1001, 3:25–38, 4:4–18.

Additionally, the '806 patent describes the preferred embodiments as including a thermo-compression sheet as an adhesion layer. Ex. 1001, 6:48–

52; 11:31–33. Similar to the description of the preferred embodiments, the abstract discloses that "[a] first semiconductor chip is produced by affixing a thermo-compression sheet to the back surface of a wafer." *Id.* at code (57). The claims, however, are not limited to a thermo-compression sheet as an adhesion layer. We find it significant that, in contrast to the abstract and description of the preferred embodiments, the claims of the '806 patent use the broader term, "adhesion layer," rather than a narrower term, such as "thermo-compression sheet."

In the absence of patentee lexicography or disavowal, it would be improper to limit the scope of the term "adhesion layer" to a pre-formed solid sheet. *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) ("Absent lexicography or disavowal, we do not depart from the plain meaning of the claims."); *In re Am. Acad. Of Sci. Tech Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) ("We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification.").

We find no lexicography or disavowal that would limit the scope of the term "adhesion layer" to a pre-formed layer or thermo-compression sheet. The Specification of the '806 patent does not limit an adhesion layer to a thermo-compression sheet. Instead, a thermo-compression sheet is disclosed as *an example* of an adhesion layer. Our finding is strongly supported by the description of Embodiment 2: "The thermo-compression sheet 6 is provided *as an adhesion layer* for holding the second semiconductor chip 22 on the first semiconductor chip 21." Ex. 1001, 11:31–33 (emphasis added). Our finding is also supported by the

description of Embodiment 1: "The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6." *Id.* at 6:48–52. We find that use of the parenthetical "(adhesion layer)" when describing Embodiment 1 has the same meaning as "as an adhesion layer" when describing Embodiment 2. *Id.* at 6:48–52, 11:31–33. In both instances, the term "adhesion layer" is describing the role of the thermo-compression sheet in the device, and the term "adhesion layer" is not being defined as a thermo-compression sheet. *Id.*

Patent Owner argues that the Specification distinguishes an adhesion layer from an adhesive. According to Patent Owner, "[a]dhesives are not adhered as a layer but are applied to adhere other surfaces together as the adhesives dry and cure." PO Resp. 24 (citing Ex. 1001, 2:23–48). We find that argument unpersuasive as it is insufficiently supported. The portion of the Specification relied on by Patent Owner does not state that an adhesion layer cannot be formed by applying an adhesive agent to a surface. Rather, that portion of the Specification speaks to only two circumstances: one where "the amount of the adhesive agent is excessive" and one where "the amount of adhesive agent is too small." Ex. 1001, 2:23–48. The evidence relied on by Patent Owner does not state that the adhesive agent does not form a layer if it is applied in the correct amount. Moreover, Patent Owner's argument is inconsistent with the extrinsic evidence showing formation of an adhesion layer. *See* Ex. 1003, 9:15–26 (disclosing that a fluid B-stageable epoxy adhesive can be rolled on as a layer prior to cure); *id.* at 6:3–4 ("During rolling step 104, the B-stageable adhesive will be in its initial fluid-

based form of a paste, gel, or liquid"); *see also* Ex. 2014 ¶ 50 (Patent Owner's expert testifying that "[p]astes and other adhesives, adhesive agents, adhesive layers or other material that are dispensed onto a substrate or chip back *are formed into a layer over time* as they harden through curing." (emphasis added)).[11] This evidence, along with a plain reading of the claims, supports a finding that applying an "adhesive agent" such as an epoxy or paste can form a layer that adheres, i.e., an "adhesion layer."

Patent Owner directs us to the Specification's disclosure that "instead of providing the thermo-compression sheet 6 in advance when the first semiconductor chip 1 is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board 5 before the first semiconductor chip 1 is mounted on the circuit board 5." Ex. 1001, 9:25–29. Patent Owner argues that this passage discloses an epoxy paste "instead of an adhesion layer." PO Sur-reply 6 (emphasis omitted). We disagree. The passage discloses a layer of epoxy paste *instead of a thermo-compression sheet*. Both alternatives may be considered an "adhesion layer," which is not mentioned in the passage. We acknowledge that the quoted Specification passage discloses that paste may be applied to the circuit board, rather than to the back surface of a semiconductor chip, as recited in the claims. *Compare* Ex. 1001, 9:25–29, *with id.* 14:1–2 (claim 2); *see also id.* at 13:49–51 (claim 1: "a first semiconductor chip having a first adhesion layer adhered to its back surface"). The Specification does not

[11] Contrary to Patent Owner's argument (PO Resp. 24), the cited testimony supports Petitioner's claim construction, not Patent Owner's. Pet. Reply 7. Mr. Elenius did not say that a hardened layer of paste or other adhesive is not an adhesion layer.

support Patent Owner's argument (PO Sur-reply 6) that the term "adhesion layer" excludes a layer of epoxy paste.

Contrary to Patent Owner's arguments (PO Sur-reply 4, 6), the absence of an express disclosure that a layer of epoxy paste may be used as the adhesion layer is not enough to exclude it from the scope of the claim term. *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."). Silence regarding alternative embodiments is not a disavowal. *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1357 (Fed. Cir. 2004) ("the applicant's choice to describe only a single embodiment does not mean that the patent clearly and unambiguously disavowed other embodiments"); *see also Luminara*, 814 F.3d at 1353 ("The standards for finding lexicography and disavowal are 'exacting.'" (citing *GE Lighting*, 750 F.3d at 1309)).

Patent Owner argues that construing "adhesion layer" as limited to a pre-formed solid sheet is necessary to achieve the '806 patent's "primary goal" of preventing overflow or underfill of the back surface of a chip with adhesive. PO Resp. 21–23; PO Sur-reply 3–4. We disagree. The '806 patent discusses drawbacks associated with two known methods for bonding chips, "an adhesive agent (paste) potting method" and "a method using a thermo-compression sheet." Ex. 1001, 2:17–57. With the first method, the adhesive agent may possibly overflow or underfill the chip, while the thermo-compression sheet requires a two-step alignment process. *Id.* The disclosed invention addresses these drawbacks by forming an adhesion layer on the backside of a semiconductor wafer before it is diced into individual

chips. *Id.* at 4:48–63. This method avoids potential overflowing and underfilling of adhesive and simplifies the alignment process. *Id.* We agree with Petitioner that the '806 patent avoids overflowing and underfilling by forming the adhesive layer in the wafer state before dicing, not by using a sheet instead of an adhesive agent. Pet. Reply 6.

Moreover, the evidence does not persuade us that a pre-formed solid sheet is necessary to avoid adhesive potentially overflowing or underfilling the space between a chip's surface and the surface on which it is mounted. The '806 patent addresses two situations: one where "the amount of the adhesive agent is excessive [and] a large amount of adhesive agent spreads beyond the outer edge of the semiconductor chip" and another where "the amount of the adhesive agent is too small [and] a gap is produced between the semiconductor chips." Ex. 1001, 2:22–46. The '806 patent does not address a situation where the correct amount of adhesive agent is applied. The problem of overflowing or underfilling adhesive (i.e., *if* an excessive or insufficient amount of adhesive agent is applied) is addressed by forming an adhesion layer on a back surface of a semiconductor wafer before it is diced into individual chips. Ex. 1001, 4:48–62, 5:15–29. There is no suggestion in the '806 patent that a pre-formed solid sheet is necessary to avoid the overflow or underfill problem. Our finding is supported by Mr. Elenius's testimony that a person of ordinary skill in the art "seeing the term 'adhesion layer' would recognize that there are multiple methods of forming an 'adhesion layer' on the back surface of the semiconductor chip." Ex. 2014 ¶ 43. At his deposition, Mr. Elenius agreed that the overflow problem occurs when the adhesive agent is in a wet form, not when it is in a dry form. Ex. 1037, 10:21–11:9. If the adhesive agent is allowed to dry or cure before

a first chip is placed on a second chip, the overflow problem may be avoided. *Id.*

For the foregoing reasons, we construe the term "adhesion layer" to mean "a layer that adheres."

D. Asserted Obviousness over Ball, Fogal, Mostafazadeh, and the Knowledge of a Skilled Artisan

Petitioner asserts that claims 1, 2, 12, 13, 23, 24, and 30 are unpatentable under § 103 over Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan. Pet. 29–59.

1. Ball (Ex. 1005)

Ball describes a multi-chip semiconductor device in which semiconductor chips (called dies) are vertically stacked on top of one another using a combination of face-down (flip-chip) or face-up (wire bond) assembly arrangements. Ex. 1005, Abstract, 1:8–12, 2:16–20. According to Ball, "flip-chip attachment" refers to a method of attaching a semiconductor chip (die) to a substrate in which "the die is inverted so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate (such as a printed circuit board)." *Id.* at 1:28–32. Ball describes state-of-the art attachment techniques as including "flip-chip attachment" and "wire bonding." *Id.* at 1:47–50. For wire bonding, "[t]he die may be oriented either face up or face down (with its active surface and bond pads either up or down with respect to the circuit board) . . . although face up orientation is more common." *Id.* at 2:16–20.

Figure 1 of Ball is reproduced below.

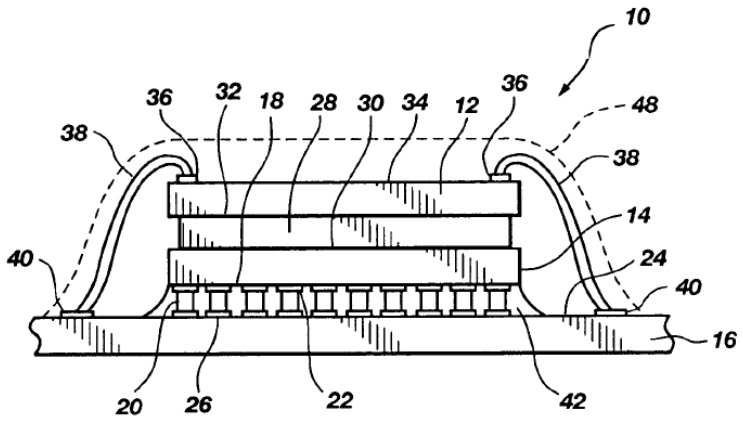


Fig. 1

Figure 1 shows a side plan view of an exemplary multi-die assembly of Ball with a flip-chip vertical stacking arrangement. *Id.* at 4:58–59, 5:1–18.

Ball describes that assembly 10 of Figure 1 comprises upper die 12, opposing lower die 14, and substrate 16. *Id.* at 5:2–3. Ball further describes that

> Fabrication of the assembly 10 comprises providing the lower die 14 having a face surface 18 with at least one flip chip electric connection 20 (such as a C4 solder bump connection, conductive polymer bump or pin connection, these and other alternatives being known in the art, by way of example) extending from a bond pad or other terminal 22 on the lower die face surface 18. The flip chip electric connections 20 extend to a surface 24 of the substrate 16 in such a manner that the flip chip electric connections 20 physically (mechanically) attach to, and make electrical contact with, lead ends, trace ends, terminals or other electrical contact elements 26 in or on the surface 24 of the substrate 16.

and that "back side 32 of the upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over a lower die back side 30." *Id.* at 5:6–20. "An adhesive requiring a curing step, such as an epoxy, is preferred, although many adhesives known in the art are suitable." *Id.* at 5:20–22.

"Substrate 16, if an insulative substrate, may itself be connected to a chassis or mother board by edge connections, bump connections, pin connections, or other conductive arrangements as known in the art." *Id.* at 5:37–40.

2. Fogal (Ex. 1004)

Fogal describes multichip modules with a wire bond stacked chip assembly arrangement. Ex. 1004, Abstract.

Figure 1 of Fogal is reproduced below.

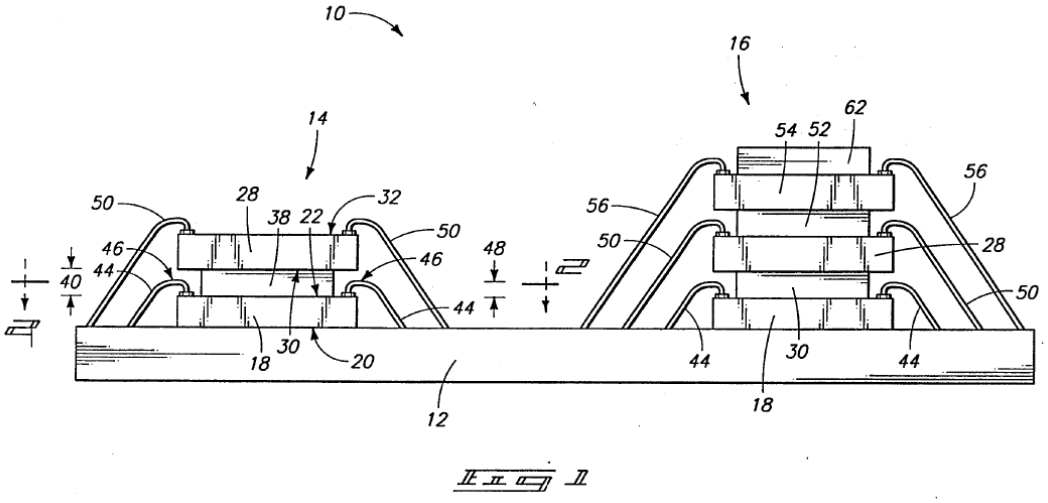


Figure 1 shows multichip module 12 with multichip stacks 14 and 16. *Id.* at 2:31–36. Stack 14 includes first chip 18 having opposed base and bonding faces 20 and 22, respectively. *Id.* at 2:36–38. Base face 20 is adhered to substrate 12 by means of an adhesive, such as "epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc." *Id.* at 2:38–41. Bonding face 22 includes bonding pads 26 that connect first chip 18 to substrate 12 via bonding wires 44. *Id.* at 2:41–43, 2:55–63. Second chip 28 includes bonding pads 36 that connect second chip 28 to substrate 12 via bonding wires 50. *Id.* at 2:44–48, 2:63–66. Fogal further describes that adhesive layer 38 is interposed between, and connects,

bonding face 22 of first chip 18 to base face 30 of second chip 28. *Id.* at 2:49–54, 2:60–63. According to Fogal, "[e]xample materials for adhesive 38 include epoxies and tape" and "[m]ost preferred is a thermoplastic tape." *Id.* at 2:66–68.

3. Mostafazadeh (Ex. 1003)

Mostafazadeh describes a method of forming an adhesive coating on a semiconductor wafer surface. Ex. 1003, Abstract. The method includes the step of forming an adhesive coating on a semiconductor wafer surface. *Id.* After the adhesive coating is dried, the semiconductor wafer is diced to form several integrated circuit dies, each having an integrated circuit and an adhesive layer. *Id.* To attach the die to the support surface, the adhesive layer is placed in contact with a die attach pad and then cured. *Id.*

According to Mostafazadeh, "[g]luing and taping are conventional techniques" to attach an individual die (a fabricated integrated circuit chip) to a structure (e.g., a connection substrate) during packaging of the individual chips. *Id.* at 1:22–25. Mostafazadeh indicates that, in conventional processes, glue is applied either directly to the support surface or directly to the die. *Id.* at 1:25–28. Mostafazadeh discusses disadvantages of applying glue to a support surface, whether in a pattern of glue drops or as a single large glue drop. *Id.* at 1:30–2:20, Figs. 1a–c. For example, with a pattern of glue drops, "there is no guarantee that the adhesive will cover the entire interface between the die and the support surface," and "the strength of the resulting bond is not optimum." *Id.* at 2:1–4, 2:12–15. Mostafazadeh states that, "[w]hile the single glue drop . . . may cover most or all of the interface, it tends to interfere with connections to the attached die by *jutting up around the die's edges*." *Id.* at 2:18–20 (emphasis added). Mostafazadeh

indicates that, in a conventional taping method, tape is applied either to the back surface of a semiconductor wafer prior to dicing or to the die support surface, but discloses that "tape has the drawback of being relatively expensive." *Id.* at 2:22–25.

In view of these shortcomings, Mostafazadeh aims to provide a method for attaching integrated circuit dies to support surfaces where "the adhesive is spread evenly and does not jut around the edges of the die." *Id.* at 2:27–29. To accomplish this objective, Mostafazadeh discloses a method of attaching an integrated circuit die to a support surface by applying an adhesive coating to the surface of a semiconductor wafer before the wafer is diced to form individual dies. *Id.* at 3:5–14. Mostafazadeh notes that, in this process, "the adhesive is applied to the semiconductor wafer as opposed to an individual support surface or an individual die as is common in the conventional processes." *Id.* at 8:2–5.

Figure 2 of Mostafazadeh is reproduced below.

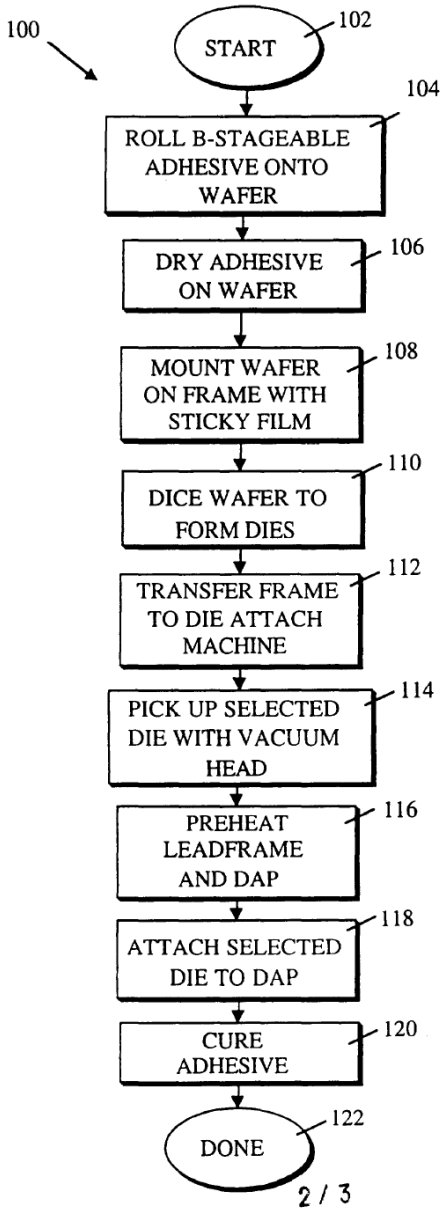


Figure 2 is a flowchart illustrating Mostafazadeh's exemplary method of attaching an integrated circuit[12] die to a support surface. *Id.* at 4:15–16.

The process of Mostafazadeh's Figure 2 begins with step 102 in which a multiplicity of integrated circuits are fabricated on a semiconductor

[12] Mostafazadeh refers to an integrated circuit as "IC." Ex. 1003, 9:20.

wafer. *Id.* at 5:22–23. Mostafazadeh describes that, after fabrication of the ICs on the semiconductor wafer, an adhesive is then rolled onto a mounting surface (i.e., the surface opposite to the IC formed surface) of the wafer "to form an adhesive coating thereon in a rolling step 104." *Id.* at 5:23–25. According to Mostafazadeh, the roller ends extend beyond a wafer surface during the application of the adhesive, which "insures that an adhesive coating . . . is formed over the entire wafer surface." *Id.* at 6:29–7:1. Mostafazadeh further describes that "in some embodiments, the adhesive may be a B-stageable epoxy." *Id.* at 3:22–23; *see also id.* at 5:25–26 ("Although a variety of adhesives can be used, B-stageable adhesives have been found to work well . . . ."). Mostafazadeh explains that "a B-stageable adhesive is an adhesive that can be applied, dried without inducing full polymerization, reflowed (typically by heating the adhesive), and then cured to form more permanent bonds." *Id.* at 5:28–6:1.

Mostafazadeh describes that "[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid." *Id.* at 6:3–4. But "once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106," which "turns the adhesive coating into a *hard surface*" if "the adhesive is good B-stageable epoxy." *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as "hardened").

After mounting the semiconductor wafer onto a film supported by a dicing frame, the wafer is then cut or diced into a multiplicity of dies or IC chips. *Id.* at 7:18–19, 7:29–8:1, Fig. 2 (steps 108, 110). After the dicing step, each die has an integrated circuit and an adhesive layer that includes

the dried adhesive coating. *Id.* at 8:1–2.

Figure 5c of Mostafazadeh is reproduced below.

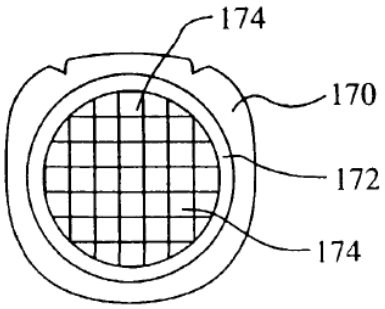


Fig. 5c

Figure 5c is a top view illustrating the result of dicing step 110 of Figure 2 forming a multiplicity of integrated circuit dies. *Id.* at 5:7–8. Figure 5c shows the result of dicing the semiconductor wafer to form several integrated circuit dies 174. *Id.* at 8:5–6.

After the dicing step, individual integrated circuit dies are attached to associated support surfaces, such as a die attach pad of a lead frame, which may be pre-heated to facilitate curing of the adhesive (B-stageable epoxy). *Id.* at 8:10–12, 8:18–25, Fig. 2 (steps 112, 114, 116). After optionally pressing the IC die onto the die attach pad, the adhesive layer is cured, and the die is electrically coupled and packaged. *Id.* at 9:25–26, Fig. 2 (steps 118, 120, 122).

According to Mostafazadeh, as the result of applying adhesive to a wafer, drying the coating to form a hardened layer, and dicing the wafer to the chip size, the adhesive layer on each individual chip is "*exactly the same size* as the mounting surface of the die." *Id.* at 9:15–16 (emphasis added). Thus, "when the die is attached to its supporting surface" during packaging of individual chips, "the adhesive *does not extend beyond* a mounting

surface of *the die*." *Id.* at 9:16–18 (emphases added).

Figure 6a of Mostafazadeh is reproduced below.

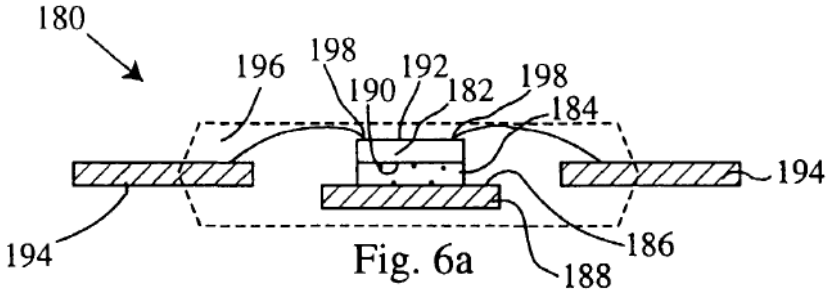


Fig. 6a

Figure 6a is a diagrammatic cross sectional side view of an exemplary packaged integrated circuit with a die attached to a support surface by an adhesive layer. *Id.* at 5:10–12.

Figure 6a shows packaged integrated circuit 180, including die 182 attached to support surface 188 via adhesive layer 184. *Id.* at 10:4–5. "The *adhesive layer 184* covers an entire mounting surface 190 of the selected integrated circuit die 182 and *does not extend beyond a boundary* of the mounting *surface 190*." *Id.* at 10:6–8 (emphases added). Mostafazadeh further describes that "more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)." *Id.* at 11:16–18.

4. Reasons to Combine

Petitioner contends it would have been obvious for a person of ordinary skill in the art to combine Ball's teachings of stacking chips with with Fogal's teaching of mounting the backside of the lowermost chip to the substrate. Pet. 29–31. Petitioner contends a person of ordinary skill in the art would have combined Ball and Fogal with Mostafazadeh's process for applying adhesive to create individual chips with adhesive back surfaces. *Id.* at 32–33. Petitioner contends a person of ordinary skill would have been

motivated to combine the teachings of the references for several reasons, including to provide a more efficient manufacturing process for multichip modules and to simplify the stacking process. *Id.* at 29–33.

Patent Owner argues that a person of ordinary skill would not have been motivated to combine Mostafazadeh with Ball and Fogal because there would have been no reasonable expectation of success and the combination would not have resulted in a functioning semiconductor device. PO Resp. 46. Patent Owner asserts that Petitioner's combination of references would fail for multiple reasons and that Mostafazadeh does not describe multi-chip stacked mounting. *Id.* at 46–60.

Having considered the evidence and arguments, we determine that the preponderance of the evidence favors Petitioner. Petitioner demonstrates persuasively that a person of ordinary skill in the art would have had reason to combine Ball's stacked multichip module with Fogal's teaching of mounting the backside of a chip to a substrate, to create a multichip module using wire bond interconnection techniques. Pet. 29–31. Petitioner further demonstrates that a person of ordinary skill in the art would have had reasons to combine Ball's stacked multichip module with Mostafazadeh's process for applying adhesive at the wafer stage and then dicing to create individual chips with adhesive backsides. *Id.* at 29–33. In particular, Petitioner shows that a person of ordinary skill in the art would have considered Mostafazadeh's teaching of applying the adhesive to a wafer surface and then subsequently dicing the wafer in order to provide a more efficient manufacturing process for multichip modules and to simplify Ball's process of stacking chips. *Id.*; *see KSR*, 550 U.S. at 417 (stating that the

"mere application of a known technique to a piece of prior art ready for the improvement" suggests obviousness).

The teachings of Ball and Fogal support Petitioner's assertion that a person of ordinary skill in the art would have been motivated to combine their teachings. Ball teaches a stacked multichip module using flip-chip and wire bond interconnections, where a lower chip is flip-chip connected to a substrate using metal bumps, and an upper chip is wire bond connected to the substrate. Ex. 1005, Abstract, 3:42–64, 4:58–59, 5:3–12, 5:18–20, 5:23–27, Fig. 1. Fogal teaches multichip modules where the backside of the lowermost chip is mounted to the substrate and electrically connected to the substrate by wire bonding. Ex. 1004, 2:38–43, 2:55–63; Figs. 1–3.

We credit Dr. Suhling's testimony that a person of ordinary skill in the art "would look to Fogal to mount the backside of the lowermost chip to the substrate, and then use the configurations in Ball to stack additional chips on top." Ex. 1002 ¶ 235; *see also id.* ("a POSITA would also understand that mounting a face-up chip to the substrate would provide additional creative options (beyond Ball's flip-chip interconnection) for configuring high-density multichip modules with multiple sizes of chips" (citing Ex. 1005, 3:33–37)).

Dr. Suhling's testimony concerning "additional creative options" is supported by Ball and Fogal. More particularly, Ball Figure 1 shows a chip stack configuration in which the lower chip is flip-chip connected to the substrate and the upper chip is face up and wire-bonded to the substrate. Ex. 1005, 5:3–27, Fig. 1. Fogal Figure 1 shows a chip stack configuration similar to Ball Figure 1, except that both the upper and lower chips are face up and wire-bonded to the substrate. Ex. 1004, 2:31–66, Fig. 1. We are

therefore persuaded that a person of ordinary skill in the art would have understood that Ball's back-to-back chip stack and Fogal's dual face up chip stack are alternative ways of vertically stacking chips to increase integrated circuit density. Ex. 1002 ¶ 235. We are also persuaded by Dr. Suhling's testimony that these two interconnection techniques—flip chip and face up with wire bonding—"were conventional in the art and well-known to a skilled artisan." *Id.* (citing Ex. 1001, Figs. 13(a), (b); Ex. 1015, Fig. 27; Ex. 1016, Figs. 1–4). Patent Owner agrees that the wire bonding and face-down bonding methods were conventional. PO Resp. 16–17 (citing Ex. 1001, 6:18–23; Ex. 2012, 46:8–48:24). In view of Ball and Fogal, we are persuaded that it would have obvious to a person of ordinary skill in the art to stack a pair of chips, as taught by Ball, with the lower chip face up with its backside mounted to a substrate, as taught by Fogal.

Mostafazadeh teaches a method for applying integrated circuit dies to support surfaces. Ex. 1003, Abstract. In Mostafazadeh's method, an adhesive coating is formed on a surface of a semiconductor wafer, the adhesive coating is dried, and the semiconductor wafer is diced to form integrated circuit dies, each having an adhesive layer on its mounting surface, i.e., its back surface. *Id.* at 3:5–11, 5:20–25, 7:9–11, 7:29–8:2, Fig. 2 (steps 104–110). A selected die is then attached to an associated support surface by placing the adhesive layer of the selected die in contact with the associated support surface. *Id.* at 3:11–13, 8:10–12, Fig. 2 (steps 112–118).

We find that the express teachings of Mostafazadeh provide reasons to apply Mostafazadeh's method to the combination of Ball and Fogal. First, Mostafazadeh teaches that "in the described process, the adhesive is applied

to the semiconductor wafer *as opposed* to an individual support surface *or an individual die* as is common in the conventional processes." Ex. 1003, 8:2–5 (emphasis added). Here, Mostafazadeh expressly teaches to substitute its die attachment method for a conventional die attachment method, as disclosed in Ball, where a layer of adhesive is applied over the back side of an individual die. *Id.*; Ex. 1005, Abstract, 3:54–59, 5:18–20. This express teaching of Mostafazadeh provides strong evidence that it would have been obvious to apply Mostafazadeh's die attachment method to a multichip device as taught by Ball and Fogal. *See, e.g., SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1359 (Fed. Cir. 2000) (reversing jury verdict of nonobviousness where "[t]he express teachings in the art provide the motivation and suggestion to modify" the disclosed method and establish a strong case of obviousness).

Second, Mostafazadeh teaches that the disclosed die attachment method has several advantages. For example, Mostafazadeh teaches that "the adhesive is spread evenly and does not jut around the edges of the die . . ." Ex. 1003, 2:28–29. According to Mostafazadeh, the adhesive layer "covers the entire mounting surface" and "does not extend beyond the mounting area boundary." *Id.* at 3:28–4:1; *see also id.* at 10:6–8 (same teaching with reference to Figure 6a). Similarly, Mostafazadeh teaches that the adhesive layer "is exactly the same size as the mounting surface of the die and is quite even." *Id.* at 9:15–16.

We find that a person of ordinary skill in the art would have recognized Mostafazadeh's disclosed advantages as directly applicable to the adhesive layer of Ball. We credit Dr. Suhling's testimony that it would have been obvious to combine Mostafazadeh's process for forming chips

with adhesive backsides with Ball and Fogal's multichip modules to make the chip stacking process more efficient. Ex. 1002 ¶¶ 128, 133, 151, 152, 230, 238, 239. We find the following testimony persuasive:

> [G]iven the competitive pressures in the semiconductor industry to make smaller and cheaper devices, manufacturers were constantly looking for ways to eliminate process steps and lower costs. One way to do this is to incorporate as many manufacturing steps as possible during the wafer fabrication stage, before the chips are diced from the wafer. This approach is standard in semiconductor manufacturing and allows manufacturing steps to be applied in batch mode rather than building individual chips one at a time. For example, photolithography, ion implantation, etching, and chemical vapor deposition layer steps—to name a few— are applied over the entire wafer to create the integrate circuits.

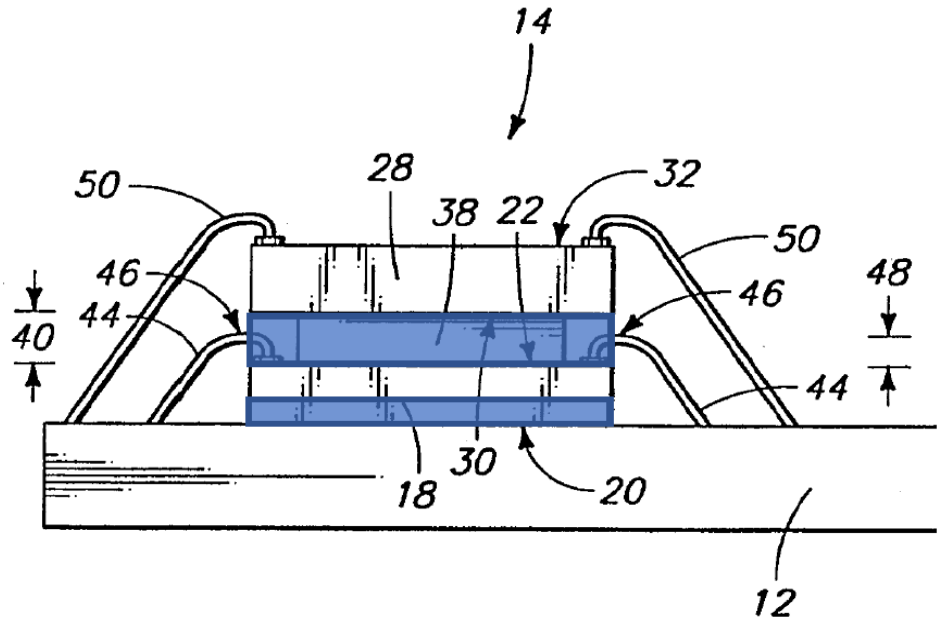
Id. ¶ 128; *see also id.* ¶¶ 151, 260 (a person of ordinary skill in the art "would also understand that chips with pre-formed adhesive on their backsides would eliminate process steps and save costs" when manufacturing multichip modules). The foregoing testimony demonstrates that Mostafazadeh's method of applying adhesive to the backside of a wafer before dicing would have eliminated process steps and lowered costs by forming adhesive-backed chips "in batch mode" rather than forming an adhesive layer on each chip "one at a time." *Id.* ¶ 128*; see Dystar Textilfarben Gmbh & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) ("[A]n implicit motivation to combine exists . . . [when] the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.").

We are similarly persuaded by the following testimony from Dr. Suhling:

> [B]y the 1990s, the semiconductor industry faced increased pressure to streamline its manufacturing processes to produce higher performance, lower cost, and smaller semiconductor packages. . . . Manufacturers looked to integrate more processes during the wafer stage since it would result in hundreds of chips with the added feature rather than incorporating features on a chip-by-chip basis after the wafer was diced. Applying the adhesive to the backside of a wafer and dicing to produce hundreds of individual chips was a common-sense approach for simplifying the chip stacking process that was well known in the art.

Ex. 1002 ¶¶ 133, 236 (citing Ex. 1005, 2:26–31). The foregoing testimony provides a persuasive reason for a person of ordinary skill in the art to use Mostafazadeh's wafer stage adhesive layer application process to simplify the stacking processes in Ball and Fogal.

Patent Owner asserts that "the combination of Mostafazadeh with Fogal fails because the resulting structure would deform and even short-circuit the bond wires extending from the substrate to the top surface of the first (lower) semiconductor chip." PO Resp. 46–47. For support, Patent Owner provides the following annotated Figure 1 of Fogal (*id.* at 48), which Patent Owner states would be the result of combining Mostafazadeh with Fogal:



Fogal at Fig. 1 (annotated)

Patent Owner's annotated Figure 1 of Fogal depicts a side view of a multichip module with what Patent Owner asserts would be Mostafazadeh's adhesive applied under chip 28 depicted in blue, which Patent Owner asserts would deform the wire bonds on bond pads 26 (not numbered).

Patent Owner contends that "[t]he pre-applied adhesive backside under chip 28 [of Fogal's Figure 1] would deform the wire bonds that are already made to the bond pads 26 located on the periphery of the top surface of first chip 18 and thereby obstruct the bond pads 26." *Id.* at 48. We disagree with Patent Owner. Patent Owner's argument is premised on a combination that Petitioner did not make. Petitioner relies on Fogal for its disclosure of mounting a first semiconductor chip's adhesive backside to a wiring layer. Pet. 38–39 (addressing claim element [1b]). Such mounting does not implicate the upper surface of the first chip where the bond pads are located. *See* Ex. 1004, Figure 1 (first chip 18 having back surface 20 contacting substrate 12, and bond pads located on top surface 22 of first chip

18). Petitioner does not rely solely on Fogal for stacking additional chips on the first chip. Instead, Petitioner asserts that a skilled artisan "would look to Fogal to mount the backside of the lowermost chip to the substrate *and then use the configurations in Ball to stack additional chips on top*." Pet. 30–31 (emphasis added); Ex. 1002 ¶ 235. Thus, Patent Owner's argument does not address the entirety of the applied prior art and is not persuasive.

Moreover, Patent Owner's argument is premised on Fogal's first and second chips having identical sizes and face surface areas. Fogal, however, expressly contemplates "chips having different size surface areas . . . in a multichip module substrate." Ex. 1004, 3:33–35. For this additional reason, Patent Owner's argument that the adhesive layer would obstruct the bond pads is not persuasive. *See* Pet. Reply 25–26.

Patent Owner further argues that the combination of Ball, Fogal, and Mostafazadeh would fail "because all three references teach an adhesive, which when applied to the back surface of the second semiconductor chip and mounted according to the method taught by Mostafazadeh, could overflow." PO Resp. 53 (citing Ex. 2014 ¶ 121). According to Patent Owner, the downward pressure during mounting "could cause adhesive to squeeze out and possibly obstruct the bond pad." *Id.* Patent Owner's argument and the corresponding testimony of Mr. Elenius are speculative and do not outweigh Petitioner's evidence of obviousness. Mostafazadeh recognizes and addresses the overflow issue. Contrary to Patent Owner's argument, Mostafazadeh explicitly provides that its adhesive layer "covers an entire mounting surface 190 of the selected integrated circuit dies 182 and *does not extend beyond a boundary of the mounting surface* 190." Ex. 1003, 10:6–9 (emphasis added). Additionally, Mostafazadeh teaches that when

"the adhesive layer is rolled on, it is exactly the same size as the mounting surface of the die and is quite even. Thus, when the die is attached to its supporting surface the adhesive does not extend beyond a mounting surface of the die." *Id.* at 9:15–18. Further, Mostafazadeh teaches that its process avoids the adhesive jutting around the edges of the die. *Id.* at 2:26–28. These teachings support that a person of ordinary skill in the art would have had a reasonable expectation of successfully applying Mostafazadeh's die attachment method to multichip device of Ball and Fogal while avoiding adhesive overflow.

Patent Owner further argues that Petitioner's combination would fail because, "[i]n a flip-chip configuration, the lower chip is mounted with bump connections to the substrate" and the heat applied to complete the bump connections "will cause the adhesive to cure and completely harden." PO Resp. 54–55 (citing Ex. 2012, 147:4–22; Ex. 2014, ¶ 121). Patent Owner's argument is not applicable to Petitioner's combination of Ball, Fogal, and Mostafazadeh, which does not involve a flip-chip configuration. In Petitioner's combination, both the lower and upper chips are face up. *See* Pet. 30–31 ("A POSITA would look to Fogal to mount the backside of the lowermost chip to the substrate and then use the configurations in Ball to stack additional chips on top."). Patent Owner then argues that, if adhesive is formed on the back of the upper chip, "[t]he adhesive on the second chip's back could overflow from its edges during mounting when pressure is applied since it has not been cured." PO Resp. 55. Patent Owner's overflow argument does not outweigh Petitioner's evidence for the reasons discussed above.

Next, Patent Owner argues that Petitioner's combination would fail because Mostafazadeh's method "requires pre-heating or flash heating of the support surface," which would cause the adhesive layer to reflow and "overflow past the edge of the chip and cover the bond pads." PO Resp. 55–56 (citing Ex. 1003, 8:19–20, 9:10–13; Ex. 2014 ¶ 123). Patent Owner's argument is not supported by Mostafazadeh, which teaches "*it is often desirable* to pre-heat the support surface to facilitate curing" (Ex. 1003, 8:19–20 (emphasis added)), but does not *require* pre-heating or flash heating, as argued by Patent Owner (PO Resp. 55). Furthermore, Mr. Elenius's testimony about adhesive overflow is speculative. Ex. 2014 ¶ 123 ("This reflowing of the B-stageable epoxies *could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads.") (emphasis added). Notably, Mr. Elenius's testimony does not take into account Mostafazadeh's teachings that the adhesive "does not jut around the edges of the die" and "does not extend beyond the mounting area boundary." Ex. 1003, 2:28–29, 3:28–4:1; *see also id.* at 9:15–16, 10:6–8 (similar teachings).

Patent Owner disputes Petitioner's contention that Mostafazadeh explicitly recommends using its adhesive process to efficiently build vertically stacked multichip modules. *See* Pet. 32 (citing Ex. 1003, 11:16–18) *see also* Pet. Reply 11 (arguing that Mostafazadeh "expressly recommended using its process" to form MCPs and MCMs "like those in Ball"). Patent Owner argues that "Mostafazadeh never designed and experimented for multi-chip stacked mounting," and its disclosure about MCPs and MCMs "appears to be limited to planar structures and not vertically stacked structures." PO Resp. 56–57; Ex. 2014 ¶ 103 *see also id.*

¶¶ 65–70 (discussing planar MCPs and MCMs); PO Sur-reply 14–15 (arguing that "Mostafazadeh's reference to MCM/MCPs was likely to be a planar structure").

We find it unnecessary to resolve the parties' dispute about whether Mostafazadeh's reference to MCPs and MCMs includes vertically stacked structures. PO Resp. 56–57; Pet. 32. It does not matter whether or not Mostafazadeh teaches vertically stacked multichip structures because undisputed evidence establishes that they were known in the art and taught by Ball and Fogal. For example, Petitioner shows persuasively that vertically stacked MCPs and MCMs were known in the art. Pet. Reply 18–19 (citing Exs. 1004, 1005, 1016, 1028); Ex. 1002 ¶¶ 58–61 (discussing prior art vertically stacked MCPs and MCMs). Dr. Suhling credibly testifies that MCPs or MCMs were known in the art well before 1998 as "3-D packaged" devices with vertically stacked IC chips. Ex. 1002 ¶¶ 58–61 (discussing vertically stacked 3-D package devices described in various prior art references (citing Ex. 1025, 220; Ex. 1027, 110; Ex. 1028, Fig. 4A; Ex. 1029, 110, Fig. 3)). *See also id.* ¶¶ 97–99 (citing Ex. 1016[13]). Fogal describes multichip modules having a stacked chip arrangement. *See* Ex. 1004, 2:31–36. Fig. 1 (showing and describing a multichip module having "a plurality of z-direction multichip stacks"). Mr. Elenius agrees that Fogal describes vertically stacked MCMs. Ex. 1037, 39:13–24. Further, Mr. Elenius admits that Figure 14(a) of the '806 patent describes "conventional vertically stacked multi-chip semiconductor devices." Ex. 2001 ¶ 40 (citing Ex. 1001, 2:17–29).

[13] Dr. Suhling refers to Exhibit 1014, but based on his description of the reference, we understand him as describing Exhibit 1016.

Patent Owner does not dispute Petitioner's showing that "a POSITA knew of vertical MCM/MCPSs at the time of the invention of the '806 patent." PO Sur-reply 15. As Patent Owner acknowledges (*id.*), the issue is *not* whether Mostafazadeh teaches vertically stacked chips, but whether a person of ordinary skill would have had a reasonable expectation of success in applying Mostafazadeh's wafer stage adhesive layer application process to Ball's vertically stacked multichip device.

Petitioner shows persuasively that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Mostafazadeh with Ball and Fogal. Pet. 32–33. The evidence discussed above concerning reasons to combine supports a reasonable expectation of success. We are also persuaded by Dr. Suhling's testimony that the "combination of Ball, Fogal, and Mostafazadeh would require no modification of the multichip modules in Ball and Fogal: rather Mostafazadeh merely explains in more detail methods known in the art for creating chips with adhesive surfaces." Ex. 1002 ¶ 239; *see also id.* ¶¶ 62–69 (describing prior art methods for applying adhesive to the backside of a wafer).

For the foregoing reasons, we find that Petitioner has demonstrated that a person of ordinary skill in the art would have had a reasonable expectation of successfully combining Ball, Fogal, and Mostafazadeh.

5. Adhesion Layer Limitations

For claim elements [1b], [1c], [2c], [23b], [23c], [24c], [30a], and [30d], the parties dispute whether the prior art teaches an "adhesion layer." *See* PO Resp. 26. For claim elements [1b], [1c], and [2c], the parties also dispute whether the prior art teaches a semiconductor chip with an "adhesion

layer adhered to its back surface where a circuit is not formed." *Id.* We address these disputes in the subsections below.

a) "adhesion layer"

Claim elements [1b] and [1c] recite an "adhesion layer":

> a first semiconductor chip having a first adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on said wiring layer through the first adhesion layer; and
>
> a second semiconductor chip having a second adhesion layer adhered to its back surface where a circuit is not formed, said first semiconductor chip being mounted on a circuit-formed front surface of said first semiconductor chip through the second adhesion layer.

Ex. 1001, 13:49–59.[14] Petitioner presents alternative contentions for the "adhesion layer" of claim elements [1b], [1c], and [2c], arguing that it is taught by the combination of Ball and Fogal, or by the combination of Ball, Fogal, and Mostafazadeh. Pet. 38–46, 51. First, Petitioner contends that the combination of Ball and Fogal's disclosure meets claim element [1b], which "is not limited . . . as to when or how the adhesive is applied." *Id.* at 42. Alternatively, Petitioner contends that, if claim elements [1b] and [1c] require a pre-applied adhesive backside, they are taught by Mostafazadeh in combination with Ball and Fogal. *Id.* at 42–46; *see also id.* at 51 (relying on the same arguments for claim element [2c] as previously presented for element [1c]).

[14] Claim element [2c] is the same as claim element [1c]. *Compare* Ex. 1001, 14:5–19, *with id.* at 13:54–59. Claim elements [23b], [23c], [24c], [30a], and [30d] recite forming an adhesion layer on a back surface of a wafer. *See, e.g, id.* at 16:36–37.

Patent Owner argues that "Ball, Fogal and Mostafazadeh all fail to disclose an adhesion layer because they disclose or teach mere adhesives, in whole or in part, including tapes that are adhered through adhesive and thermoplastic layers that are not pre-formed and can deform during the attachment or assembly process of the semiconductor device." PO Resp. 27.

Having considered the parties' arguments and evidence, we determine that Petitioner meets its burden of proof for claim elements [1b], [1c], and [2c] based on both of Petitioner's alternative contentions regarding an "adhesion layer."[15]

First, we agree with Petitioner that claims 1 and 2 are not limited as to when or how an adhesion layer is formed. Pet. 42. Claim 1 is directed to a semiconductor device, and elements [1b] and [1c] recite "a first semiconductor chip having a first adhesion layer adhered to its back surface" and "a second semiconductor chip having a second adhesion layer adhered to its back surface," respectively. Ex. 1001, 13:49–55. In contrast to the exemplary embodiments in the written description, claim 1 does not require that the adhesion layer be adhered to the back surface of the first semiconductor chip in advance or when it is in the wafer state. *See, e.g.,* Ex. 1001, 3:38–41, 4:4–18 (disclosing that "the insulating adhesion layer . . . [is] disposed on the back surface of the second semiconductor chip in advance"); *id.* at 4:48–54, 5:15–21 (disclosing that "the second semiconductor chip has the insulating adhesion layer adhered to its back surface in advance when being in the wafer state"). Claim 2 is similar to

[15] For claim elements [23b], [23c], [24c], [30a], and [30d], we rely only on Petitioner's second alternative, which is based a combination of Ball, Fogal, and Mostafazadeh.

claim 1 in this respect, whereas other claims require forming an adhesion layer on a back surface of a wafer. *See, e.g., id.* at 16:63–66 (claim 24: "a second semiconductor chip produced by forming an adhesion layer on a back surface of a wafer having a desired circuit formed on its front surface and by dicing the wafer"); *id.* at 17:60–18:7 (claim 30 recites the steps of "forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface" and "producing separate second semiconductor chips from said second wafer by dicing").

For the reasons discussed in Section II.C. above, we construe "adhesion layer" to mean "a layer that adheres." Our claim construction does not limit when or how an adhesion layer is formed.

Under our claim construction, we agree with Petitioner that the combination of Ball and Fogal discloses claim element [1b]. *See* Pet. 38–42. Ball teaches vertically stacked chips, but as Petitioner acknowledges (*id.* at 38), Ball's figures do not show a chip stack in which the lower chip is face up, as required by claim element [1b]. For this arrangement, Petitioner relies on Fogal, which discloses first chip 18's base face 20 is adhered to substrate 12 "by means of an adhesive, such as epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc.". Ex. 1004, 2:38–43; *see also id.* at 3:10–12; Ex. 1002 ¶ 256 (a person of ordinary skill would understand that the backside of Fogal's first chip may contain an adhesive layer for mounting to the substrate instead of placing the adhesive on the substrate). We find that these disclosures in Fogal teach an "adhesion layer" as recited in claim element [1b].

We also find that the combination of Ball and Fogal discloses an "adhesion layer" as recited in claim elements [1c] and [2c]. *See* Pet. 45–46,

51. As discussed by Petitioner (*id.*), Fogal discloses that adhesive layer 38 is interposed between and connects bonding face 22 of first chip 18 and base face 30 of second chip 28. *Id.* at 2:49–54; Fig. 1 (showing multichip stack 14 including, from top to bottom, second chip 28, adhesive layer 38, and first chip 18). We find that Fogal's adhesive layer 38 teaches an "adhesion layer" as recited in claim elements [1c] and [2c]. *See* Ex. 1002 ¶ 262–264.

Second, we agree with Petitioner that, even if claim elements [1b], [1c], and [2c] require a pre-applied adhesive backside, then Mostafazadeh in combination with Ball and Fogal teaches these elements. Pet. 42–44, 46. For the reasons discussed in Section II.D.4. above, we find that a person of ordinary skill in the art would have had reasons to combine Ball and Fogal's stacked die multichip module with Mostafazadeh's process for applying adhesive at the wafer stage and then dicing to create individual chips with adhesive backsides. Petitioner shows persuasively that using Mostafazadeh's process to produce individual chips, such as Fogal's first chip 18 and second chip 28, having circuitry on one side and a pre-applied adhesive on the other side, will result in a first semiconductor chip as recited in claim element [1b] and a second semiconductor chip as recited in each of claim elements [1c] and [2c]. *See* Pet. 43–44 (discussing Mostafazadeh's process for producing individual dies having an integrated circuit and an adhesive layer).

We also find that Mostafazadeh teaches the step of forming an adhesion layer on a back surface of a wafer, as recited in claim elements [23b], [23c], [24c], [30a], and [30d]. Pet. 56–59. As discussed above, Mostafazadeh teaches forming an adhesive coating on the back surface of a semiconductor wafer, drying the adhesive coating, and dicing

the semiconductor wafer to form individual integrated circuit dies, each having an adhesive layer on its back surface. Ex. 1004, 3:5–11, 5:20–25, 7:9–11, 7:29–8:2, Fig. 2 (steps 104–110).

Patent Owner's counterarguments are based on its contentions that an "adhesion layer" is a "pre-formed layer that is adhered." PO Resp. 27–32. We do not adopt Patent Owner's claim construction for the reasons discussed in Section II.C.1. above. We disagree with Patent Owner's counterarguments about the prior art for the same reasons.

b) "adhesion layer adhered to its back surface where a circuit is not formed"

Claim elements [1b], [1c], and [2c] each recite a semiconductor chip having an "adhesion layer adhered to its back surface where a circuit is not formed." Ex. 1001, 13:50–56, 14:5–7.

As discussed above, Petitioner contends that the combination of Ball, Fogal and Mostafazadeh teaches these claim elements. Pet. 38–46, 51. Patent Owner disputes Petitioner's contention, arguing that these claim elements require an adhesion layer that covers the entire back surface of the chip, which is not shown by Ball or Fogal. PO Resp. 34–38.

After considering the parties' arguments and evidence, we determine that Petitioner meets its burden of proof for these claim elements.

For claim element [1b], Petitioner shows persuasively that Fogal discloses a first semiconductor chip (Fogal's first chip 18) having a first adhesion layer ("adhesive, such as epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc.") adhered to its back surface (base face 20) where a circuit is not formed. Pet. 38–39 (citing Ex. 1004, 1:46–47, 2:31–36, Fig. 1). For claim element [1c], Petitioner shows persuasively that Fogal discloses a second semiconductor chip (Fogal's second chip 28)

having a second adhesion layer ("adhesive layer 38") adhered to its back surface (base face 30) where a circuit is not formed. Pet. 45–46 (citing Ex. 1004, 2:44–54, 2:63–66, Fig. 1).

Fogal supports our finding. As to element [1b], Figures 1 and 2 of Fogal show that when base face 20 of first chip 18 is adhered to substrate 12, its bonding face 22 includes bonding pads 26 peripheral to central area 24 (Ex. 1004, 2:28–43), and bond wires 44 and 50 provide electrical connection between pads 26 and substrate 12 (*id.* at 2:28–43). We credit Dr. Suhling's testimony that a person of ordinary skill in the art would have understood that the chip bond pads are located on the same surface as the circuitry and that the adhesive layer is adhered to the backside of the chip, not the circuit side. Ex. 1002 ¶ 256. As to element [1c], Fogal discloses that second chip 28 includes bonding face 32 which electrically connects second chip to the wiring layer. Ex. 1004, 2:44–46, 2:63–66. We credit Dr. Suhling's testimony that a person of ordinary skill in the art would have understood Fogal's bonding face 32 is the surface where the semiconductor circuitry is formed, and thus the backside of second chip 28 is adhered to the front surface of first chip 18 through an adhesion layer. Ex. 1002 ¶¶ 263–264.

Patent Owner argues that to meet claim elements [1b], [1c], and [2c], a reference must show that an adhesion layer extends to cover the entire back surface of the first (element [1b]) or second (elements [1c], [2c]) semiconductor chip where a circuit is not formed. PO Resp. 33, 39. We find no support in the claim language or other intrinsic evidence for Patent Owner's argument. In our view, the phrase "back surface where a circuit is not formed" identifies the back side of the chip as opposed to the front side, where a circuit is formed. Ex. 1001, 13:50–51 (claim element [1b]). The

claim language as a whole supports our interpretation. Claim 24, for example, recites "an insulating substrate including a wiring layer on its *front surface* and a packaging-use external terminal on its *back surface*." *Id.* at 16:54–56. Here, the term "back surface" refers to the surface opposite the "front surface" and does not require the entire back surface. *See id.* at Fig. 1 (showing external terminals 10 covering less than the entire back surface of insulating substrate 3).

The Specification portions and expert testimony cited by Patent Owner do not support a requirement that an adhesion layer cover the entire back surface of the second semiconductor chip where a circuit is not formed. PO Resp. 33–34 (citing Ex. 1001, 2:23–26, 6:48–51, 6:56–59, Fig. 10; Ex. 2014 ¶ 54). The '806 patent discusses the problem of excessive adhesive agent extending beyond the outer edge of the semiconductor chip (Ex. 1001, 2:23–26), but this discussion does not support Patent Owner's argument that an adhesion layer must cover the entire back surface of the second chip. Mr. Elenius testifies that the claim language "comports with the problem the '806 patent sought to solve" (Ex. 2014 ¶ 54), but, tellingly, does not say that the claims require an adhesion layer that covers the entire back surface of the second semiconductor chip.

The remaining portions of the Specification cited by Patent Owner do not support interpreting claim elements [1b], [1c], and [2c] as requiring an adhesion layer that covers the entire back surface of the second semiconductor chip. Ex. 1001, 6:48–51, 6:56–59 (describing Figure 1 embodiment with adhesion layer between first and second semiconductor chips); *id.* at Fig. 10 (showing back-to-back chip stack with adhesion layer between the chips). Figures 1 and 10 are two-dimensional cross-sectional

views of a three-dimensional semiconductor device and thus cannot, on their own, show the entire back surface of a semiconductor chip. Neither the figures themselves, nor the descriptions of the figures, show how much of the back surface of the chip is covered by an adhesion layer. Even if Figures 1 and 10 showed an adhesion layer covering the entire back surface of a semiconductor chip, we are not persuaded that this feature should be read from the Specification into the claims. *In re Am. Acad. Of Sci. Tech Ctr.*, 367 F.3d at 1369.

Patent Owner argues that Ball does not teach claim elements [1b], [1c], and [2c] because "Ball does not disclose a first semiconductor chip with an adhesion layer adhered to its entire back surface (where a circuit is not formed)." PO Resp. 34 (citing Ex. 2014 ¶ 75). We disagree. Patent Owner's argument is not applicable to Petitioner's obviousness combination, which relies on Fogal to teach the first and second semiconductor chips of claim elements [1b], [1c], and [2c]. Pet. 38–39, 45–46.

Patent Owner argues that Fogal does not teach claim elements [1b], [1c], and [2c] because Fogal "teaches that the adhesives should be applied to extend to only a part of the back surface of the first chip. PO Resp. 35 (citing Ex. 1004, 2:51–54, Fig. 2; Ex. 2013 ¶ 94). Patent Owner's argument is not persuasive because it is based on an incorrect claim interpretation, as previously discussed.

Furthermore, Patent Owner's argument does not address Petitioner's alternative contention which relies on Mostafazadeh to teach the claimed adhesion layers. Pet. 42, 46. Even if Patent Owner were correct that the claim language requires the adhesion layer to cover the entire back surface of the second semiconductor chip, we find that Mostafazadeh teaches this

limitation. Ex. 1003, 10:6–8 ("The adhesive layer 184 covers the entire mounting surface 190 of the selected integrated circuit die 182 and does not extend beyond a boundary of the mounting surface 190."); *see also id.* at 6:28–7:1 (disclosing that "the roller ends 154 are arranged to extend beyond a wafer surface 162 during the application of the adhesive" which "[e]nsures that an adhesive coating 164 *is formed over the entire wafer surface 162*" depicted in Figure 4a) (emphasis added). And consistent with our claim construction in Section II.C.1., Mostafazadeh's fluid-based adhesive, e.g., a B-stageable epoxy, forms an "adhesion layer" after it is rolled onto a surface and dried to form a hard layer. Ex. 1003, 6:3–6, 7:9–16, 13:8–12 (claim 7: "the drying step turns the adhesive coating into a hard surface"); Ex. 2014 ¶ 50.

6. Packaging-use External Terminal and Via Hole

Claim elements [23a] and [24a] recite "an insulating substrate including … a packaging-use external terminal on its back surface … the packaging-use external terminal being electrically connected to said wiring layer through a via hole." *E.g.*, Ex. 1001, 16:30–36. Petitioner relies on Ball's definition of a Ball Grid Array (BGA) and argues that a person of ordinary skill in the art would have understood that a BGA package included "packaging-use external terminals" to connect the bottom-side of the substrate to a chassis or motherboard. Pet. 54–55 (citing Ex. 1005, 1:16–20). Petitioner points to Ball's disclosure of "bump connections" to evince such external terminals, and asserts that the skilled artisan would understand that Ball's reference to "bump connections" are terminals necessary to connect the semiconductor package to other components. Pet. Reply 19–20 (citing Ex. 1005, 5:37–40; Ex. 1002 ¶¶ 37–38, 187–193; Ex. 1037, 49:25–

50:3; Ex. 2012, 64:15–73:15). Petitioner relies on Aoki[16] Figure 1 and Figure 13(a) of the '806 patent as evidence that "packaging-use external terminals" electrically connected by "through-holes" to the wiring layer were known in the art before 1998 (Pet. 55–56 (citing Ex. 1001, Fig. 13(a); Ex. 1015, Fig. 1, ¶¶ 67, 82, 83)), and that a person of ordinary skill in the art would have understood that Ball's BGA multichip module included "packaging-use external terminals . . . connected to said wiring layer through a via hole." *Id.* at 56 (citing Ex. 1002 ¶¶ 286–293).

Patent Owner argues that Ball, Fogal, and Mostafazadeh fail to disclose a "packaging-use external terminal" and a "via-hole." PO Resp. 40–44; PO Sur-reply 15–18. Patent Owner argues that a "packaging-use external terminal" and "via hole" are not admitted prior art and not within the general knowledge of a person of ordinary skill in the art. PO Resp. 15–18, 44–46; PO Sur-reply 18–21, 22–23. Patent Owner argues there would have been no motivation to combine Ball and Aoki, and Aoki does not help a skilled artisan understand Ball's "bump connections" as under-substrate connections. PO Resp. 60–66; PO Sur-reply 22. Patent Owner argues that Petitioner introduces a new rationale in the reply brief by relying on Ball's disclosure of "bump connections." PO Sur-reply 24–25.

After considering the parties' arguments and evidence, we determine that Petitioner has met its burden of proof for claim elements [23a] and [24a].

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[16] Jap. Patent App. No. 121002/1997 to Aoki et al., published May 6, 1997 (Ex. 1015). It is undisputed that Aoki is prior art to the '806 patent under 35 U.S.C. § 102(b). Pet. 12; PO Resp. 14–16. Aoki Figures 1 and 24 are replicated in the '806 patent as Figures 13(a) and 13(b), respectively.

Claim elements [23a] and [24a] recite "a packaging-use external terminal" on the "back surface" of the substrate, whereas the BGA described in Ball column one (Ex. 1005, 1:16–20) is on top of the substrate. *See* Ex. 2014 ¶ 85 (Mr. Elenius: "Ball's BGA is a first-level flip chip interconnect (i.e., between IC and next level of package) and not a second-level interconnect (i.e., between the semiconductor package and next level of assembly)."). Petitioner, however, does not contend that Ball's BGA is itself "a packaging-use external terminal." Instead, Petitioner contends that a person of ordinary skill in the art would have understood that a BGA package would have included "packaging-use external terminals" to connect the bottom-side of the substrate to a chassis or motherboard. Pet. 54–55. We find that Petitioner's contention is persuasive and supported by the evidence, including Ball's disclosure and the testimony of both parties' experts. Ex. 1002 ¶ 182; Ex. 1005, 5:37–40; Ex. 1037, 49:2–17.

Under cross-examination by Patent Owner, Dr. Suhling directed us to Ball's disclosure of bump connections on the back surface of the substrate.

> Q. Can we look at [Ball] Figure 1 again?
>
> A. Yes.
>
> Q. Is there anything shown below substrate 16?
>
> A. There is nothing shown, but again I would suggest that that was -- that a person state in the art -- familiar with the state of the art would understand that there would be an additional set of solder ball connections underneath 16 that connect to a larger printed circuit board or motherboard. That's what he is suggesting in this paragraph in column 5 that starts on line 37 and goes to line 42, where he talks about substrate 16 can be connected to a motherboard by using bump connections. He just hasn't illustrated them for some reason in Figure 1.

> Q. And just to clarify your position, he has not explicitly disclosed it in Figure 1, correct?
>
> A. Figure 1 does not show the solder joint connections below the substrate, the semiconductor device substrate number 16 that would be used to attach it to a printed circuit board, but he does talk about it, like I said, in column 5.

Ex. 2012, 71:10–72:5 (referring to Ex. 1005, 5:37–42). In the foregoing testimony, Dr. Suhling directs us to Ball's disclosure that the substrate "may itself be connected to a chassis or mother board by edge connections, bump connections, pin connections, or other conductive arrangements as known in the art." Ex. 1005, 5:37–40.

It is undisputed that Ball's "bump connections" (*id.*) are terminals. *See* Ex. 1037, 52:16–18 (Mr. Elenius agreeing that Ball (Ex. 1005, 5:37–40) describes terminals). The surrounding testimony shows that Mr. Elenius used the word "terminal" to include "packaging-use external terminals." *Id.* at 47:17–21 ("Q. . . . Is packaging use[] external terminal a term that you've heard -- are there other terms in the art that refer to the same thing, these points of external connection? A. JEDEC uses the term terminal.").

Although the experts disagree about whether Ball's "bump connections" (Ex. 1005, 5:37–40) are on the back surface of the substrate, we find Dr. Suhling's testimony more persuasive than Mr. Elenius's. Dr. Suhling testifies that Ball's "bump connections" are located underneath the substrate. Ex. 2012, 71:10–72:5 (quoted above); *id.* at 74:4–14 (testifying that, in Ball, bump connections and pin connections "occur on the bottom of the substrate 16"). We are unpersuaded by Mr. Elenius's contrary view that, in Ball, "bump connections" could refer to "solder pads (e.g., bumps) on the top surface of the substrate." Ex. 2014 ¶ 86; *see also*

Ex. 1037, 51:14–52:15 (similar testimony). We find that Mr. Elenius's description of "bumps on the top surface of the substrate" is inconsistent with Ball's description of "bump connections" that connect the substrate to a chassis or motherboard. Ex. 1005, 5:37–40. In order to connect the substrate to a chassis or motherboard, the bump connections must be underneath the substrate. *Id.*; *see* Ex. 2014 ¶ 131 (describing a "motherboard" as "another external substrate, which is usually a PCB . . . that the packaged semiconductor is mounted to").

In view of the foregoing, we find that a person of ordinary skill in the art would have understood that a BGA package, as disclosed in Ball, would have included a "packaging-use external terminal" to connect the bottom-side of the substrate to a chassis or motherboard. Pet. 54–55; Ex. 1002 ¶ 182. The experts agree that such terminals are necessary to make an operable device. Dr. Suhling testified:

> Q. And in [Ball Figure 1], there's no showing of any connections below the substrate 16, correct?
>
> A. Yes, as we've discussed, the connections below 16 are not shown; but if this device is to be attached to a larger printed circuit board, a motherboard, which hold[s] multiple semiconductor devices, it would have to have some kind of connections from 16 to the printed circuit board, and traditionally those are another set of solder bumps underneath number 16.

Ex. 2012, 77:23–78:6; *see also id.* at 74:24–75:13 (explaining that "there often are several layers of bumps" including "a second set of solder bump connections that connect the substrate in the semiconductor device to the motherboard or larger printed circuit board").

Mr. Elenius agrees that connection terminals are necessary to make an operable device.

> Q. If you didn't have terminals, would the semiconductor device be operable?
>
> A. No.
>
> Q. So you have to have these terminals in order for it to be structurally attached to and electrically communicate with any other -- any other type of component, whether it be a motherboard and the components thereon?
>
> A. There has to be some type of terminal to make that communication.

Ex. 1037, 49:7–15. Although Mr. Elenius testified there are "many forms of terminals" (*id.* at 49:16–17), he also agreed that Ball's "bump connections" are terminals. *Id.* at 52:16–18.

We are also persuaded by Petitioner's argument that a person of ordinary skill in the art would have understood that Ball's bump connections are connected to the wiring layer through via holes in the insulating substrate. Pet. 56. In this regard, we rely on Dr. Suhling's testimony that, "while Ball does not go as far as depicting through-holes and external connections[,] . . . they must be there for the device to work." Ex. 1002 ¶ 185. Dr. Suhling reiterated this point at his deposition:

> Q. And if the bumps are below the substrate, there would be need of a -- some sort of connection that passes through the substrate to connect those bumps to the semiconductor device above the insulated substrate, correct?
>
> A. That is totally true. The substrate, number 16, in Ball's Figure 1 would have to have a set of electrical pathways from its top surface, as shown in Figure 1, to the bottom surface.
>
> Q. And at least in the figures, no such electrical connections are shown or explicitly disclosed, correct?
>
> A. Again, they are not shown, but a person of skill in the art would know they have to be there. Anytime you say "substrate" or "printed circuit board," one of skill in the art would understand

> there are internal attributes and components that help connect electrically from the top to the bottom.

Ex. 2012, 75:14–76:22. When asked to compare Ball Figure 1 to Aoki Figure 1, Dr. Suhling testified:

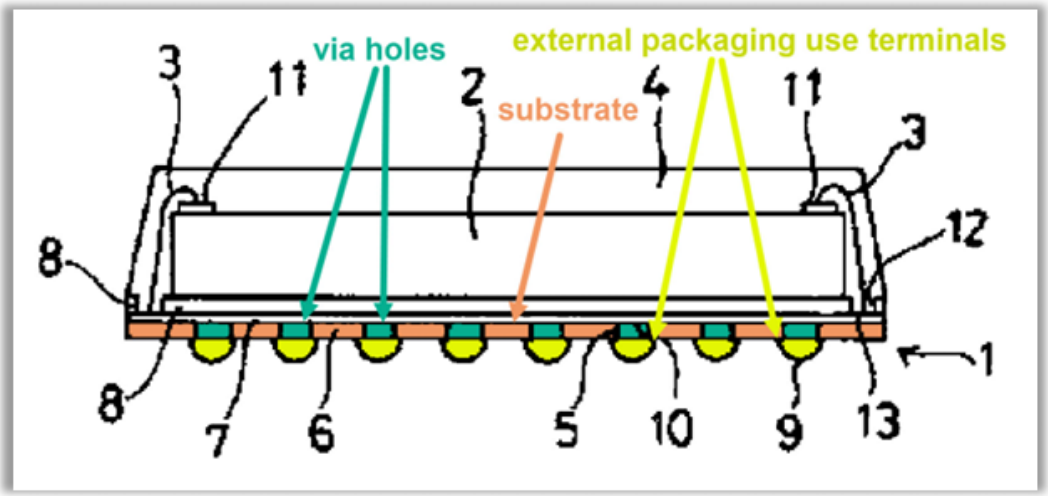
> And I think similarly in Ball, . . . a person of skill in the art would understand that the substrate number 16 has to have similar through-holes and wiring patterns inside of it to take those connections number -- bond pads number 26 on the top of substrate 16 and bring them down to the bottom electrically so that it can connect -- this device can connect to a printed circuit board.

Id. at 78:22–79:24.

Petitioner also persuades us that packaging-use external terminals and via holes (or "through holes") were known in the art and that such knowledge would have informed the skilled artisan's understanding of Ball's multichip semiconductor package. It is undisputed that packaging-use external terminals and via holes are disclosed in Aoki. Pet. 12–14; PO Resp. 14–16; Ex. 1015, ¶¶ 80–88, Fig. 1 (showing and describing a semiconductor device with through holes 5 and external connection terminals 9); *id.* ¶¶ 16–24, Fig. 24 (showing and describing a semiconductor device with through holes 51 and external connection terminals 59). Aoki Figures 1 and 24 are replicated in the '806 patent Figures 13(a) and 13(b), respectively, where they are described as showing chip size package structures made by "conventional" wire bonding and face-down bonding methods. Ex. 1001, 6:18–23. The '806 patent discusses Figures 13(a) and 13(b) in the background of the invention section, which identifies through holes 45 and 61 and external connection-use terminals 49 and 69, respectively. *Id.* at 1:28–52. Patent Owner argues that "Applicant did not

admit that the external connection terminal package and via holes are prior art." PO Resp. 15–18. We see no need to resolve the parties' dispute about whether packaging-use external terminals and via holes are applicant-admitted prior art (AAPA) because, as discussed above, it is undisputed that these features are disclosed in Aoki and that Aoki is prior art to the '806 patent under § 102(b). Pet. 12; PO Resp. 14–16.

We find that Aoki Figure 1 provides persuasive support for Petitioner's contention that a person of ordinary skill in the art would have understood Ball's device as including a packaging-use external terminal and via hole for electrically connecting the wiring layer to a chassis or motherboard. Pet. 55–56. Petitioner's annotation of Aoki Figure 1 is reproduced below.



Aoki - Figure 1

Pet. 55. Aoki Figure 1, as annotated by Petitioner, shows a semiconductor device including insulating substrate 6, via holes 5, and external packaging use terminals 9. *Id.* Aoki discloses "substrate 6 with insulation properties as the external connection insulation material," which has "through holes 5"

and "wiring pattern 7" on its upper surface. Ex. 1015 ¶ 82. These disclosures support Petitioner's contention. Aoki further discloses

> external connection terminal 9 is formed on the underside of the substrate 6, and the wiring pattern 7 has an external connection area 10, which is an external connection terminal formation point for connecting the wiring pattern 7 and the external connection terminal 9 via through holes 5.

Id. ¶ 83. Aoki's disclosures support Petitioner's contention that a person of ordinary skill in the art would have understood Ball's device as including external connection terminals (bump connections) and through holes (via holes) for electrically connecting the wiring layer on top of the substrate to a chassis or motherboard beneath the substrate. Pet. 55–56. As Dr. Suhling testifies, a person of ordinary skill in the art would have understood that substrate 16 of Ball needs to include through holes, similar to Aoki's via holes in substrate 6, to make electrical connections from bond pads on top of substrate 16 to the printed circuit board beneath the substrate. Ex. 2012, 79:4–24.

We find that Aoki provides persuasive support for Dr. Suhling's opinions that "package use external terminals electrically connected by through-holes to the wiring layer on the substrate were standard knowledge in the state-of-the-art particularly for BGA assemblies" and "because Ball discloses BGA multichip modules, and because these concepts were well-known in the state of the art and necessary for the flip-chip device to work, Ball and the knowledge of a skilled artisan render obvious the packaging-use external terminals and through holes for connecting to printed circuit boards" as required by claim elements [23a] and [24a]. Ex. 1002 ¶ 293.

We have considered Patent Owner's argument that Ball, Fogal, and Mostafazadeh fail to disclose a "packaging-use external terminal" and a "via-hole." PO Resp. 40–44; PO Sur-reply 15–18. As discussed above, we are persuaded that a person of ordinary skill in the art would have understood that Ball's "bump connections" (Ex. 1005, 5:37–40) are packaging-use external terminals as recited in claim elements [23a] and [24a], and that a person of ordinary skill in the art would have understood that these bump connections are connected to the wiring layer through via holes, similar to the manner in which Aoki's external connection terminals 9 are connected to wiring pattern 7 via through holes 5. Ex. 1002 ¶¶ 288–293; Ex. 1015 ¶¶ 82, 83, Fig. 1.

Patent Owner asserts that "Ball's reference to a bump connection is . . . ambiguous as to whether it's a BGA under the substrate connected through via holes because *to be a under substrate ball-grid array, it needs to teach via holes as well*" and "*if bumps were located under the substrate, connections through the substrate would be necessary*." PO Resp. 44 (emphasis added). The italicized portions of Patent Owner's assertion support Dr. Suhling's testimony that a person of ordinary skill in the art would have understood that via holes are needed to connect Ball's "bump connections" to the wiring layer. Ex. 1002 ¶¶ 288–293; Ex. 2012, 75:14–22, 78:22–79:24. Contrary to the non-italicized portions of Patent Owner's assertion, we find that Ball unambiguously discloses bump connections located beneath the substrate. Ex. 1005, 5:37–40; Ex. 2012, 71:10–72:5, 74:4–14, 77:23–78:6.

We have also considered Patent Owner's argument that a "packaging-use external terminal" and "via hole" are not within the general knowledge

of a person of ordinary skill in the art. PO Resp. 44–46; PO Sur-reply 18–21, 22–23. As discussed above, it is undisputed that these features are disclosed in Aoki, which together with Dr. Suhling's testimony, is sufficient to establish that packaging-use external terminals and via holes were within the knowledge of a person of ordinary skill in the art. Ex. 1002 ¶¶ 92–95, 288–293; Ex. 1015 ¶¶ 16–24, 80–88, Figs. 1, 24; Ex. 2012, 78:7–81:4. *See Koninklijke Philips*, 948 F.3d at 1337–38 (holding that the Board properly relied on expert evidence, corroborated by a reference outside of Petitioner's obviousness combination, to conclude that a claim limitation missing from that combination "was not only in the prior art, but also within the general knowledge of a skilled artisan").

We have also considered Patent Owner's argument that there would have been no motivation to combine Ball and Aoki. PO Resp. 60–67. That argument is inapt because Petitioner and Dr. Suhling rely on Aoki to show the knowledge of a person of ordinary skill in the art and how a skilled artisan would have understood Ball's disclosure. Pet. 54–56; Pet. Reply 22–25; Ex. 1002 ¶¶ 288–293; *see* Tr. 56:1–7 (Patent Owner acknowledging that Petitioner does not need to show a motivation to combine Ball and Aoki). In any event, we find that the record supports a reason or motivation for combining a multichip device, as disclosed in Ball, with a skilled artisan's knowledge of packaging-use external terminals and via holes. The experts agree that electrical connections between the substrate's wiring layer and a chassis or motherboard are necessary for Ball's flip chip device to work (Ex. 1037, 49:7–15; Ex. 2012, 75:14–22, 77:23–78:6, 78:22–79:24), and Aoki establishes that packaging-use external

terminals and via holes were known structures for providing such connections (Ex. 1002 ¶¶ 290–293; Ex. 1015 ¶¶ 16–24, 80–88, Figs. 1, 24).

We have also considered Patent Owner's argument that Aoki does not help a skilled artisan understand Ball's "bump connections" as under-substrate connections. PO Sur-reply 21–22. That argument is in essence a dispute about whether Ball's "bump connections" are underneath the substrate or on top of the substrate. *Id.* As discussed above, based on the express disclosure of Ball (Ex. 1005, 5:37–40), we find that Dr. Suhling's view that Ball's "bump connections" are underneath the substrate is more persuasive than Mr. Elenius's view that they are on the top surface of the substrate. *Compare* Ex. 2012, 71:10–72:5, 74:4–14 (Dr. Suhling's testimony), *with* Ex. 1037, 51:14–52:15; Ex. 2014 ¶ 86 (Mr. Elenius's testimony).

We have also considered Patent Owner's argument that Petitioner introduces a new rationale in the reply brief by relying on Ball's "bump connections" as disclosing the claimed packaging-use external terminals. PO Sur-reply 24. The Federal Circuit instructs that "in some circumstances the Board acts within its discretion when declining to consider a new theory of unpatentability raised by petitioner in reply." *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1383 (Fed. Cir. 2023). "In other circumstances, . . . a reply may be proper if it is responsive and simply expands on previously raised arguments." *Id.* at 1384.

Under the circumstances of this case, we find that Petitioner's reliance on Ball's "bump connections" as disclosing the claimed packaging-use external terminals is responsive to Patent Owner's arguments and appropriately expands on arguments raised in the Petition. Although not in

the context of discussing a "packaging-use external terminal," the Petition and Dr. Suhling's direct testimony discuss Ball's disclosure of "bump connections." Pet. 20 (referencing Ball Figure 1: "substrate 16 connects to a chassis or mother board by edge connections, bump connections, pin connections, or other conductive arrangements known in the art," citing Ex. 1015, 5:37–40) Ex. 1002 ¶ 110 (same). Furthermore, the Petition and Dr. Suhling assert that a person of ordinary skill in the art would have understood that Ball "included 'packaging-use external terminals' to connect the bottom-side of the substrate to another chassis or motherboard." Pet. 54–55; Ex. 1002 ¶ 182. We find it significant that the Petition and Dr. Suhling use the same language, "chassis or motherboard," when discussing Ball's disclosure of "bump connections" and when discussing the claimed "packaging-use external terminal." *Compare* Pet. 20 *and* Ex. 1002 ¶ 110 (discussing Ball's "bump connections"), *with* Pet. 54–55 *and* Ex. 1002 ¶ 182 (discussing a "packaging-use external terminal").

Petitioner's reliance on Ball's "bump connections" in the reply brief is responsive to Patent Owner's arguments. As part of its argument that Ball fails to disclose a "packaging-use external terminal," Patent Owner quotes Ball's disclosure that "[s]ubstrate 16, if an insulative substrate, may itself be connected to a chassis or mother board by edge connections, bump connections, pin connections, or other conductive arrangements as known in the art." PO Resp. 43–44 (citing Ex. 1015, 5:37–42). Patent Owner then argues that "Ball's reference to a bump connection is . . . ambiguous." *Id.* at 44 (citing Ex. 2014 ¶ 86). In the cited testimony, Mr. Elenius quotes Ball's disclosure of "bump connections" and opines that a "bump connection" may

be "solder pads (e.g., bumps) on the top surface of the substrate." Ex. 2014 ¶ 86.

With the foregoing argument and evidence, Patent Owner raised the issue of whether Ball's "bump connections" disclose the claimed "packaging-use external terminal." Petitioner's reply argument is directly responsive to Patent Owner's argument and evidence. Pet. Reply 19–20, 25. And Petitioner's reply argument is a fair extension of Petitioner's previously raised argument that a person of ordinary skill in the art would have understood that Ball "included 'packaging-use external terminals' to connect the bottom-side of the substrate to a chassis or motherboard." Pet. 54–55; Ex. 1002 ¶ 182.

Based on the evidence before us, we determine that Petitioner has shown that the combination of Ball and the knowledge of a person of ordinary skill in the art discloses claim element

7. Remaining Elements and Dependent Claims 12 and 13

We have reviewed Petitioner's undisputed showings and find that the combined teachings of Ball, Fogal, and Mostafazadeh teach or suggest the remaining limitations recited in independent claims 1, 2, 23, 24, and 30, as well as dependent claims 12 and 13. We further find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner as explained above. Pet. 29–59; PO Resp. 26–48 (presenting arguments regarding limitations discussed above and motivation to combine the references, but no other arguments regarding the remaining limitations of claims).

8. Conclusion

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 2, 12, 13, 23, 24, and 30 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, and the knowledge of a skilled artisan.

E. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Ahmad, and the Knowledge of a Skilled Artisan

Petitioner asserts that dependent claims 6, 7, 9, 10, 25, and 26 are unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Ahmad, and the knowledge of a skilled artisan. Pet. 60–66. Petitioner explains that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, Mostafazadeh, Ahmad, and the knowledge of a skilled artisan because Ahmad relates to semiconductor devices and specifically teaches vertically stacking semiconductor chips on top of one another to create multichip modules. Pet. 60 (citing Ex. 1006, 1:5–7, 3:11–27). According to Petitioner, Ahmad also solves the same problem as Ball and Mostafazadeh—producing higher performance, lower cost, and smaller semiconductor packages. *Id.* (citing Ex. 1005, 2:26–31; Ex. 1003, 2:27–29; Ex. 1006, 1:62–67). Petitioner asserts that Ahmad teaches using an interposer as a support member when stacking a larger chip on top of a smaller one and that this arrangement of chips (i.e., a bigger chip on top of a smaller chip) allows for more efficient wiring configurations. *Id.* at 61 (citing Ex. 1006, Fig. 2, 2:1–34, 4:40–49, 5:8–25; Ex. 1002 ¶¶ 313–316).

Petitioner provides a detailed analysis showing where it contends each limitation of dependent claims 6, 7, 9, 10, 25, and 26 is taught in Ahmad, and explains why a person of ordinary skill in the art would have been

motivated to combine Ball, Mostafazadeh, and Ahmad. Pet. 61–66; Ex. 1002 ¶¶ 317–326. Patent Owner relies on its arguments for claims 1, 2, 23, and 24, from which these claims depend. *See* PO Resp. 67. Based on Petitioner's undisputed showing, we find that the combination of references discloses all of the limitations of these claims, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the claims with a reasonable expectation of success.

We conclude that Petitioner has shown by a preponderance of the evidence that claims 6, 7, 9, 10, 25, and 26 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, Ahmad, and the knowledge of a skilled artisan.

F. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Weinberg, and the Knowledge of a Skilled Artisan

Petitioner asserts that dependent claims 14 and 15 are unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Weinberg, and the knowledge of a skilled artisan. Pet. 67–70. Petitioner provides a detailed analysis showing where it contends each limitation of claims 14 and 15 is taught in Weinberg, and explains why a person of ordinary skill in the art would have been motivated to combine the teachings of the references. *Id.*; Ex. 1002 ¶¶ 327–335. Patent Owner relies on its arguments for claims 1 and 2, from which these claims depend. *See* PO Resp. 68. Based on Petitioner's undisputed showing, we find that the combination of references discloses all of the limitations of these claims, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the claims with a reasonable expectation of success.

We conclude that Petitioner has shown by a preponderance of the evidence that claims 14 and 15 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, Weinberg, and the knowledge of a skilled artisan.

G. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Ma, and the Knowledge of a Skilled Artisan

Petitioner asserts that dependent claims 16–19 are unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Ma, and the knowledge of a skilled artisan. Pet. 71–75. Petitioner provides a detailed analysis showing where it contends each additional limitation of these claims is taught in Ma, and explains why a person of ordinary skill in the art would have been motivated to combine the teachings of the references. *Id.*; Ex. 1002 ¶¶ 336–344. Patent Owner relies on its arguments for claims 1 and 2, from which these claims depend. *See* PO Resp. 68. Based on Petitioner's undisputed showing, we find that the combination of references discloses all of the limitations of these claims, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the claims with a reasonable expectation of success.

We conclude that Petitioner has shown by a preponderance of the evidence that claims 16–19 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, Ma, and the knowledge of a skilled artisan.

H. Asserted Obviousness over Ball, Fogal, Mostafazadeh, Tsumura, and the Knowledge of a Skilled Artisan

Petitioner asserts that dependent claim 32 is unpatentable under § 103 over Ball, Fogal, Mostafazadeh, Tsumura, and the knowledge of a skilled artisan. Pet. 75–79. Petitioner provides detailed analysis showing where it

contends each additional limitation of claim 32 is taught in Tsumura, and explains why a person of ordinary skill in the art would have been motivated to combine the teachings of the references. *Id.*; Ex. 1002 ¶¶ 345–360. Patent Owner relies on its arguments for claim 30, from which claim 32 depends. *See* PO Resp. 68–69. Based on Petitioner's undisputed showing, we find that the combination of references discloses all of the limitations of this claim, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the subject matter of claim 32 with a reasonable expectation of success.

We conclude that petitioner has shown by a preponderance of the evidence that claim 32 would have been obvious over the combination of Ball, Fogal, Mostafazadeh, Tsumura, and the knowledge of a skilled artisan.

III. MOTION TO EXCLUDE

Petitioner moves to exclude four exhibits submitted by Patent Owner:

(1) Exhibits 2002 and 2015 under each of the Federal Rules of Evidence (FRE) 402 and 901; and

(2) Exhibits 2003 and 2011 under FRE 402.

Mot. Exclude 1–4. Patent Owner opposes. Paper 36.

We do not discuss or cite any of these exhibits in this Decision, or rely on any of them in reaching our determination that all of the challenged claims are unpatentable. Because their presence in the record would not affect our analysis in this Decision, we dismiss as moot Petitioner's motion with respect to these exhibits.

IV. CONCLUSION

Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable as summarized below:

Claims	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 12, 13, 23, 24, 30	103(a)	Ball, Fogal, Mostafazadeh	1, 2, 12, 13, 23, 24, 30	
6, 7, 9, 10, 25, 26	103(a)	Ball, Fogal, Mostafazadeh, Ahmad	6, 7, 9, 10, 25, 26	
14, 15	103(a)	Ball, Fogal, Mostafazadeh, Weinberg	14, 15	
16–19	103(a)	Ball, Fogal, Mostafazadeh, Ma	16–19	
32	103(a)	Ball, Fogal, Mostafazadeh, Tsumura	32	
Overall Outcome			1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, 32	

V. ORDER

In consideration of the foregoing, it is

ORDERED that Petitioner has shown that claims 1, 2, 6, 7, 9, 10, 12–19, 23–26, 30, and 32 of the '806 patent are unpatentable; and

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed as moot; and

FURTHER ORDERED that because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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