

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00073
Patent 6,352,879 B1

Before MINN CHUNG, JULIA HEANEY, and SHELDON M. McGEE,
Administrative Patent Judges.

Opinion of the Board filed by *Administrative Patent Judge* CHUNG.

Opinion Dissenting filed by *Administrative Patent Judge* McGEE.

CHUNG, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–15 (the “challenged claims”) of U.S. Patent No. 6,352,879 B1 (Ex. 1001, “the ’879 patent”). Katana Silicon Technologies LLC (“Patent Owner”) timely filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). Pursuant to our authorization (Ex. 3001), the parties filed briefs further addressing claim construction of “adhesion layer.” Paper 10 (“Reply”); Paper 12 (“Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review is authorized when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” After considering the information presented in the Petition, Preliminary Response, Reply, and Sur-reply, we determine that the information presented establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review of all challenged claims of the ’879 patent, based on all grounds raised in the Petition.

II. BACKGROUND

A. Related Matters

According to the parties, the ’879 patent is the subject of the following district court litigation: *Katana Silicon Techs., LLC v. Micron Tech., Inc.*, 1:22-cv-00282 (D. Idaho). Paper 5, 1; Pet. 2.

The '879 patent is one of several patents owned by Patent Owner that are challenged by Petitioner in various petitions for *inter partes* review, including in IPR2023-00071, IPR2023-00072, and IPR2023-00105.

B. Real Party-in-Interest

Petitioner identifies itself, Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC as the real parties-in-interest. Pet. 2. Patent Owner identifies itself as the sole real party-in-interest. Paper 5, 1.

C. The '879 Patent

The '879 patent describes a miniaturized semiconductor device having a chip size package (CSP) that includes multiple semiconductor chips stacked vertically inside the package (in an arrangement called a stacked package structure). Ex. 1001, 1:15–20, 1:53–65, 2:63–65.

Figure 14(a) of the '879 patent is reproduced below.

FIG.14 (a)

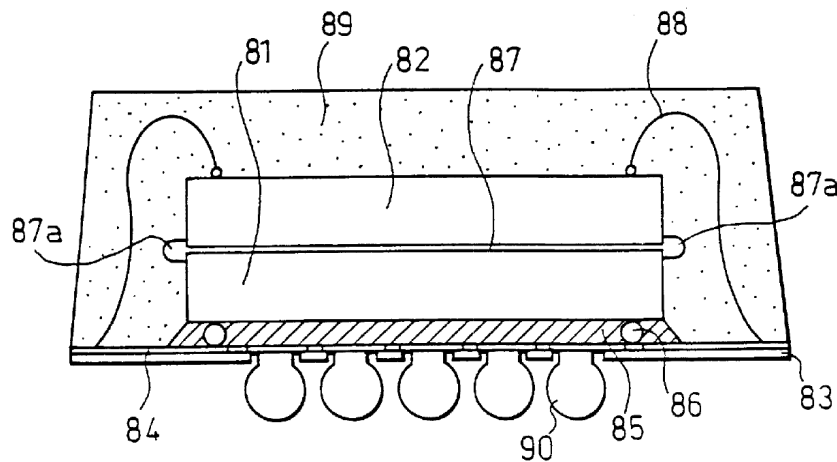


Figure 14(a) shows a cross-sectional view of a conventional semiconductor device having a stacked package structure. *Id.* at 6:24–26.

The '879 patent describes that in a conventional semiconductor device where multiple semiconductor chips are stacked and laminated, two different

methods are used to bond the laminated semiconductor chips to each other in a stacked package—“an adhesive agent (paste) potting method” and “a method using a thermo-compression sheet.” *Id.* at 2:16–21. According to the ’879 patent, in the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent may spread and overflow beyond the outer edge of the semiconductor chips, as illustrated in Figure 14(a) (showing adhesive agent 87 between semiconductor chips 81 and 82 overflowing beyond the edges of the chips). *Id.* at 2:23–29. Such overflowed adhesive agent may come in contact with wires in the package or the electropad of the semiconductor chips. *Id.* at 2:30–42. The ’879 patent describes that “[o]n the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82 . . . causing problems such as separation of the semiconductor chip 82 from the semiconductor chip 81.” *Id.* at 2:44–48.

According to the ’879 patent, the conventional method using a thermo-compression sheet for bonding semiconductor chips during packaging also has shortcomings. *Id.* at 2:49–56, 4:12–21. In the conventional method, the thermo-compression sheet is disposed on the surface of a first semiconductor chip, and then a second semiconductor chip is adhered to the thermo-compression sheet. *Id.* at 9:46–50. The ’879 patent describes that in the conventional thermo-compression sheet method, the thermo-compression sheet must have the same size as semiconductor chip 82 and must be placed accurately at a specific location on semiconductor chip 81. *Id.* at 2:49–53. “In addition, the semiconductor chip 82 must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet.” *Id.* at 2:53–56.

The '879 patent purports to avoid these problems or complications in the conventional method by forming an adhesion layer “in advance” on a back surface of a wafer when the semiconductor chips are in a “wafer state” during the semiconductor fabrication process before the wafer is cut or diced to produce individual chips. *Id.* at 4:18–63. Specifically, the '879 patent describes

[a] method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:

- (a) *forming a first insulating adhesion layer on a back surface of a first wafer* having a circuit formed on its front surface;
- (b) *producing separate first semiconductor chips from the first wafer by dicing*;
- (c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;
- (d) *forming a second insulating adhesion layer on a back surface of a second wafer* having a circuit formed on its front surface;
- (e) *producing separate second semiconductor chips from the second wafer by dicing*;
- (f) *mounting the second semiconductor chip on the first semiconductor chip* with its back surface facing the first semiconductor chip;
- (g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;
- (h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and
- (i) sealing the first and semiconductor chips and the wires.

Id. at 4:21–44 (emphases added).

According to the '879 patent, “[w]ith the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface *in advance when being in the wafer state*,” “the adhesive agent does not overflow the space between

the first and second semiconductor chips” and “the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip.” *Id.* at 4:45–56 (emphasis added).

The '879 patent describes two embodiments. *Id.* at 6:30–12:67. In both embodiments, a thermo-compression sheet is adhered or affixed to the back surface of a wafer to form an adhesion layer “in advance” before the wafer is cut or diced to produce individual pieces of semiconductor chips with an adhesion layer, which are then stacked and bonded to each other in a multi-chip semiconductor device package. *Id.* at 9:17–50, 12:32–44.

Figure 1 of the '879 patent is reproduced below.

FIG. 1

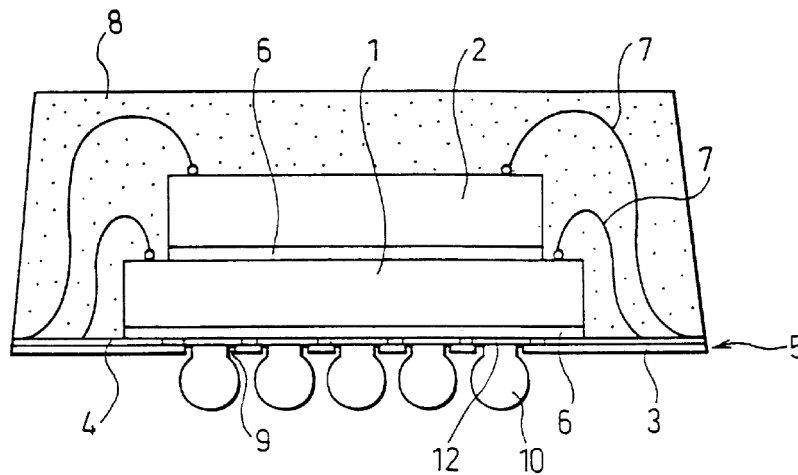


Figure 1 shows a cross-sectional view of a semiconductor device in accordance with the first embodiment of the '879 patent. *Id.* at 5:34–36.

As shown in Figure 1, in a semiconductor device of the first embodiment, “a first semiconductor chip 1 and a second semiconductor chip 2 are laminated . . . on a circuit board 5 including an insulating

substrate 3 and a wiring layer 4 mounted on the insulating substrate 3.” *Id.* at 6:37–41, Fig. 1. The ’879 patent refers to the surface (front surface) of a semiconductor chip on which a circuit element is formed as a “circuit formed surface” and the surface of the opposite side of the chip as a “back surface.” *Id.* at 6:42–46. In the first embodiment depicted in Figure 1, semiconductor chip 1 is disposed with its back surface facing insulating substrate 3. *Id.* at 6:47–48, Fig. 1. “The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6.” *Id.* at 6:48–52.

The ’879 patent describes that “[w]hen the first semiconductor chip 1 is in a wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips 1.” *Id.* at 9:18–22. Similarly, “[w]hen the second semiconductor chip 2 is in the wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce separate pieces of second semiconductor chips 2.” *Id.* at 9:32–36.

According to the ’879 patent,

By affixing the thermo-compression sheet 6 to the back surface of the second semiconductor chip 2 in advance, accurate positioning is necessary only when mounting the second semiconductor chip 2 on the first semiconductor chip 1. Therefore, since one step requiring accurate positioning is omitted in the process for manufacturing the semiconductor device in accordance with the present embodiment, this manufacturing process is simplified compared with the conventional process in which the thermo-compression sheet 6 is disposed on the circuit formed surface of the first

semiconductor chip 1, and then the second semiconductor chip 2 is adhered to the thermo-compression sheet 6.

Id. at 9:41–50.

Figure 10 of the '879 patent is reproduced below.

FIG.10

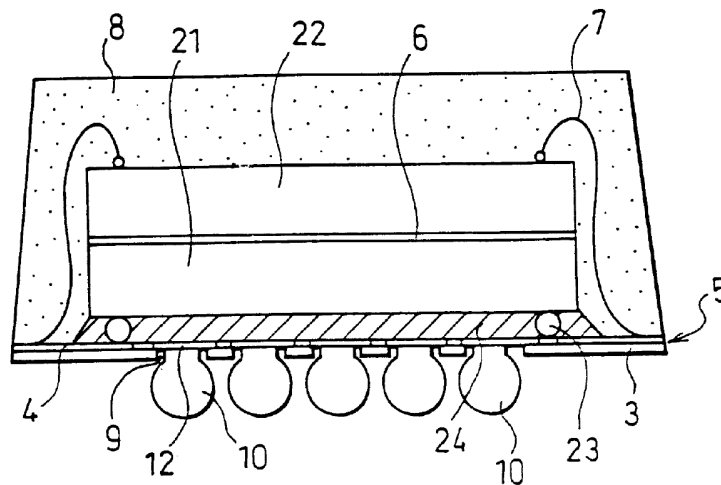


Figure 10 shows a cross-sectional view of a semiconductor device arranged in accordance with the second embodiment of the '879 patent. *Id.* at 6:7–9, 11:17–18.

As shown in Figure 10, circuit board 5 includes insulating substrate 3, and wiring layer 4 formed on the insulating substrate. *Id.* at 11:21–23. In the second embodiment, “a first semiconductor chip 21 is mounted on a circuit board 5 with its circuit formed surface facing the circuit board 5, i.e., facing down” (*id.* at 11:19–21) and “[a] second semiconductor chip 22 is mounted on the back surface of the first semiconductor chip 21 through a thermo-compression sheet 6” (*id.* at 11:23–25). In this arrangement, the back surface of second semiconductor chip 22 faces the back surface of first semiconductor chip 21. *Id.* at 11:25–27. “Namely, the back surfaces of the

first semiconductor chip 21 and the second semiconductor chip 22 are adhered to each other through the thermo-compression sheet 6.” *Id.* at 11:27–29.

The ’879 patent describes that “[w]hen the second semiconductor chip 22 is in a state of wafer, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips 22.” *Id.* at 12:32–36. According to the ’879 patent, “[l]ike the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet 6 to the back surface of the second semiconductor chip 22 in advance.” *Id.* at 12:39–44.

D. Illustrative Claims

Of the challenged claims, claims 1, 7, 10, and 15 are independent. Claims 1 and 7 are illustrative of the challenged claims and are reproduced below.

1. A method of manufacturing a semiconductor device comprising:
 - (a) forming a first adhesion layer on a back surface of a first wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;
 - (b) producing separate first semiconductor chips from said first wafer by dicing;
 - (c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer;
 - (d) forming a second adhesion layer on a back surface of a second wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;

- (e) producing separate second semiconductor chips from said second wafer by dicing; and
- (f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip.

Ex. 1001, 13:45–61.

7. A method of manufacturing a semiconductor device comprising:

- (a) forming an insulating layer and a metal bump on a wiring layer;
- (b) mounting a first semiconductor chip on said wiring layer with its circuit-formed surface facing said wiring layer;
- (c) forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer;
- (d) producing separate second semiconductor chips from the wafer by dicing;
- (e) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip;
- (f) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a wire; and
- (g) sealing said first and second semiconductor chips and said wire.

Id. at 14:64–15:16.

E. Prior Art and Declaration Evidence

Petitioner cites the following references in its challenge to patentability:

U.S. Patent No. 4,821,944, issued Apr. 18, 1989 (Ex. 1007, “Tsumura”);

U.S. Patent No. 5,323,060, issued June 21, 1994 (Ex. 1004, “Fogal”);

U.S. Patent No. 7,166,495 B2, filed Feb. 20, 1996 (Ex. 1005, “Ball”);

U.S. Patent No. 6,682,954 B1, filed Jan. 31, 1997 (Ex. 1009, “Ma”);

and

International Publication WO 1996/13066, published May 2, 1996 (Ex. 1003, “Mostafazadeh”).

Petitioner also relies on additional patents listed in the Table of Exhibits, including U.S. Patent No. 4,688,075 (Ex. 1030, “Phy”), U.S. Patent No. 5,411,921 (Ex. 1031, “Negoro”), U.S. Patent No. 5,762,744 (Ex. 1032, “Shibata”), U.S. Patent No. 5,110,388 (Ex. 1033, “Komiya”), and U.S. Patent No. 6,007,920 (Ex. 1034, “Umehara”). Pet. vi, 3.

Petitioner supports its challenge with a declaration from Jeffrey C. Suhling, Ph.D. (Ex. 1002, “Suhling Declaration”). Patent Owner has submitted a declaration from Peter Elenius (Ex. 2001, “Elenius Declaration”) in support of Patent Owner’s Preliminary Response.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 4–5).

Claim(s) Challenged	35 U.S.C. §	Reference(s)
7	103(a) ¹	Ball, Mostafazadeh

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the ’879 patent has an effective filing date prior to the effective date of the

Claim(s) Challenged	35 U.S.C. §	Reference(s)
8, 9	103(a)	Ball, Mostafazadeh, Tsumura
1, 2, 10, 11, 15	103(a)	Ball, Fogal, Mostafazadeh
3, 4, 12	103(a)	Ball, Fogal, Mostafazadeh, Tsumura
5, 6, 13, 14	103(a)	Ball, Fogal, Mostafazadeh, Ma

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the relevant time is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical “person of ordinary skill in the art,” from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct “presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan.” *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Citing testimony from Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art at the priority date of the ’879 patent would have had

applicable AIA amendment, we refer to the pre-AIA version of § 103.

i) a bachelor-level degree in electrical engineering, mechanical engineering, material science, or a related subject and five or more years of experience working in the field of semiconductor packaging; ii) a Master's-level degree in mechanical engineering, electrical engineering, material science, or a related field, and at least 1-3 years of experience in the design/development of semiconductor packages; or iii) a Ph.D.-level degree in mechanical engineering, material science, electrical engineering, or a related field, and at least some experience in the area of semiconductor packaging.

Pet. 17 (citing Ex. 1002 ¶¶ 28–32). Petitioner further states that “[a]dditional education may substitute for professional experience, and significant work experience may substitute for formal education.” *Id.*

Patent Owner's declarant, Mr. Elenius, states that a person of ordinary skill in the art would have had “a bachelor's degree in electrical, mechanical or materials engineering and two to three years of experience in the design or development of semiconductor manufacturing, or the equivalent.”

Ex. 2001 ¶ 32. Mr. Elenius further states that “[a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.” *Id.*

Although the proposals for the level of skill in the art by the parties' declarants have differences in wording, we do not find the proposals to be materially different. For purposes of this Decision, we find no meaningful differences between the parties' respective definitions that would materially alter the outcome of this Decision. Thus, although we do not find the parties' proposals for the level of skill in the art to be materially different, for purposes of this Decision, based on our review of the '879 patent, the types of problems and solutions described in the '879 patent, and cited prior

art, we adopt and apply Petitioner’s definition of the level of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, we construe a patent claim “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2022). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the effective filing date of the patent application and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that a person of ordinary skill in the art reading the ’879 patent would understand the term “electrode section” recited in the challenged claims to mean “electrical terminals, usually called bond pads, that are part of the substrate’s wiring layer.” Pet. 16 (citing Ex. 1002 ¶¶ 103–107). At this time, Patent Owner does not dispute Petitioner’s proposed construction of “electrode section.” *See generally* Prelim. Resp. For purposes of this Decision, we need not construe the term “electrode section” because the parties do not identify any material issue that would turn on the construction. *See VividTechs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that only terms that are in controversy need to be construed, and “only to the extent necessary to

resolve the controversy”); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

Patent Owner contends that the term “adhesion layer” recited in the challenged independent claims should be construed to mean “a pre-formed layer that is adhered.” Prelim. Resp. 12–14. All the challenged independent claims recite “forming” an “adhesion layer.” Ex. 1001, 13:45–56, 14:64–15:6, 15:45–47, 16:48–59. Although it is not entirely clear what Patent Owner means by “forming a pre-formed layer,” Patent Owner argues that applying an adhesive on a wafer to form an adhesive coating, as disclosed in Mostafazadeh, does not meet the “adhesion layer” limitation under Patent Owner’s proposed construction of the term. *See, e.g.*, Prelim. Resp. 19–21. Although Patent Owner’s argument raises an issue of claim construction, the issue is closely related to the issue of whether Mostafazadeh teaches “forming” an “adhesion layer” recited in the challenged independent claims. Thus, we address this issue in the context of the patentability discussion in Section III.C.4.b below.

Apart from this term, no other claim terms need to be construed expressly for purposes of this Decision. *See Vivid Techs.*, 200 F.3d at 803.

C. Asserted Obviousness Over Ball and Mostafazadeh

Petitioner asserts that claim 7 is unpatentable under § 103 over Ball and Mostafazadeh. Pet. 5, 25–42. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 17–29. Based on the record presented and for the reasons discussed below, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.² *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)); see *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that “some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]”).

“Whether prior art invalidates a patent claim as obvious is determined from the perspective of one of ordinary skill in the art.” *Star Scientific, Inc.*

² The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

v. R.J. Reynolds Tobacco Co., 655 F.3d 1364, 1374 (Fed. Cir. 2011). Further, “the assessment of a claim’s patentability is inextricably tied to a skilled artisan’s knowledge and skill level.” *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Permissible uses of general knowledge of one having ordinary skill under § 103 include providing a motivation to combine and supplying a claim limitation, if supported by evidence of record. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1363 (Fed. Cir. 2013); *see also Qualcomm*, 24 F.4th at 1376 (permissible uses of what a skilled artisan would have known at the time of the invention include “furnishing a motivation to combine” and “supplying a missing claim limitation” (citing *Randall Mfg.*, 733 F.3d at 1363; *Koninklijke Philips*, 948 F.3d at 1337–38)).

We analyze the asserted ground based on obviousness with the principles identified above in mind.

2. Overview of *Ball* (Ex. 1005)

Ball describes a multi-chip semiconductor device in which semiconductor chips (called dies) are vertically stacked on top of one another using a combination of face-down (flip-chip) or face-up (wire bond) assembly arrangements. Ex. 1005, Abstract, 1:8–12, 2:16–20. According to Ball, “flip-chip attachment” refers to a method of attaching a semiconductor chip (die) to a substrate in which “the die is inverted so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate (such as a printed circuit board).” *Id.* at 1:28–32.

Figure 1 of Ball is reproduced below.

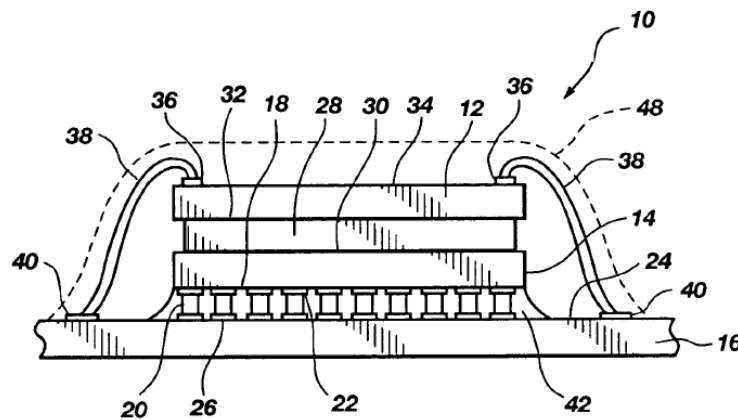


Fig. 1

Figure 1 shows a side plan view of an exemplary multi-die assembly of Ball with a flip-chip vertical stacking arrangement. *Id.* at 4:58–59, 5:1–18.

Ball describes that assembly 10 of Figure 1 comprises upper die 12, opposing lower die 14, and substrate 16. *Id.* at 5:2–3. Ball further describes that

Fabrication of the assembly 10 comprises providing the lower die 14 having a face surface 18 with at least one flip chip electric connection 20 (such as a C4 solder bump connection, conductive polymer bump or pin connection, these and other alternatives being known in the art, by way of example) extending from a bond pad or other terminal 22 on the lower die face surface 18. The flip chip electric connections 20 extend to a surface 24 of the substrate 16 in such a manner that the flip chip electric connections 20 physically (mechanically) attach to, and make electrical contact with, lead ends, trace ends, terminals or other electrical contact elements 26 in or on the surface 24 of the substrate 16.

and that “back side 32 of the upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over a lower die back side 30.” *Id.* at 5:6–20.

“An adhesive requiring a curing step, such as an epoxy, is preferred, although many adhesives known in the art are suitable.” *Id.* at 5:20–22.

3. *Overview of Mostafazadeh (Ex. 1003)*

Mostafazadeh describes a method of forming an adhesive coating on a semiconductor wafer surface. Ex. 1003, Abstract. The adhesive coating is dried, and the semiconductor wafer is diced to form several integrated circuit dies, each having an integrated circuit and an adhesive layer. *Id.*

According to Mostafazadeh, “[g]luing and taping are conventional techniques” to attach an individual die (a fabricated integrated circuit chip) to a structure (e.g., a connection substrate) during packaging of the individual chips. *Id.* at 1:22–25. Mostafazadeh states that a disadvantage of the conventional processes applying glue on an individual die during packaging is that the glue “tends to interfere with connections to the attached die by *jutting up around the die’s edges.*” *Id.* at 2:18–20 (emphasis added). Mostafazadeh purports to avoid this shortcoming in the conventional glue technique by applying, before a semiconductor wafer is diced to form individual dies, an adhesive coating to the entire surface of the semiconductor wafer “as opposed to an individual support surface or an individual die[,] as is common in the conventional processes.” *Id.* at 8:2–5.

Mostafazadeh also discloses that “[w]hen taping is contemplated[,] the tape is typically applied . . . to the back surface of a semiconductor wafer prior to dicing.” *Id.* at 2:22–23. Mostafazadeh states, however, that “tape has the drawback of being relatively expensive.” *Id.* at 2:24–25.

Mostafazadeh states that “[i]n view of the forgoing, an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly and *does not jut around the edges of the die* would be advantageous.” *Id.* at 2:27–29 (emphasis added).

Figure 2 of Mostafazadeh is reproduced below.

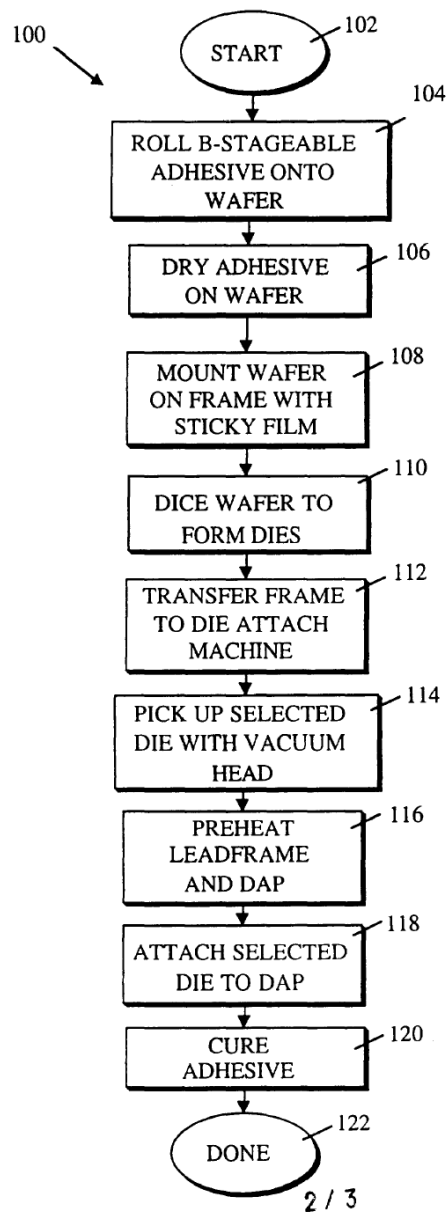


Figure 2 is a flowchart illustrating Mostafazadeh's exemplary method of attaching an integrated circuit³ die to a support surface. *Id.* at 4:15–16.

The process of Mostafazadeh's Figure 2 begins with step 102 in which a multiplicity of integrated circuits are fabricated on a semiconductor

³ Mostafazadeh refers to an integrated circuit as "IC." Ex. 1003, 9:20.

wafer. *Id.* at 5:22–23. Mostafazadeh describes that after fabrication of the ICs on the semiconductor wafer, an adhesive is then rolled onto a mounting surface (i.e., the surface opposite to the IC formed surface) of the wafer “to form an adhesive coating thereon in a rolling step 104.” *Id.* at 5:23–25. According to Mostafazadeh, the disclosed process “insures that an adhesive coating . . . is formed over the entire wafer surface.” *Id.* at 6:29–7:1. Mostafazadeh further describes that “in some embodiments, the adhesive may be a B-stageable epoxy.” *Id.* at 3:22–23.

Mostafazadeh describes that “[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid.” *Id.* at 6:3–4. But “once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106,” which “turns the adhesive coating into a *hard surface*” if “the adhesive is good B-stageable epoxy.” *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as “hardened”).

The wafer is then cut or diced into a multiplicity of dies or IC chips in dicing step 110. *Id.* at 7:29–8:1. After the dicing step, each die has an integrated circuit and an adhesive layer that includes the dried adhesive coating. *Id.* at 8:1–2. The result of dicing the semiconductor wafer in step 110 to form several integrated circuit dies 174 is shown in Figure 5c. *Id.* at 8:5–6.

Figure 5c of Mostafazadeh is reproduced below.

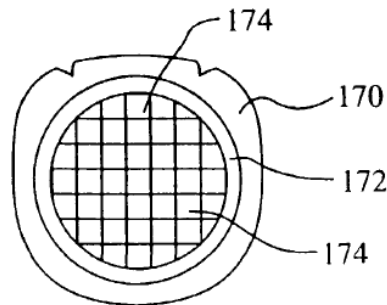


Fig. 5c

Figure 5c is a top view illustrating the result of dicing step 110 of Figure 2 forming a multiplicity of integrated circuit dies. *Id.* at 5:7–8.

According to Mostafazadeh, as a result of applying adhesive to a wafer, drying the coating to form a hardened layer, and dicing the wafer to the chip size, the adhesive layer on each individual chip is “*exactly the same size as the mounting surface of the die.*” *Id.* at 9:15–16 (emphasis added). Thus, “when the die is attached to its supporting surface” during packaging of individual chips, “the adhesive *does not extend beyond* a mounting surface of *the die.*” *Id.* at 9:16–18 (emphases added).

Figure 6a of Mostafazadeh is reproduced below.

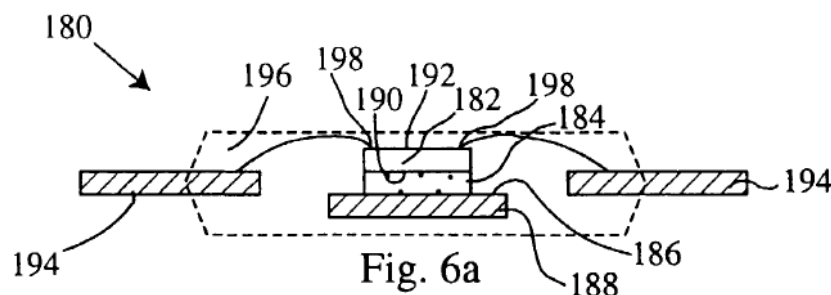


Fig. 6a

Figure 6a is a diagrammatic cross sectional side view of an exemplary packaged integrated circuit with a die attached to a support surface by an adhesive layer. *Id.* at 5:10–12.

As shown in Figure 6a, in packaged integrated circuit 180, die 182 is attached to its support surface 188 via adhesive layer 184. *Id.* at 10:4–5. “The *adhesive layer 184* covers an entire mounting surface 190 of the selected integrated circuit die 182 and *does not extend beyond a boundary* of the mounting *surface 190*.” *Id.* at 10:6–8 (emphases added). Mostafazadeh further describes that “more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs).” *Id.* at 11:16–18.

4. Independent Claim 7 as Obvious over Ball and Mostafazadeh

Petitioner contends that the combination of Ball and Mostafazadeh teaches or suggests all elements of claim 7 and that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball and Mostafazadeh to arrive at the subject matter recited in claim 7. Pet. 25–42. At this stage of the proceeding, Patent Owner contests Petitioner’s showings only on limitation (c) of claim 7 and the reasons to combine the references. Prelim. Resp. 16.

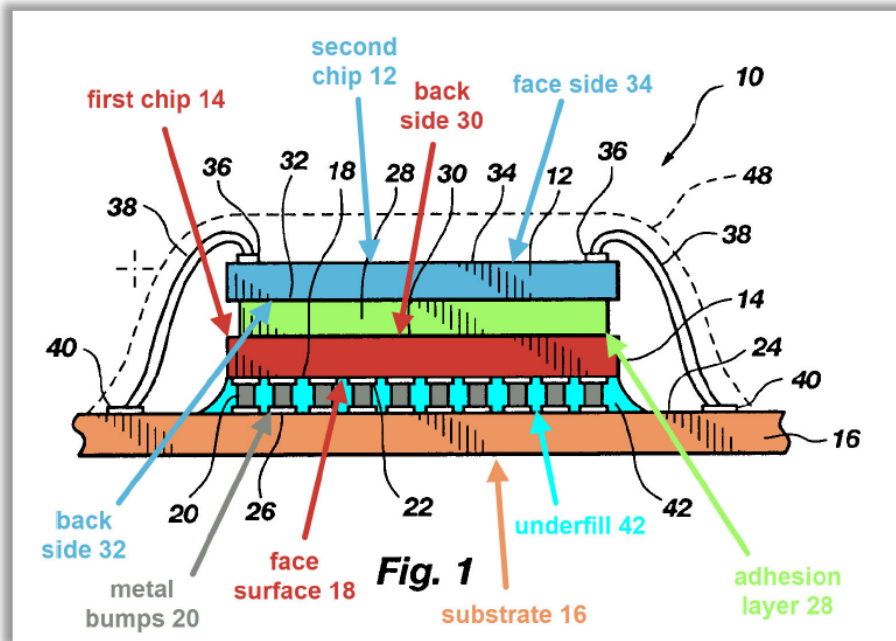
a. Petitioner’s Assertions

In its proposed combination of Ball and Mostafazadeh, Petitioner relies on Ball as teaching all of the elements of claim 7, except for limitations (c) and (d) reciting the steps of forming an adhesion layer on a wafer and producing semiconductor chips from the wafer by dicing, for which Petitioner further relies on Mostafazadeh and the knowledge of one of ordinary skill in the art. Pet. 25–42.

Specifically, Petitioner asserts that the embodiment depicted in Figure 1 of Ball teaches or suggests all elements of claim 7 relating to the

assembly of a “flip-chip” stacked package arrangement of semiconductor chips in a semiconductor device. Pet. 26, 28–34, 37–42.

Figure 1 of Ball as annotated by Petitioner is reproduced below.



Pet. 18. Annotated Figure 1 of Ball, reproduced above, illustrates Petitioner’s alleged identification in Ball of the structural arrangement of a semiconductor device recited in claim 7. *Id.* at 18–19, 26, 28–34, 37–42.

According to Petitioner, Ball’s Figure 1 discloses stacked die multichip module 10 (the recited “semiconductor device”) comprising upper die 12 (the claimed “second semiconductor chip”) and opposing lower die 14 (the claimed “first semiconductor chip”). Pet. 18, 26 (citing Ex. 1005, 4:58–59, 5:3–6, 5:18–20, Fig. 1).

Petitioner further asserts that “lead end or trace end patterns 26 aligned with the bump connections 20 on the front surface 18 of lower die 14” assembled on top surface 24 of substrate 16 depicted in Figure 1 teaches the recited “wiring layer.” *Id.* at 28–29 (citing Ex. 1005, 3:51–53,

5:12–1, Fig. 1). Additionally, Petitioner contends that “Ball’s electrical connections 20—located between the lower die’s bond pad 22 and the electrical components 26 of the wiring layer on the substrate 16—are the claimed ‘*metal bumps*.’” *Id.* at 30 (citing Ex. 1005, 5:12–52, Fig. 1).

Petitioner further asserts that Ball’s “underfill 42 between the lower die 14 (first semiconductor chip) and the electrical components 26 (wiring layer) on substrate 16” teaches or suggests the claimed “insulating layer.” *Id.* at 31 (citing Ex. 1005, 5:28–33; Ex. 1002 ¶ 136). Petitioner argues that Ball, therefore, teaches or suggests “(a) forming an insulating layer and a metal bump on a wiring layer,” as recited in claim 7. *Id.* at 28–31 (citing Ex. 1002 ¶¶ 130–136).

Petitioner asserts that “Ball also teaches attaching a chip to a substrate using a flip-chip interconnection.” Pet. 29. According to Petitioner, Ball defines “[f]lip chip attachment” as “a method of attaching a semiconductor die to a substrate in which the die is inverted so that the connecting conductor pad on the face of the device is set on mirror-image pads on the substrate . . . and bonded by solder reflux or a conductive polymer curing.” *Id.* (citing Ex. 1005, 1:28–33, 1:25–27, 3:42–53, 5:6–12).

Petitioner contends that the flip-chip arrangement described in Ball teaches “(b) mounting a first semiconductor chip on said wiring layer with its circuit-formed surface facing said wiring layer,” as recited in claim 7, because Figure 1 of Ball discloses lower die 14 (the claimed “first semiconductor chip”) that has “a circuit formed on its face (front) side 18,” which is “facing and mounted to the wiring layer on substrate 16 by electrical connections 20 (*metal bumps*).” Pet. 31–34 (citing Ex. 1005, 1:25–27, 5:1–52, Fig. 1; Ex. 1002 ¶¶ 137–144). Petitioner further contends

that Ball also teaches “(e) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip” because Figure 1 of Ball discloses mounting backside 32 of upper die 12 (the claimed “second semiconductor chip”) to backside 30 of lower die 14 (the claimed “first semiconductor chip”) in a back-to-back arrangement. *Id.* at 37–38 (citing Ex. 1005, 5:18–26; Ex. 1002 ¶¶ 152–153).

Petitioner further asserts that Ball teaches “(f) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a wire,” as recited in claim 7, because Figure 1 of Ball discloses upper die 12 (the claimed “second semiconductor chip”) is wire bonded to the wiring layer on substrate 16 with bond wire 38 via bond pads 36 and electrical terminal 40 (the claimed “electrode section”). Pet. 38–40 (citing Ex. 1005, 5:23–27, Fig. 1; Ex. 1002 ¶¶ 154–163).

Petitioner next contends that Ball teaches “(g) sealing said first and second semiconductor chips and said wire” because Figure 1 of Ball discloses that the dies and wires are encapsulated or sealed by dashed line 48. Pet. 40–41 (citing Ex. 1005, 4:5–10). According to Petitioner, the terms “sealing” and “encapsulating” are used interchangeably in the semiconductor industry and “sealing” or “encapsulating” chips and wires within a semiconductor package was within the state of the art and within the knowledge of an ordinarily skilled artisan. *Id.* at 42 (citing Ex. 1002 ¶¶ 164–165).

Finally, addressing the limitation reciting “(c) forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer,” Petitioner asserts that

although Ball discloses that “a backside 32 of upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over the lower die back side,” Ball does not describe how the layer of adhesive is formed on upper die 12. Pet. 34 (citing Ex. 1005, 5:3–26). For this teaching missing from Ball, Petitioner relies on Mostafazadeh and the knowledge of a person of ordinary skill in the art at the time of the invention of the ’879 patent. *Id.* at 34–37.

First, Petitioner asserts that “[i]n 1998, the idea of forming an adhesive thin film on the backside of a wafer was decades old.” Pet. 34. Citing the testimony of Dr. Suhling, Petitioner further contends that “as early as 1983, industry leaders like Fairchild Semiconductor and National Semiconductor applied *thin films* to the backsides of wafers at least to support the wafer during the dicing process and to create chips with adhesive backsides for mounting to substrates.” *Id.* at 27 (emphasis added) (citing Ex. 1002 ¶¶ 62–69 (discussing Phy, Negoro, Shibata, Komiyama, and Umehara)); *see also id.* at 34–35. Petitioner asserts that “[n]umerous patents—some filed more than fifteen years before the ’879 patent’s priority date and describing the exact same process—prove the idea existed in the state of the art, was well-within the knowledge of a skilled artisan, and was nothing more than a common-sense fabrication step.” *Id.* at 27 (citing Ex. 1002 ¶¶ 62–69).

Petitioner contends that “Mostafazadeh—a National Semiconductor patent—is just one example of the many patents that teaches this process” and that Mostafazadeh further teaches “using its adhesive application process ‘to form multichip packages (MCPs) or multichip modules (MCMs).’” Pet. 35 (citing Ex. 1003, 11:16–18). Referencing Figure 2 of

Mostafazadeh (reproduced above in Section III.C.3), Petitioner asserts that Mostafazadeh discloses a process in which a multiplicity of integrated circuits are fabricated on a semiconductor wafer and “an adhesive is then rolled onto a mounting surface of the wafer to form an adhesive coating.” *Id.* at 35–36 (citing Ex. 1003, 5:20–23, 6:8–24, Fig. 2). Petitioner further asserts that in Mostafazadeh’s process, the adhesive coating is then dried and the wafer is cut into a multiplicity of dies, producing individual pieces of dies having an integrated circuit and an adhesive layer. *Id.* at 36 (citing Ex. 1003, 7:28–8:6, Fig. 5c). Citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have understood that the combination of Mostafazadeh and Ball teaches how to apply adhesive to the backside of a wafer to produce individual chips, like those used in Ball, having circuitry on one side and a pre-applied adhesive on the other. *Id.* at 36 (citing Ex. 1002 ¶¶ 145–150).

Similarly, Petitioner asserts that Mostafazadeh teaches “(d) producing separate second semiconductor chips from the wafer by dicing,” as recited in claim 7, because Mostafazadeh discloses applying an adhesive on the semiconductor wafer and then dicing the wafer to form a “***multiplicity of dies***” having “***an integrated circuit and an adhesive layer.***” Pet. 37 (citing Ex. 1003, Abstract, 1:14–15, 3:7–8, 3:22–23, 4:12–13, 5:22–7:16, 7:28–8:5, Fig. 5c). Citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have understood that, as Mostafazadeh expressly recognizes, dicing a wafer results in “*separate second semiconductor chips.*” *Id.* (citing Ex. 1002 ¶ 151).

Addressing the reasons to combine Ball and Mostafazadeh, Petitioner asserts that both references are in the same field of methods for

manufacturing semiconductor devices and that both references specifically teach vertically stacking semiconductor chips on top of one another to create multichip modules. Pet. 25. Petitioner further argues that a person of ordinary skill in the art would have combined Ball with Mostafazadeh because Ball teaches methods for stacking chips with adhesive backsides and Mostafazadeh teaches a method that produces individual chips with adhesive backsides that would simplify the stacking process in Ball. *Id.* at 26–27 (citing Ex. 1002 ¶¶ 121–128).

Specifically, Petitioner argues that individual chips with adhesive backsides created by Mostafazadeh’s process would have been beneficial in the stacking process in Ball because the adhesive layer on the individual chips or dies does not “jut around the edges of the die.” Pet. 26 (citing Ex. 1003, 2:26–28); *see also id.* at 21–22 (explaining that Mostafazadeh discloses “an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly ***and does not jut around the edges of the die***” and “[t]he adhesive layer material substantially does not extend beyond the mounting area boundary” (underlined emphasis added) (citing Ex. 1003, 2:27–29, 3:29–4:1)); Ex. 1002 ¶ 126.

As discussed above, citing the testimony of Dr. Suhling, Petitioner asserts that the process of applying thin films to the backsides of wafers to create chips with adhesive backsides “was well-within the knowledge of a skilled artisan, and was nothing more than a common-sense fabrication step.” Pet. 27 (citing Ex. 1002 ¶¶ 62–69). Thus, Petitioner argues that a person of ordinary skill in the art would have known that “applying the adhesive to the backside of a wafer and dicing to produce hundreds of

individual chips was a common-sense approach and one that would simplify the chip-stacking process.” *Id.*; Ex. 1002 ¶ 127.

Lastly, Petitioner argues that Mostafazadeh explicitly recommends using its adhesive process to efficiently build multichip modules. Pet. 27 (citing Ex. 1003, 11:16–18 (“In addition, more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs).”). Petitioner asserts, therefore, a person of ordinary skill in the art would have been motivated to combine the teachings of Mostafazadeh and Ball, with a reasonable expectation of success, to utilize Mostafazadeh’s process resulting in hundreds of individual chips with adhesive backsides for use in building the vertical chip stacks and multichip modules described in Ball. *Id.* at 27–28 (citing Ex. 1002 ¶¶ 121–128).

b. Patent Owner’s Arguments and Our Analysis

At this stage of the proceeding, Patent Owner contests Petitioner’s showings only on limitation (c) of claim 7 and the reasons to combine the references. Prelim. Resp. 16. We address each of Patent Owner’s arguments in turn.

First, Patent Owner asserts that the claim term “adhesion layer” recited in claim 7 should be construed to mean “a pre-formed layer that is adhered” and, under that claim construction, Mostafazadeh does not meet limitation (c). Prelim. Resp. 12–14, 16, 19–21. Petitioner disagrees and argues that the term “adhesion layer” should be accorded its plain and ordinary meaning. Reply 2–3. Petitioner argues that, to the extent express construction of this term is necessary, the plain and ordinary meaning of

“adhesion layer” is “a layer that adheres” in view of the ’879 patent’s intrinsic record. *Id.* at 3.

Addressing the claim construction issue, we note that the claim term “adhesion layer” is recited only in the challenged independent claims and in no other claims of the ’879 patent. *See* Ex. 1001, 13:45–16:65. And each of the independent claims recites “forming” an “adhesion layer” “on a back surface” of a “wafer.” *Id.* at 13:47–49, 13:54–56, 15:4–6, 15:45–47, 16:48–50, 16:56–58. In view of this claim language, we construe the relevant claim language “forming an adhesion layer on a back surface of a wafer” as a whole, not just a single term “adhesion layer” in isolation from the rest of the claim language. *See Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1311 (Fed. Cir. 2003) (“[T]he claim limitation, as a whole, [] must be considered in claim construction.”); *United States v. Telectronics, Inc.*, 857 F.2d 778, 781 (Fed. Cir. 1988) (holding that district court’s interpretation of the term “avoid” without regard to the rest of the limitation was error); *see also Lexion Med., LLC v. Northgate Techs., Inc.*, 641 F.3d 1352, 1356 (Fed. Cir. 2011) (“[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms.”); *IGT v. Bally Gaming Int’l, Inc.*, 659 F.3d 1109, 1117 (Fed. Cir. 2011) (“We caution that claim language must be construed in the context of the claim in which it appears. *Extracting a single word from a claim divorced from the surrounding limitations can lead construction astray.*” (emphasis added)); *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999) (“Proper claim construction . . . demands interpretation of the entire claim in context, not a single element in isolation.”).

Considering the claim language, the Oxford English Dictionary defines “form” as “[t]o construct, frame; to make, bring into existence, produce.”⁴ Thus, the plain meaning of the claim term to “form[] an adhesion layer on a back surface of a wafer” is “to construct or make an adhesion layer on a back surface of a wafer.” At this time, we do not perceive anything in the claim language that requires any specific method to construct an adhesion layer on a wafer surface. Thus, at least based on the claim language, we are not persuaded at this time that the challenged claims require adhering a pre-formed adhesion layer to a surface of a wafer, as Patent Owner contends.

Citing the Specification of the ’879 patent, Patent Owner contends that the recited “adhesion layer” is “a pre-formed layer that is adhered” to the back surface of a wafer because the ’879 patent describes that the “[second semiconductor’s] back surface is *adhered to* the thermo-compression sheet 6.” Prelim. Resp. 12 (citing Ex. 1001, 6:48–52). The language cited by Patent Owner comes from the ’879 patent’s description of Figure 1, which shows “a semiconductor device in accordance with *the first embodiment*” of the ’879 patent. Ex. 1001, 5:34–36 (emphasis added), 6:37–52. A particular embodiment appearing in the written description is generally not incorporated into a claim if the claim language is broader than the embodiment. *SuperGuide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (citation omitted). Further, “it is improper to read limitations from a preferred embodiment described in the specification—

⁴ Oxford English Dictionary Online (March 2023), <https://www.oed.com/view/Entry/73422?rskey=aCEUF4&result=2&isAdvanced=false> (accessed April 20, 2023) (Ex. 3002, 4).

even if it is the only embodiment—into the claims *absent a clear indication* in the intrinsic record that the patentee intended the claims to be so limited.” *Epos Techs. Ltd. v. Pegasus Techs. Ltd.*, 766 F.3d 1338, 1341 (Fed. Cir. 2014) (emphasis added).

Similarly, although the Specification’s description of the second embodiment also states that “[w]hen the second semiconductor chip 22 is in a state of wafer, the insulating *thermo-compression sheet 6 is adhered to the back surface of the wafer*” (Ex. 1001, 12:32–34) (emphasis added), this does not limit the challenged claims to the feature described in the Specification but not recited in the claims—“a pre-formed adhesion layer” that “is adhered to” a wafer surface. *See Cadence Pharm. Inc. v. Exela PharmSci Inc.*, 780 F.3d 1364, 1369 (Fed. Cir. 2015) (even if “all of the embodiments discussed in the patent” included a specific limitation, it would not be “proper to import from the patent’s written description limitations that are not found in the claims themselves”); *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (“the specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal”) (citation omitted).

In what appears to be an argument for implied disclaimer or implicit definition in the Specification, Patent Owner asserts that the ’879 patent distinguishes a pre-formed adhesion layer, such as a solid adhesive sheet, from “a liquid or semi-liquid viscous adhesive agents that are coated or deposited on, which may result in overflowing or spreading out from the back surface of a semiconductor chip.” Prelim. Resp. 13 (citing Ex. 1001, 2:23–58, Fig. 14(b)). According to Patent Owner, in the conventional technique, “the patentee recognized an adhesive or paste that can flow

during mounting of the chip caused ‘overflow’ and ‘gap’ problems due to excessive or insufficient adhesive, respectively.” Sur-reply 2 (emphasis added) (citing Ex. 1001, 2:12–20, 2:39–43). Patent Owner contends that “the patentee’s solution is [to] . . . [u]se a pre-formed solid sheet **and** attach that sheet to the back surface of the wafer first before cutting and placing the chip.” *Id.* at 3. Patent Owner argues, therefore, applying an adhesive on a wafer to form an adhesive coating, as disclosed in Mostafazadeh, is distinguished from the claimed “adhesion layer” in the ’879 patent. Prelim. Resp. 13–14, 19–21.

At this stage of the proceeding, based on the record presented, we find Patent Owner’s arguments and evidence unpersuasive. As Patent Owner acknowledges, the ’879 patent expressly discloses an embodiment where a first semiconductor chip is mounted in a package using a paste or epoxy adhesive. *See* Ex. 1001, 9:21–28; Prelim. Resp. 14 (quoting Ex. 1001, 9:25–30). The portion of the Specification cited by Patent Owner describes

*The first semiconductor chip 1 is mounted on the circuit board 5 at a location inside a mount location recognition-use mark 15 provided on the circuit board 5. Here, instead of providing the thermocompression sheet 6 in advance when the first semiconductor chip 1 is in the wafer state, an insulating **paste** made of **epoxy** resins, etc. may be applied onto the circuit board 5 before the first semiconductor chip 1 is mounted on the circuit board 5.*

Ex. 1001, 9:21–28 (emphases added).

As set forth above, the portion of the Specification cited by Patent Owner describes two alternative embodiments of mounting the first semiconductor chip on the circuit board—adhering a thermo-compression sheet during wafer processing to create a first semiconductor chip with a

layer of thermo-compression sheet, or, in the alternative, applying a paste of epoxy to the circuit board to mount the first semiconductor chip on the circuit board. *Id.* As discussed above, the plain meaning of the claim term “forming an adhesion layer” is “to construct or make an adhesion layer.” *See* Ex. 3002, 4. Thus, the plain meaning of “forming an adhesion layer” covers both alternative embodiments discussed above—adhering a thermo-compression sheet or applying a paste of epoxy—because both alternative approaches “construct or make an adhesion layer.” Therefore, based on the claim language and the disclosures in the Specification, the intrinsic record does not support excluding all uses of paste or epoxy from the term “forming an adhesion layer.”

Patent Owner further asserts that using individual semiconductor chips manufactured by Mostafazadeh’s process to assemble a multichip stacked package will “cause adhesive to squeeze out and possibly obstruct the bond pad, resulting in the very failure that the ’879 patent sought to avoid.” Prelim. Resp. 24. According to Patent Owner, “Mostafazadeh did not recognize, foresee, or try to solve the problem of adhesive overflow to cover the bond pads.” *Id.* at 25.

As discussed above, however, Petitioner argues that a person of ordinary skill in the art would have known that using individual chips with adhesive backsides created by Mostafazadeh’s process would have been beneficial because the adhesive layer on the chips “does not ‘*jut around the edges of the die.*’”⁵ Pet. 27 (emphasis added) (citing Ex. 1003, 2:26–28).

⁵ The verb “jut” means “to (cause to) stick out, especially above or past the edge or surface of something.” Cambridge English Dictionary, <https://dictionary.cambridge.org/us/dictionary/english/jut>. Ex. 3003, 1.

As set forth below, Petitioner further argues persuasively that this feature of Mostafazadeh is similar to the purported improvement over conventional techniques described in the '879 patent—to avoid overflowing of adhesive beyond the edges of the chips.

Moreover, like the '879 patent, Mostafazadeh describes its inventive process as “an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly ***and does not jut around the edges of the die***[.]” (*Compare* Mostafazadeh at 2:27-29 (describing “an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly”) *with* the '879 patent at 4:8-10 (describing the need to avoid “a situation where the excessively applied adhesive agent overflows the space between the first and second semiconductor chips.”); *see also* (Mostafazadeh at 2:27-29, 3:29-4:1 (“The adhesive layer material substantially does not extend beyond the mounting area boundary.”), 9:15-18, 10:6-8.)

Id. at 21–22 (underlined emphases added).

As discussed above in Section III.C.3, in Mostafazadeh’s process, although “[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid” (Ex. 1003, 6:3–4), “once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106,” which “turns the adhesive coating into a *hard surface*” if “the adhesive is good B-stageable epoxy.” *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as “hardened”). Thus, according to Mostafazadeh, “when the die is attached to its supporting surface” during packaging of individual chips, “the adhesive *does not extend beyond a mounting surface of the die.*” *Id.* at 9:16–18 (emphases added). In other words, Mostafazadeh expressly discloses that its process results in creating

individual semiconductor chips with a solidified adhesive layer that does *not* extend or overflow beyond the edges of the chips during packaging.

In addition, contrary to Patent Owner's assertion that "Mostafazadeh did not recognize, foresee, or try to solve the problem of adhesive overflow to cover the bond pads" (Prelim. Resp. 25), Mostafazadeh states that a disadvantage of the conventional processes applying glue on an individual die during packaging is that the glue "tends to interfere with connections to the attached die by *jutting up around the die's edges*." Ex. 1003, 2:18–20 (emphasis added). Mostafazadeh further states that "[i]n view of the forgoing, an improved cost effective method for applying integrated circuit dies to support surfaces such that the adhesive is spread evenly and *does not jut around the edges of the die* would be advantageous." *Id.* at 2:27–29 (emphasis added).

Patent Owner further asserts that in Mostafazadeh "the die attach pad that the chip is to be mounted to," i.e., the substrate or supporting structure of a semiconductor package, is pre-heated just before the die is attached, which "*could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads." Prelim. Resp. 25 (emphasis added) (citing Ex. 1003, 9:10–13; Ex. 2001 ¶ 94). In the cited paragraph of his Declaration, Mr. Elenius states that

Mostafazadeh teaches a method of mounting that requires pre-heating and flash heating immediately prior to and during mounting, *possibly* causing overflow and covering of the bond pads. Mostafazadeh explains, the die attach pad that the chip is to be mounted to should be pre-heated or flash heated just before the epoxy-covered die is attached. In one embodiment that uses a B-stage adhesive, this heating will cause "the B-stageable adhesive dried in step 106 [to] reflow to form a stronger bond between the integrated circuit die and a die attach pad during the

attachment step 118.” This reflowing *could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads.

Ex. 2001 ¶ 94 (emphases added) (citing Ex. 1003, 9:10–13). In the very next paragraph following that cited by Patent Owner and Mr. Elenius, however, Mostafazadeh discloses that “when *the die is attached* to its supporting surface *the adhesive does not extend beyond a mounting surface of the die.*” Ex. 1003, 9:16–18 (emphases added). Neither Patent Owner nor Mr. Elenius addresses this express disclosure of Mostafazadeh that appears contrary to Patent Owner’s assertions, nor do they explain adequately why the solidified adhesive layer of Mostafazadeh nonetheless “*could* cause the adhesive used to overflow past the edge of the chip.” Thus, based on the current record, we find Patent Owner’s argument and Mr. Elenius’s testimony to be at best speculative and contrary to the express disclosure of Mostafazadeh.

Although disclaimer or redefinition of a term in the specification may be implied under certain circumstances, *see, e.g., SightSound Techs., LLC v. Apple Inc.*, 809 F.3d 1307, 1317 (Fed. Cir. 2015), the standards for finding lexicography and disavowal are exacting. *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014). To act as its own lexicographer, a patentee must “clearly set forth a definition of the disputed claim term,” and “clearly express an intent to define the term.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Similarly, a disclaimer or disavowal of claim scope must be “clear and unmistakable, requiring ‘words or expressions of manifest exclusion or restriction’ in the intrinsic record.” *Unwired Planet, LLC v. Apple Inc.*, 829

F.3d 1353, 1358 (Fed. Cir. 2016) (quoting *Teleflex, Inc. v. Ficos N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)).

At this stage of the proceeding, based on the current record, we determine that the '879 patent's disparagement of the conventional technique of applying adhesive paste on an individual chip *during packaging* is insufficient to rise to the level of such "clear and unmistakable" disclaimer. The Specification does not exclude from the term "forming an adhesion layer on a back surface of a wafer" Mostafazadeh's wafer fabrication process of applying epoxy and drying it to form a hardened or solidified adhesive layer on the back surface of a wafer *before* the individual chip are created. The parties are invited to brief further on this issue during trial.

Patent Owner further contends that, under the doctrine of claim differentiation, "adhesives that [are] coated on" a wafer must be distinguished from the recited "forming" an "adhesion layer" because limitation (a) of claim 10 recites "applying *an adhesive paste* on a wiring layer," whereas limitation (b) of claim 10 recites "forming an adhesion layer on a back surface of a wafer on which no circuit is formed." Prelim. Resp. 14 (citing Ex. 1001, 10:39–45). Patent Owner, however, does not cite any authority for the proposition that the doctrine of claim differentiation applies to differences in the claim language between *different elements of the same claim*. The concept of claim differentiation "normally means that limitations stated in dependent claims are not to be read into the independent claim from which they depend." *Nazomi Commc'ns, Inc. v. Arm Holdings, PLC*, 403 F.3d 1364, 1370 (Fed. Cir. 2005). Thus, based on the current record, we find Patent Owner's claim differentiation argument unpersuasive.

Patent Owner next argues that the Specification makes clear that a paste is different from the adhesion layer because in describing an embodiment relating to claim 10, the '879 patent states

instead of providing the thermocompression sheet 6 in advance when the first semiconductor chip 1 is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board 5 before the first semiconductor chip 1 is mounted on the circuit board 5.

Prelim. Resp. 14 (emphases added) (quoting Ex. 1001, 9:25–30).

Patent Owner's argument turns the doctrine of lexicography or specification disclaimer on its head. The paragraph of the Specification cited by Patent Owner describes

When the first semiconductor chip 1 is in a wafer state, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer. Then, the wafer is cut to produce separate pieces of first semiconductor chips 1. *The first semiconductor chip 1 is mounted on the circuit board 5 at a location inside a mount location recognition-use mark 15 provided on the circuit board 5. Here, instead of providing the thermocompression sheet 6 in advance when the first semiconductor chip 1 is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board 5 before the first semiconductor chip 1 is mounted on the circuit board 5.*

Ex. 1001, 9:17–28 (emphases added). As discussed above, the portion of the Specification cited by Patent Owner describes alternative embodiments of mounting the first semiconductor chip on the circuit board—adhering a thermo-compression sheet during wafer processing to create a first semiconductor chip with a layer of thermo-compression sheet, or, in the alternative, applying a paste of epoxy to the circuit board to mount the first semiconductor chip on the circuit board. Rather than operating as a

disclaimer to limit the scope of the claims, such disclosure of alternative embodiments proves the opposite—i.e., the claim term “forming an adhesion layer” covers both alternative embodiments of adhering a thermo-compression sheet or applying a paste of epoxy.

Based on the record presented and for the foregoing reasons, we determine that Petitioner has shown sufficiently that Mostafazadeh teaches or suggests limitation (c) of claim 7.

Although we determine, for purposes of this Decision, that Mostafazadeh’s solidified epoxy process teaches or suggests “forming an adhesion layer on a back surface of a wafer,” as recited in claim 7, we additionally discuss Mostafazadeh’s disclosure of applying tape to the back surface of a semiconductor wafer in order to provide guidance and notice to the parties of the issues that would benefit from further development during trial.

As Patent Owner acknowledges, Mostafazadeh expressly contemplates applying tape to the back surface of a semiconductor wafer prior to dicing. Ex. 1003, 2:22–23 (“When *taping is contemplated*[,] the tape is typically applied . . . to the back surface of a semiconductor wafer prior to dicing.”) (emphasis added); Prelim. Resp. 24 (citing Ex. 1003, 2:22–29). In other words, Mostafazadeh discloses that in its process discussed above, an adhesive tape may be applied on the back surface of a wafer to form an adhesive layer thereon instead of applying epoxy and drying it to form a solidified adhesive layer.

As discussed above, Petitioner contends that at the time of the invention, the process of applying *thin films* to the backsides of wafers to create chips with adhesive backsides “was well-within the knowledge of a

skilled artisan, and was nothing more than a common-sense fabrication step.” Pet. 27 (citing Ex. 1002 ¶¶ 62–69 (discussing Phy, Negoro, Shibata, Komiyama, and Umehara)); *see also id.* at 34–35. Petitioner also asserts that “Mostafazadeh . . . is just one *example* of the many patents that teaches this process.” *Id.* at 35 (emphasis added).

In the cited paragraphs of his Declaration, Dr. Suhling discusses in detail the disclosures in Phy, Negoro, Shibata, Komiyama, and Umehara regarding the well-known techniques of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet on a wafer’s backside to form an adhesive layer before the wafer is cut or diced to produce individual semiconductor chips. Ex. 1002 ¶¶ 63 (Phy discloses applying a double-sided adhesive tape to the backside of a wafer and dicing the wafer to produce semiconductor chips (citing Ex. 1030, 2:44–3:2, 3:57–61, 4:11–21, Fig. 2)), 64 (discussing similar disclosures in Negoro (citing Ex. 1031, 2:44–3:2, 3:57–61, 4:11–21, Fig. 2)), 65 (Shibata discloses applying a pre-formed adhesive film to the back of a wafer, which remains on the bottom of each chip when the wafer is diced (citing Ex. 1032, 1:38–55)), 66 (Komiyama discloses adhering a tape to a wafer backside and dicing and mounting the chip to a leadframe via the adhesive on its backside (citing Ex. 1033, 2:16–29)), 67–68 (Umehara describes the shortcomings of the conventional method in which “the adhesive outflows the IC chips” during packaging and discloses an improved method that solves this problem by bonding a thermo-compression sheet to a backside of a wafer and dicing the wafer to produce IC chips with an adhesive layer (citing Ex. 1034, 1:45–2:4, 7:3–27, 7:46–50)).

In view of Petitioner’s argument and the evidence presented, we interpret the Petition as relying on Mostafazadeh, Phy, Negoro, Shibata, Komiyama, and Umehara for their teachings of applying an adhesive tape, adhesive film, or thermo-compression bonding sheet on a wafer’s backside to form an adhesive layer, as part of the general knowledge of a skilled artisan in the asserted ground of obviousness over Ball and Mostafazadeh. *See Koninklijke Philips*, 948 F.3d at 1338 (finding that the Board properly determined that the challenged claims would have been obvious over SMIL 1.0 “in light of the general knowledge of a skilled artisan” when “the Board relied on expert evidence, which was corroborated by Hua, in concluding that pipelining was not only in the prior art, but also within the general knowledge of a skilled artisan”); *see also Lone Star Silicon Innovations LLC v. Iancu*, 809 F. App’x 773, 777 (Fed. Cir. 2020) (finding that the petitioner properly relied on additional references in an asserted ground of obviousness over Watatani and Tanaka when “the additional references were being relied on exclusively for their teachings about what was well-known in the art”) (nonprecedential). Under this interpretation, Mostafazadeh’s disclosure of applying an adhesive tape to a wafer’s back surface would have provided a motivation to combine Ball and Mostafazadeh with the teachings of Phy, Negoro, Shibata, Komiyama, and Umehara regarding the details of how to utilize adhesive tapes, films, or thermo-compression sheets in Mostafazadeh’s process.

We alternatively interpret Petitioner’s citation to Phy, Negoro, Shibata, Komiyama, and Umehara as providing evidence of what a person of ordinary skill in the art would have understood Mostafazadeh’s disclosure of using tape to teach. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1372–

73 (Fed. Cir. 2019). That is, a person of ordinary skill in the art reading Mostafazadeh would have known that Mostafazadeh's taping method may be implemented using the well-known techniques of applying an adhesive tape, adhesive film, or thermo-compression sheet to the back surface of a semiconductor wafer prior to dicing, as described in detail in Phy, Negoro, Shibata, Komiyama, and Umehara. Under these circumstances, Petitioner need not "demonstrate a sufficient motivation to combine the . . . references," i.e., a motivation to combine Mostafazadeh with Phy, Negoro, Shibata, Komiyama, and Umehara. *See Realtime Data*, 912 F.3d at 1373.

Perhaps anticipating this line of analysis, Patent Owner argues that Mostafazadeh teaches away from using an adhesive tape in the proposed combination because Mostafazadeh states that tape has the drawback of being expensive. Prelim. Resp. 24 (citing Ex. 1003, 2:22–25; Ex. 2001 ¶ 93). Although Mostafazadeh states "tape has the drawback of being *relatively expensive*" (Ex. 1003, 2:24–25 (emphasis added)), economic costs do not necessarily counsel against a beneficial combination or modification, unless there was some technological incompatibility that prevented the combination or a significant technical challenge that would teach away from the combination. *See Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1013 (Fed. Cir. 1983) ("[T]he fact that the two disclosed apparatus would not be combined by businessmen *for economic reasons* is not the same as saying that it could not be done because skilled persons in the art felt that there was some technological incompatibility that prevented their combination. Only the latter fact is telling on the issue of nonobviousness." (emphasis added)). In addition, "the teaching away inquiry does not focus on whether a person of ordinary skill in the art would have merely favored one disclosed option

over another disclosed option.” *Bayer Pharma AG v. Watson Lab ’ys, Inc.*, 874 F.3d 1316, 1327 (Fed. Cir. 2017). “In assessing whether prior art teaches away, that better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.” *Id.* (quotation mark omitted) (citation omitted). “When there are only two possible formulations and both are known in the art at the time, the fact that there may be reasons a skilled artisan would prefer one over the other does not amount to a teaching away from the lesser preferred but still *workable option.*” *Id.* (emphasis added).

In his Declaration, Mr. Elenius states that “a tape cannot be coated on using the Mostafazadeh’s fabrication method,” but does not explain why or provide any supporting evidence for his testimony. Ex. 2001 ¶ 93. Thus, Mr. Elenius’s testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *see also Rohm and Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997) (nothing requires a fact finder to credit the inadequately explained testimony of an expert).

At this stage of the proceeding, based on the current record, we determine that Mostafazadeh’s statement that “tape has the drawback of being relatively expensive” is not likely to amount to teaching away, absent a persuasive showing of some technological incompatibility or a significant technical challenge in using an adhesive tape, film, or thermo-compression sheet in the wafer process of Mostafazadeh. The parties are invited to brief this issue further during trial.

Patent Owner further asserts that a person of ordinary skill in the art would not have been motivated to combine Ball and Mostafazadeh with a reasonable expectation of success because “the combination would not result in a functioning semiconductor device.” Prelim. Resp. 21–22. Patent Owner argues that using semiconductor chips manufactured by Mostafazadeh’s process in the multichip package of Ball would have caused the overflow problem rendering the resulting package inoperative. *Id.* at 24–25. For the reasons discussed above, we find Patent Owner’s argument unpersuasive for being contrary to the express disclosures of Mostafazadeh.

Lastly, Patent Owner contends that a person of ordinary skill in the art would have expected the combination of Ball and Mostafazadeh to fail because “Mostafazadeh did not contemplate multi-chip stacking and the accompanying multiple step chip-to-substrate and chip-to-chip mounting.” Prelim. Resp. 26 (citing Ex. 2001 ¶ 97). In the cited paragraph of his Declaration, Mr. Elenius opines

The statement in Mostafazadeh that its process can be used when “more than one integrated circuit die [is] packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)” appears to be mere speculation. At the time of Mostafazadeh’s filing MCPs and MCMs were most commonly planar structures versus stacked semiconductor chip structures.

Ex. 2001 ¶ 97. Mr. Elenius, however, does not explain the basis for his testimony or cite supporting evidence. Thus, Mr. Elenius’s testimony is conclusory and entitled to little weight. *See* 37 C.F.R. § 42.65.

In his Declaration, Dr. Suhling testifies that given the express teachings in Mostafazadeh about using its adhesive process to efficiently build multichip modules such as MCPs or MCMs, a person of ordinary skill

in the art would have been motivated to combine the teachings of Mostafazadeh and Ball, with a reasonable expectation of success, to utilize Mostafazadeh's process resulting in hundreds of individual chips with adhesive backsides for use in building the vertical chip stacks and multichip modules described in Ball. Ex. 1002 ¶ 128 (citing Ex. 1003, 11:16–18); Pet. 27–28 (citing Ex. 1002 ¶¶ 121–128). Dr. Suhling further explains that MCPs or MCMs—which are “3-D packaged” devices with vertically stacked IC chips—were known in the art well before 1998. Ex. 1002 ¶¶ 58–61 (discussing vertically stacked 3-D package devices described in various prior art references (citing Ex. 1025, 220; Ex. 1027, 110; Ex. 1028, Fig. 4A; Ex. 1029, 110, Fig. 3)). Based on the current record, we find Dr. Suhling's testimony credible and supported by the evidence Dr. Suhling cites.

c. Conclusion as to Claim 7 as Obvious Over Ball and Mostafazadeh

Based on the current record and for the foregoing reasons, we determine, for purposes of this Decision, that Petitioner has shown sufficiently that the combination of Ball and Mostafazadeh, in light of the general knowledge of a skilled artisan, teaches or suggests all claim elements of claim 7. We also find, for purposes of this Decision, Petitioner has provided sufficient explanation and evidence to show that a person of ordinary skill in the art would have been motivated to combine Ball and Mostafazadeh, as proposed by Petitioner, with a reasonable expectation of success.

Accordingly, based on the current record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to

claim 7 under 35 U.S.C. § 103 as obvious over the combination of Ball and Mostafazadeh in light of the general knowledge of a skilled artisan.

D. Asserted Obviousness over Ball, Mostafazadeh, and Tsumura

In this asserted ground of obviousness, Petitioner adds the teachings of Tsumura to those of Ball and Mostafazadeh and challenges claims 8 and 9 as obvious over the combination of Ball, Mostafazadeh, and Tsumura. Pet. 43–48. Patent Owner does not respond specifically to Petitioner’s challenge to these dependent claims beyond Patent Owner’s arguments advanced with respect to claim 7 discussed above. *See* Prelim. Resp. 16–17.

Claims 8 and 9 depend from claim 7. Petitioner contends that Tsumura teaches or suggests the limitations additionally recited in dependent claims 8 and 9. Pet. 44–48. Tsumura describes a thermo-compression bonding method for bonding a wire onto a material such as an aluminum electrode of a semiconductor chip. Ex. 1007, Abstract, 2:28–30. Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 8 and 9 is taught in Tsumura, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 44–48. Petitioner also explains that a person of ordinary skill in the art would have looked to Tsumura for details on how to wire-bond the various components in the multichip modules of Ball and Mostafazadeh. *Id.* at 43. Petitioner explains persuasively that a person of ordinary skill in the art would have been motivated to combine Ball and Mostafazadeh with Tsumura because Tsumura provides an efficient, straightforward, wire-bonding technique that complements the wire-bonding steps already disclosed in Ball and Mostafazadeh and known in the art. *Id.* (citing Ex. 1002 ¶¶ 166–168).

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 8 and 9 as unpatentable under § 103 over Ball, Mostafazadeh, and Tsumura.

E. Asserted Obviousness over Ball, Fogal, and Mostafazadeh

Petitioner asserts that claims 1, 2, 10, 11, and 15 are unpatentable under § 103 over Ball, Fogal, and Mostafazadeh. Pet. 5, 49–64. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 17–29. For the reasons discussed below, we determine that, on the present record, the information presented shows a reasonable likelihood that Petitioner would prevail on this ground with respect to at least one challenged claim.

1. Overview of Fogal (Ex. 1004)

Fogal describes multichip modules with a wire bond stacked chip assembly arrangement. Ex. 1004, Abstract.

Figure 1 of Fogal is reproduced below.

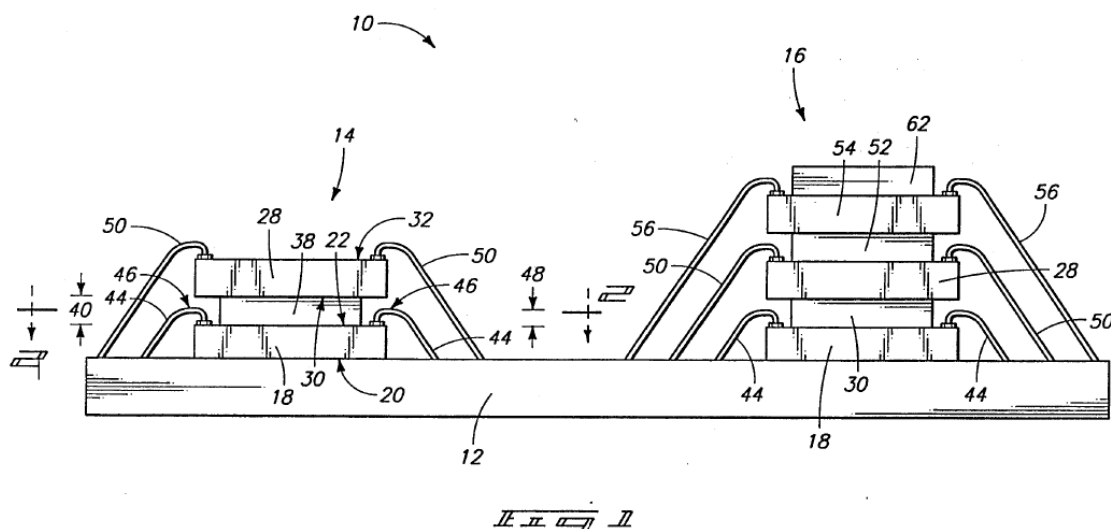


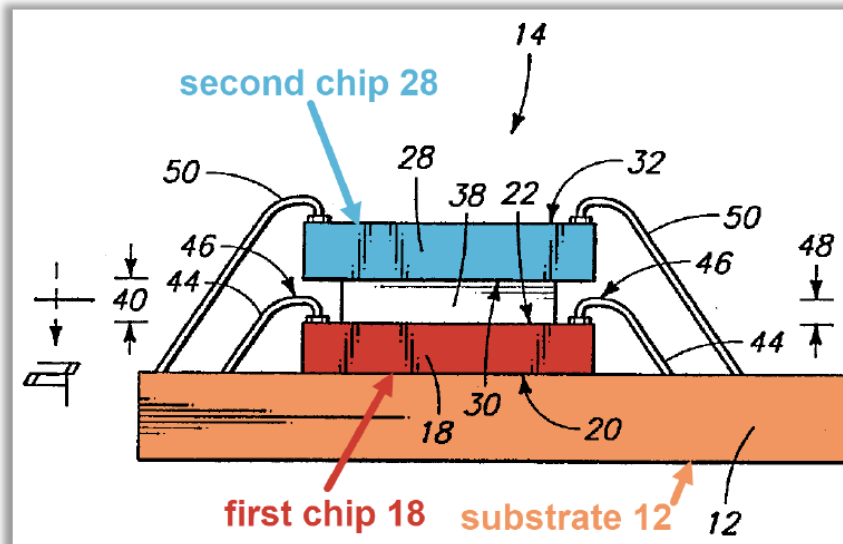
Figure 1 shows a side elevational view of an exemplary multichip module of Fogal. *Id.* at 1:45–46.

As illustrated in Figure 1, Fogal describes that base face 20 is adhered to substrate 12 by means of an adhesive, such as “epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc.” *Id.* at 2:38–41. According to Fogal, bonding face 22 includes bonding pads 26 that connect first chip 18 to substrate 12 via bonding wires 44. *Id.* at 2:41–43, 2:55–63. Second chip 28 includes bonding pads 36 that connect second chip 28 to substrate 12 via bonding wires 50. *Id.* at 2:49–66. Fogal further describes that adhesive layer 38 is interposed between, and connects, bonding face 22 of first chip 18 to base face 30 of second chip 28. *Id.* at 2:49–54, 2:60–63.

*2. Independent Claims 1, 10, and 15 as Obvious over
Ball, Fogal, and Mostafazadeh*

As discussed above in Section III.C.4, each of challenged independent claims 1, 10, and 15 recites “forming” an “adhesion layer” “on a back surface” of a “wafer” and “producing separate . . . semiconductor chips from” the “wafer by dicing,” as similarly recited in independent claim 7. Ex. 1001, 13:47–58, 15:4–8, 15:45–49, 16:48–50, 16:56–60. For these limitations of challenged independent claims 1, 10, and 15, Petitioner cites to and relies on its analysis regarding Petitioner’s application of Mostafazadeh to limitations (c) and (d) of claim 7 discussed above in Section III.C.4.a. Pet. 52–53, 56–57, 61–62, 63–64. For the rest of the claim elements relating to the assembly of a semiconductor device with a stacked package arrangement of semiconductor chips, Petitioner relies on Fogal and Ball.

Figure 1 of Fogal as annotated by Petitioner is reproduced below.



Fogal - Figure 1

Pet. 54. Annotated Figure 1 of Fogal reproduced above, illustrates Petitioner's identification in Fogal of the structural arrangement of a semiconductor device recited in claims 1, 10, and 15.

For example, Petitioner contends that Fogal and Ball teach “(c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer” and “(f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip,” as recited in claim 1, because Ball discloses a wiring layer and Fogal discloses that base face 20 of first chip 18 is adhered to substrate 12 “by means of an adhesive, such as epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc.” and second chip 28 is adhered to the top of first chip 18. Pet. 53–55, 57 (citing Ex. 1004, 1:46–47, 2:31–41, Fig. 1; Ex. 1005, 2:26–20, 3:51–53, 5:12–18; Ex. 1002 ¶¶ 205–210, 214–216).

Petitioner asserts that Fogal and Ball teach “(a) applying an adhesive paste on a wiring layer, and thereafter, mounting a first semiconductor chip on said wiring layer with a back surface of said semiconductor chip facing said wiring layer, the back surface having no circuit formed thereon” and “(d) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip,” as recited in independent claim 10 for similar reasons. *Id.* at 60–61, 62. Petitioner also contends that Fogal and Ball teach “(c) mounting at least one of said first semiconductor chips on a wiring layer with the back surface of the at least one first semiconductor chip facing said wiring layer” and “(f) mounting at least one of said second semiconductor chips on said at least one of said first semiconductor chip with the back surface of the at least one second semiconductor chip facing said at least one of said first semiconductor chips,” as recited in independent claim 15, citing to Petitioner’s analysis of limitations (c) and (f) of claim 1. *Id.* at 63, 64.

Addressing the reasons to combine the references, Petitioner asserts that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh because all three references are in the same field of semiconductor multichip modules and address the same issues of making a smaller, cheaper, and denser multichip module. Pet. 49. Petitioner further contends that a person of ordinary skill in the art reading Ball would have looked to Fogal for its disclosure of mounting the backside of a chip to a substrate, which was well-known in the art at the time of the invention. *Id.* at 50 (citing Ex. 1002 ¶ 188).

In addition, Petitioner asserts that a person of ordinary skill in the art would have been motivated to combine Mostafazadeh’s adhesive process

with the method of manufacturing multichip modules taught in Ball and Fogal because using chips with adhesive backsides would make building multichip modules more efficient. *Id.* at 51 (citing Ex. 1003, 11:16–18). Citing the testimony of Dr. Suhling, Petitioner argues that a person of ordinary skill in the art would have been motivated to combine, with a reasonable expectation of success, Mostafazadeh’s adhesive application process resulting in hundreds of chips with adhesive backsides for wire bond interconnections, where the lower chip’s backside is directly mounted onto the substrate as described in Fogal and for attaching chips back-to-back on top of the bottom chip as described in Ball because Mostafazadeh merely explains in more detail methods known in the art for creating chips with adhesive surfaces. *Id.* (citing Ex. 1002 ¶¶ 187–196).

Patent Owner asserts that Mostafazadeh does not teach an “adhesion layer” under its proposed construction of term, presenting essentially the same arguments discussed above with respect to obviousness of claim 7 over Ball and Mostafazadeh. Prelim. Resp. 18–21; Sur-reply 2–4. For the reasons discussed in Section III.C.4.b above, at this stage of the proceeding, we find Patent Owner’s arguments unpersuasive.

Patent Owner additionally argues that Fogal does not teach an “adhesion layer” under Patent Owner’s claim construction. Prelim. Resp. 18–19. Patent Owner’s argument is unavailing because Petitioner relies on Mostafazadeh, not Fogal, as teaching “forming” an “adhesion layer” “on a back surface” of a “wafer” as recited in independent claims 1, 10, and 15. Pet. 52, 56, 61, 63.

Patent Owner further asserts that a person of ordinary skill in the art would not have been motivated to combine Ball, Fogal, and Mostafazadeh

with a reasonable expectation of success because “the combination would not result in a functioning semiconductor device.” Prelim. Resp. 21–22. Patent Owner argues that using semiconductor chips manufactured by Mostafazadeh’s process in the multichip package of Ball and Fogal would have caused the overflow problem rendering the resulting package inoperative. *Id.* at 24–25. For the reasons discussed above in Section III.C.4.b, we find Patent Owner’s argument unpersuasive because it is contrary to the express disclosures of Mostafazadeh.

Lastly, Patent Owner argues that the proposed combination of Mostafazadeh with Fogal fails “because the resulting structure would deform and even short-circuit the bond wires extending from the substrate to the top surface of the first (lower) semiconductor chip.” Prelim. Resp. 22–23 (citing Ex. 2001 ¶¶ 87, 98). To illustrate its argument, Patent Owner presents an annotated figure illustrating the combined stacked chip structure of Mostafazadeh with Fogal. *Id.* at 23.

Patent Owner’s argument is unavailing because, as discussed above, Petitioner relies on Fogal and Ball, not Mostafazadeh, as teaching the claim elements relating to the assembly of a semiconductor device with a stacked package arrangement of semiconductor chips. Pet. 53–55, 57, 60–61, 62, 63, 64. Petitioner relies on Mostafazadeh as teaching or suggesting “forming” an “adhesion layer” “on a back surface” of a “wafer” and “producing separate . . . semiconductor chips from” the “wafer by dicing” as recited in challenged independent claims 1, 10, and 15. *Id.* at 52–53, 56–57, 61–62, 63–64.

In addition, to the extent Patent Owner’s argument is premised on physical incorporation of Mostafazadeh’s structure into Fogal’s multichip

structure, we disagree with Patent Owner because “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.” *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) (*quoting In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Based on the current record and for the foregoing reasons, we determine, for purposes of this Decision, that Petitioner has shown sufficiently that Ball, Fogal, and Mostafazadeh in light of the general knowledge of a skilled artisan teaches or suggests all claim elements of challenged independent claims 1, 10, and 15. We also find, for purposes of this Decision, Petitioner has provided sufficient explanation and evidence to show that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, and Mostafazadeh, as proposed by Petitioner, with a reasonable expectation of success.

Accordingly, based on the current record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 1, 10, and 15 under 35 U.S.C. § 103 as obvious over the combination of Ball, Fogal, and Mostafazadeh in light of the general knowledge of a skilled artisan.

*3. Dependent Claims 2 and 11 as Obvious over
Ball, Fogal, and Mostafazadeh*

Claim 2 depends from claim 1 and claim 11 depends from claim 10. Petitioner asserts that Fogal teaches the additionally recited limitations of claims 2 and 11. Pet. 58–60, 62. Petitioner provides detailed analysis

showing where it contends each additional limitation of dependent claims 2 and 11 is taught in Fogal, which we find sufficiently persuasive on the current record and at this stage of the proceeding. *Id.*

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to independent claims 1 and 10 discussed above. *See* Prelim. Resp. 17.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 1 and 11 as unpatentable under § 103 over Ball, Fogal, and Mostafazadeh.

F. Asserted Obviousness over Ball, Fogal, Mostafazadeh, and Tsumura or Ma

Claims 3 and 4 depend from claim 1 and additionally recite limitations similar to the limitations recited in claim 8. Claim 12 depends from claim 10 and recites additional limitations similar to the limitations recited in claim 8.

Petitioner contends that Tsumura teaches or suggests the limitations additionally recited in dependent claims 3, 4, and 12, citing to Petitioner's analysis of claim 8. Pet. 65–67.

Patent Owner does not respond specifically to Petitioner's challenge to these dependent claims beyond Patent Owner's arguments advanced with respect to claims 1 and 10 discussed above. *See* Prelim. Resp. 29.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 3, 4, and 12 as unpatentable under § 103 over Ball, Fogal, Mostafazadeh, and Tsumura.

Claims 5 and 6 depend from claim 1 and claims 13 and 14 depend from claim 10. Petitioner contends that Ma teaches or suggests the limitations additionally recited in dependent claims 5, 6, 13, and 14. Pet. 68–74. Ma describes mounting a patch die on the top surface of a primary die in a semiconductor package “to achieve an upgrade, modify chip operating parameters[,] or remedy a design or fabrication problem” of the primary die. Ex. 1009, Abstract, 1:14–19, 4:18–25. Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 5, 6, 13, and 14 is taught in Ma, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 68–74.

Petitioner explains that a person of ordinary skill in the art would have been motivated to combine Ball, Fogal, and Mostafazadeh with Ma because Ma cites Fogal on its face. Pet. 67; Ex. 1009, code (56). In addition, according to Petitioner, Ma addresses the same problem as Ball and Fogal—decreasing package size. Pet. 68 (citing Ex. 1009, 4:18–20; Ex. 1005, 2:26–31; Ex. 1004, 1:11–40). Petitioner also explains that a person of ordinary skill in the art would have understood that Ma’s teachings would be useful if the packages disclosed in Ball or Fogal needed to be upgraded, modified, or fixed. *Id.* at 67–68 (citing Ex. 1009, 4:5–12).

Patent Owner does not respond specifically to Petitioner’s challenge to these dependent claims beyond Patent Owner’s arguments advanced with respect to independent claims 1 and 10 discussed above. *See* Prelim. Resp. 29–30.

Based on the current record, we determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 5,

6, 13, and 14 as unpatentable under § 103 over Ball, Fogal, Mostafazadeh, and Ma.

IV. CONCLUSION

For the foregoing reasons, taking into account the arguments and evidence presented in Preliminary Response, Reply, and Sur-reply, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in proving that at least one challenged claim of the '879 patent is unpatentable. Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

At this stage of the proceeding, we have not made a final determination as to the patentability of any of the challenged claims. Our final determination will be based on the record as fully developed during trial.

V. ORDER

In consideration of the foregoing, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is hereby instituted as to claims 1–15 of the '879 patent on all grounds presented in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, commencing on the entry date of this Decision.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES, LLC,
Patent Owner.

IPR2023-00073
Patent 6,352,879 B1

Before MINN CHUNG, JULIA HEANEY, and SHELDON M. McGEE,
Administrative Patent Judges.

McGEE, *Administrative Patent Judge*, dissenting.

I respectfully dissent from the majority's decision to institute trial in this proceeding. In my view, the current record supports Patent Owner's claim construction of the phrase "adhesion layer" as "a pre-formed layer that is adhered," i.e., not the liquid or semi-liquid adhesive agents disclosed in the applied prior art. Based on what appears to be the proper construction of

the phrase “adhesion layer” recited in each challenged independent claim, I am not persuaded that Petitioner’s proffered arguments and evidence are sufficient to demonstrate a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. I would, therefore, deny institution.

I. CLAIM CONSTRUCTION

Petitioner challenges all issued claims 1–15 of the ’879 patent. Pet. 4–5. Of those claims, claims 1, 7, 10, and 15 are independent. Ex. 1001, 13:45–16:65. Each of those independent claims recites forming one or more “adhesion layer[s].” *Id.* Therefore, by extension, each challenged claim requires forming an “adhesion layer.”

In the Petition, Petitioner stated that it “does not believe construction of any term is necessary to resolve the invalidity challenges set forth in [the] Petition,” but “reserves the right to . . . respond to any constructions that Patent Owner presents in this proceeding.” Pet. 14–15.

Patent Owner argues that “the term ‘adhesion layer’ should be construed to mean ‘a pre-formed layer that is adhered,’” and argues that we should adopt this construction for several reasons. Prelim. Resp. 12–14. In particular, Patent Owner argues that the ’879 patent describes the adhesion layer as “a layer that is adhered.” *Id.* at 12 (citing Ex. 1001, 6:47–52). Patent Owner also asserts that the ’879 patent distinguishes the claimed “adhesion layer” from liquid or semi-liquid viscous adhesive agents that are coated or deposited on [a surface] which may result in overflowing or spreading out from the back surface of a semiconductor chip.” *Id.* at 13. Patent Owner points to three separate examples of how the ’879 patent distinguishes between an “adhesion layer” and an “adhesive agent.” *Id.* at

13–14. Namely, Patent Owner contends that the ’879 patent discloses a “manufacturing method [where] the second semiconductor chip has the insulating adhesion layer ***adhered to*** its back surface in advance when being in the wafer state.” *Id.* at 13 (citing Ex. 1001, 5:16–17) (emphasis in original). Patent Owner asserts that the ’879 patent discloses that, in the manufacturing method employing an “adhesion layer,” there is no “adhesive agent” that “overflow[s] the space between the first and second semiconductor chips,” which is described as a disadvantage of using adhesives in a conventional processing method. *Id.* (citing Ex. 1001, 5:23–28, 1:23–48⁶). Next, Patent Owner points to Figures 14(a) and 14(b), which Patent Owner asserts “distinguishes between a solid sheet and a liquid or semi-liquid viscous adhesive agent.” *Id.* (citing Ex. 1001, 2:23–58; Fig. 14(b)). Here, Patent Owner asserts that “[i]tem 91 is a discretely placed, chip size adhesive sheet that does not overflow or underfill the back surface of the semiconductor chip while 87a is an adhesive agent that does,” and points to Figure 14(b) for support. *Id.* Finally, Patent Owner contends that claim 10 distinguishes between applying an adhesive paste and forming an adhesion layer. *Id.* at 14 (citing Ex. 1001, claim 10, 9:25–30).

Petitioner sought leave to file a Reply to address Patent Owner’s proffered claim construction of the term “adhesion layer,” which Patent Owner did not oppose. Ex. 3001. After we authorized Petitioner’s reply and Patent Owner’s sur-reply, the parties timely filed that additional briefing. Papers 10, 12.

⁶ Patent Owner’s citation to column 1 here appears to be a typographical error as the disadvantages of applying an “adhesive agent” are set forth in column 2 of the ’879 patent. *See* Ex. 1001, 2:18–43.

After considering the parties' fully briefed claim construction arguments at this stage of the proceeding, it is my view that Patent Owner has the better position. And for the reasons that follow, Petitioner's arguments set forth in its reply (Paper 10) do not persuade me otherwise on the preliminary record. I address what I view as the deficiencies in Petitioner's claim construction arguments below.

Petitioner first asserts that Patent Owner's proposed construction directly contradicts a "prior admission" that the phrase "adhesion layer" is "easily understandable." Paper 10, 1. Petitioner asserts that, in "argu[ing] that the phrase 'adhesion layer' should be given its 'plain and ordinary meaning,'" Patent Owner "conceded that there was 'nothing in the prosecution history that rises to a clear intention to limit the scope of adhesion layer.'" *Id.* (citing Ex. 1036, 19). Petitioner contends that Patent Owner "previously championed the exact opposite construction that it now asks the Board to adopt—and does so without any attempt to justify or explain its about-face." Paper 10, 1.

I disagree with this line of argument. In the district court litigation to which Petitioner refers, Western Digital Technologies, Inc. ("Western Digital")—who is not a party in this proceeding—argued that the term "adhesion layer" should be limited to the "thermo-compression sheet" embodiment disclosed in the '879 patent. Ex. 1036, 19. In response to that argument, Patent Owner argued that the claimed "adhesion layer" should not be so limited, but should instead be given its plain and ordinary meaning. *Id.* In my view, Petitioner mischaracterizes Patent Owner's statements made in the *Western Digital* litigation by reproducing only a select portion of Patent Owner's statement regarding the '879 patent prosecution history.

Paper 10, 1. Specifically, Petitioner asserts that Patent Owner “also conceded that there was ‘nothing in the prosecution history that rises to a clear intention to limit the scope of adhesion layer’.” *Id.* But Petitioner’s reproduction of Patent Owner’s argument conspicuously omits Patent Owner’s reference to the “thermo-compression sheet” embodiment. *Compare* Paper 10, 1 (“Katana also conceded that there was ‘nothing in the prosecution history that rises to a clear intention to limit the scope of adhesion layer’”), *with* Ex. 1036, 19 (“Western Digital cannot identify anything in the prosecution history that rises to a clear intention to limit the scope of ‘adhesion layer’ to *thermo-compression sheet*.” (emphasis added)). In other words, Petitioner’s selective quotation of Patent Owner’s argument in the *Western Digital* litigation appears to suggest that Patent Owner argued the prosecution history of the ’879 patent does not limit the phrase “adhesion layer” *at all*. But, in context, Patent Owner was merely responding to Western Digital’s proffered claim construction which was narrower than Patent Owner’s. *See* Paper 12, 1 (“Critically, Western Digital never took the position that ‘adhesion layer’ could simply be an adhesive” and “the dispute implicated by Micron’s IPR Petition is a new one; it was never raised in *Western Digital* and was therefore never addressed in the claim construction briefing.”). Thus, I am not persuaded that Patent Owner is taking a contrary claim construction position here than that asserted in the *Western Digital* litigation.

Petitioner next asserts that the ’879 patent exemplifies an “adhesion layer” as not only a “thermo-compression sheet,” but also an “adhesive agent,” a “paste,” and an “adhesive sheet.” Paper 10, 2. Petitioner asserts further that “nothing in the intrinsic record remotely suggests that the

patentee acted as his own lexicographer” by, for example, “(1) limiting the ‘adhesion[] layer’ to a ‘pre-formed’ layer; (2) disavowing the use of adhesive agents or pastes as the adhesion layer; or (3) using ‘adhesive’ and ‘adhesion’ as mutually exclusive terms.” *Id.* at 2–3.

On this preliminary record, I disagree. As I see it, the ’879 patent appears to repeatedly distinguish between an “adhesion layer” and an “adhesive agent.” *See* Ex. 1001, 2:12–17 (describing a fabrication method using an “adhesive agent (paste)” and a separate method using “a thermo-compression sheet”)⁷; *id.* at 2:18–43 (explaining that “if the amount of the *adhesive agent* is excessive, a large amount of *adhesive agent* spreads beyond the outer edge of the semiconductor chip” as depicted in Figure 14(a) where adhesive agent 87 between chips 81 and 82 overflows as adhesive agent 87a, and that “if the amount of the *adhesive agent* is too small, a gap is produced between the semiconductor chips 81 and 82 (emphases added)); *id.* at 3:14–24 (distinguishing between using an adhesion layer to affix a second semiconductor chip to a first semiconductor chip and “a situation in which [] excessively applied *adhesive agent* overflows the space between the first and second semiconductor chips” (emphasis added)); *id.* at 4:21–60 (disclosing a manufacturing method where “forming . . . [an] adhesion layer” on a surface results in no overflow of an “adhesive agent” from the space between the first and second semiconductor chips); *id.* at 4:61–5:23 (describing a manufacturing method where an “adhesion layer [is] adhered to” a surface, wherein no “adhesive agent” “overflow[s] the space between the first and second semiconductor chips”); *id.* at 15:39–46

⁷ The ’879 patent describes the “thermo-compression sheet” as an “adhesion layer.” Ex. 1001, 6:50–51.

(claiming a step of “applying an adhesive paste” and a separate step of “forming an adhesion layer”); *see also* Paper 12, 4–5 (explaining that “claim 10 recites a single ‘adhesion layer’ applied to the back surface of a wafer, but does not recite the same for the paste,” which “confirms that the [’879 patent] distinguish sharply between a ‘paste’ and an ‘adhesion layer’”).

“A long line of cases indicates that evidence intrinsic to the patent—particularly the patent’s specification, including the inventor’s statutorily-required written description of the invention—is the primary source for determining claim meaning,” which is a “proposition [that] has been accepted doctrine in patent law for many years.” *Astrazeneca AB v. Mut. Pharm. Co., Inc.*, 384 F.3d 1333, 1336–37 (Fed. Cir. 2004); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (en banc) (our reviewing court explaining that “our cases recognize that the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess” and that “[i]n such cases, the inventor’s lexicography governs”). Here, the ’879 patent appears to contain sufficient disclosure that distinguishes between an “adhesion layer” and “adhesive agent,” e.g., a “paste.” Thus, on this preliminary record, I disagree with Petitioner that the intrinsic “record lacks any clear statement” that the phrase “adhesion layer” is mutually exclusive from an “adhesive agent” or “paste.” Paper 10, 2–3.

Next, Petitioner contends that Patent Owner’s construction of “adhesion layer” is erroneous. Paper 10, 3–5. Specifically, Petitioner asserts that “the term ‘pre-formed’ does not appear anywhere in ’879 patent,” that Patent Owner “fails to even explain what a ‘pre-formed layer’

is,” and that Patent Owner “makes [it] abundantly clear that only ‘thermo-compression sheets’ could render the ’879 patent invalid.” *Id.* at 3.

Contrary to Petitioner’s position, however, Patent Owner does not appear to argue that “adhesion layer” should be limited to the thermo-compression sheet embodiment and that only that embodiment could invalidate the ’879 patent. *See* Prelim. Resp. 13–14 (asserting that “in describing the thermo-compression sheet *as one embodiment* of the adhesion layer, *the patentee intended adhesion layer to mean ‘a pre-formed layer that is adhered.’*” (emphases added)); *see also* Ex. 1036, 19 (arguing in the Western Digital litigation against such a construction). Thus, it is unclear to me on this record how Petitioner determines that Patent Owner is asserting “that only ‘thermo-compression sheets’ could render the ’879 patent invalid.” Paper 10, 3.

Next, Petitioner repeats its contention that the ’879 patent fails to distinguish between solid sheets and other types of adhesive agents because the ’879 patent recognizes problems associated with each. Paper 10, 4. On this preliminary record, and for the reasons I have already explained, I am not persuaded by Petitioner’s argument regarding a lack of distinction between these terms. And I furthermore disagree with Petitioner’s seeming suggestion here that because thermo-compression sheets and adhesive agents each have drawbacks associated with their individual use, there exists no distinction between these elements. In other words, “thermo-compression sheets” and “adhesive agents” do not become identical elements just because they individually have different problems associated with their separate use. Moreover, because the ’879 patent identifies distinct *problems* with using thermo-compression sheets vis-à-vis adhesive agents, this suggests to me

that the '879 patent views such sheets and agents as separate and distinct *elements*. Compare Ex. 1001, 2:18–43 (explaining that using an excessive amount of adhesive agent causes “a large amount of adhesive agent” to spread and overflows the space between semiconductors 81 and 82, and that “if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82,” which causes “problems such as separation of the semiconductor chip 82 from the semiconductor chip 81”), with *id.* at 2:44–51 (explaining that “using a thermo-compression sheet requires the steps of placing members at the right locations” on the semiconductor chip).

Petitioner asserts next that Patent Owner relies on features not recited in the claims to support its construction, and that the claimed step of forming an adhesion layer is not limited to a specific process. Paper 10, 4–5. Petitioner also asserts that no claim recites preventing overflow of an adhesive. *Id.* at 4. I disagree with that line of argument, however, because it ignores the critical role that the specification plays in the claim construction analysis. “[T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Here again, the specification of the '879 patent appears to distinguish repeatedly between an “adhesion layer” and an “adhesive agent.” The '879 patent teaches that adhesive agents have the potential to “overflow” the space between the semiconductor chips when excessively applied. Ex. 1001, 2:18–38, 3:23 4:4. In my view, the claim need not recite such a functional feature because the specification’s disclosure is highly relevant to our claim construction analysis. And

contrary to Petitioner’s apparent position (Paper 10, 4–5), I do not see how the step of forming an adhesion layer needs to be limited to an express process in the specification for us to properly construe the meaning of “forming an adhesion layer.” In this regard, the ’879 patent discloses “[a] method of manufacturing a semiconductor device . . . [which] includes the steps of: (a) forming a first insulating adhesion layer on a back surface of a first wafer” and “(d) forming a second insulating adhesion layer on a back surface of a second wafer.” Ex. 1001, 4:21–31. The ’879 patent explains that “[w]ith the *above manufacturing method* . . . the first or second semiconductor chip has the first or second insulating adhesion layer *adhered to its back surface in advance when being in the wafer state.*” Ex. 1001, 4:44–47 (emphases added). This suggests to me that the adhesion layer “forming” steps are met by adhering an adhesion layer to the semiconductor chip’s back surface. And this disclosure appears to me to support Patent Owner’s argument that the adhesion layer is a “pre-formed layer that is adhered.” In other words, an “adhesion layer” cannot be “adhered” to a surface unless it is already formed as a layer, i.e., it already exists as a “pre-formed layer.”

Petitioner also asserts that the ’879 patent does not distinguish between the terms “adhesive” and “adhesion” because “it uses ‘adhesive’ to refer both to a solid sheet and a liquid/semi-liquid adhesive.” Paper 10, 5. I also disagree with that argument on this preliminary record because it seems to amount to no more than selective quotation of “adhesive” and “adhesion” out of context. The claim construction inquiry does not center on the terms “adhesive” and “adhesion” to the exclusion of other terms associated with these words. The issue before us is whether the term “adhesion *layer*”

includes “adhesive *agents*” such as the fluid-based adhesives⁸ disclosed in the relied-upon prior art. On the current record, I am not persuaded that it does.

Finally, Petitioner asserts that Patent Owner “misapplies the doctrine of claim differentiation . . . by arguing that claim 2’s recitation of a paste proves that ‘a paste is different from the adhesion layer.’” Paper 10, 5. According to Petitioner, the claim equates a “paste” with a “first adhesion layer,” because the claim recites “a second adhesion layer,” which “clearly implies the existence of a first adhesion layer, and the only other adhering element in the claim would be the ‘paste.’” *Id.* This argument is not well-taken because claim 2 of the ’879 patent does not contain the term “paste.” To the extent Petitioner intended to refer to claim 10 of the ’879 patent here—which does recite the term “paste”—I disagree with this line of argument because claim 10 does not recite a “second adhesion layer.” Ex. 1001, 15:44. Rather, the claim requires “forming an *adhesion layer* on a back surface of a wafer” after the step of “applying an *adhesive paste* on a wiring layer.” *Id.* at 15:39–46 (emphases added). Because the ’879 patent uses separate terminology in claiming these separate steps, it is my view at this stage of the proceeding that their meaning is presumed to be different. *See CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) (“In the absence of any evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings.”).

⁸ *See* Pet. 36 (“The adhesive is a fluid-based form of a paste, gel, or liquid.” (citing Mostafazadeh 6:3–4)).

In sum, on this preliminary record, I agree with Patent Owner that the term “adhesion layer” should be construed to be “a pre-formed layer that is adhered” because that construction appears to be supported by the intrinsic record. Prelim. Resp. 12.

II. PETITIONER’S CHALLENGES

Each of Petitioner’s challenges relies on Mostafazadeh’s “adhesive application process” to evince the claimed step of “forming” the “adhesion layer.” *See* Pet. 34 (asserting for element [c] in claim 7 that “Ball . . . does not describe how the adhesive is formed on the chip” and relying on “Mostafazadeh [to] provide[] these wafer fabrication details”); *id.* at 52, 56 (referring back to the claim 7[c] analysis for claim elements 1[a] and 1[d]); *id.* at 61, 63 (referring back to the analysis for claim elements 1[a] and 1[d] for claim elements 10[b], 15[a] and 15[b]).

The disclosure of Mostafazadeh that Petitioner relies on, however, discusses application of an adhesive that is “a fluid-based form of a paste, gel, or liquid” to a wafer. Pet. 36 (citing Ex. 1003, 6:3–4). According to Petitioner, the “adhesive layer” that results from Mostafazadeh’s process after the fluid-based adhesive dries amounts to the claimed “adhesion layer.” *Id.* at 36–37.

I am not persuaded on this preliminary record that Petitioner’s reliance on Mostafazadeh’s “fluid-based” adhesive such as a “paste,” which is applied to a wafer in a “rolling” step and ultimately dries, is sufficient to meet the reasonable likelihood standard required for instituting trial. 35 U.S.C. § 314(a). In particular, I have concerns that Petitioner relies on prior art disclosing applying a fluid-based adhesive to a wafer which subsequently dries to evince “adhesion layer” formation, when the ’879

patent appears to distinguish between an “adhesion layer” that is “adhered to” a surface, and an “adhesive agent” or “paste” that is applied to a surface and may “overflow.” Ex. 1001, 2:12–43, 3:14–24, 4:21–58, 5:12–26, 9:24–28, 15:37–46. Because of that, I would find that this Petition fails to meet the institution standard, and would deny the Petition.

I, therefore, dissent from the majority’s decision to institute trial, with respect.

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PETITIONER:

Amy Simpson
Amanda Tessar
PERKINS COIE LLP
simpson-ptab@perkinscoie.com
tessar-ptab@perkinscoie.com

PATENT OWNER:

Howard Lim
Scott Breedlove
Michael Pomeroy
CARTER ARNETT PLLC
hlim@carterarnett.com
sbreedlove@carterarnett.com
mpomeroy@carterarnett.com