

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00073
Patent 6,352,879 B1

Before ELIZABETH M. ROESEL, JULIA HEANEY, and
SHELDON M. McGEE, *Administrative Patent Judges*.

Opinion for the Board filed by *Administrative Patent Judge* McGEE.

Opinion Concurring filed by *Administrative Patent Judge* McGEE.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–15 (the “challenged claims”) of U.S. Patent No. 6,352,879 B1 (Ex. 1001, “the ’879 patent”). We instituted this *inter partes* review as to all challenged claims. Paper 13 (“Inst. Dec.” or “DI”).

Katana Silicon Technologies LLC (“Patent Owner”) filed a Patent Owner Response (Paper 26, “PO Resp.”); Petitioner filed a Reply to the Patent Owner Response (Paper 27, “Pet. Reply”); and Patent Owner filed a Sur-reply (Paper 28, “PO Sur-reply”). Petitioner filed the Declaration of Jeffrey C. Suhling, Ph.D. (Ex. 1002) in support of the Petition, and Patent Owner filed the Declaration of Peter Elenius in support of its Response (Ex. 2014). The parties also filed transcripts of the depositions of Dr. Suhling (Ex. 2012) and Mr. Elenius (Ex. 1037).

An oral hearing was held on February 15, 2024, and a transcript of the hearing is included in the record. Paper 39 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–15 of the ’879 patent. For the reasons discussed below, we hold that Petitioner has demonstrated by a preponderance of the evidence that claims 1–15 are unpatentable.

A. *Real Parties-in-Interest*

Petitioner identifies Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC as the real parties-in-

interest. Pet. 2. Patent Owner identifies itself as the real party-in-interest. Paper 5, 1.

B. Related Proceedings

According to the parties, the '879 patent is the subject of the following district court litigation: *Katana Silicon Techs. LLC v. Micron Tech., Inc.*, 1:22-cv-00282 (D. Idaho). Paper 5, 1; Pet. 2.

The '879 patent is one of several patents owned by Patent Owner that are challenged by Petitioner in various petitions for *inter partes* review, including in IPR2023-00071, IPR2023-00072, and IPR2023-00105.

C. The '879 patent

The '879 patent describes a miniaturized semiconductor device having a chip size package (CSP) that includes multiple semiconductor chips stacked vertically inside the package (in an arrangement called a stacked package structure). Ex. 1001, 1:18–23, 2:60–62.

Figure 14(a) of the '879 patent is reproduced below.

FIG.14 (a)

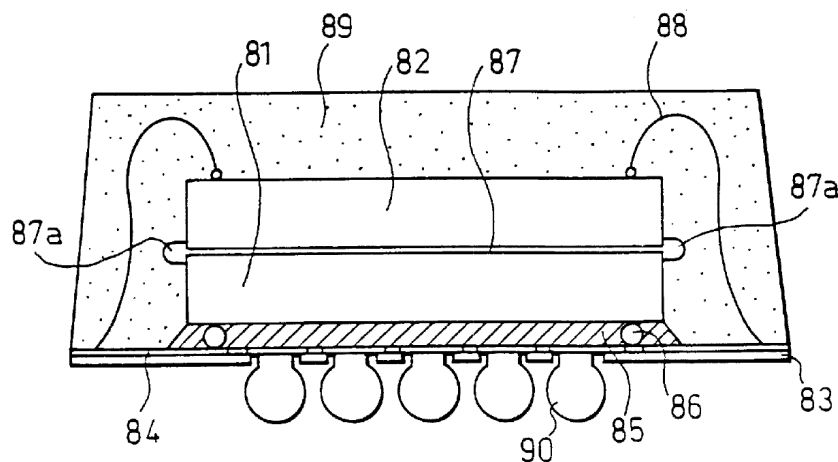


Figure 14(a) shows a cross-sectional view of a conventional

semiconductor device having a stacked package structure. *Id.* at 6:25–27.

The '879 patent describes that in a conventional semiconductor device where multiple semiconductor chips are stacked and laminated, two different methods are used to bond the laminated semiconductor chips to each other in a stacked package—“an adhesive agent (paste) potting method” and “a method using a thermo-compression sheet.” *Id.* at 2:12–17. According to the '879 patent, in the potting method, if the amount of the adhesive agent is excessive, a large amount of adhesive agent may spread and overflow beyond the outer edge of the semiconductor chips, as illustrated in Figure 14(a) (showing adhesive agent 87 between semiconductor chips 81 and 82 overflowing beyond the edges of the chips). *Id.* at 2:18–24. Such overflowed adhesive agent may come in contact with wires in the package or the electropad of the semiconductor chips. *Id.* at 2:31–38. The '879 patent describes that “[o]n the other hand, if the amount of the adhesive agent is too small, a gap is produced between the semiconductor chips 81 and 82 . . . causing problems such as separation of the semiconductor chip 82 from the semiconductor chip 81.” *Id.* at 2:39–43.

According to the '879 patent, the conventional method using a thermo-compression sheet for bonding semiconductor chips during packaging also has shortcomings. *Id.* at 2:44–51, 4:7–16. In the conventional method, the thermo-compression sheet is disposed on the surface of a first semiconductor chip, and then a second semiconductor chip is adhered to the thermo-compression sheet. *Id.* at 9:46–50. The '879 patent describes that in the conventional thermo-compression sheet method, the thermo-compression sheet must have the same size as semiconductor chip 82 and must be placed accurately at a specific location on

semiconductor chip 81. *Id.* at 2:45–49. “In addition, the semiconductor chip 82 must be bonded to the thermo-compression sheet so as to be located exactly on the top of the thermo-compression sheet.” *Id.* at 2:49–52.

The ’879 patent purports to avoid these problems or complications in the conventional method by forming an adhesion layer “in advance” on a back surface of a wafer when the semiconductor chips are in a “wafer state” during the semiconductor fabrication process before the wafer is cut or diced to produce individual chips. *Id.* at 4:13–53. Specifically, the ’879 patent describes

[a] method of manufacturing a semiconductor device in accordance with the present invention includes the steps of:

- (a) forming a first insulating adhesion layer on a back surface of a first wafer having a circuit formed on its front surface;
- (b) producing separate first semiconductor chips from the first wafer by dicing;
- (c) mounting the first semiconductor chip on a wiring layer with its back surface facing the wiring layer;
- (d) forming a second insulating adhesion layer on a back surface of a second wafer having a circuit formed on its front surface;
- (e) producing separate second semiconductor chips from the second wafer by dicing;
- (f) mounting the second semiconductor chip on the first semiconductor chip with its back surface facing the first semiconductor chip;
- (g) wire-bonding the first semiconductor chip to an electrode section of the wiring layer with a wire;
- (h) wire-bonding the second semiconductor chip to an electrode section of the wiring layer with a wire; and
- (i) sealing the first and semiconductor chips and the wires.

Id. at 4:21–43.

According to the '879 patent, “[w]ith the above manufacturing method, since the first or second semiconductor chip has the first or second insulating adhesion layer adhered to its back surface *in advance when being in the wafer state*,” “the adhesive agent does not overflow the space between the first and second semiconductor chips” and “the first or second semiconductor chip can be mounted at a desired location without the step of accurately positioning the first or second insulating adhesion layer on the first or second semiconductor chip.” *Id.* at 4:44–58 (emphasis added).

The '879 patent describes two embodiments. *Id.* at 6:34–12:67. In both embodiments, a thermo-compression sheet is adhered or affixed to the back surface of a wafer to form an adhesion layer “in advance” before the wafer is cut or diced to produce individual pieces of semiconductor chips with an adhesion layer, which are then stacked and bonded to each other in a multi-chip semiconductor device package. *Id.* at 9:16–50, 12:29–44.

Figure 1 of the '879 patent is reproduced below.

FIG. 1

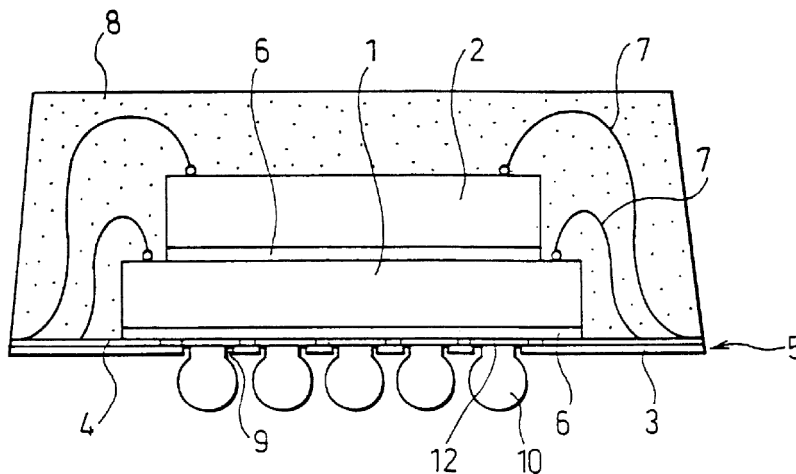


Figure 1 shows a cross-sectional view of a semiconductor device in accordance with the first embodiment of the '879 patent. *Id.* at 5:34–36.

As shown in Figure 1, in a semiconductor device of the first embodiment, “a first semiconductor chip 1 and a second semiconductor chip 2 are laminated . . . on a circuit board 5 including an insulating substrate 3 and a wiring layer 4 mounted on the insulating substrate 3.” *Id.* at 6:38–41, Fig. 1. The '879 patent refers to the surface (front surface) of a semiconductor chip on which a circuit element is formed as a “circuit formed surface” and the surface of the opposite side of the chip as a “back surface.” *Id.* at 6:43–46. In the first embodiment depicted in Figure 1, semiconductor chip 1 is disposed with its back surface facing insulating substrate 3. *Id.* at 6:47–48, Fig. 1. “The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6.” *Id.* at 6:48–52.

Figure 10 of the '879 patent is reproduced below.

FIG.10

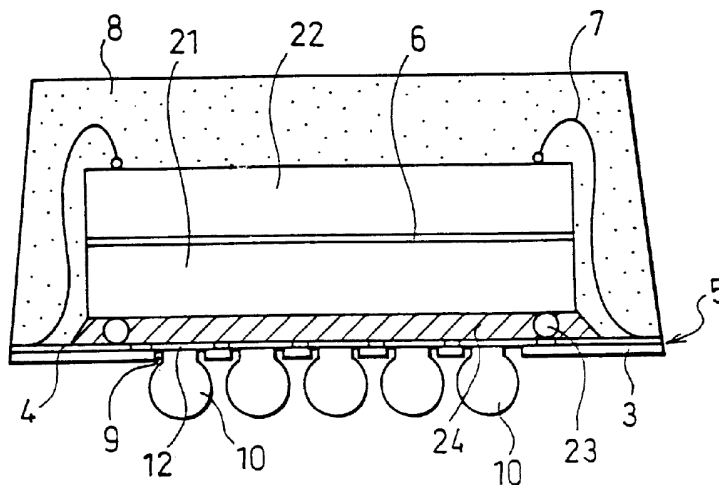


Figure 10 shows a cross-sectional view of a semiconductor device arranged in accordance with the second embodiment of the '879 patent. *Id.* at 6:7–9.

As shown in Figure 10, circuit board 5 includes insulating substrate 3, and wiring layer 4 formed on the insulating substrate. *Id.* at 11:21–23. In the second embodiment, “a first semiconductor chip 21 is mounted on a circuit board 5 with its circuit formed surface facing the circuit board 5, i.e., facing down” (*id.* at 11:19–21) and “[a] second semiconductor chip 22 is mounted on the back surface of the first semiconductor chip 21 through a thermo-compression sheet 6” (*id.* at 11:23–25). In this arrangement, the back surface of second semiconductor chip 22 faces the back surface of first semiconductor chip 21. *Id.* at 11:25–27. “Namely, the back surfaces of the first semiconductor chip 21 and the second semiconductor chip 22 are adhered to each other through the thermo-compression sheet 6.” *Id.* at 11:27–29.

The '879 patent describes that “[w]hen the second semiconductor chip 22 is in a state of wafer, the insulating thermo-compression sheet 6 is adhered to the back surface of the wafer, and then the wafer is cut to produce chips, i.e., separate pieces of second semiconductor chips 22.” *Id.* at 12:32–36. According to the '879 patent, “[l]ike the manufacturing process described in the first embodiment, the process for manufacturing the semiconductor device in accordance with the present embodiment is simplified by adhering the thermo-compression sheet 6 to the back surface of the second semiconductor chip 22 in advance.” *Id.* at 12:39–44.

D. Illustrative Claims

Of the challenged claims, claims 1, 7, 10, and 15 are independent. Claims 1 and 7 are illustrative of the challenged claims and are reproduced below, with numbering added to each element as set forth in the Petition.

1. A method of manufacturing a semiconductor device comprising:

- (a) forming a first adhesion layer on a back surface of a first wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;
- (b) producing separate first semiconductor chips from said first wafer by dicing;
- (c) mounting said first semiconductor chip on a wiring layer with its back surface facing said wiring layer;
- (d) forming a second adhesion layer on a back surface of a second wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer;
- (e) producing separate second semiconductor chips from said second wafer by dicing; and
- (f) mounting said second semiconductor chip on said first semiconductor chip with its back surface facing said first semiconductor chip.

Ex. 1001, 13:45–61.

7. A method of manufacturing a semiconductor device comprising:

- (a) forming an insulating layer and a metal bump on a wiring layer;
- (b) mounting a first semiconductor chip on said wiring layer with its circuit-formed surface facing said wiring layer;
- (c) forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer;

- (d) producing separate second semiconductor chips from the wafer by dicing;
- (e) mounting said second semiconductor chip on said first semiconductor chip with the back surface of the second semiconductor chip facing said first semiconductor chip;
- (f) wire-bonding an electrode section of said second semiconductor chip to an electrode section of said wiring layer with a wire; and
- (g) sealing said first and second semiconductor chips and said wire.

Id. at 14:64–15:16.

E. Instituted Grounds of Unpatentability

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
7	103(a) ¹	Ball, ² Mostafazadeh ³
8, 9	103(a)	Ball, Mostafazadeh, Tsumura ⁴
1, 2, 10, 11, 15	103(a)	Ball, Fogal, ⁵ Mostafazadeh
3, 4, 12	103(a)	Ball, Fogal, Mostafazadeh, Tsumura

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the '879 patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

² U.S. Patent No. 7,166,495 B2 to Ball, issued Jan. 23, 2007 (Ex. 1005).

³ Int. Pub. WO1996/13066 by Mostafazadeh et al., published May 2, 1996 (Ex. 1003).

⁴ U.S. Patent No. 4,821,944 to Tsumura, issued Apr. 18, 1989 (Ex. 1007).

⁵ U.S. Patent No. 5,323,060 to Fogal, issued June 21, 1994 (Ex. 1004).

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
5, 6, 13, 14	103(a)	Ball, Fogal, Mostafazadeh, Ma ⁶

II. ANALYSIS

A. *Principles of Law*

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.⁷ *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)); see *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688

⁶ U.S. Patent No. 6,682,954 B1 to Ma, issued January 27, 2004 (Ex. 1009).

⁷ The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that “some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]”)).

“Whether prior art invalidates a patent claim as obvious is determined from the perspective of one of ordinary skill in the art.” *Star Scientific, Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1374 (Fed. Cir. 2011).

Further, “the assessment of a claim’s patentability is inextricably tied to a skilled artisan’s knowledge and skill level.” *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1376 (Fed. Cir. 2022). Permissible uses of general knowledge of one having ordinary skill under § 103 include providing a motivation to combine and supplying a claim limitation, if supported by evidence of record. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020); *Randall Mfg. v. Rea*, 733 F.3d 1355, 1363 (Fed. Cir. 2013); *see also Qualcomm*, 24 F.4th at 1376 (permissible uses of what a skilled artisan would have known at the time of the invention include “furnishing a motivation to combine” and “supplying a missing claim limitation” (citing *Randall Mfg.*, 733 F.3d at 1363; *Koninklijke Philips*, 948 F.3d at 1337–38)).

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include the “(1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of workers active in the field.” *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic*

Equip. Co. v. All Orthopedic Appliances, Inc., 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.*

Citing testimony from Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art at the priority date of the '879 patent would have had

i) a bachelor-level degree in electrical engineering, mechanical engineering, material science, or a related subject and five or more years of experience working in the field of semiconductor packaging; ii) a Master's-level degree in mechanical engineering, electrical engineering, material science, or a related field, and at least 1-3 years of experience in the design/development of semiconductor packages; or iii) a Ph.D.-level degree in mechanical engineering, material science, electrical engineering, or a related field, and at least some experience in the area of semiconductor packaging.

Pet. 17 (citing Ex. 1002 ¶¶ 28–32). Petitioner further states that “[a]dditional education may substitute for professional experience, and significant work experience may substitute for formal education.” *Id.*

Patent Owner's declarant, Mr. Elenius, states that a person of ordinary skill in the art would have had “a bachelor's degree in electrical, mechanical or materials engineering and two to three years of experience in the design or development of semiconductor manufacturing, or the equivalent.”

Ex. 2014 ¶ 32. Mr. Elenius further states that “[a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.” *Id.*

For purposes of this Decision, we find no meaningful differences between the parties' respective definitions that would materially alter the outcome of this Decision. Nevertheless, based on our review of the '879 patent, the types of problems and solutions described in the '879 patent, and

cited prior art, we adopt and apply Petitioner’s definition of the level of ordinary skill in the art.

C. *Claim Construction*

We apply the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2023). Under that standard, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In the Decision on Institution, the majority determined that only the claimed phrase “forming an adhesion layer on a back surface of a wafer” should be construed.⁸ DI 31–32; *see Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (stating “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Specifically, the

⁸ On the preliminary record, I disagreed with the majority’s construction of the claim limitation “forming an adhesion layer on a back surface of a wafer,” and filed a dissenting opinion. DI 59–71. My concurring opinion, filed *infra*, addresses how my views have changed regarding the proper construction of “adhesion layer” based on the fully developed record.

majority construed “forming an adhesion layer on a back surface of a wafer” as “to construct or make an adhesion layer on a back surface of a wafer.”⁹ DI 32.

During trial, Patent Owner continued to seek construction of the term “adhesion layer,” while Petitioner argued that the term does not necessarily require construction. *See* PO Resp. 21–24; PO Sur-reply 1; Pet. Reply 3. On the complete record, we determine that construction of “adhesion layer” is necessary to resolve the controversy.

1. “*adhesion layer*”

In the table below, we set forth Petitioner’s and Patent Owner’s positions on the term “adhesion layer,” and our construction after considering the entire record.

Petitioner	Patent Owner	PTAB
ordinary meaning, i.e., a layer that adheres	a pre-formed layer that is adhered	a layer that adheres

Patent Owner argues an “adhesion layer” means “a pre-formed layer that is adhered.” PO Resp. 21. According to Patent Owner, an “adhesion layer” is “pre-formed like a solid sheet, as opposed to an adhesive agent, an

⁹ Such a construction informed the meaning of the term “forming” more than it did the term “adhesion layer.” Thus, no meaningful construction of “adhesion layer” was previously made of record. *See* Pet. Reply 3 (noting that “the panel majority did not construe this term”). For the sake of consistency between this Final Written Decision and those in the related proceedings IPR2023-00071 and IPR2023-00072, we expressly construe the term “adhesion layer” here, and apply that construction in our analysis of the claimed “forming” of an adhesion layer on a back surface of a wafer on which no circuit is formed recited in each independent claim. Ex. 1001, claims 1, 7, 10, and 15.

adhesive, or an adhesive layer that is completely or partially comprised of a liquid or a viscous semi-liquid.” *Id.* Petitioner opposes Patent Owner’s construction and argues “adhesion layer” should be given its ordinary meaning, i.e., a layer that adheres. Pet. Reply 3–4. On the fully developed record, we find that Petitioner’s construction, “a layer that adheres,” is more strongly supported by the evidence than Patent Owner’s construction, “a pre-formed layer that is adhered.”

Our analysis begins with the claim language itself, where the term “adhesion layer” appears in each of the ’879 patent’s independent claims. For example, claim 1 recites “forming a first *adhesion layer* on a back surface of a first wafer on which no circuit is formed” and “forming a second *adhesion layer* on a back surface of a second wafer on which no circuit is formed.” Ex. 1001, 13:47–55 (emphases added). Claims 7, 10, and 15 each recites similar language of forming an adhesion layer. *Id.* at 15:4–5, 15:44–45, 16:48–57. In the absence of contrary evidence, we must assume that the term “adhesion layer” has the same meaning in all claims of the ’879 patent. *In re Varma*, 816 F.3d 1352, 1363 (Fed. Cir. 2016) (“the principle that the same phrase in different claims of the same patent should have the same meaning is a strong one, overcome only if ‘it is clear’ that the same phrase has different meanings in different claims,” quoting *Fin Control Sys. Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001)).

The claim language, “forming” an “adhesion layer *on* a back surface,” suggests strongly that an “adhesion layer” may be formed *in situ* on the back surface of a wafer. The testimony of Patent Owner’s expert, Mr. Elenius, supports this interpretation. See Ex. 2014 ¶¶ 43, 50 (testifying that a person of ordinary skill in the art “would recognize that there are multiple methods

of forming an ‘adhesion layer’ on the back surface of the semiconductor chip” and that “[p]astes and other adhesives, adhesive agents, adhesive layers or other material that are dispensed onto a substrate or chip back *are formed into a layer over time as they harden through curing*” (emphasis added)). Thus, the language of the claims of the ’879 patent does not support Patent Owner’s construction that the “adhesion layer” must be a pre-formed layer that is adhered. *Cf.* PO Resp. 21–23 (arguing for that construction).

Patent Owner nevertheless attempts to support its construction that an “adhesion layer” is “a fully formed layer in advance.” PO Resp. 22. Specifically, Patent Owner argues that the terms “adhesion layer” and “adhesive agent” are distinct, referencing claim 10 wherein step (a) requires “applying an adhesive paste on a wiring layer . . .” and step (b) recites “forming an adhesion layer on a back surface of a wafer” *Id.*; Ex. 1001, 15:37–44. According to Patent Owner, “[t]he patentee’s explicit act of claiming them differently—as a paste and as an adhesion layer—further evidences that the patentee did not intend an adhesion layer to be an adhesive such as an epoxy paste or other substance that can flow during manufacture.” PO Resp. 23.

While Patent Owner is correct that separate terminology is used in steps 10(a) and 10(b), this alone does not persuade us that Patent Owner’s claim construction for “adhesion layer” is correct. Simply put, the issue is not whether “adhesive paste” is coterminous with an “adhesion layer” as set forth in claim 10.¹⁰ Rather, what is dispositive to the correct claim

¹⁰ “In the absence of any evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings.”

construction is whether the record supports a conclusion that an “adhesive agent” such as an adhesive paste can be applied to a surface and thus *form* an “adhesion layer” as recited in each independent claim. As discussed below, the complete record supports such a finding. We therefore find that Patent Owner points to nothing in the claim language that supports a finding that an “adhesion layer” must be “pre-formed” as a solid sheet before it is adhered to the back surface of a wafer.

We next turn to the ’879 patent Specification, which also suggests strongly that an “adhesion layer” may be formed *in situ* on the back surface of a wafer and need not be pre-formed. The term “adhesion layer” appears multiple times in the “summary of the invention” in contexts similar to the claims, and its use supports a finding that an “adhesion layer” may be formed from an “adhesive agent” such as an epoxy or paste. Ex. 1001, 2:66–5:31.

Specifically, the ’879 patent discloses a method of manufacturing a semiconductor device including steps of forming a first and second insulating adhesion layer “on a back surface” of a first and second wafer, respectively. Ex. 1001, 4:21–44. In that method, the *adhesion layer* is adhered to the back surface of a semiconductor chip in advance when the chip is in the wafer state. *Id.* at 4:45–48; *see also id.* at 5:12–15 (setting forth a similar method where the adhesion layer is adhered to the back surface of a semiconductor chip in advance when the chip is in the wafer state). According to the ’879 patent, these methods have several advantages, including that “*the adhesive agent* does not overflow the space between the

CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG, 224 F.3d 1308, 1317 (Fed. Cir. 2000).

first and second semiconductor chips.” *Id.* at 4:54–56, 5:21–23 (emphasis added).

We find it significant that the ’879 patent refers to “the adhesive agent” with respect to “the above manufacturing method[s],” while the enumerated method steps include forming an adhesion layer, without expressly mentioning an “adhesive agent.” *Id.* at 4:21–44, 4:61–5:11. Importantly, the ’879 patent does not say that an “adhesive agent” is not used in these methods. Rather, the ’879 patent uses language that implies that an “adhesive agent” is indeed present and that it “does not overflow the space between the first and second semiconductor chips.” *Id.* at 4:54–56, 5:21–23. Moreover, we observe that no other reference to adhesion or adhesives is mentioned with respect to these manufacturing methods. *Id.* at 4:21–5:27. Thus, we find that the ’879 patent discloses a direct relationship between “the adhesive agent” and the formation of the “adhesion layer” in the manufacturing methods disclosed in the preceding paragraphs. *Id.* at 4:23–25, 4:31–33, 4:54–56, 5:1–2, 5:21–23. In other words, the antecedent for “the adhesive agent” is the “adhesion layer” disclosed in the preceding paragraphs describing the method steps. *Id.* The reference to an “adhesive agent” in conjunction with an “adhesion layer” strongly supports our finding that an adhesion layer, as recited in the claims, may be formed from an adhesive agent. *Id.*; *see* Pet. Reply 4–5 (relying on this portion of the Specification as support for Petitioner’s claim construction).

Furthermore, when describing the semiconductor device structure, the summary of the invention uses the phrase, “in the case of using [a/the] thermo-compression sheet” immediately after discussing “a situation in which the excessively applied adhesive agent overflows the space between

the first and second semiconductor chips.” Ex. 1001, 3:22–35, 4:3–16. We agree with Petitioner (Pet. Reply 5) that the phrase, “in the case of using [a/the] thermo-compression sheet,” implies that an adhesion layer can be formed using *either* a thermo-compression sheet or an adhesive agent, so long as the adhesion layer is adhered to the back surface of the semiconductor chip. Ex. 1001, 3:22–35, 4:3–16.

Additionally, the ’879 patent describes in both of its preferred embodiments that a thermo-compression sheet is provided as an adhesion layer. Ex. 1001, 6:47–52; 11:29–32. Similar to the description of the preferred embodiments, the abstract discloses that “[a] first semiconductor chip is produced by affixing a thermo-compression sheet to the back surface of a wafer.” *Id.* at code (57). The claims, however, are not limited to a thermo-compression sheet as an adhesion layer. We find it significant that, in contrast to the abstract and description of the preferred embodiments, the claims of the ’879 patent use the broader term, “adhesion layer,” rather than a narrower term, such as “thermo-compression sheet.”

In the absence of patentee lexicography or disavowal, it would be improper to limit the scope of the term “adhesion layer” to a pre-formed solid sheet consistent with Patent Owner’s proffered construction. *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (“Absent lexicography or disavowal, we do not depart from the plain meaning of the claims.”); *In re Am. Acad. Of Sci. Tech Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (“We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification.”).

We find no lexicography or disavowal that would limit the scope of the term “adhesion layer” to a pre-formed layer as argued by Patent Owner, or a thermo-compression sheet. The Specification does not limit an adhesion layer to a thermo-compression sheet. Rather, a thermo-compression sheet is merely disclosed as *an example* of an adhesion layer. Our finding is strongly supported by the description of Embodiment 2: “The thermo-compression sheet 6 *is provided as an adhesion layer* for holding the second semiconductor chip 22 on the first semiconductor chip 21.” Ex. 1001, 11:30–32 (emphasis added). Our finding is also supported by the description of Embodiment 1: “The second semiconductor chip 2 is mounted on the circuit formed surface of the first semiconductor chip 1 through a thermo-compression sheet (adhesion layer) 6 so that its back surface is adhered to the thermo-compression sheet 6.” *Id.* at 6:48–52. We find that use of the parenthetical “(adhesion layer)” when describing Embodiment 1 has the same meaning as “as an adhesion layer” when describing Embodiment 2. *Id.* at 6:48–52; 11:30–32. In both instances, the term “adhesion layer” is describing the role of the thermo-compression sheet, and “adhesion layer” is not being defined here as the thermo-compression sheet embodiment.

Patent Owner argues that the Specification distinguishes an adhesion layer from an adhesive. According to Patent Owner, “[a]dhesives are not adhered as a layer but are applied to adhere other surfaces together as the adhesives dry and cure.” PO Resp. 24 (citing Ex. 1001, 2:18–43). We find that argument unpersuasive as it is insufficiently supported. The portion of the Specification relied on by Patent Owner does not state that an adhesion layer cannot be formed by applying an adhesive agent to a surface. Rather,

that portion of the Specification speaks to only two circumstances: one where “the amount of the adhesive agent is excessive” and one where “the amount of adhesive agent is too small.” Ex. 1001, 2:18–43. The evidence relied on by Patent Owner does not state that the adhesive agent does not form a layer if it is applied in the correct amount.

Moreover, Patent Owner’s argument is inconsistent with the extrinsic evidence showing formation of an adhesion layer. *See* Ex. 1003, 9:15–26 (disclosing that a fluid B-stageable epoxy adhesive can be rolled on as a layer prior to cure); *id.* at 6:3–4 (“During rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid”); *see also* Ex. 2014 ¶ 50 (Patent Owner’s expert testifying that “[p]astes and other adhesives, adhesive agents, adhesive layers or other material that are dispensed onto a substrate or chip back *are formed into a layer over time* as they harden through curing.” (emphasis added)).¹¹ This evidence, along with a plain reading of the claims, supports a finding that applying an “adhesive agent” such as an epoxy or paste can form a layer that adheres, i.e., an “adhesion layer.”

Patent Owner directs us to the Specification’s disclosure that “instead of providing the thermo-compression sheet 6 in advance when the first semiconductor chip 1 is in the wafer state, an insulating paste made of epoxy resins, etc. may be applied onto the circuit board 5 before the first semiconductor chip 1 is mounted on the circuit board 5.” Ex. 1001,

¹¹ Contrary to Patent Owner’s argument (PO Resp. 24), the cited testimony supports Petitioner’s claim construction, not Patent Owner’s. Pet. Reply 7. Mr. Elenius did not say that a hardened layer of paste or other adhesive is not an adhesion layer.

9:24–28. Patent Owner argues that this passage discloses an epoxy paste “instead of an adhesion layer.” PO Sur-reply 6 (emphasis omitted). We disagree. The passage discloses a layer of epoxy paste *instead of a thermo-compression sheet*. Both alternatives may be considered an “adhesion layer,” which is not mentioned in the passage.¹² Contrary to Patent Owner’s arguments (*id.* at 4, 6), the absence of an express disclosure that a layer of epoxy paste may be used as the adhesion layer is not enough to exclude it from the scope of the claim term. *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (“[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal.”). Silence regarding alternative embodiments is not a disavowal. *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1357 (Fed. Cir. 2004) (“the applicant’s choice to describe only a single embodiment does not mean that the patent clearly and unambiguously disavowed other embodiments”); *see also Luminara*, 814 F.3d at 1353 (“The standards for finding lexicography and disavowal are ‘exacting.’” (citing *GE Lighting*, 750 F.3d at 1309)).

Patent Owner argues that construing “adhesion layer” as limited to a pre-formed solid sheet is necessary to achieve the ’879 patent’s “primary goal” of preventing overflowing or underfilling the back surface of a chip with adhesive. PO Resp. 21; PO Sur-reply 4. Again, we disagree. The ’879

¹² We acknowledge that the Specification discloses that paste may be applied to the circuit board, rather than to the back surface of a semiconductor wafer, as recited in the claims. *Compare* Ex. 1001, 9:24–28, *with id.* at 13:47–48 (claim 1: “forming a first adhesion layer on a back surface of a first wafer”). The Specification does not support Patent Owner’s argument (PO Sur-reply 6) that the term “adhesion layer” excludes a layer of epoxy paste.

patent discusses drawbacks associated with two known methods for bonding chips, “an adhesive agent (paste) potting method” and “a method using a thermo-compression sheet.” Ex. 1001, 2:12–52. With the first method, the adhesive agent may possibly overflow or underfill the chip, while the thermo-compression sheet requires a two-step alignment process. *Id.* The disclosed invention addresses the potential overflow and alignment problems by forming an adhesion layer on the backside of a semiconductor wafer before it is diced into individual chips. *Id.* at 4:21–55. This method avoids potential overflowing of adhesive and simplifies the alignment process. *Id.* at 4:45–60. We agree with Petitioner that the ’879 patent avoids overflowing by forming the adhesive layer in the wafer state before dicing, not by using a sheet instead of an adhesive agent. Pet. Reply 6.

Moreover, the evidence does not persuade us that a pre-formed solid sheet is necessary to avoid the adhesive potentially overflowing the space between a chip’s surface and the surface on which it is mounted. As set forth above, the ’879 patent addresses two situations: one where “the amount of the adhesive agent is excessive [and] a large amount of adhesive agent spreads beyond the outer edge of the semiconductor chip” and another where “the amount of the adhesive agent is too small [and] a gap is produced between the semiconductor chips.” Ex. 1001, 2:18–41. The ’879 patent does not address a situation where the correct amount of adhesive agent is applied.

The problem of overflowing adhesive (i.e., *if* an excessive amount of adhesive agent is applied) is addressed by forming an adhesion layer on a back surface of a semiconductor wafer before it is diced into individual chips. *Id.* at 4:48–63, 5:15–27. There is no suggestion that a pre-formed

solid sheet is necessary to avoid that potential overflow problem. Our finding is supported by Mr. Elenius’s testimony that a “[person of ordinary skill in the art (POSITA)] seeing the term ‘adhesion layer’ would recognize that there are multiple methods of forming an ‘adhesion layer’ on the back surface of the semiconductor chip.” Ex. 2014 ¶ 43. At his deposition, Mr. Elenius agreed that the overflow problem occurs when the adhesive agent is in a wet form, not when it is in a dry form. Ex. 1037, 10:21–11:9. If the adhesive agent is allowed to dry or cure before a first chip is placed on a second chip, the overflow problem may be avoided. *Id.*

For these reasons, we construe the term “adhesion layer” to mean “a layer that adheres.”

D. Asserted Obviousness of Claim 7 Over Ball and Mostafazadeh

Petitioner asserts that claim 7 is unpatentable under § 103 over Ball and Mostafazadeh. Pet. 4, 25–42.

1. Overview of Ball (Ex. 1005)

Ball describes a multi-chip semiconductor device in which semiconductor chips (called dies) are vertically stacked on top of one another using a combination of face-down (flip-chip) and face-up (wire bond) assembly arrangements. Ex. 1005, Abstract, 1:8–12, Figs. 1–4. According to Ball, “flip-chip attachment” refers to a method of attaching a semiconductor chip (die) to a substrate in which “the die is inverted so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate (such as a printed circuit board).” *Id.* at 1:28–32. Ball describes state-of-the art attachment techniques as including “flip-chip attachment” and “wire bonding.” *Id.* at 1:47–50. For wire bonding, “[t]he die may be oriented either face up or face down (with its active

surface and bond pads either up or down with respect to the circuit board)
. . . although face up orientation is more common.” *Id.* at 2:16–20.

Figure 1 of Ball is reproduced below.

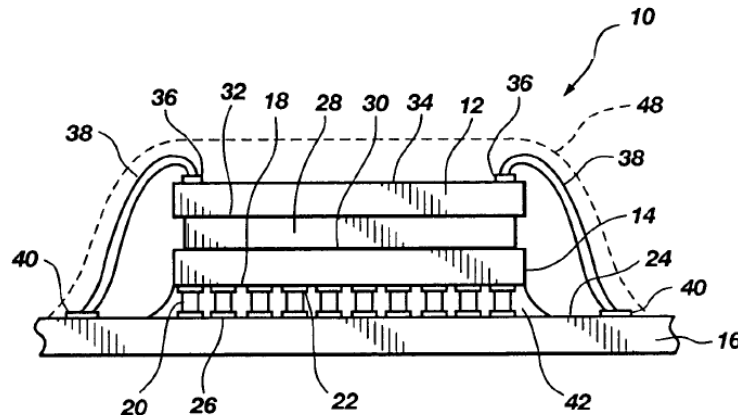


Fig. 1

Figure 1 shows a side plan view of an exemplary multi-die assembly of Ball with a flip-chip vertical stacking arrangement. *Id.* at 4:58–59, 5:1–18.

Ball describes that assembly 10 of Figure 1 comprises upper die 12, opposing lower die 14, and substrate 16. *Id.* at 5:2–6. Ball further describes that

Fabrication of the assembly 10 comprises providing the lower die 14 having a face surface 18 with at least one flip chip electric connection 20 (such as a C4 solder bump connection, conductive polymer bump or pin connection, these and other alternatives being known in the art, by way of example) extending from a bond pad or other terminal 22 on the lower die face surface 18. The flip chip electric connections 20 extend to a surface 24 of the substrate 16 in such a manner that the flip chip electric connections 20 physically (mechanically) attach to, and make electrical contact with, lead ends, trace ends, terminals or other electrical contact elements 26 in or on the surface 24 of the substrate 16.

and that “back side 32 of the upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over a lower die back side 30.” *Id.* at 5:6–20.

“An adhesive requiring a curing step, such as an epoxy, is preferred, although many adhesives known in the art are suitable.” *Id.* at 5:20–22.

“Substrate 16, if an insulative substrate, may itself be connected to a chassis or mother board by edge connections, bump connections, pin connections, or other conductive arrangements as known in the art.” *Id.* at 5:37–40.

2. Overview of Mostafazadeh (Ex. 1003)

Mostafazadeh describes a method of attaching an integrated circuit die to a support surface. Ex. 1003, Abstract. The method includes the step of forming an adhesive coating on a semiconductor wafer surface. *Id.* After the adhesive coating is dried, and the semiconductor wafer is diced to form several integrated circuit dies, each having an integrated circuit and an adhesive layer. *Id.* To attach the die to the support surface, the adhesive layer is placed in contact with a die attach pad and then cured. *Id.*

According to Mostafazadeh, “[g]luing and taping are conventional techniques” to attach an individual die (a fabricated integrated circuit die or chip) to a support structure (e.g., a connection substrate) during packaging. *Id.* at 1:22–25. Mostafazadeh indicates that, in conventional processes, glue is applied either directly to the support surface or directly to the die. *Id.* at 1:25–28. Mostafazadeh discusses disadvantages of applying glue to a support surface, whether in a pattern of glue drops or as a single large glue drop. *Id.* at 1:30–2:20, Figs. 1a–c. For example, with a pattern of glue drops, “there is no guarantee that the adhesive will cover the entire interface between the die and the support surface,” and “the strength of the resulting bond is not optimum.” *Id.* at 2:1–4, 2:12–15. Mostafazadeh states that, “[w]hile the single glue drop . . . may cover most or all of the interface, it tends to interfere with connections to the attached die by *jutting up around*

the die's edges.” *Id.* at 2:18–20 (emphasis added). Mostafazadeh indicates that, in a conventional taping method, tape is applied either to the back surface of a semiconductor wafer prior to dicing or to the die support surface, but discloses that “tape has the drawback of being relatively expensive.” *Id.* at 2:22–25.

In view of these shortcomings, Mostafazadeh aims to provide a method for attaching integrated circuit dies to support surfaces where “the adhesive is spread evenly and does not jut around the edges of the die.” *Id.* at 2:27–29. To accomplish this objective, Mostafazadeh discloses a method of attaching an integrated circuit die to a support surface by applying an adhesive coating to the entire surface of the semiconductor wafer before the wafer is diced to form individual dies. *Id.* at 3:5–14. Mostafazadeh notes that, in this process, “the adhesive is applied to the semiconductor wafer as opposed to an individual support surface or an individual die as is common in the conventional processes.” *Id.* at 8:2–5.

Figure 2 of Mostafazadeh is reproduced below.

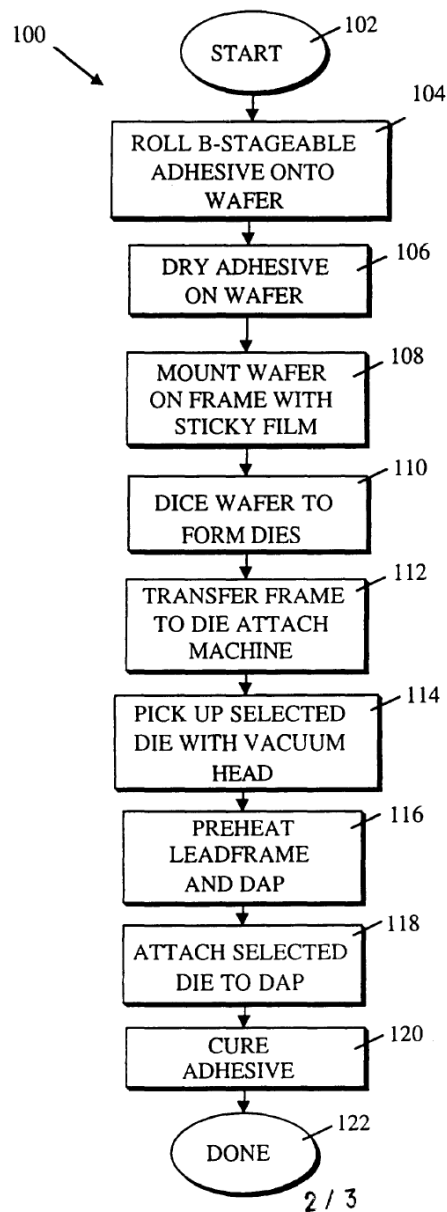


Figure 2 is a flowchart illustrating Mostafazadeh's method of attaching an integrated circuit¹³ die to a support surface. *Id.* at 4:15–16.

The process of Mostafazadeh's Figure 2 begins with step 102 in which a multiplicity of integrated circuits are fabricated on a semiconductor

¹³ Mostafazadeh refers to an integrated circuit as "IC." Ex. 1003, 9:20.

wafer. *Id.* at 5:22–23. Mostafazadeh describes that after fabrication of the ICs on the semiconductor wafer, an adhesive is then rolled onto a mounting surface (i.e., the surface opposite to the IC formed surface) of the wafer “to form an adhesive coating thereon in a rolling step 104.” *Id.* at 5:23–25. According to Mostafazadeh, the roller ends extend beyond a wafer surface during the application of the adhesive, which “[e]nsures that an adhesive coating . . . is formed over the entire wafer surface.” *Id.* at 6:29–7:1. Mostafazadeh further describes that “in some embodiments, the adhesive may be a B-stageable epoxy.” *Id.* at 3:22–23; *see also id.* at 5:25–26 (“Although a variety of adhesives can be used, B-stageable adhesives have been found to work well . . .”). Mostafazadeh explains that “a B-stageable adhesive is an adhesive that can be applied, dried without inducing full polymerization, reflowed (typically by heating the adhesive), and then cured to form more permanent bonds.” *Id.* at 5:28–6:1.

Mostafazadeh describes that “[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid.” *Id.* at 6:3–4. But “once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106,” which “turns the adhesive coating into a hard surface” if “the adhesive is good B-stageable epoxy.” *Id.* at 7:9–15 (emphasis added); *see also id.* at 7:22–23 (describing the dried adhesive coating as “hardened”).

After mounting the semiconductor wafer onto a film supported by a dicing frame, the wafer is then cut or diced into a multiplicity of dies or IC chips. *Id.* at 7:18–19, 7:29–8:1, Fig. 2 (steps 108, 110). After the dicing step, each die has an integrated circuit and an adhesive layer that includes

the dried adhesive coating. *Id.* at 8:1–2.

Figure 5c of Mostafazadeh is reproduced below.

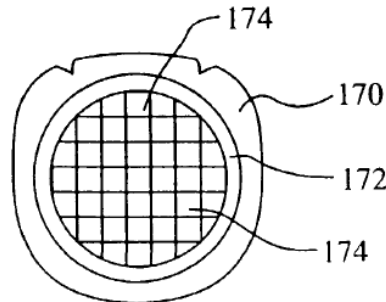


Fig. 5c

Figure 5c is a top view illustrating the result of dicing step 110 of Figure 2 forming a multiplicity of integrated circuit dies 174. *Id.* at 5:7–8. Figure 5c shows the result of dicing the semiconductor wafer to form several integrated circuit dies 174. *Id.* at 8:5–6.

According to Mostafazadeh, as the result of applying adhesive to a wafer, drying the coating to form a hardened layer, and dicing the wafer to the chip size, the adhesive layer on each individual chip is “*exactly the same size as the mounting surface of the die.*” *Id.* at 9:15–16 (emphasis added). Thus, “when the die is attached to its supporting surface” during packaging of individual chips, “the adhesive *does not extend beyond* a mounting surface of *the die.*” *Id.* at 9:16–18 (emphases added).

Figure 6a of Mostafazadeh is reproduced below.

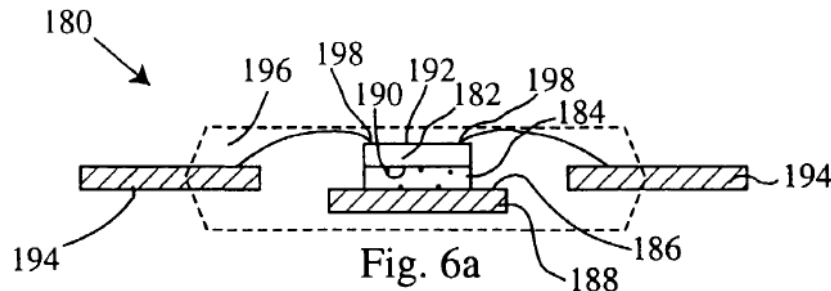


Figure 6a is a diagrammatic cross sectional side view of an exemplary packaged integrated circuit with a die attached to a support surface by an adhesive layer. *Id.* at 5:10–12.

Figure 6a shows a packaged integrated circuit 180, including die 182 is attached to support surface 188 via adhesive layer 184. *Id.* at 10:4–5. “The *adhesive layer 184* covers an entire mounting surface 190 of the selected integrated circuit die 182 and *does not extend beyond a boundary* of the mounting *surface 190*.” *Id.* at 10:6–8 (emphases added). Mostafazadeh further describes that “more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs).” *Id.* at 11:16–18.

3. *Motivation to Combine*

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball and Mostafazadeh to arrive at the subject matter recited in claim 7 with a reasonable expectation of success. Pet. 25–28, 36–37. More particularly, Petitioner contends it would have been obvious for a person of ordinary skill in the art to combine Ball’s teachings of stacking chips, with Mostafazadeh’s process for applying adhesive to create individual chips with adhesive backsides. *Id.* at 25–26, 36–37. Petitioner contends a person of ordinary skill would have been motivated to combine the teachings of Ball and Mostafazadeh for several reasons, including to provide a more efficient manufacturing process for multichip modules and to simplify the stacking process. *Id.* at 25–28.

Patent Owner argues that a person of ordinary skill would not have been motivated to combine Mostafazadeh with Ball because there would have been no reasonable expectation of success, and the combination would

not have resulted in a functioning semiconductor device.¹⁴ PO Resp. 26, 34–48. Specifically, Patent Owner asserts that Petitioner’s combination of Ball and Mostafazadeh would fail for multiple reasons and that Mostafazadeh does not describe multi-chip stacked mounting. *Id.* at 34–48.

Having considered the evidence and arguments, we determine that the preponderance of the evidence favors Petitioner. Petitioner demonstrates persuasively that a person of ordinary skill in the art would have had reasons to combine Ball’s stacked multichip module using flip-chip and wire bond connections with Mostafazadeh’s process for applying adhesive to create individual chips with adhesive backsides. Pet. 25–28. In particular, Petitioner shows that a person of ordinary skill in the art would have considered Mostafazadeh’s teaching of applying the adhesive to a wafer surface and then subsequently dicing the wafer in order to provide a more efficient manufacturing process for multichip modules and to simplify Ball’s process of stacking chips. *Id.*; *see KSR*, 550 U.S. at 417 (stating that the “mere application of a known technique to a piece of prior art ready for the improvement” suggests obviousness).

The teachings of both Ball and Mostafazadeh support Petitioner’s combination. Ball teaches a stacked multichip module using flip-chip and wire bond interconnections, where a lower chip is flip-chip connected to a substrate using metal bumps, and an upper chip is wire bond connected to the substrate. Ex. 1005, Abstract, 3:42–64, 4:58–59, 5:3–12, 5:18–20, 5:23–

¹⁴ For claim 7, Patent Owner cross-references its arguments for claim 1, including its arguments against a motivation to combine Ball and Mostafazadeh with U.S. Patent No. 5,323,060 (“Fogal”). *See* PO Resp. 25–26, 34–48. For claim 7, we limit our discussion to Ball and Mostafazadeh because Petitioner’s challenge of claim 7 does not rely on Fogal.

27, Fig. 1. Ball teaches that the upper chip is attached to the lower chip in a back-to-back arrangement with a layer of adhesive applied over a back side of the lower die. *Id.*

Mostafazadeh teaches a method for attaching integrated circuit dies to support surfaces. Ex. 1003, Abstract. In Mostafazadeh's method, an adhesive coating is formed on a surface of a semiconductor wafer, the adhesive coating is dried, and the semiconductor wafer is diced to form integrated circuit dies, each having an adhesive layer on its mounting surface, i.e., its back surface. *Id.* at 3:5–11, 5:20–25, 7:9–11, 7:29–8:2, Fig. 2 (steps 104–110). A selected die is then attached to an associated support surface by placing the adhesive layer of the selected die in contact with the associated support surface. *Id.* at 3:11–13, 8:10–12, Fig. 2 (steps 112–118).

We find that the express teachings of Mostafazadeh provide reasons to apply Mostafazadeh's method to Ball. First, Mostafazadeh teaches that “in the described process, the adhesive is applied to the semiconductor wafer *as opposed* to an individual support surface *or an individual die* as is common in the conventional processes.” Ex. 1003, 8:2–5 (emphasis added). Here, Mostafazadeh expressly teaches to substitute its die attachment method for a conventional die attachment method, as disclosed in Ball, where a layer of adhesive is applied over the back side of an individual die. *Id.*; Ex. 1005, Abstract, 3:54–59, 5:18–20. This express teaching of Mostafazadeh provides strong evidence that it would have been obvious to apply Mostafazadeh's die attachment method to Ball's multichip device. *See, e.g., SIBIA Neurosciences, Inc. v. Cadus Pharm. Corp.*, 225 F.3d 1349, 1359 (Fed. Cir. 2000) (reversing jury verdict of nonobviousness where “[t]he

express teachings in the art provide the motivation and suggestion to modify” the disclosed method and establish a strong case of obviousness).

Second, Mostafazadeh teaches that the disclosed die attachment method has several advantages. For example, Mostafazadeh teaches that “the adhesive is spread evenly and does not jut around the edges of the die.” Ex. 1003, 2:28–29. According to Mostafazadeh, the adhesive layer “covers the entire mounting surface” and “does not extend beyond the mounting area boundary.” *Id.* at 3:28–4:1; *see also id.* at 10:6–8 (same teaching with reference to Figure 6a). Similarly, Mostafazadeh teaches that the adhesive layer “is exactly the same size as the mounting surface of the die and is quite even.” *Id.* at 9:15–16.

We find that a person of ordinary skill in the art would have recognized Mostafazadeh’s disclosed advantages as directly applicable to the adhesive layer of Ball. For example, a skilled artisan would have recognized that it would have been advantageous to use Mostafazadeh’s process for forming an adhesion layer in making the device of Ball Figure 1 by preparing either upper die 12 or lower die 14 with adhesive layer 28 on its backside. Ex. 1003, 7:28–8:6, Fig. 5c; Ex. 1005, 5:18–20, Fig. 1. In this regard, we credit Dr. Suhling’s testimony that a person of ordinary skill in the art “would have recognized that [in Ball] the adhesive could be applied to the backside of the first chip or the backside of the second chip, and that either approach would allow the two chips to be mounted together.” Ex. 1002 ¶ 122; *see also id.* ¶ 125 (A person of ordinary skill in the art “would know that the adhesive must be applied to at least one of the chip’s backsides to mount them back-to-back.”).

We also credit Dr. Suhling’s testimony that it would have been obvious to combine Mostafazadeh’s process for forming chips with adhesive backsides with Ball’s multichip modules to make the chip stacking process more efficient. Ex. 1002 ¶¶ 127–128. We find the following testimony persuasive:

[G]iven the competitive pressures in the semiconductor industry to make smaller and cheaper devices, manufacturers were constantly looking for ways to eliminate process steps and lower costs. One way to do this is to incorporate as many manufacturing steps as possible during the wafer fabrication stage, before the chips are diced from the wafer. This approach is standard in semiconductor manufacturing and allows manufacturing steps to be applied in batch mode rather than building individual chips one at a time. For example, photolithography, ion implantation, etching, and chemical vapor deposition layer steps—to name a few—are applied over the entire wafer to create the integrate circuits.

Id. ¶ 122; *see also id.* ¶ 149 (a person of ordinary skill in the art “would also understand that chips with pre-formed adhesive backsides would eliminate process steps and save costs” when manufacturing multichip modules). The foregoing testimony demonstrates that Mostafazadeh’s method of applying adhesive to the backside of a wafer before dicing would have eliminated process steps and lowered costs by forming adhesive-backed chips “in batch mode” rather than forming an adhesive layer on each chip “one at a time.”

Id. ¶ 122; *see Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (“[A]n implicit motivation to combine exists [when] . . . the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.”).

We are similarly persuaded by the following testimony from Dr. Suhling:

[B]y the 1990s, the semiconductor industry faced increased pressure to streamline its manufacturing processes to produce higher performance, lower cost, and smaller semiconductor packages. . . . Manufacturers looked to integrate more processes during the wafer stage since it would result in hundreds of chips with the added feature rather than incorporating features on a chip-by-chip basis after the wafer was diced. Applying the adhesive to the backside of a wafer and dicing to produce hundreds of individual chips was a common-sense approach for simplifying the chip stacking process that was well known in the art.

Ex. 1002 ¶ 127 (citing Ex. 1005, 2:26–31). The foregoing testimony provides a persuasive reason for a person of ordinary skill in the art to have used Mostafazadeh’s wafer stage adhesive layer application process when manufacturing Ball’s multichip devices.

Petitioner and Dr. Suhling contend that “Mostafazadeh explicitly recommends using its adhesive process to efficiently build multichip modules, citing Mostafazadeh’s disclosure that “more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs).” Pet. 27; Ex. 1002 ¶ 128; Ex. 1003, 11:16–18; *see also* Pet. Reply 11 (arguing that Mostafazadeh “expressly recommended using its process” to form MCPs and MCMs “like those in Ball”). Patent Owner and Mr. Elenius dispute Petitioner’s contention, asserting that Mostafazadeh’s disclosure about MCPs and MCMs “appears to be limited to planar structures and not vertically stacked structures.” PO Resp. 44–45; Ex. 2014 ¶ 103; *see also id.* ¶¶ 65–70 (discussing planar MCPs and MCMs); PO Sur-reply 14–15

(arguing that “Mostafazadeh’s reference to MCM/MCPs was likely to be a planar structure”).

We find it unnecessary to resolve the parties’ dispute about whether Mostafazadeh’s reference to MCPs and MCMs includes vertically stacked structures. PO Resp. 44–48; Pet. Reply 18–20; PO Sur-reply 15. It does not matter whether Mostafazadeh teaches vertically stacked multichip structures because undisputed evidence establishes that they were known in the art and taught by Ball.

On this point, Dr. Suhling credibly testifies that MCPs or MCMs were known in the art well before 1998 as “3-D package[d]” devices with vertically stacked IC chips. Ex. 1002 ¶¶ 58–61 (discussing vertically stacked 3-D package devices described in various prior art references (citing Ex. 1025, 220; Ex. 1027, 110; Ex. 1028, Fig. 4A; Ex. 1029, 110, Fig. 3)). *See also id.* ¶¶ 96–98 (citing Ex. 1016¹⁵). In addition, Fogal describes multichip modules having a stacked chip arrangement. *See* Ex. 1004, 2:31–36, Fig. 1 (showing and describing a multichip module having “a plurality of z-direction multichip stacks”). Mr. Elenius agrees that Fogal describes vertically stacked MCMs. Ex. 1037, 39:13–24. Further, Mr. Elenius admits that Figure 14(a) of the ’879 patent describes “conventional vertically stacked multi-chip semiconductor devices.” Ex. 2001 ¶ 40 (citing Ex. 1001, 2:17–25).

Patent Owner does not dispute Petitioner’s showing that a POSITA knew of vertical MCMs and MCPs at the time of the invention of the ’879 patent. PO Sur-reply 14; Pet. Reply 18–19 (asserting that vertically stacked

¹⁵ Mr. Elenius refers to Exhibit 1014, but based on his description of the reference, we understand him as describing Exhibit 1016.

MCPs and MCMs were known in the art, citing Exs. 1004, 1005, 1016, 1028); Ex. 1002 ¶¶ 58–61 (discussing prior art vertically stacked MCPs and MCMs). As Patent Owner acknowledges (PO Sur-reply 15), the issue is *not* whether Mostafazadeh teaches vertically stacked chips, but whether a person of ordinary skill would have had a reasonable expectation of success in applying Mostafazadeh’s teaching about adhesive-backed chips to Ball’s vertically stacked multichip device.

Petitioner shows persuasively that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Mostafazadeh and Ball. Pet. 26–28. The evidence discussed above concerning reasons to combine supports a reasonable expectation of success. We are also persuaded by Dr. Suhling’s testimony that “the combination of Ball and Mostafazadeh would not require any modification of the multichip modules in Ball: rather, a [person of ordinary skill in the art] would realize that Mostafazadeh merely explains in more detail methods known in the art for creating chips with adhesive surfaces.” Ex. 1002 ¶ 128; *see also id.* ¶¶ 62–69 (describing prior art methods for applying adhesive to the backside of a wafer).

We are persuaded by Petitioner’s evidence of obviousness notwithstanding Patent Owner’s assertion that “Petitioner’s proposed combinations would fail.” PO Resp. 39.

First, Patent Owner argues that a person of ordinary skill in the art would have recognized that the combination would not result in a functioning semiconductor device because both “references teach an adhesive, which when applied to the back surface of the second semiconductor chip and mounted according to the method taught by

Mostafazadeh, could overflow.” PO Resp. 41, 42 (citing Ex. 2014 ¶ 121). According to Patent Owner, the downward pressure during mounting “could cause adhesive to squeeze out.” *Id.* at 41. We find that Patent Owner’s argument and the corresponding testimony of Mr. Elenius are speculative and do not outweigh Petitioner’s evidence of obviousness. The overflow issue was recognized and addressed by Mostafazadeh. Contrary to Patent Owner’s argument, Mostafazadeh provides explicitly that its adhesive layer “covers an entire mounting surface 190 of the selected integrated circuit dies 182 and *does not extend beyond a boundary of the mounting surface 190.*” Ex. 1003, 10:6–9 (emphasis added). Additionally, Mostafazadeh teaches that when “the adhesive layer is rolled on, it is exactly the same size as the mounting surface and is quite even. Thus, when the die is attached to its supporting surface the adhesive does not extend beyond the mounting surface of the die.” *Id.* at 9:15–18. Further, Mostafazadeh teaches that its process avoids the adhesive jutting around the edges of the die. *Id.* at 2:26–28. These teachings support that a person of ordinary skill in the art would have had a reasonable expectation of successfully applying Mostafazadeh’s die attachment method to Ball’s multichip device while avoiding adhesive overflow.

Next, Patent Owner argues that Petitioner’s combination would fail because, “[i]n a flip-chip configuration, the lower chip is mounted with bump connections to the substrate” and the heat applied to complete the bump connection “will cause the adhesive to cure and completely harden.” PO Resp. 42–43 (citing Ex. 2012, 147:4–22; Ex. 2014 ¶ 121). As Patent Owner acknowledges, however, that argument assumes that adhesive is formed on the back of the lower chip, rather than on the upper chip. *Id.* In

other words, Patent Owner’s argument addresses one adhesive application alternative—i.e., forming an adhesion layer on the back of the *lower* chip—which is not necessary to assemble Ball’s multichip device. Patent Owner then argues that, if adhesive is formed on the back of the *upper* chip, “[t]he adhesive on the second chip’s back could overflow from its edges during mounting when pressure is applied since it has not been cured.” *Id.* Patent Owner’s overflow argument, however, does not outweigh Petitioner’s evidence for the reasons discussed above.

Next, Patent Owner argues that Petitioner’s combination would fail because Mostafazadeh’s method “requires pre-heating or flash heating of the support surface,” which would cause the adhesive layer to reflow and “overflow past the edge of the chip and cover the bond pads.” PO Resp. 43–44 (citing Ex. 1003, 8:19–20, 9:10–13; Ex. 2014 ¶ 123). Patent Owner’s argument is not supported by Mostafazadeh, which teaches “*it is often desirable* to pre-heat the support surface to facilitate curing” (Ex. 1003, 8:19–20 (emphasis added)), but does not *require* pre-heating or flash heating, as argued by Patent Owner (PO Resp. 43). Furthermore, Mr. Elenius’s testimony about adhesive overflow is speculative. Ex. 2014 ¶ 123 (“This reflowing of the B-stageable epoxies *could* cause the adhesive used to overflow past the edge of the chip and cover the bond pads.”) (emphasis added). Mr. Elenius’s testimony does not take into account Mostafazadeh’s teachings that the adhesive “does not jut around the edges of the die” and “does not extend beyond the mounting area boundary.” Ex. 1003, 2:28–29, 3:28–4:1; *see also id.* at 9:15–16, 10:6–8 (similar teachings). Furthermore, Mr. Elenius does not account for Mostafazadeh’s teaching that various adhesives can be used, and “the drying, heating, pre-

heating, and flash heating temperature ranges may vary upon the adhesive used.” *Id.* at 10:20–26.

Patent Owner and Mr. Elenius underestimate the level of ordinary skill in the art and the skilled artisan’s ability to select materials, temperatures, and times that would have achieved a functional device. Viewing the evidence as a whole, we are persuaded that a person of ordinary skill in the art would have had a reasonable expectation of successfully combining Ball and Mostafazadeh while avoiding overflow of adhesive.

For the foregoing reasons, we find that Petitioner has established that it would have been obvious to combine the teachings of Ball and Mostafazadeh.

4. *Adhesion Layer*

The parties’ dispute focuses on limitation 7(c), which recites “forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer.” Ex. 1001, 15:4–6.

Petitioner asserts that

Ball explains that lower die 14 has adhesive layer 28 formed on its back surface 30 and states that ‘a backside 32 of upper die 12 is adhered to the lower die 14 with a layer of adhesive 28 applied over the lower die back side.’ . . . [but] does not describe how the adhesive is formed on the chip. Instead, Mostafazadeh provides these wafer fabrication details.

Pet. 34.

Petitioner sets forth where it believes Mostafazadeh discloses forming an adhesion layer on a back surface of a wafer as claimed. *Id.* at 35–36.

According to Petitioner, “the combination of Ball and Mostafazadeh teach ‘*forming an adhesion layer on a back surface of a wafer on which no circuit*

is formed, whereby a circuit is formed on a front surface of the wafer.” Id. at 36–37 (citing Ex. 1002 ¶¶ 145–150).

Patent Owner argues that Ball and Mostafazadeh do not disclose an “adhesion layer” and also do not disclose the claimed step of “forming an adhesion layer on a back surface of a wafer on which no circuit is formed” as set forth in limitation 7(c). PO Resp. 25–26.¹⁶

After considering both parties’ arguments, we determine that Petitioner meets its burden of proof for claim limitation 7(c). For the reasons discussed in the preceding subsection, we find that a person of ordinary skill in the art would have had reasons to combine Ball’s stacked die multichip module with Mostafazadeh’s process for applying adhesive at the wafer stage and then dicing to create individual chips with adhesive backsides.

Petitioner shows persuasively that Mostafazadeh teaches both an “adhesion layer,” and the step of “forming an adhesion layer on a back surface of a wafer on which no circuit is formed, whereby a circuit is formed on a front surface of the wafer,” as recited in claim limitation 7(c). Pet. 35–36. Our finding is supported by Mostafazadeh’s Figure 2, which shows step 104 as “roll B-stageable adhesive onto wafer” and step 106 as “dry adhesive on wafer.” Ex. 1003, Fig. 2. Our finding is further supported by Mostafazadeh’s disclosure that the process of Figure 2 begins at step 102 “with the fabrication of a semiconductor wafer having a multiplicity of integrated circuits formed thereon.” *Id.* at 5:20–23. Our finding is further

¹⁶ Patent Owner responds to Petitioner’s challenge to claim 7 by cross-referencing its arguments against Petitioner’s challenge to claim 1. See PO Resp. 26–48 (addressing claim 1).

supported by Mostafazadeh’s disclosure that, “[a]fter fabrication of the semiconductor wafer, an adhesive is then rolled onto a mounting surface of the wafer to form an adhesive coating thereon in rolling step 104.” *Id.* at 5:23–25; *see also id.* at 6:25–26 (“Once the adhesive has been coated on the roller 150, it is rolled onto the semiconductor wafer 160 in step 104.”). We also rely on Mostafazadeh’s disclosure that “once the adhesive has been applied to the wafer to form the adhesive coating in step 104, the adhesive coating is dried in a drying step 106.” *Id.* at 7:9–11. Mostafazadeh refers to the structure that results from these steps as an “adhesive layer.” *Id.* at Abstract, 1:3–5 (the invention “relates to rolling adhesives onto semiconductor wafers to form adhesive layers on semiconductor dies.”).

For the reasons discussed in Section II.C.1. above, we construe “adhesion layer” to mean “a layer that adheres.” Under our claim construction, Petitioner shows persuasively that Mostafazadeh discloses forming an “adhesion layer.” Pet. 35–36. According to Mostafazadeh, “B-stageable adhesives have been found to work well.” Ex. 1003, 5:25–28. Mostafazadeh explains that “a B-stageable adhesive is an adhesive that can be applied, dried without inducing full polymerization, reflowed (typically by heating the adhesive), and then cured to form more permanent bonds.” *Id.* at 5:28–6:1. Mostafazadeh discloses that, “[d]uring rolling step 104, the B-stageable adhesive will be in its initial fluid-based form of a paste, gel, or liquid.” *Id.* at 6:3–4. Mostafazadeh further discloses that “[w]hen the adhesive is a good B-stageable epoxy, [the drying] step 106 turns the adhesive coating into a hard surface, but the epoxy does not undergo a full polymerization.” *Id.* at 7:13–15. Mostafazadeh teaches that, after the drying step, the adhesive-coated semiconductor wafer is diced to form individual

dies, each with an adhesive layer. *Id.* at Abstract, 3:8–11, 7:18–8:8, Fig. 2 (steps 108, 110). An individual die is then attached to a support surface, such as a die attach pad, by placing the die’s adhesive layer in contact with the surface and curing the adhesive. *Id.* at Abstract, 3:11–15, 8:10–10:2. According to Mostafazadeh, the die attach process results in a secure bond between the die and the support surface. *Id.* at 8:10–10:2. In view of these disclosures, we find that Mostafazadeh’s adhesive layer is “a layer that adheres.”

Patent Owner argues first that Ball does not disclose an “adhesion layer” as recited in limitation 7(c). PO Resp. 28. We do not need to address Patent Owner’s argument because the Petition relies on Mostafazadeh, not Ball, as disclosing the “adhesion layer.” Pet. 35–36.

Patent Owner argues next that Mostafazadeh does not disclose an “adhesion layer.” PO Resp. 32–33. In particular, Patent Owner urges that Mostafazadeh’s adhesive “is rolled onto a semiconductor wafer 160 using a roller 150 to form an adhesive coating 164.” *Id.* at 32 (citing Ex. 1003, 3:7–8, 6:25–29, Fig. 4a). Patent Owner asserts that Mostafazadeh’s “adhesive is preferably a ‘B-stageable epoxy’” which “are liquid or semi-liquid viscous liquids that are applied by coating.” *Id.* Patent Owner relies on its claim construction of “adhesion layer,” arguing that Mostafazadeh’s “roll coated epoxy does not disclose an adhesion layer, which is a pre-formed layer that is adhered.” *Id.*

Patent Owner’s argument is premised on an incorrect claim construction. *See* Section II.C.1. As set forth above, the fully developed record supports a construction where an “adhesion layer” is “a layer that adheres.” And for the reasons discussed above, we find that Mostafazadeh

indeed discloses a layer that adheres, i.e., an “adhesion layer.” Pet. 35–36. Our finding is further supported by the testimony of Patent Owner’s expert, Mr. Elenius, that “[p]astes and other adhesives, adhesive agents, adhesive layers or other material that are dispensed onto a substrate or chip back are *formed into a layer over time as they harden through curing.*” Ex. 2014 ¶ 50 (emphasis added).

Patent Owner argues next that limitation 7(c) requires “that an adhesion layer extends to cover the entire back surface of the wafer” and that “if the adhesion layer only covers a portion of the back surface of the wafer, the limitation is not disclosed or taught.” PO Resp. 33 (citing Ex. 1001, 6:48–51; Fig. 1).

We disagree with Patent Owner. Limitation 7(c) merely recites that the adhesion layer is formed “on a back surface of a wafer on which no circuit is formed.” There is no language in claim 7 requiring the adhesion layer to cover the entirety of the wafer’s back surface. In our view, the phrase “a back surface of a wafer on which no circuit is formed” identifies the back side of the chip as opposed to the front side, where a circuit is formed. Ex. 1001, 15:4–6 (limitation 7(c)). Moreover, Patent Owner’s apparent reliance on Figure 1 of the ’879 patent to support such an implied construction falls short. Figure 1 is a two-dimensional cross-sectional view of a three-dimensional semiconductor device and thus cannot, on its own, establish whether adhesion layer 6 covers the entirety of the back surface of first semiconductor chip 1. Ex. 1001, 5:34–36. Even if Figure 1 were shown to evince adhesion layer formation over the entirety of the back surface, Patent Owner does not explain, and we do not discern, how Figure 1 should be construed as limiting on claim 7 because Figure 1 merely depicts

one of several embodiments.

Finally, even if Patent Owner’s construction were correct that limitation 7(c) requires “that an adhesion layer extends to cover the entire back surface of the wafer,” it is taught by Mostafazadeh. *See* Ex. 1003, 6:28–7:1 (disclosing that “the roller ends 154 are arranged to extend beyond a wafer surface 162 during the application of the adhesive” which “[e]nsures that an adhesive coating 164 *is formed over the entire wafer surface 162*” depicted in Figure 4a) (emphasis added). And consistent with our claim construction in Section II.C.1., Mostafazadeh’s fluid-based adhesive, e.g., a B-stageable epoxy, forms an “adhesion layer” after it is rolled onto a surface and dried to form a hard layer. Ex. 1003, 6:3–6, 7:9–16, 13:8–12 (claim 7: “the drying step turns the adhesive coating into a hard surface”); Ex. 2014 ¶ 50.

Based on our review of the Mostafazadeh disclosures relied on by Petitioner vis-à-vis the correct construction of the claim term “adhesion layer,” we find that Mostafazadeh discloses limitation 7(c). Pet. 34–36.

5. *Remaining Elements and Conclusion*

Based on Petitioner’s undisputed showings, we find that the combined teachings of Ball and Mostafazadeh teach or suggest the remaining limitations recited in claim 7. We furthermore find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner and explained above. Pet. 25–34, 37–42; *see* PO Resp. 25–48 (presenting arguments regarding limitation 7(c) and motivation to combine, but no other arguments regarding the remaining limitations).

We thus conclude that Petitioner has shown by a preponderance of the evidence that claim 7 is unpatentable over the combined disclosures of Ball and Mostafazadeh.

E. Asserted Obviousness of Claims 8 and 9 over Ball, Mostafazadeh, and Tsumura

Petitioner asserts that claims 8 and 9 are unpatentable under § 103 over Ball, Mostafazadeh, and Tsumura. Pet. 43–48.

1. Overview of Tsumura (Ex. 1007)

Tsumura describes a method for bonding a wire onto a material such as an aluminum electrode of a semiconductor chip. Ex. 1007, Abstract, 2:47–55. Tsumura describes multiple steps for its wire bonding method, including: (1) pulling a copper wire through a through-hole of a capillary tip; (2) forming a copper ball at the end of the copper wire; (3) lowering the capillary tip until the copper ball contacts an aluminum electrode of a semiconductor chip; (4) heating the metal ball so that it becomes “plastically deformed” and the copper ball and the aluminum electrode are bonded. *Id.* at 3:53–4:16.

2. Analysis

Petitioner explains that a person of ordinary skill in the art would have been motivated to combine Ball, Mostafazadeh, and Tsumura because Ball and Mostafazadeh related to semiconductor devices and methods of manufacturing semiconductor devices, and Tsumura describes “a method for bonding a wire onto a material, such as an aluminum electrode, of a semiconductor chip.” Pet. 43 (citing Ex. 1003, 2:27–29; Ex. 1005, 2:26–31; Ex. 1007, Abstract, 2:28–30). Petitioner contends that both Ball and Mostafazadeh disclose wire bonding but do not discuss it in detail, and thus,

a person of ordinary skill in the art would have consulted Tsumura for wire bonding details. Pet. 43. Petitioner contends that a person of ordinary skill in the art would have combined the three references because “Tsumura provides an efficient, straightforward wire bonding technique that complements the wire bonding steps already in Ball and Mostafazadeh and known in the art.” *Id.* Additionally, Petitioner contends that a person of ordinary skill in the art would have had a reasonable expectation of success combining the three references because they “teach compatible methods for manufacturing semiconductor devices.” *Id.* (citing Ex. 1002 ¶¶ 166–168).

Petitioner provides detailed analysis showing where it contends each additional limitation of dependent claims 8 and 9 is taught or suggested by Ball or Tsumura, and explains why a person of ordinary skill in the art would have been motivated to combine Ball, Mostafazadeh, and Tsumura. Pet. 43–48 (citing Ex. 1002 ¶¶ 170–180, 185). Patent Owner does not contest Petitioner’s challenge regarding claims 8 and 9 beyond its arguments submitted with respect to claim 7. PO Resp. 26.

Thus, based on Petitioner’s undisputed showings with respect to claims 8 and 9, we find that the combined teachings of Ball, Mostafazadeh, and Tsumura teach or suggest the remaining limitations recited in these claims. We furthermore find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner. Pet. 25–28, 43; PO Resp. 26 (relying solely on its claim 7 arguments to establish that claims 8 and 9 are “not obvious”).

We thus conclude that Petitioner has shown by a preponderance of the evidence that claims 8 and 9 are unpatentable over the combined disclosures of Ball, Mostafazadeh, and Tsumura.

F. Asserted Obviousness of Claims 1, 2, 10, 11, and 15 over Ball, Fogal, and Mostafazadeh

Petitioner asserts that claims 1, 2, 10, 11, and 15 are unpatentable under § 103 over Ball, Fogal, and Mostafazadeh. Pet. 67.

1. *Overview of Fogal (Ex. 1004)*

Fogal describes a multichip module having a stacked chip arrangement with bonding wires bonded between each chip and the module substrate. Ex. 1004, Abstract.

Figure 1 of Fogal is reproduced below.

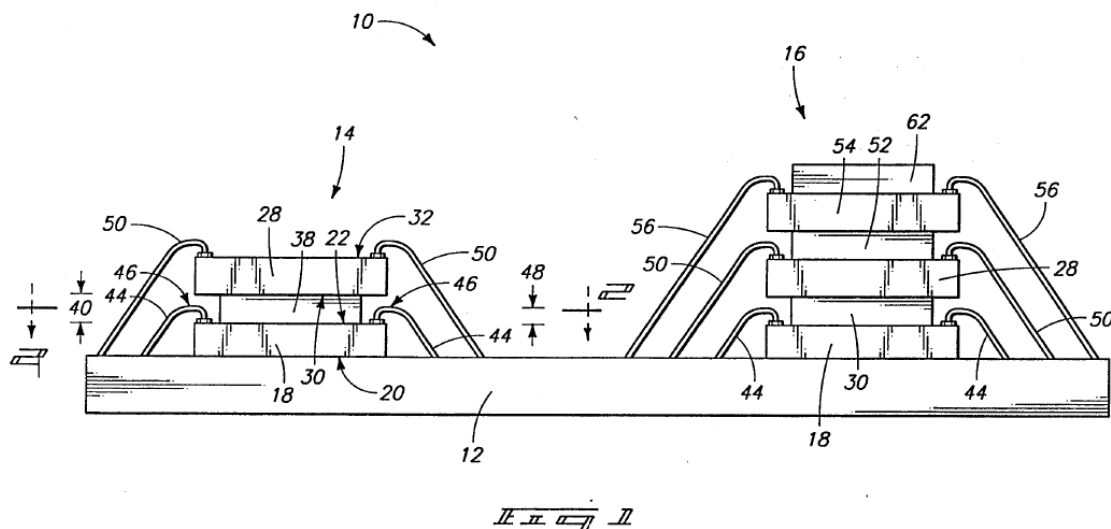


Figure 1 shows multichip module 12 with multichip stacks 14 and 16. *Id.* at 2:31–36. Stack 14 includes first chip 18 having opposed base and bonding faces 20 and 22, respectively. *Id.* at 2:36–38. Base face 20 is adhered to substrate 12 by means of an adhesive, such as “epoxy, thermoplastic materials, tape, tape coated with thermoplastic materials, etc.” *Id.* at 2:38–

41. Bonding face 22 includes bonding pads 26 that connect first chip 18 to substrate 12 via bonding wires 44. *Id.* at 2:41–43, 2:55–63. Second chip 28 includes bonding pads 36 that connect second chip 28 to substrate 12 via bonding wires 50. *Id.* at 2:44–48, 2:63–66. Fogal further describes that adhesive layer 38 is interposed between, and connects, bonding face 22 of first chip 18 to base face 30 of second chip 28. *Id.* at 2:49–54, 2:60–63. According to Fogal, “[e]xample materials for adhesive 38 include epoxies and tape.” *Id.* at 2:66–67.

2. *Motivation to Combine*

Petitioner argues that a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh to arrive at the subject matter of claims 1, 2, 10, 11, and 15 with a reasonable expectation of success. Pet. 49–51.

We have already addressed the parties’ arguments regarding whether a person of ordinary skill in the art would have been motivated to combine the teachings of Ball and Mostafazadeh, finding that Petitioner has established that such a motivation would have existed. *See* Section II.D.3., *supra*. The following discussion focuses on reasons for combining Ball and Mostafazadeh with Fogal.

Petitioner asserts that a person of ordinary skill in the art would have been motivated to combine the teachings of Fogal with those of Ball and Mostafazadeh because “Ball and Fogal solve the same issue: producing higher performance, lower cost, and smaller semiconductor packages, whereas Mostafazadeh provides a process that makes vertically stacking chips more efficient.” Pet. 49. According to Petitioner, “Ball states that wire bonding begins by ‘attaching a semiconductor die to the surface of a

printed circuit board with an appropriate adhesive” and that the skilled artisan would “look to Fogal and its figures for mounting the backside of a chip to a substrate.” *Id.* at 49–50.

Petitioner points out similarities between Ball and Fogal’s teachings of vertically stacking chips and asserts that the skilled artisan would have combined “Ball and Fogal with Mostafazadeh because Ball and Fogal teach vertically stacking chips and Mostafazadeh teaches a method for producing individual chips with adhesive back surfaces that would simplify the stacking processes in Ball and Fogal” for the same reasons Petitioner set forth with respect to the Ball and Mostafazadeh combination. Pet. 50–51 (referencing *id.* at 25–28).

Petitioner also asserts that the skilled artisan would have been “motivated to combine Mostafazadeh’s adhesive process with the method of manufacturing multichip modules taught in Ball and Fogal because using chips with adhesive backsides would make building multichip modules more efficient” and because “Mostafazadeh explicitly recommends doing so.” Pet. 51. According to Petitioner, the combination of Ball, Fogal, and Mostafazadeh would require no modification of the multichip modules in Ball and Fogal and that Mostafazadeh merely explains in more detail the methods already known in the art for creating chips with adhesive surfaces. *Id.* (citing Ex. 1002 ¶¶ 187–196).

Patent Owner argues that a person of ordinary skill in the art would not have combined Fogal with Ball and Mostafazadeh. PO Resp. 34–48. We find that a person of ordinary skill in the art would have recognized Mostafazadeh’s disclosed advantages as directly applicable to Fogal’s vertically stacked multichip module. For example, a skilled artisan would

have recognized that it would have been advantageous to use Mostafazadeh's process for forming an adhesion layer in making Fogal's vertically stacked multichip module. Ex. 1003, 7:28–8:6, Fig. 5c; Ex. 1004, 1:46–47; 2:31–43, Fig. 1.

In this regard, we credit Dr. Suhling's testimony that a person of ordinary skill in the art "would look to Fogal to mount the backside of the lowermost chip to the substrate, and then use the configurations in Ball to stack additional chips on top." Ex. 1002 ¶ 192; *see also id.* ("a POSITA would also understand that mounting a face-up chip to the substrate would provide additional creative options (beyond Ball's flip-chip interconnection) for configuring high-density multichip modules with multiple sizes of chips." (citing Ex. 1005, 3:33–37)).

Dr. Suhling's testimony concerning "additional creative options" is supported by Ball and Fogal. More particularly, Ball Figure 1 shows a chip stack configuration in which the lower chip is flip-chip connected to the substrate and the upper chip is face up and wire-bonded to the substrate. Ex. 1005, 5:3–27, Fig. 1. Fogal Figure 1 shows a chip stack configuration similar to Ball Figure 1, except that the lower chip is face up and both the upper and lower chips are wire-bonded to the substrate. Ex. 1004, 2:31–66, Fig. 1. We are therefore persuaded that a person of ordinary skill in the art would have understood that Ball's back-to-back chip stack and Fogal's dual face up chip stack are alternative ways of vertically stacking chips to increase integrated circuit density. Ex. 1002 ¶ 192. We are also persuaded by Dr. Suhling's testimony that these two interconnection techniques—flip-chip and face up with wire bonding—"were conventional in the art and well-known to a skilled artisan long before the '879 patent's 1998 priority date."

Id. (citing Ex. 1001, Figs. 13(a), (b); Ex. 1015, Fig. 27; Ex. 1016, Figs. 1–4). And Patent Owner agrees that the wire bonding and face-down bonding methods were conventional. PO Resp. 16 (citing Ex. 1001, 6:19–24; Ex. 2012, 46:8–48:24).

We also credit Dr. Suhling’s testimony that it would have been obvious to combine Mostafazadeh’s process for forming chips with adhesive backsides with Ball’s and Fogal’s multichip modules to simplify the chip stacking process. Ex. 1002 ¶ 193. We find the following testimony persuasive:

[B]y the 1990s, the semiconductor industry faced increased pressure to streamline its manufacturing processes to produce higher performance, lower cost, and smaller semiconductor packages. . . . Manufacturers looked to integrate more processes during the wafer stage since it would result in hundreds of chips with the added feature rather than incorporating features on a chip-by-chip basis after the wafer was diced. Applying the adhesive to the backside of a wafer and then dicing it to produce hundreds of individual chips was a common-sense approach for simplifying the chip stacking process that was well known in the art.

Id. (citing Ex. 1005, 2:26–31). This testimony provides a persuasive reason for a person of ordinary skill in the art to have used Mostafazadeh’s wafer stage adhesive layer application process when manufacturing Ball’s and Fogal’s multichip devices. As such, Petitioner persuasively demonstrates that Mostafazadeh’s method of applying adhesive to the backside of a wafer before dicing would have eliminated process steps and lowered costs. *See Dystar*, 464 F.3d at 1368.

Petitioner and Dr. Suhling contend that Mostafazadeh explicitly recommends using its adhesive process to efficiently build multichip

modules, citing Mostafazadeh's disclosure that "more than one integrated circuit die may be packaged in a single encapsulating package to form multichip packages (MCPs) or multichip modules (MCMs)." Pet. 51; Ex. 1002 ¶ 195; Ex. 1003, 11:16–18. Patent Owner and Mr. Elenius dispute Petitioner's contention, asserting that Mostafazadeh's disclosure about MCPs and MCMs "appears to be limited to planar structures and not vertically stacked structures." PO Resp. 44–45; Ex. 2014 ¶ 103; *see also id.* ¶¶ 65–70 (discussing planar MCPs and MCMs).

As we stated in Section II.D.3. above, we find it unnecessary to resolve the parties' dispute about whether Mostafazadeh's reference to MCPs and MCMs includes vertically stacked structures. It does not matter whether or not Mostafazadeh teaches vertically stacked multichip structures because undisputed evidence establishes that they were known in the art and taught by Ball and Fogal.

On this point, Dr. Suhling credibly testifies that MCPs or MCMs were known in the art well before 1998 as "3-D package[d]" devices with vertically stacked IC chips. Ex. 1002 ¶¶ 58–61 (discussing vertically stacked 3-D package devices described in various prior art references (citing Ex. 1025, 220; Ex. 1027, 110;¹⁷ Ex. 1028, Fig. 4A; Ex. 1029, 110, Fig. 3)). *See also id.* ¶¶ 96–98 (citing Ex. 1016¹⁸). In addition, Fogal describes multichip modules having a stacked chip arrangement and was filed more

¹⁷ The vertically stacked 3-D package illustrated in paragraph 60 of Dr. Suhling's appears on page 60 of Exhibit 1027. We thus treat Dr. Suhling's citation to page 110 as a typographical error.

¹⁸ Mr. Elenius refers to Exhibit 1014, but based on his description of the reference, we understand him as describing Exhibit 1016.

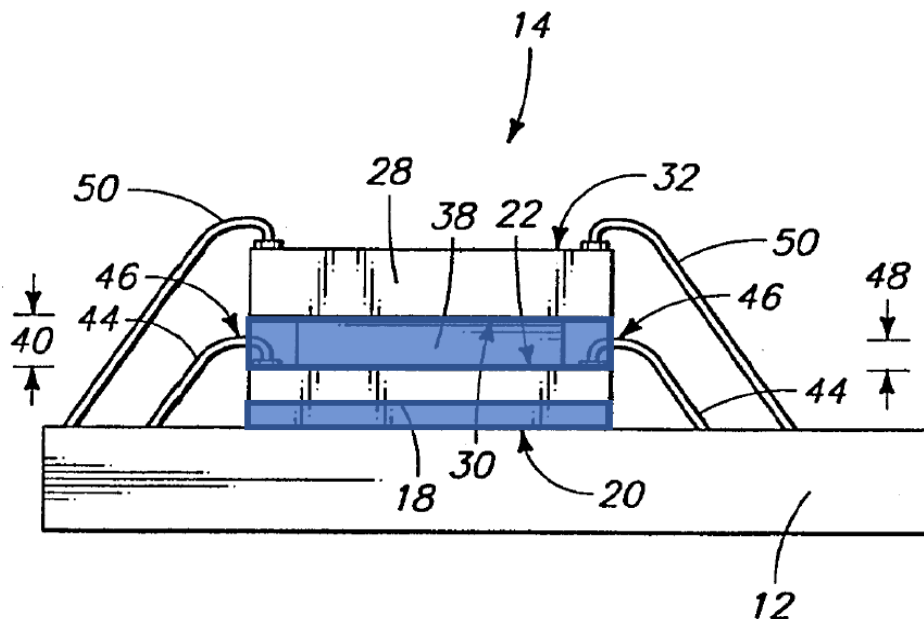
than a year prior to Mostafazadeh. *See* Ex. 1004, code (22). Mr. Elenius agrees that Fogal describes vertically stacked MCMs. Ex. 1037, 39:13–24. Further, Mr. Elenius admits that Figure 14(a) of the '879 patent describes “conventional vertically stacked multi-chip semiconductor devices.” Ex. 2001 ¶ 40 (citing Ex. 1001, 2:17–25).

Patent Owner does not dispute Petitioner’s showing that a POSITA would have known of vertical MCMs and MCPs at the time of the invention of the '879 patent. PO Sur-reply 14; Pet. Reply 18–19 (asserting that vertically stacked MCPs and MCMs were known in the art, citing Exs. 1004, 1005, 1016, 1028); Ex. 1002 ¶¶ 58–61 (discussing prior art vertically stacked MCPs and MCMs). As Patent Owner acknowledges (PO Sur-reply 15), the issue is *not* whether Mostafazadeh teaches vertically stacked chips, but whether a person of ordinary skill would have had a reasonable expectation of success in applying Mostafazadeh’s teaching about adhesive-backed chips to the vertically stacked multichip devices disclosed in Ball and Fogal.

Petitioner shows persuasively that a person of ordinary skill in the art would have had a reasonable expectation of success in combining Mostafazadeh, Ball, and Fogal. Pet. 26–28, 49–51. The evidence discussed above concerning reasons to combine supports a reasonable expectation of success. We are also persuaded by Dr. Suhling’s testimony that the “combination of Ball, Fogal, and Mostafazadeh would require no modification of the multichip modules in Ball and Fogal: rather, Mostafazadeh merely explains in more detail methods known in the art for creating chips with adhesive surfaces.” Ex. 1002 ¶ 196; *see also id.* ¶¶ 62–

69 (describing prior art methods for applying adhesive to the backside of a wafer).

We are persuaded by Petitioner’s evidence of obviousness notwithstanding Patent Owner’s assertion that “Petitioner’s proposed combinations would fail.” PO Resp. 34. Specifically, Patent Owner asserts first that “the combination of Mostafazadeh with Fogal fails because the resulting structure would deform the bond wires extending from the substrate to the top surface of the first (lower) semiconductor chip.” *Id.* at 35. For support, Patent Owner provides (*id.* at 36) the following annotated Figure 1 of Fogal, which Patent Owner states would be the result of combining Mostafazadeh with Fogal:



Fogal at Fig. 1 (annotated)

Patent Owner’s annotated Figure 1 of Fogal depicts a side view of a multichip module with what Patent Owner asserts would be Mostafazadeh’s adhesive applied under chip 28 depicted in blue, which Patent Owner asserts would deform the wire bonds on bond pads 26 (not numbered).

Patent Owner contends that “[t]he pre-applied adhesive backside under chip 28 [of Fogal’s Figure 1] would deform the wire bonds that are already made to the bond pads 26 located on the periphery of the top surface of first chip 18 and also obstruct the bond pads 26.” *Id.* We disagree with Patent Owner for several reasons.

First, Patent Owner’s argument is premised on a combination that Petitioner did not make. Petitioner relies on Fogal for its disclosure of mounting a first semiconductor chip on a wiring layer with its back surface facing the wiring layer. Pet. 53–54 (addressing limitation 1[c]). Such mounting does not implicate the upper surface of the first chip where the bond pads are located. *See* Ex. 1004, Fig. 1 (first chip 18 having back surface 20 contacting substrate 12, and bond pads located on top surface 22 of first chip 18). Petitioner does not rely solely on Fogal for stacking additional chips on the first chip. Instead, Petitioner asserts that a skilled artisan “would look to Fogal to mount the backside of the lowermost chip to the substrate *and then use the configurations in Ball to stack additional chips on top.*” Pet. 50 (emphasis added); Ex. 1002 ¶ 192. Petitioner explains how Ball discloses limitation 1[f] requiring mounting the second chip on the first chip with the second chip’s back surface facing the first chip, and how Fogal also teaches this limitation. Pet. 57 (referencing arguments for limitation 7[e]). Thus, Patent Owner’s argument does not address the entirety of the applied prior art and is not persuasive.

Moreover, Patent Owner’s argument is premised on Fogal’s first and second chips having identical sizes and face surface areas. Fogal, however, expressly contemplates “chips having different size surface areas . . . in a multichip module substrate.” Ex. 1004, 3:33–35. Thus, Petitioner persuades

us that the combination of Fogal with Ball and Mostafazadeh would not result in an adhesive layer 38 that obstructs the bond pads. Pet. Reply 20–21.

Patent Owner’s next argument pertaining to Fogal is that combining Fogal with Ball and Mostafazadeh would fail “because both references [Fogal and Ball] teach an adhesive, which when applied to the back surface of the second semiconductor chip and mounted according to the method taught by Mostafazadeh, could overflow.” PO Resp. 41, 42 (citing Ex. 2014 ¶ 121).¹⁹ According to Patent Owner, the downward pressure during mounting “could cause adhesive to squeeze out.” *Id.* at 41. We addressed this argument with respect to Ball and Mostafazadeh in Section II.D.3., *supra*. We find that the same analysis applies equally here to Fogal because Patent Owner’s argument and the corresponding testimony of Mr. Elenius are speculative and do not outweigh Petitioner’s evidence of obviousness. As we stated in Section II.D.3., Mostafazadeh recognized and addressed the overflow issue. Contrary to Patent Owner’s argument, Mostafazadeh explicitly provides that its adhesive layer “covers an entire mounting surface 190 of the selected integrated circuit dies 182 and *does not extend beyond a boundary of the mounting surface 190.*” Ex. 1003, 10:6–9 (emphasis added). Additionally, Mostafazadeh teaches that when “the adhesive layer is rolled on, it is exactly the same size as the mounting surface and is quite even. Thus, when the die is attached to its supporting surface the adhesive

¹⁹ Patent Owner’s argument regarding the “flip-chip configuration” (PO Resp. 42–43) is inapplicable to our discussion of this challenge because the methods of the challenged claims do not manufacture such a flip-chip configuration.

does not extend beyond the mounting surface of the die.” *Id.* at 9:15–18. Further, Mostafazadeh teaches that its process avoids the adhesive jutting around the edges of the die. *Id.* at 2:26–28. These teachings support that a person of ordinary skill in the art would have had a reasonable expectation of successfully applying Mostafazadeh’s die attachment method to Fogal’s multichip device while avoiding adhesive overflow.

Patent Owner and Mr. Elenius underestimate the level of ordinary skill in the art and the skilled artisan’s ability to select materials, temperatures, and times that would have achieved a functional device. Viewing the evidence as a whole, we are persuaded that a person of ordinary skill in the art would have had a reasonable expectation of successfully combining Fogal, Ball, and Mostafazadeh while avoiding overflow of adhesive.

In sum, we are not persuaded by Patent Owner’s arguments that Petitioner’s proffered combination would result in a non-functional device. And for the foregoing reasons, we find that Petitioner has established that it would have been obvious to combine the teachings of Ball and Mostafazadeh with those of Fogal.

3. *Adhesion Layer*

The parties’ dispute focuses on limitations 1(a), 1(d), 10(b), 15(a), and 15(d). Limitation 1(a) recites the step of “forming a first adhesion layer on a back surface of a first wafer on which no circuit is formed, a circuit being formed on a front surface of the first wafer.” Ex. 1001, 13:47–49. Limitations 1(d), 10(b), 15(a), and 15(d) are similar to limitation 1(a). Petitioner contends that Mostafazadeh teaches these limitations, relying on

the same arguments and evidence for limitations 1(a), 1(d), 10(b), 15(a), and 15(d) as it presents for limitation 7(c). Pet. 52, 56, 61, 63.

Patent Owner likewise relies on the same arguments for limitations 1(a), 1(d), 10(b), 15(a), and 15(d) as it presents for limitation 7(c). PO Resp. 25–34.²⁰

For the reasons discussed in Section II.D.4., we determine that Petitioner has met its burden of proof for limitations 1(a), 1(d), 10(b), 15(a), and 15(d).

4. *Remaining Elements and Conclusion*

We have reviewed Petitioner’s undisputed showings, and find that the combined teachings of Ball, Fogal, and Mostafazadeh teach or suggest the remaining limitations recited in claims 1, 2, 10, 11, and 15. We furthermore find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner as explained above. Pet. 25–28, 49–64; *see* PO Resp. 26–48 (presenting arguments regarding limitations pertaining to forming an adhesion layer and motivation to combine the references, but no other arguments regarding the remaining limitations of claims 1, 2, 10, 11, and 15).

We thus conclude that Petitioner has shown by a preponderance of the evidence that claims 1, 2, 10, 11, and 15 is unpatentable over the combined disclosures of Ball, Fogal, and Mostafazadeh.

²⁰ Patent Owner argues that Fogal’s epoxy and thermoplastic tape do not disclose an adhesion layer. PO Resp. 28–34. We do not need to address this argument because we, like Petitioner, rely on Mostafazadeh, not Fogal, to teach an adhesion layer. Pet. 52, 56, 61, 63.

G. Asserted Obviousness of Claims 3, 4, and 12

Petitioner asserts that claims 3, 4, and 12 are unpatentable over the combined teachings of Ball, Fogal, Mostafazadeh, and Tsumura. Pet. 64–67. Specifically, Petitioner contends that these references teach or suggest all limitations claims 3, 4, and 12, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the claims with a reasonable expectation of success. *Id.*; *see also id.* at 25–28, 49–51 (setting forth why a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh with a reasonable expectation of success); Ex. 1002 ¶¶ 244–248.

Patent Owner relies on its previous and unpersuasive arguments provided for claims 1 and 10 from which these claims depend. PO Resp. 48–49. We have reviewed Petitioner’s undisputed showings, and find that the combined teachings of Ball, Fogal, Mostafazadeh, and Tsumura teach or suggest the limitations recited in claims 3, 4, and 12. We furthermore find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner. Pet. 25–28, 49–51, 64–67; Ex. 1002 ¶¶ 244–248.

We thus conclude that Petitioner has shown by a preponderance of the evidence that claims 3, 4, and 12 are unpatentable over the combined disclosures of Ball, Fogal, Mostafazadeh, and Tsumura.

H. Asserted Obviousness of Claims 5, 6, 13, and 14

Petitioner asserts that claims 5, 6, 13, and 14 are unpatentable over the combined teachings of Ball, Fogal, Mostafazadeh, and Ma. Pet. 67–74.

Specifically, Petitioner contends that these references teach or suggest all limitations claims 5, 6, 13, and 14, and that a person of ordinary skill in the art would have been motivated to combine the teachings of these references to arrive at the claims with a reasonable expectation of success. *Id.*; *see also id.* at 25–28, 49–51 (setting forth why a person of ordinary skill in the art would have been motivated to combine the teachings of Ball, Fogal, and Mostafazadeh with a reasonable expectation of success); Ex. 1002 ¶¶ 250–263.

Patent Owner relies on its previous and unpersuasive arguments provided for claims 1 and 10 from which these claims depend. PO Resp. 49. We have reviewed Petitioner’s undisputed showings, and find that the combined teachings of Ball, Fogal, Mostafazadeh, and Ma teach or suggest the limitations recited in claims 5, 6, 13, and 14. We furthermore find that a person of ordinary skill in the art would have been motivated to combine those teachings of the relied upon prior art with a reasonable expectation of success as set forth by Petitioner. Pet. 25–28, 49–51, 67–68; Ex. 1002 ¶¶ 250–263.

We thus conclude that Petitioner has shown by a preponderance of the evidence that claims 5, 6, 13, and 14 are unpatentable over the combined disclosures of Ball, Fogal, Mostafazadeh, and Ma.

III. MOTION TO EXCLUDE

After timely filing its evidentiary objections (Paper 21), Petitioner moved to exclude four exhibits submitted by Patent Owner (Paper 32, “Mot. Exclude”). Petitioner moves to exclude:

- (1) Exhibit 2002 under each of the Federal Rules of Evidence (FRE)

402 and 901; and

(2) Exhibits 2003 and 2011 under FRE 402.

Mot. Exclude 1–4. Patent Owner responded (Paper 34, “Opp. Mot.”), agreeing to withdraw contested Exhibit 2015. Opp. Mot. 1. Petitioner filed a Reply to Patent Owner’s Opposition. Paper 35.

We do not rely on any of Exhibits 2002, 2003, 2011, or 2015 in reaching our determination that all of the challenged claims are unpatentable. Thus, Petitioner’s Motion to Exclude is dismissed as moot.

IV. CONCLUSION

Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable as summarized below:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
7	103(a)	Ball, Mostafazadeh	7	
8, 9	103(a)	Ball, Mostafazadeh, Tsumura	8, 9	
1, 2, 10, 11, 15	103(a)	Ball, Fogal, Mostafazadeh	1, 2, 10, 11, 15	
3, 4, 12	103(a)	Ball, Fogal, Mostafazadeh, Tsumura	3, 4, 12	
5, 6, 13, 14	103(a)	Ball, Fogal, Mostafazadeh, Ma	5, 6, 13, 14	
Overall Outcome			1–15	

V. ORDER

In consideration of the foregoing, it is

ORDERED that Petitioner has shown that claims 1–15 of the '879 patent are unpatentable; and

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed;

FURTHER ORDERED that because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES, LLC,
Patent Owner.

IPR2023-00073
Patent 6,352,879 B1

Before ELIZABETH M. ROESEL, JULIA HEANEY, and
SHELDON M. McGEE, *Administrative Patent Judges*.

McGEE, *Administrative Patent Judge*, concurring.

I write this additional concurring opinion to explain my initial views (expressed in my dissent from the Decision to Institute) regarding Patent Owner’s proffered claim construction for the term “adhesion layer” vis-à-vis the panel’s claim construction determination now—which I join—on the fully developed record.

My dissent at the institution stage focused largely²¹ on how the '879 patent distinguishes between the terms “adhesive agent” (embodied in the '879 patent as a “paste”), and an “adhesion layer” (embodied in the '879 patent as a “thermo-compression sheet”). DI 60–69. Based on the '879 patent's use of different terminology to describe these elements, and because the '879 patent discloses that there are problems with applying an “adhesive agent” that are different from the problems associated with applying the thermo-compression sheet embodiment of the “adhesion layer,” I was (and remain) of the view that “adhesion layer” is not coterminous with “adhesive agent” in the context of the '879 patent. What has changed for me on the complete record is that a preponderance of evidence supports a claim construction that the step of “forming a[n] . . . adhesion layer” as recited in each independent claim includes applying a liquid “adhesive agent,” e.g., a paste or an epoxy, to a surface and allowing it to *form a layer over time* as it hardens through curing. Ex. 2014²² ¶¶ 43, 50. I also agree with my colleagues that the intrinsic evidence supports that an “adhesion layer” may be formed *in situ* on the back surface of a wafer. *See* Section II.C.1. *supra*.

Furthermore, I have reached the determination on the complete record along with my colleagues that Patent Owner did not disavow applying an adhesive agent, e.g., a paste, to a surface (as disclosed in Mostafazadeh) that then forms into a layer over time, from the meaning of “forming a[n] . . .

²¹ My dissent also identified what I believed were—and still view as—Petitioner's i) mischaracterization of the record (DI 62–63) and ii) erroneous assertions regarding Patent Owner's construction (*id.* at 65–66).

²² This testimony was filed October 17, 2023, approximately five months after the Decision to Institute issued on May 15, 2023.

adhesion layer” as recited in each independent claim of the ’879 patent. Because of that lack of any clear disavowal, the plain and ordinary meaning of “adhesion layer” encompasses such layers that adhere.

At bottom, I view the terms “adhesive agent” and “adhesion layer” as distinct elements as set forth in the ’879 patent. But the fully developed record supports a conclusion that applying an “adhesive agent” to a surface and allowing it to form a layer over time *creates* a layer that adheres, i.e., an “adhesion layer.” Ex. 2014 ¶ 50. And that process is disclosed expressly in Mostafazadeh as relied on by Petitioner as discussed fully in the Final Written Decision.

IPR2023-00073
Patent 6,352,879 B1

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