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571-272-7822

Paper 9
Date: June 14, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

KATANA SILICON TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00105
Patent 6,731,013 B2

Before MINN CHUNG, JULIA HEANEY, and BRIAN D. RANGE, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1–25 (the "challenged claims") of U.S. Patent No. 6,731,013 B2 (Ex. 1001, "the '013 patent").

Katana Silicon Technologies LLC ("Patent Owner") timely filed a Preliminary Response. Paper 8 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314; 37 C.F.R. § 42.4(a). Under 35 U.S.C. § 314(a), institution of an *inter partes* review may not be authorized unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Upon consideration of the Petition and the Preliminary Response, we conclude that the information presented does not show there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of any challenged claim of the '013 patent. Accordingly, we do not institute an *inter partes* review.

II. BACKGROUND

A. Related Matters

According to the parties, the '013 patent is the subject of the following district court litigation: *Katana Silicon Techs. LLC v. Micron Tech., Inc.*, 1:22-cv-00282 (D. Idaho). Paper 6, 1; Pet. 2.

The '013 patent is one of several patents owned by Patent Owner that are challenged by Petitioner in various petitions for *inter partes* review, including in IPR2023-00071, IPR2023-00072, and IPR2023-00073.

B. Real Party-in-Interest

Petitioner identifies itself, Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC as the real parties-in-interest. Pet. 2. Patent Owner identifies itself as the sole real party-in-interest. Paper 6, 1.

C. The '013 Patent

The '013 patent describes a miniaturized semiconductor device having a chip size package (CSP) that includes a wiring substrate. Ex. 1001, 1:7–18, Abstract.

Figure 21 of the '013 patent is reproduced below.

FIG.21

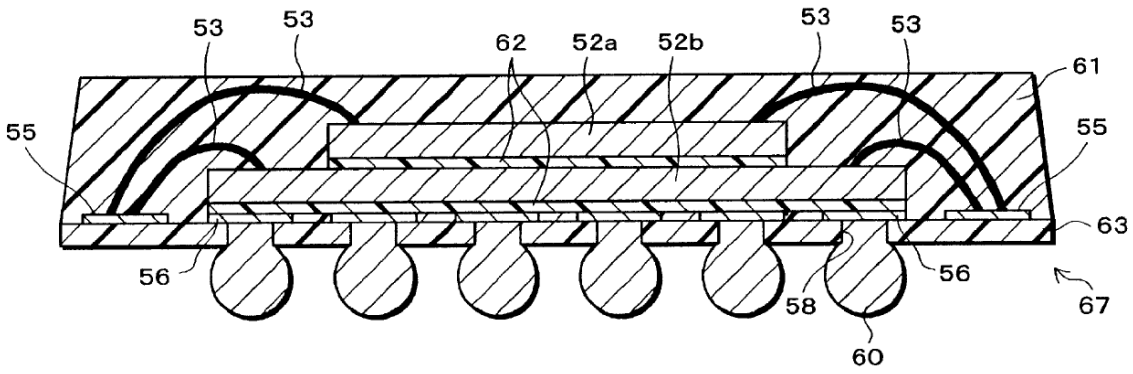


Figure 21 shows a cross-sectional view of a conventional semiconductor device having a stacked package. *Id.* at 2:19–20, 5:37–38.

The '013 patent describes that the stacked package shown in Figure 21 has semiconductor chips 52*a* and 52*b*, which are stacked together and mounted on wiring substrate 67. *Id.* at 2:19–22. Further, external connection terminal 60 is provided in a matrix pattern on land section 56 in the stacked package so that the external connection terminal 60 hangs down from the lower surface of the wiring substrate 67. *Id.* at 2:23–27.

The '013 patent describes the process of fabricating the stacked package shown in Figure 21 as follows:

> In the first place, the first semiconductor chip 52*b* is die-bonded on the wiring substrate 67 with its circuit forming surface facing upward, and then the second semiconductor chip 52*a* is die-bonded thereon.

> Thereafter, each semiconductor chip 52*a*, 52*b* is connected to the terminal section 55 of the wiring substrate 67 with an Au wire 53 by wire bonding. In addition, each semiconductor chip 52*a*, 52*b*, and the Au wire 53 are sealed with a resin sealing section 61 by transfer molding. Then, a solder ball is provided as the external connection terminal 60 on the land 56 by reflow soldering. The ball is used as the external connection terminal 60. The stacked package mentioned above is produced this way.

Id. at 2:31–43.

The ’013 patent further describes that during the wire bonding process, the wiring substrate is placed bottom side down on the stage of a wire-bonder and load is applied on terminal section 55 for bonding wire 53 to the terminal section. *Id.* at 3:21–23. According to the ’013 patent, because the bottom side of the substrate lies flat on the stage during wire bonding, the wire bonding load applied on terminal section 55 is held sufficiently by the stage and the wiring substrate does not deform or bend during wire bonding. *Id.* at 3:19–25.

When the substrate is a multi-layer wiring substrate, however, the load applied during the wire bonding process may deform the substrate, resulting in inadequate wire bonding and causing electrical connection failure between the semiconductor chip and the terminal section 55. *Id.* at 2:52–3:12.

Figure 22 of the ’013 patent is reproduced below.

FIG.22

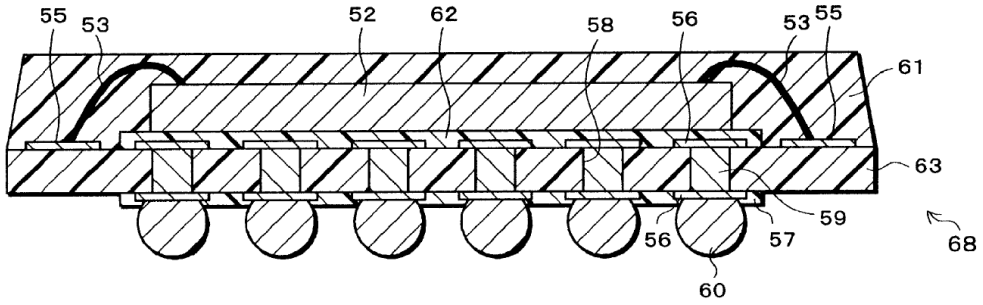


Figure 22 shows a cross-sectional view of a conventional semiconductor device with a multi-layer wiring substrate. *Id.* at 2:49–51, 5:39–40.

As illustrated in Figure 22, multi-layer wiring substrate 68 has a wiring pattern on both sides of the substrate—the side where the semiconductor chip is mounted (called side A) and the opposite, bottom side (called side B) where the external connection terminal 60 is formed. *Id.* at 2:49–57. The wiring pattern of side B is usually protected with solder resist 57. *Id.* at 2:57–58. According to the ’013 patent, in a multi-layer wiring substrate, the wiring pattern and solder resist on side B protrude downward, which may cause inadequate wire bonding during the wire bonding process. *Id.* at 3:26–32, 3:45–56.

Figure 23 of the ’013 patent is reproduced below.

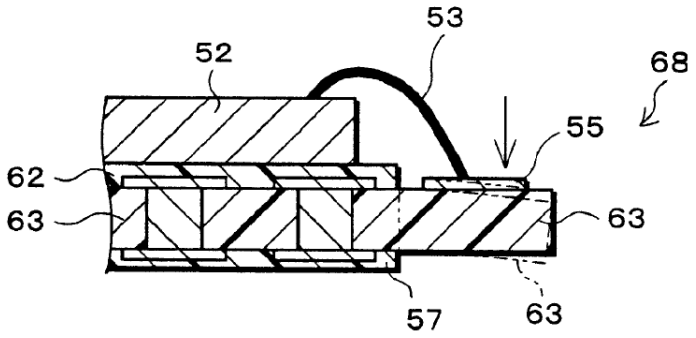


Figure 23 is a cross sectional view of a portion of a conventional semiconductor device with a multi-layer wiring substrate. *Id.* at 2:65–67, 5:41–43.

As illustrated in Figure 23, when a load is applied during wire bonding on terminal section 55 in the downward arrowhead direction (in the direction of thickness of insulating substrate 63), insulating substrate 63 deforms in the direction of thickness, which may result in inadequate wire bonding and cause electrical connection failure between the semiconductor chip and the terminal section 55. *Id.* at 3:3–12, 3:41–56.

Against this backdrop, the ’013 patent purports to provide a support pattern on side B of the substrate to prevent deformation of the substrate during wire bonding and improve wire bonding connection. *Id.* at 3:60–4:11.

Under the heading “SUMMARY OF THE INVENTION,” the ’013 patent states that “[t]he object of the present invention is to provide a wiring substrate, a semiconductor device, and a package stack semiconductor device, all with improved reliability of connection by suppressing occurrence of inadequate electrical connection.” *Id.* at 3:60–64. The ’013 patent further states that

> A wiring substrate of the present invention, in order to achieve the foregoing object, includes an insulating substrate, a terminal section for wire bonding or flip-chip connection and a *support pattern*, provided on a surface of the other side of the surface where the terminal section is provided, and on a position corresponding to the terminal section, for improving reliability of connection of wire bonding.
>
> Therefore, this structure can suppress deformation of the insulating substrate *by the support pattern*, even when the terminal section is pressed in wire bonding or other connection methods. As a result, *reliability of connection in wire bonding* or other connection methods, *can be improved* than conventionally.

Id. at 3:65–4:11 (emphases added).

Figure 1 of the ’013 patent is reproduced below.

FIG.1

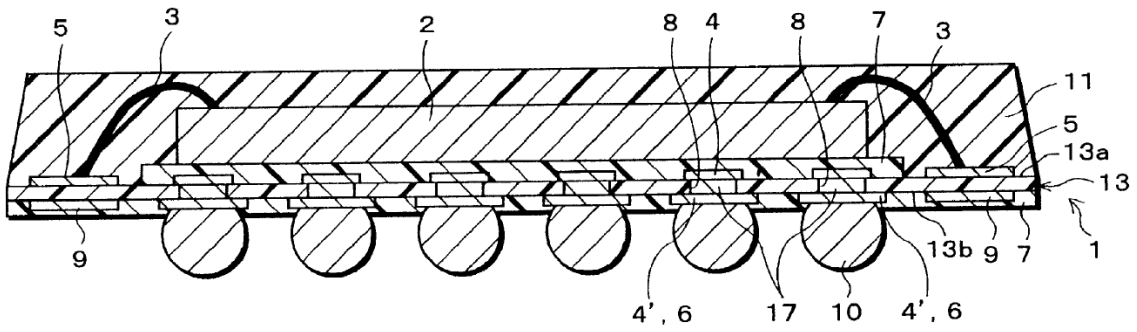


Figure 1 is a cross sectional view of an exemplary semiconductor device. *Id.* at 5:51–52.

As shown in Figure 1, the semiconductor device of this embodiment has wiring substrate 1, semiconductor chip 2, gold (Au) wires 3 (bonding wire section), solder resist 7, external connection terminal 10, and resin sealing section 11. *Id.* at 5:60–64. The semiconductor chip 2 is mounted on

the wiring substrate 1 by die bonding. *Id.* at 6:1–2. The Au wires 3 electrically connect terminal sections 5 on the wiring substrate 1 to the semiconductor chip 2 by wire bonding. *Id.* at 6:2–4. The '013 patent refers to the side of the wiring substrate on which semiconductor chip 2 is mounted as side A 13*a* and the other side of the substrate where external connection terminal 10 is formed as side B 13*b*. *Id.* at 6:8–13.

The '013 patent describes that on side B 13*b* of wiring substrate 1 support pattern 9 is provided corresponding to each of terminal sections 5 formed on side A 13*a*. *Id.* at 6:62–65. The '013 patent further describes that wiring pattern 4 is formed on side A 13*a* and wiring pattern 4′ on side B 13*b* to electrically connect terminal sections 5 to land sections 6. *Id.* at 6:29–57.

According to the '013 patent

> the wiring substrate 1 according to the present invention has the support pattern 9 which is provided on side B 13*b* corresponding in position to the terminal sections 5, taking into consideration the height of other sections such as the wiring pattern 4′ on side B 13*b*. This allows the load to be supported on the support pattern 9 in wire bonding, thus preventing deformation of the wiring substrate 13 (elastic deformation or plastic deformation) when applying a load.
>
> Therefore, the wiring substrate 1 allows a load to be accurately applied at a pre-set value, thereby ensuring electrical connection between the Au wires 3 and the terminal sections 5.

Id. at 7:46–59.

The '013 patent further describes that external connection terminal section 10 is provided in the form of solder balls by reflow soldering on land sections 6 on side B 13*b*. *Id.* at 6:8–14.

Figures 2(a) and 2(b) of the ’013 patent are reproduced below.

FIG.2 (a)

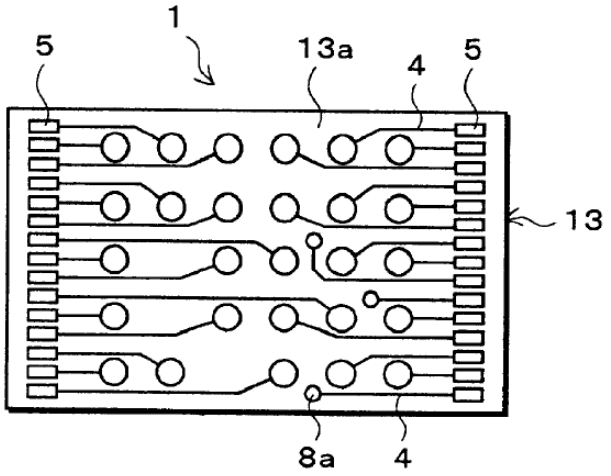
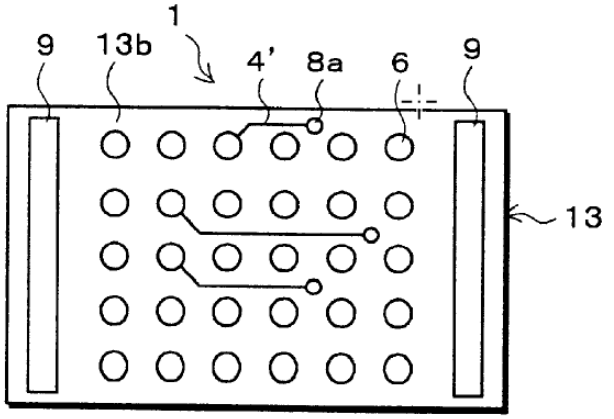


FIG.2 (b)



Figures 2(a) and 2(b) are explanatory drawings showing wiring substrate 1 used in the semiconductor device of Figure 1, where Figure 2(a) shows wiring pattern 4 on side A 13*a* of the substrate, and Figure 2(b) shows wiring pattern 4′ on side B 13*b*. *Id.* at 5:52–59.

As illustrated in Figure 2(a), wiring pattern 4 on side A 13*a* makes electrical connection between terminal sections 5 and land sections 6. *Id.* at 6:29–32. Figures 2(a) and 2(b) illustrate that wiring pattern 4 on side A 13*a* and wiring pattern 4′ on side B 13*b* make electrical connection between terminal sections 5 and land sections 6 via through hole sections 8*a*. *Id.* at 6:40–57.

D. Illustrative Claim

Of the challenged claims, claims 1, 6, 7, 8, 11, 13, 14, 18, and 20 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below.

> 1. A wiring substrate comprising:
>
> an insulating substrate;
>
> a terminal section, provided on a first surface of the insulating substrate, for making connection by wire bonding;
>
> a land section, provided on the insulating substrate, for an external connection terminal;
>
> wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section; and
>
> a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection, wherein the support pattern is not electrically connected to one of the terminal section and first and second land section.

Ex. 1001, 18:42–57.

E. Prior Art and Declaration Evidence

Petitioner cites the following references in its challenge to patentability:

U.K. Patent Application No. GB 2,093,401, published Sept. 2, 1982 (Ex. 1009, "Miura");

Japanese Patent Application No. 1997/121002, published May 6, 1997 (Ex. 1006, "Aoki");

U.S. Patent No. 5,639,695, issued June 17, 1997 (Ex. 1013, "Jones");

U.S. Patent No. 5,656,550, issued Aug. 12, 1997 (Ex. 1008, "Tsuji");

U.S. Patent No. 5,854,507, issued Dec. 29, 1998 (Ex. 1012, "Miremadi");

Japanese Patent Application No. 1999/8474, published Jan. 12, 1999 (Ex. 1010, "Tokuno"); and

U.S. Patent No. 6,028,358, issued Feb. 22, 2000 (Ex. 1011, "Suzuki").

Petitioner supports its challenge with a declaration from Jeffrey C. Suhling, Ph.D. (Ex. 1002, "Suhling Declaration"). Patent Owner has submitted a declaration from Peter Elenius (Ex. 2001, "Elenius Declaration") in support of Patent Owner's Preliminary Response.

F. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 5).

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–5, 11	103(a)[1]	Tsuji, General Knowledge of a Person of Ordinary Skill in the Art (POSITA)
1–6, 8–17	103(a)	Miura, Aoki, General Knowledge of a POSITA
7, 18, 19	103(a)	Miura, Tokuno, General Knowledge of a POSITA
20, 22–25	103(a)	Miura, Aoki, Suzuki, General Knowledge of a POSITA

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the '013 patent has an effective filing date prior to the effective date of the applicable AIA amendment, we refer to the pre-AIA version of § 103.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
21	103(a)	Miura, Aoki, Suzuki, Miremadi, General Knowledge of a POSITA
1, 2, 4, 6, 8, 11, 13, 14, 20	103(a)	Jones, General Knowledge of a POSITA

III. ANALYSIS

A. Level of Ordinary Skill in the Art

The level of ordinary skill in the pertinent art at the relevant time is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To assess the level of ordinary skill, we construct a hypothetical "person of ordinary skill in the art," from whose vantage point we assess obviousness and claim interpretation. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). This legal construct "presumes that all prior art references in the field of the invention are available to this hypothetical skilled artisan." *Id.* (citing *In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)).

Citing testimony from Dr. Suhling, Petitioner asserts that a person of ordinary skill in the art at the priority date of the '013 patent would have had

> i) a bachelor-level degree in electrical engineering, mechanical engineering, material science, or a related subject and five or more years of experience working in the field of semiconductor packaging; ii) a Master's-level degree in mechanical engineering, electrical engineering, material science, or a related

> field, and at least 1-3 years of experience in the design/development of semiconductor packages; or iii) a Ph.D.-level degree in mechanical engineering, material science, electrical engineering, or a related field, and at least some experience in the area of semiconductor packaging.

Pet. 16 (citing Ex. 1002 ¶¶ 32–37). Petitioner further states that "[a]dditional education may substitute for professional experience, and significant work experience may substitute for formal education." *Id.*

Patent Owner's declarant, Mr. Elenius, states that a person of ordinary skill in the art would have had "a bachelor's degree in electrical, mechanical or materials engineering and two to three years of experience in the design or development of semiconductor manufacturing, or the equivalent." Ex. 2001 ¶ 32. Mr. Elenius further states that "[a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education." *Id.*

Although the proposals for the level of skill in the art by the parties' declarants have differences in wording, we do not find the proposals to be materially different. For purposes of this Decision, we find no meaningful differences between the parties' respective definitions that would materially alter the outcome of this Decision. Thus, although we do not find the parties' proposals for the level of skill in the art to be materially different, for purposes of this Decision, based on our review of the '013 patent, the types of problems and solutions described in the '013 patent, and cited prior art, we adopt and apply Petitioner's definition of the level of ordinary skill in the art.

B. Claim Construction

In an *inter partes* review, we construe a patent claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2022). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the effective filing date of the patent application and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner asserts that a person of ordinary skill in the art would understand the claim term "a support pattern, provided on the second surface" recited in all challenged independent claims to mean a "support section that is part of a wiring pattern formed on the substrate's second surface." Pet. 14 (citing Ex. 1002 ¶¶ 119–121, 133–134).

At this time, Patent Owner does not dispute Petitioner's proposed construction of "a support pattern, provided on the second surface." *See generally* Prelim. Resp. For purposes of this Decision, we need not construe this term because the parties do not identify any material issue that would turn on the construction. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the

controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

As discussed in Section III.H.2 below, we determine that the claim term "a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection" requires the recited "support pattern" to be capable of "improving wire bonding connection." No other claim terms need to be construed expressly for purposes of this Decision.

C. Asserted Obviousness over Tsuji and General Knowledge of a Person of Ordinary Skill in the Art

Petitioner asserts that claims 1–5 and 11 are unpatentable under § 103(a) over Tsuji in view of the general knowledge of a person of ordinary skill in the art. Pet. 27–40. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 16–25. Based on the record presented and for the reasons discussed below, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that the subject matter of claims 1–5 and 11 would have been obvious over Tsuji in view of the general knowledge of a person of ordinary skill in the art.

1. Relevant Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any

differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations.[2] *Graham*, 383 U.S. at 17–18.

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")); *see Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366–67 (Fed. Cir. 2012) (holding that "some kind of motivation must be shown from some source, so that the [trier of fact] can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented [invention]")). Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

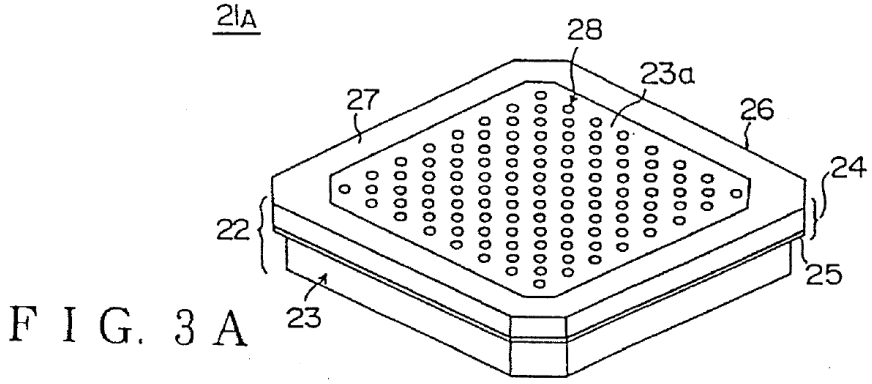
We analyze the asserted ground based on obviousness with the principles identified above in mind.

2. Overview of Tsuji (Ex. 1008)

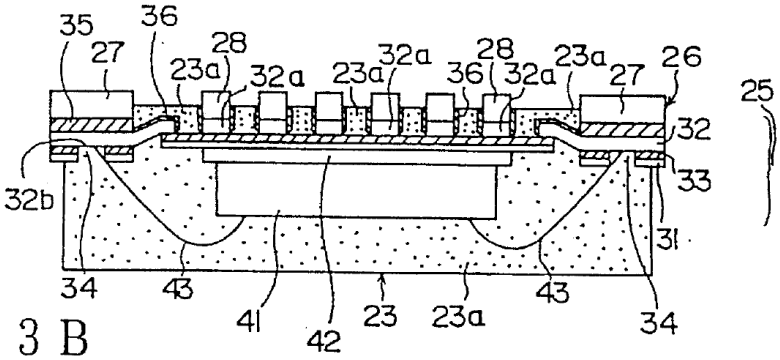
Tsuji describes a semiconductor device in which a plurality of outer terminals are arranged in a lattice formation on a flat surface. Ex. 1008, 1:15–17.

[2] The parties do not present arguments or evidence related to such secondary considerations. Therefore, secondary considerations do not constitute part of our analysis in this Decision.

Figures 3A and 3B of Tsuji are reproduced below.



F I G. 3 A



F I G. 3 B

Figure 3A is a perspective view showing a semiconductor device of a first embodiment of Tsuji with the bottom surface facing up, and Figure 3B is a sectional view of the semiconductor device of Figure 3A. *Id.* at 9:34–38.

Tsuji describes that outer terminal portion 26 at the bottom of the semiconductor device is made of a conductive metal, such as copper. *Id.* at 9:44–45. In a periphery of the outer terminal 26, frame terminal 27 is formed. *Id.* at 9:45–46. Inside the frame terminal 27, a number of pole terminal portions 28 are arranged in a lattice formation. *Id.* at 9:46–49.

As illustrated in Figure 3B, semiconductor chip 41 is mounted on base layer 31 through adhesive 42. *Id.* at 9:59–61.

Figures 16A and 16B of Tsuji are reproduced below.

FIG. 16A

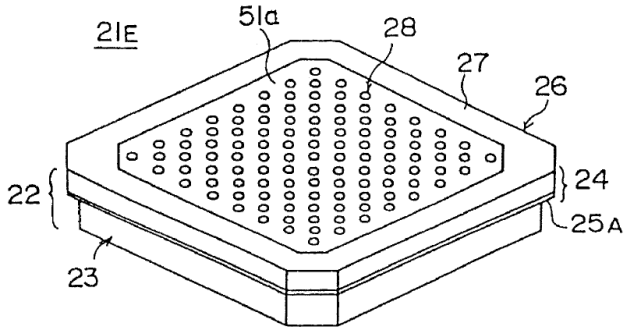
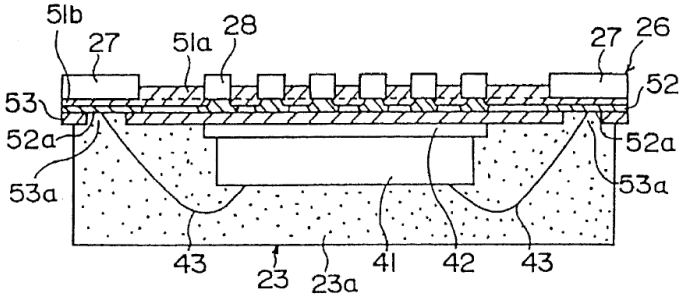


FIG. 16B



Figures 16A and 16B are schematic illustrations showing a semiconductor device of a second embodiment of Tsuji. *Id.* at 14:1–2. Figure 16A is a perspective view and Figure 16B is a sectional view. *Id.* at 14:2–3.

Outer terminal portion 26 comprises frame terminal 27 at the periphery and pole terminal portions 28 arranged in a lattice formation inside the frame terminal 27. *Id.* at 14:19–22. Semiconductor chip 41 is mounted on insulating layer 53 through adhesive 42. *Id.* at 14:38–40.

Tsuji describes that outer terminal portion 26 is fabricated using the same process for both the first and second embodiments. *Id.* at 11:13–55, 14:54–55, Figs. 6–8B. According to Tsuji, the process starts with a solid copper plate. *Id.* at 11:16–17. Then frame terminal 27 and pole terminal portions 28 are created with recess portions between them by using a half-etching process or by stamping a protrusion pattern using a press. *Id.* at 11:17–55. The result is a copper plate with frame terminal 27 connected to

pole terminal portions 28 through thin plate portions or recess portions. *Id.* at 11:25–27.

Figures 17A to 17D of Tsuji are reproduced below.

FIG. 17A

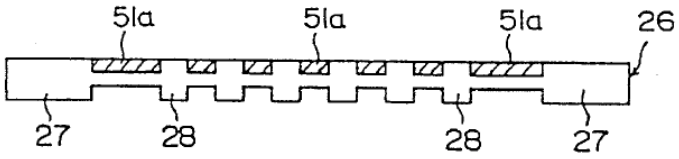


FIG. 17B

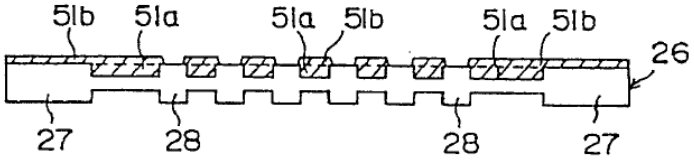


FIG. 17C

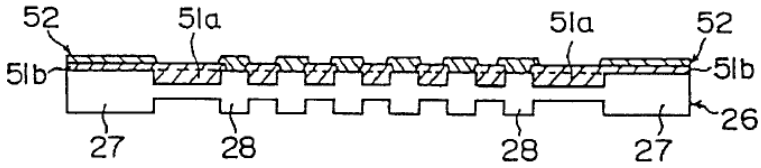
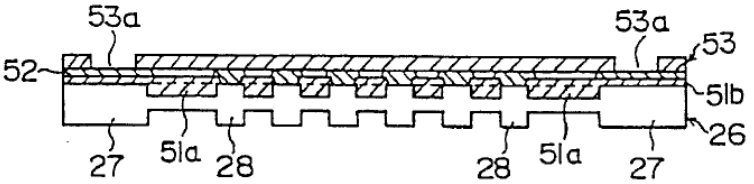


FIG. 17D



Figures 17A, 17B, 17C, and 17D are schematic illustrations showing the process of fabricating a semiconductor device of the second embodiment of Tsuji using outer terminal portion 26 created by the method described above. *Id.* at 14:52–55.

As shown in Figures 17A, 17B, 17C, and 17D, frame terminal 27 is electrically connected to pole terminal portions 28. *Id.* at 14:55–56. On the side of outer terminal portion 26 where a semiconductor chip is to be mounted, first insulating layer 51*a*, second insulating layer 51*b*, and third insulating layer 53 are formed. *Id.* at 14:64–15:20.

Figures 18A and 18B of Tsuji are reproduced below.

FIG. 18A

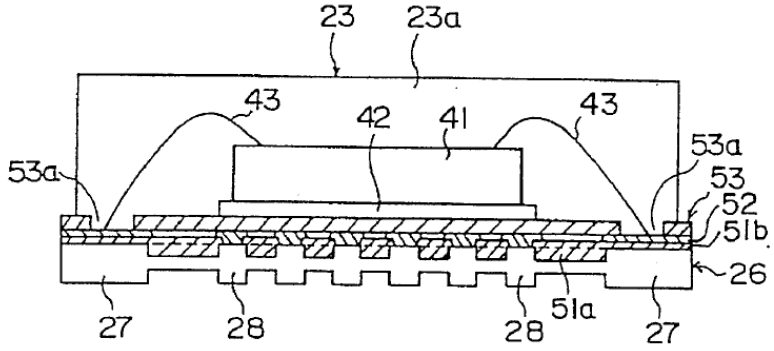
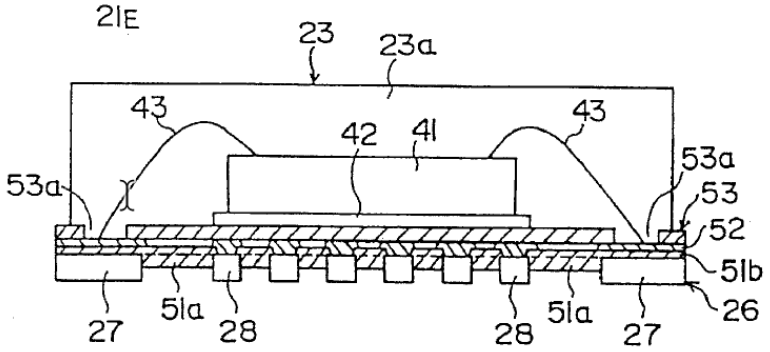


FIG. 18B



Figures 18A and 18B are sectional views showing a final step of producing a semiconductor device of the second embodiment. *Id.* at 15:21–22.

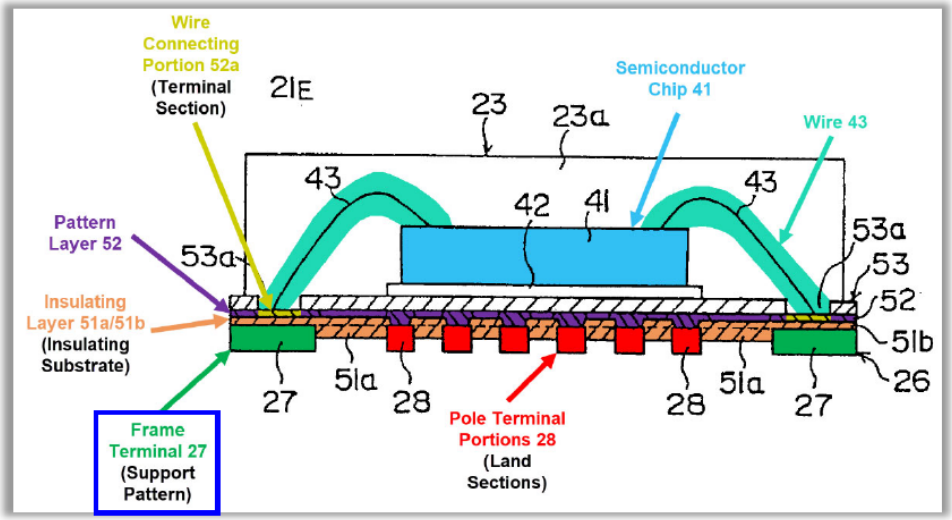
As shown in Figure 18A, semiconductor chip 41 is mounted on insulating layer 53 through adhesive 42. *Id.* at 15:22–25, Fig. 18A. At the point of the fabrication process depicted in Figure 18A, outer terminal portion 26 at the bottom or base of the semiconductor device is still a solid copper plate with frame terminal 27 electrically connected to pole terminal portions 28 through thin plate portions or recess portions. *Id.* at 11:25–27, 14:55–56; *see also id.* at 12:63–65 ("[T]he frame terminal 27 is still electrically connected to the pole terminal portions 28."). Tsuji describes that "[s]ubsequently, a bottom surface of the outer terminal 26 is etched in

order to separate each of the pole terminal portions 28 and the frame terminal 27," as shown in Figure 18B. *Id.* at 15:31–33, Fig. 18B. In other words, the thin plate portions or recess portions between frame terminal 27 and pole terminal portions 28 are removed (by etching) to electrically separate pole terminal portions 28 from each other and from frame terminal 27. *Id.* at 11:25–27, 14:55–56, 15:31–33, 15:46 ("the thin portions 29 are removed by . . . etching").

3. Claim 1

Petitioner contends that Tsuji in view of the general knowledge of a person of ordinary skill in the art teaches the preamble and all limitations of claim 1. Pet. 27–34. In particular, Petitioner relies on Tsuji's second embodiment depicted in Figure 18B as teaching nearly all limitations of claim 1.

Figure 18B of Tsuji as annotated by Petitioner is reproduced below.



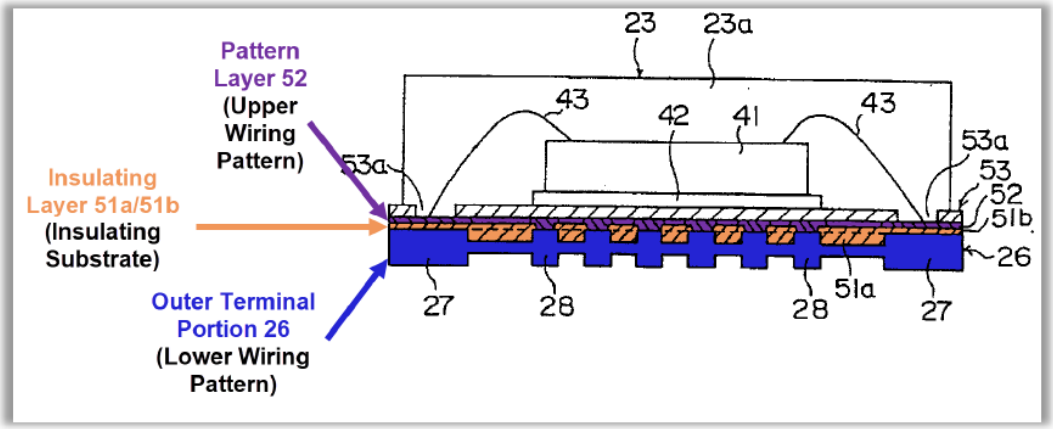
Tsuji - Figure 18B

Pet. 32. Annotated Figure 18B of Tsuji reproduced above illustrates Petitioner's alleged identification in Tsuji of certain limitations recited in claim 1. *Id.* at 27–30, 32–34.

For example, referencing Tsuji's Figure 18B, Petitioner draws an alleged correspondence between (1) Tsuji's insulating layer 51a/51b (annotated in brown) and the recited "insulating substrate" (Pet. 28); (2) Tsuji's pattern layer 52a/53a (annotated in yellow green) and the recited "terminal section, provided on a first surface of the insulating substrate" (*id.* at 29); (3) Tsuji's pole terminal portions 28 (annotated in red) and the recited "land section" (*id.* at 30); (4) Tsuji's pattern layer 52 (annotated in purple) and the recited "wiring patterns . . . provided on the first surface" (*id.* at 31); and (5) Tsuji's frame terminal 27 (annotated in green) and the recited "support pattern, provided on the second surface corresponding in position to the terminal section" (*id.* at 32–33).

Petitioner, however, does not identify in Tsuji's Figure 18B "wiring patterns . . . provided on . . . a second surface on the other side of the first surface" recited in claim 1. Instead, Petitioner goes back in time in Tsuji's process of fabricating the second embodiment device and relies on Figures 17A–17D and 18A of Tsuji as teaching this limitation. Pet. 31–32.

Figure 18A of Tsuji as annotated by Petitioner is reproduced below.



Tsuji - Figure 18A

Pet. 31. Annotated Figure 18A of Tsuji reproduced above, illustrates Petitioner's alleged identification in Tsuji of "wiring patterns . . . provided on . . . a second surface on the other side of the first surface" recited in claim 1. *Id.*

Specifically, Petitioner asserts that outer terminal portion 26 shown in Figure 18A of Tsuji (annotated in blue) discloses "wiring patterns . . . provided on . . . a second surface on the other side of the first surface," as recited in claim 1. Pet. 31–32 ("[O]uter terminal portion 26 . . . is the lower wiring pattern.") (citing Ex. 1008, 14:32–34, 10:7–10, 14:45–46, Fig. 18A). Petitioner further argues that outer terminal portion 26 shown in Figure 18A discloses "wiring patterns . . . provided on . . . a second surface . . . *for making electrical connection between the terminal section and the land section*" because "Tsuji's semiconductor device 21e in Figures 17A-17D and 18A shows that pattern layer 52 (*terminal section*) is on the opposite side of the insulating layer (*insulating substrate*) from outer terminal portion 26a (*land section*) and electrically connected at positions corresponding to the pole terminal portions 28." *Id.* at 32 (citing Ex. 1002 ¶¶ 151–155).

As discussed in Section III.C.2 above, at the point in time of the fabrication process of a semiconductor device depicted in Figure 18A (and Figures 17A through 17D), Tsuji's outer terminal portion 26 at the base of the semiconductor device is still a solid copper plate where frame terminal 27 is electrically connected to pole terminal portions 28 through thin plate portions or recess portions. Ex. 1008, 11:25–27, 14:55–56; *see also id.* at 12:63–65 ("[T]he frame terminal 27 is still electrically connected to the pole terminal portions 28."). In other words, Petitioner appears to argue that Tsuji's copper plate (terminal portion 26) at the base of the

semiconductor device depicted in Figure 18A with the thin plate portions electrically connecting frame terminal 27 to pole terminal portions 28 is the "wiring patterns . . . provided on . . . a second surface . . . for making electrical connection between the terminal section and the land section." Pet. 31–32.

The problem with Petitioner's argument is that Petitioner also relies on Tsuji's frame terminal 27 as disclosing claim 1's limitation reciting "a support pattern, provided on the second surface . . . wherein the support pattern is *not electrically connected* to one of the terminal section and first and second land section." *See* Pet. 32–34. As discussed above, Petitioner concedes that in Tsuji's Figure 18A, pattern layer 52 (the alleged "terminal section") is electrically connected to pole terminal portions 28 (the alleged "land sections"). *Id.* at 32. And in Tsuji's Figure 18A, frame terminal 27 is electrically connected to all pole terminal portions 28. Thus, in the unfinished interim semiconductor device of Tsuji's second embodiment depicted in Figure 18A, frame terminal 27 (the alleged "support pattern") is electrically connected to *all* of pattern layer 52 (the alleged "terminal section") and pole terminal portions 28 (the alleged "land sections") and, therefore, does not meet claim 1's limitation reciting "a support pattern, provided on the second surface . . . wherein the support pattern is *not* electrically connected to one of the terminal section and first and second land section."

Indeed, Patent Owner asserts that Tsuji does not disclose the "support pattern" limitation because "frame terminal 27 . . . is electrically connected to both the terminal section and land section contrary to this claim element." Prelim. Resp. 21–22.

Claim 1 is an apparatus claim, as are all other challenged independent claims. Claim 1, thus, requires each recited element within one apparatus. Tsuji, however, does not show that its semiconductor device relied on by Petitioner to compare to the challenged claims has frame terminal 27 *both* electrically connected and *not* electrically connected to pole terminal portions 28 at the same time. In other words, Tsuji's semiconductor device, as modified by Petitioner, may conceivably meet either the "wiring patterns" limitation or the "support pattern" limitation of claim 1, but not both.[3]

In his Declaration, Dr. Suhling opines that "'wiring patterns' on both sides of a substrate were well known in the field before the 2000 timeframe, and was admitted at least in the Background of the Invention section of the '013 patent." Ex. 1002 ¶ 155. Dr. Suhling does not explain, however, how "wiring patterns, respectively provided on the first surface and a second surface on the other side of the first surface, *for making electrical connection between the terminal section and the land section*" were well known in the field before the priority date of the '013 patent. *Id.* Nor does he explain how "wiring patterns . . . for making electrical connection between the terminal section and the land section" were admitted in the Background of the Invention section of the '013 patent. *Id.*

Petitioner contends that "wiring layers on both sides of a substrate capable of connecting terminals and lands were well within the general

[3] To be clear, we do not determine whether Tsuji discloses the "wiring patterns" limitation or the "support pattern" limitation. Our finding that Tsuji cannot disclose *both* of these limitations is sufficient to support our determination that Petitioner does not demonstrate a reasonable likelihood of prevailing in this ground.

knowledge of a POSITA as admitted by Applicant." Pet. 48–49 (citing Pet. § IV.C ("State of the Art and Applicant Admitted Prior Art")).

Although the Background of the Invention section of the '013 patent discusses a conventional semiconductor device with a multi-layer wiring substrate with wiring patterns on both sides of the substrate (Ex. 1001, 2:44–3:56), neither Dr. Suhling nor Petitioner identify any disclosure in the Background of the Invention section of the '013 patent of a conventional semiconductor device which includes wiring patterns on side A and side B "for making electrical connection between the terminal section and the land section," as required by claim 1. *See* Pet. 11–14 (§ IV.C); Ex. 1002 ¶¶ 151–155.

Based on the record before us, Petitioner has not set forth sufficient argument and supporting evidence to demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claim 1 would have been obvious over Tsuji in view of the general knowledge of a person of ordinary skill in the art.

4. Independent Claim 11

Petitioner acknowledges that claims 1 and 11 recite the identical "wiring patterns" and "support pattern" limitations. Pet. 34. For these limitations of claim 11, Petitioner cites to and relies on its analysis of claim 1 discussed above. *Id.* Thus, for the same reasons discussed above with respect to claim 1, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claim 11 would have been obvious over Tsuji in view of the general knowledge of a person of ordinary skill in the art.

5. Dependent Claims 2–5

Claims 2–5 depend from claim 1. Petitioner's arguments and evidence presented with respect to these dependent claims only address the additionally recited limitations of claims 2–5, and, therefore, do not remedy the deficiencies in Petitioner's analysis of claim 1 discussed above. *See* Pet. 38–40. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 2–5 are unpatentable under § 103(a) over Tsuji in view of the general knowledge of a person of ordinary skill in the art.

D. Asserted Obviousness over Miura, Aoki, and General Knowledge of a Person of Ordinary Skill in the Art

Petitioner contends that claims 1–6 and 8–17 are unpatentable under § 103(a) over the combination of Miura and Aoki in view of the general knowledge of a person of ordinary skill in the art. Pet. 41–62. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 25–42. Based on the record presented and for the reasons discussed below, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that the subject matter of claims 1–6 and 8–17 would have been obvious over Miura and Aoki in view of the general knowledge of a person of ordinary skill in the art.

1. Overview of Miura (Ex. 1009)

Miura describes a semiconductor element connected to leads, which are in turn connected to external terminals. Ex. 1009, code (57).

Figures 4 and 5 of Miura are reproduced below.

FIG.4

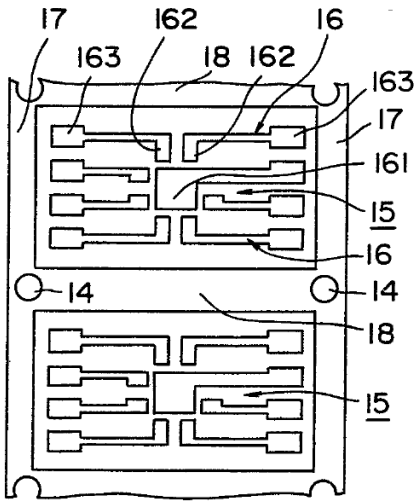
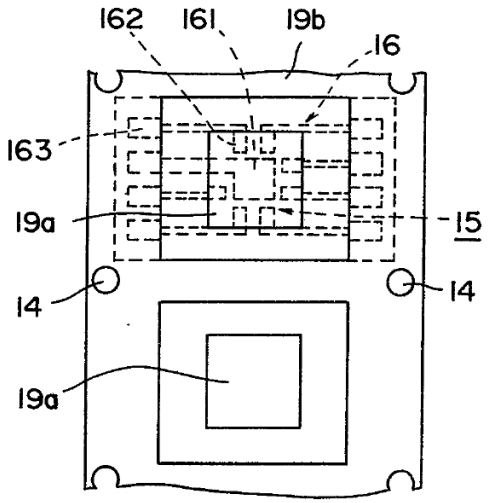


FIG.5



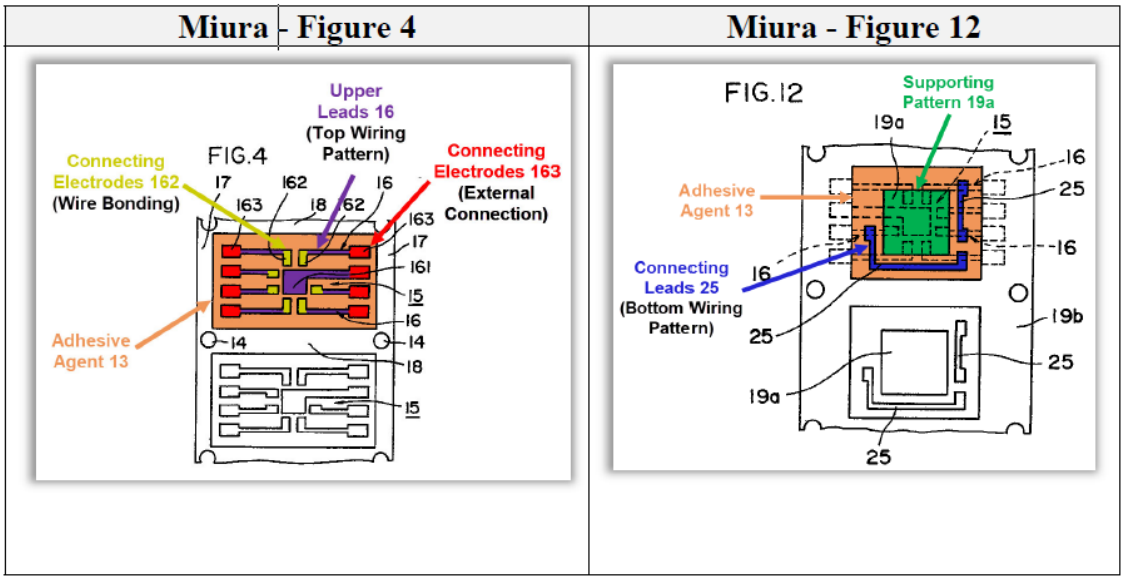
Figures 4 and 5 show views in the sequence of the steps for manufacturing a semiconductor device according Miura. Ex. 1009, 2:119–123.

Referencing Figure 4, Miura describes that each of leads 16 comprises connecting electrode 162 at one end and connecting electrode 163 at the other end. *Id.* at 4:3–9. Connecting electrode 162 is for wire bonding connection to a semiconductor element and connecting electrode 163 for making connection to an external terminal. *Id.* According to Miura, Figure 5 shows supporting patterns 19a and 19b formed on the other surface of the semiconductor device of Figure 4. *Id.* at 4:27–30. Miura describes that supporting patterns 19a and 19b are formed by etching copper film 12 (not shown), leaving a portion corresponding to the connecting electrodes 162 and 163. *Id.* at 4:33–36.

2. Claim 1

Petitioner contends that Miura in view of the general knowledge of a person of ordinary skill in the art teaches the preamble and all limitations of claim 1. Pet. 43–51.

Figures 4 and 12 of Miura as annotated by Petitioner are reproduced below.



Pet. 48. Annotated Figures 4 and 12 of Miura reproduced above illustrate Petitioner's alleged identification in Miura of certain limitations recited in claim 1. *Id.*

Referencing Miura's Figure 4, Petitioner alleges a correspondence between (1) Miura's connecting electrodes 162 (annotated in yellow) and the recited "terminal section, provided on a first surface of the insulating substrate" (*id.* at 44–45); (2) Miura's connecting electrodes 163 (annotated in red) and the recited "land section" (*id.* at 46–47); and (3) Miura's upper leads 16 (annotated in purple) and the recited "wiring patterns . . . provided on the first surface" (*id.* at 48).

Referencing Figure 12 of Miura, Petitioner contends that Miura's supporting pattern 19a (annotated in green) teaches or suggests "a support pattern, provided on the second surface corresponding in position to the terminal section," as recited in claim 1. Pet. 49–50.

Petitioner further contends that Miura's connecting leads 25 shown in Figure 12 of Miura teaches "wiring patterns . . . provided on . . . a second surface on the other side of the first surface, for making electrical connection between the terminal section and the land section," as recited in claim 1, because "[a]s shown in Figure 12, connecting leads 25 electrically connect the connecting electrodes 162 (*terminal sections*) with connecting electrodes 163 (*land sections*)." Pet. 48 (citing Ex. 1009, 4:28–39).

The cited portion of Miura, however, has no discussion of connecting leads 25, let alone a discussion suggesting that connecting leads 25 electrically connect the connecting electrodes 162 with the connecting electrodes 163. We reproduce an illustrative portion of Miura below.

> The other copper film 12 of the composite film 10 is etched as shown in Fig. 5. More specifically, supporting patterns 19a and 19b are formed on the other surface of the composite film by removing a portion of the copper film 12 by etching the same in a doughnut shape. More specifically, the supporting patterns 19a and 19b are formed by etching the other copper film 12 leaving a portion corresponding to the fixing pad 161 and the connecting electrodes 162 and 163 and a portion corresponding to the series patterns 17 and the connecting patterns 18 formed on one surface of the composite film.

Ex. 1009, 4:27–39.

Petitioner further contends that a person of ordinary skill in the art would have understood that "the upper and lower copper layers correspond to wiring patterns on both surfaces of the insulating substrate." Pet. 48

(citing Ex. 1002 ¶¶ 216–221). Petitioner, however, does not explain how Miura teaches or suggests "wiring patterns . . . provided on . . . a second surface on the other side of the first surface, for *making electrical connection between the terminal section and the land section*," as recited in claim 1.

> In the cited paragraph of his Declaration, Dr. Suhling states
>
> Miura additionally explains in reference to Figure 12:
>
> > The embodiment shown is structured such that not only the supporting patterns 19a and 19b but also the connecting leads 25 are formed by the use of the other copper film 12 of the composite film. Thus, a multilayered connection can be performed by using the inventive composite film. (Miura, 5:73-77.)

Ex. 1002 ¶ 220 (quoting Ex. 1009, 5:73–77). Again, Dr. Suhling does not explain how the cited portion of Miura discloses connecting leads 25 (the alleged "wiring patterns . . . provided on . . . a second surface on the other side of the first surface") "making electrical connection between" connecting electrodes 162 (the alleged "terminal section") and connecting electrodes 163 (the alleged "land section"), as required by claim 1.

Dr. Suhling further opines that "'wiring patterns' on both sides of a substrate were well known in the field before the 2000 timeframe, and was admitted at least in the Background of the Invention section of the '013 patent." Ex. 1002 ¶ 221. Petitioner similarly contends that "wiring layers on both sides of a substrate capable of connecting terminals and lands were well within the general knowledge of a POSITA as admitted by Applicant." Pet. 48–49 (citing Pet. § IV.C ("State of the Art and Applicant Admitted Prior Art")). For the reasons discussed above in Section III.C.3, we find

Petitioner's argument and Dr. Suhling's testimony unpersuasive and unsupported by evidence of record.

Based on the record before us, Petitioner has not set forth sufficient argument and supporting evidence to demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claim 1 would have been obvious over Miura and Aoki in view of the general knowledge of a person of ordinary skill in the art.

3. Independent Claims 6, 8, 11, 13, and 14

Petitioner acknowledges that claims 1, 6, 8, 11, 13, and 14 recite identical or nearly identical "wiring patterns" limitations. Pet. 52, 53, 54, 57, 58. For these limitations of claims 6, 8, 11, 13, and 14, Petitioner cites to and relies on its analysis of claim 1 discussed above. *Id.* Thus, for the same reasons discussed above with respect to claim 1, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claims 6, 8, 11, 13, and 14 would have been obvious over Miura and Aoki in view of the general knowledge of a person of ordinary skill in the art.

4. Dependent Claims 2–5, 9, 10, 12, and 15–17

Claims 2–5 depend from claim 1; claims 9, 10, and 12 depend from claim 8; and claims 15–17 depend from claim 14. Petitioner's arguments and evidence presented with respect to these dependent claims only address the additionally recited limitations of claims 2–5, 9, 10, 12, and 15–17, and, therefore, do not remedy the deficiencies in Petitioner's analysis of independent claims 1, 8, and 14 discussed above. *See* Pet. 58–62. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 2–5, 9, 10, 12, and 15–17 are unpatentable

under § 103(a) over Miura and Aoki in view of the general knowledge of a person of ordinary skill in the art.

E. Asserted Obviousness over Miura, Tokuno, and General Knowledge of a Person of Ordinary Skill in the Art

Petitioner contends that claims 7, 18, and 19 are unpatentable under § 103(a) over the combination of Miura and Tokuno in view of the general knowledge of a person of ordinary skill in the art. Pet. 62–74.

For independent claims 7 and 18, Petitioner concedes that claims 6, 7, and 18 recite the identical "wiring patterns" limitation and cites to and relies on its analysis of claim 6 discussed above. Pet. 68, 71. Thus, for the same reasons discussed above with respect to claim 6, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claims 7 and 18 would have been obvious over Miura and Tokuno in view of the general knowledge of a person of ordinary skill in the art.

Claim 19 depends from claim 18. For claim 19, Petitioner cites to and relies on its analysis of claim 12 discussed above. Pet. 74. Thus, for the same reasons discussed above with respect to claim 12, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claim 12 would have been obvious over Miura and Tokuno in view of the general knowledge of a person of ordinary skill in the art.

F. Asserted Obviousness over Miura, Aoki, Suzuki, and General Knowledge of a Person of Ordinary Skill in the Art

Petitioner contends that claims 20 and 22–25 are unpatentable under § 103(a) over the combination of Miura, Aoki, and Suzuki in view of the general knowledge of a person of ordinary skill in the art. Pet. 74–79.

For the "wiring patterns" limitation of independent claim 20, Petitioner cites to and relies on its analysis of independent claim 11 discussed above, applying Miura to the "wiring patterns" limitation of claim 11. Pet. 77. Thus, for the same reasons discussed above with respect to claim 11, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of independent claim 20 would have been obvious over Miura, Aoki, and Suzuki in view of the general knowledge of a person of ordinary skill in the art.

Claims 22–25 depend from claim 20. Petitioner's arguments and evidence presented with respect to these dependent claims only address the additionally recited limitations of claims 22–25, and, therefore, do not remedy the deficiencies in Petitioner's analysis of independent claim 20 discussed above. *See* Pet. 77–79. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 22–25 are unpatentable under § 103(a) over Miura, Aoki, and Suzuki in view of the general knowledge of a person of ordinary skill in the art.

G. Asserted Obviousness over Miura, Aoki, Suzuki, Miremadi, and General Knowledge of a Person of Ordinary Skill in the Art

Claim 21 depends from claim 20. In this asserted ground of obviousness, Petitioner adds the teachings of Miremadi to the combination of Miura, Aoki, and Suzuki in view of the general knowledge of a person of ordinary skill in the art and challenges claim 21 as obvious over the combination of Miura, Aoki, Suzuki, and Miremadi in view of the general knowledge of a person of ordinary skill in the art. Pet. 79.

Petitioner's arguments and evidence presented with respect to claim 21 only address the additionally recited limitations of claim 21, and,

therefore, do not remedy the deficiencies in Petitioner's analysis of independent claim 20 discussed above. *See* Pet. 79. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 21 is unpatentable under § 103(a) over Miura, Aoki, Suzuki, and Miremadi in view of the general knowledge of a person of ordinary skill in the art.

H. Asserted Obviousness over Jones and General Knowledge of a Person of Ordinary Skill in the Art

Petitioner contends that claims 1, 2, 4, 6, 8, 11, 13, 14, and 20 are unpatentable under § 103(a) over Jones in view of the general knowledge of a person of ordinary skill in the art. Pet. 79–94. Patent Owner disputes Petitioner's contentions. Prelim. Resp. 44–49. Based on the record presented and for the reasons discussed below, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that the subject matter of claims 1, 2, 4, 6, 8, 11, 13, 14, and 20 would have been obvious over Jones in view of the general knowledge of a person of ordinary skill in the art.

1. Overview of Jones (Ex. 1013)

Jones describes a ball-grid array (BGA) semiconductor package that includes a substrate attached to a support substrate. Ex. 1013, Abstract.

Figure 1 of Jones is reproduced below.

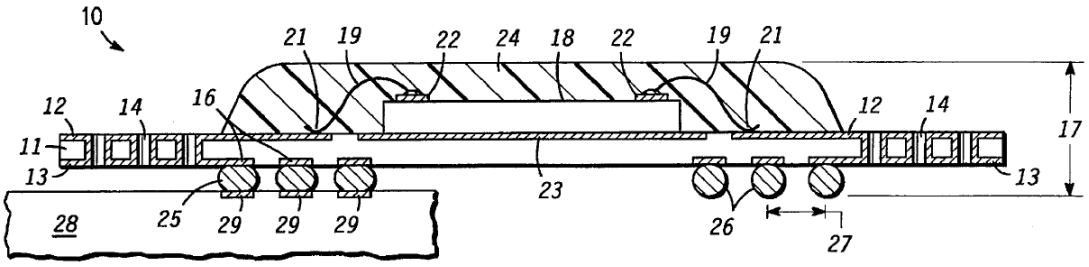


FIG. 1
-PRIOR ART-

Figure 1 of Jones illustrates a cross-sectional view of a prior art BGA package. Ex. 1013, 1:63–64.

As shown in Figure 1, BGA package 10 comprises substrate 11 and integrated circuit or semiconductor chip 18 attached to the upper surface of substrate 11. *Id.* at 2:13–15, 2:31–33. Semiconductor chip 18 has bonding pads 22 that are electrically connected via wire 19 to conductive traces 12 formed on the top of substrate 11. *Id.* at 2:34–38. Conductive solder balls 26 are each attached to ball pad 16. *Id.* at 2:41–42. Jones further describes that once BGA package 10 is completed, conductive solder balls 26 are later connected to a next level of assembly or printed circuit board 28 using a standard solder reflow process. *Id.* at 2:47–49.

According to Jones, existing BGA packages have several disadvantages including:

> a high profile on the order of 2.4 millimeters (mm); collapse of the solder balls at reflow to a height determined by ball and ball pad size; and a fatigue failure rate of the solder joints during temperature cycling based on the higher strain levels in solder joints with lower height to diameter ratios.

Id. at 1:46–53. Jones further describes the disadvantages of conventional BGA packages as follows.

> BGA package 10 has several disadvantages. BGA package 10 typically has a high profile with a height 17 on the order of 2.4 mm. Also, semiconductor die 18 exerts significant stress on those conductive solder balls 26 directly beneath or in close proximity to the outer edge of semiconductor die 18, when BGA package 10 is mounted to an application board and subjected to temperature cycling. This stress distorts the solder joints and can ultimately result in solder joint failure.

Id. at 2:58–66.

Against this backdrop, Jones describes embodiments of a BGA package that includes a substrate attached to a support substrate, which provides a low profile and functions as a standoff that limits the collapse of the conductive solder balls when the BGA semiconductor package is attached to an application board. *Id.* at Abstract.

Figure 2 of Jones is reproduced below.

FIG. 2

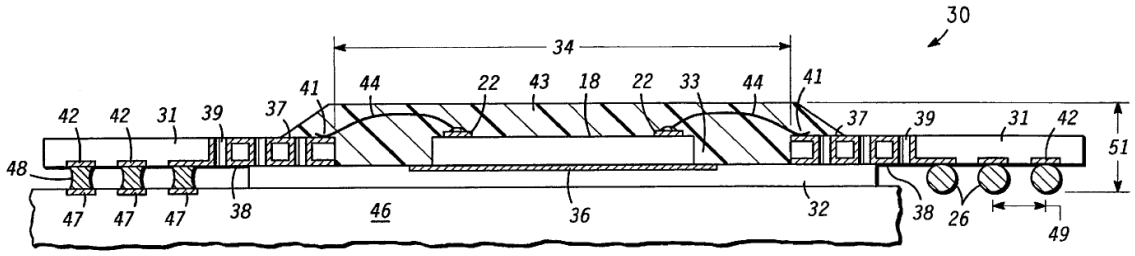


Figure 2 of Jones illustrates a cross-sectional view of an embodiment of perimeter BGA package 30. *Id.* at 1:65–67, 3:4–6.

Jones describes that BGA package 30 comprises a substrate structure including substrate 31 and support substrate 32 attached to substrate 31. *Id.* at 3:6–8. According to Jones, "[b]y using a two substrate construction comprising substrate 31 and support substrate 32, overall height 51 of BGA package 30 is reduced on the order of 0.9 to 1.4 mm or 42 to 58%, for example." *Id.* at 3:24–27. Jones further describes that once BGA

package 30 is formed or completed, "[b]y placing conductive solder balls 26 further away from semiconductor die 18, less stress is imparted to the solder joints when BGA package 30 is mounted to an application board and subjected to temperature cycling." *Id.* at 4:3–7. Similarly, Jones describes:

> When BGA package 30 is mounted to PC board 46, support substrate 32 is in close proximity to PC board 46 and acts as standoff, which limits the collapse of conductive solder balls 26 during the mounting process. When the collapse is limited, the solder joints are taller than in standard BGA packages. Taller solder joints have been shown to be more reliable because the larger aspect ratio lowers solder joint strain. This provides an advantage over BGA package 10 because it allows a manufacturer to reduce pitch 49 between conductive solder balls 26 and therefore the size of solder balls 26 without sacrificing reliability.

Id. at 4:21–31. In addition, Jones describes that

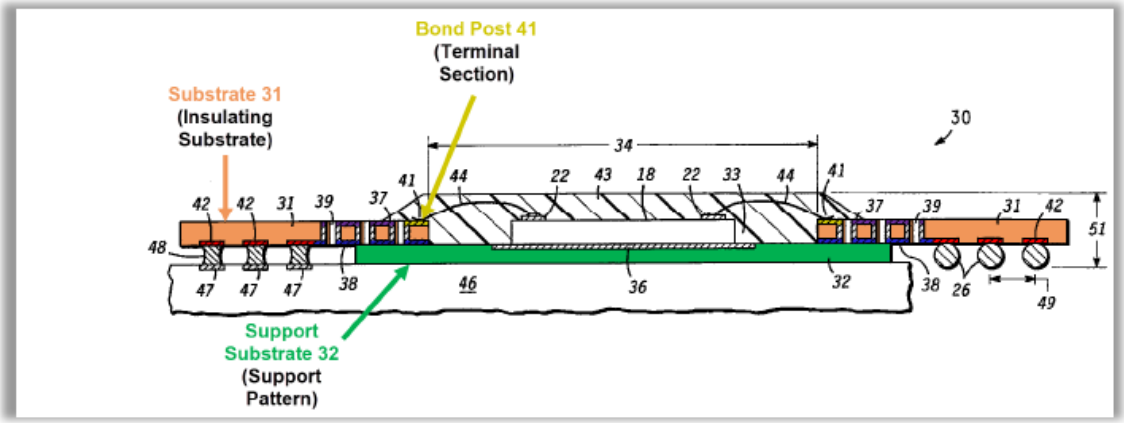
> Support substrate 32 also provides for a thinner profile of BGA package 30 compared to [prior art] BGA package 10. When substrate 31 and support substrate 32 comprise an organic epoxy-glass resin, BGA package 30 has a height 51, which is on the order of 1.0 to 1.5 mm. This is significantly less than height 17 of BGA package 10.

Id. at 4:34–40.

2. Claim 1

Petitioner contends that Jones in view of the general knowledge of a person of ordinary skill in the art teaches the preamble and all limitations of claim 1. Pet. 80–85. In particular, Petitioner relies on support substrate 32 shown in Jones's Figure 2 as teaching "a support pattern, provided on the second surface corresponding in position to the terminal section, for improving wire bonding connection," as recited in claim 1. *Id.* at 83–84.

Figure 2 of Jones as annotated by Petitioner is reproduced below.



Jones - Figure 2

Pet. 83. Annotated Figure 2 of Jones reproduced above illustrates Petitioner's alleged identification in Jones of certain limitations recited in claim 1. *Id.* at 80–84.

Petitioner asserts that support substrate 32 (annotated in green) shown in Jones's Figure 2 teaches the recited "support pattern . . . for improving wire bonding connection" because support substrate 32 "minimize[s] stress exerted by the chip and strengthen[s] electrical connections." Pet. 83 (citing Ex. 1013, 3:24–25, 2:60–7:3).

Patent Owner argues that the cited portions of Jones do not describe that support substrate 32 improves wire bonding connection. Prelim. Resp. 46–47 (citing Ex. 2001 ¶¶ 116–117). We agree with Patent Owner's argument.

As discussed above in Section III.H.1, Jones describes that prior art BGA package 10 had several disadvantages including that "semiconductor die 18 exerts significant stress on those conductive solder balls 26 directly beneath or in close proximity to the outer edge of semiconductor die 18, *when BGA package 10 is mounted to an application board* and subjected to

temperature cycling." Ex. 1013, 2:58–64 (emphasis added). Jones further describes that "[t]his stress distorts the solder joints and can ultimately result in solder joint failure" when mounting completed BGA package 10 on an application board, e.g., a motherboard. *Id.* at 2:64–66; *see also id.* at 2:47–49 ("Conductive solder balls 26 are *later connected* to a *next level of assembly* or *printed circuit board* 28 using a standard solder reflow process." (emphases added)).

As also discussed in Section III.H.1 above, Jones describes an embodiment of BGA package 30 that purportedly minimizes this problem—i.e., once BGA package 30 is formed or completed, "[b]y placing conductive solder balls 26 further away from semiconductor die 18, less stress is imparted to the solder joints *when BGA package 30 is mounted to an application board* and subjected to temperature cycling." *Id.* at 4:3–7 (emphasis added). Similarly, Jones describes:

> *When BGA package 30 is mounted to PC board 46*, *support substrate 32* is in close proximity to PC board 46 and *acts as standoff*, which limits the collapse of conductive solder balls 26 *during the mounting process*. When the collapse is limited, the solder joints are taller than in standard BGA packages. Taller solder joints have been shown to be more reliable because the larger aspect ratio *lowers solder joint strain*.

Id. at 4:21–28 (emphases added).

In other words, the cited portions of Jones describe a problem of solder joint failure when mounting a completed conventional BGA package on a motherboard—i.e., a problem of electrical connection between a completed BGA package and the motherboard, *not* a problem of wire bonding during the fabrication of the BGA package. And Jones discloses an embodiment of BGA package 30 with support substrate 32, which acts as

stand off during the mounting process to reduce strain on solder joint between the completed BGA package 30 and the motherboard, *not* to "minimize stress" of wire bonding during the fabrication of BGA package 30.

Petitioner does not identify, nor do we discern, any disclosure in Jones of support substrate 32 "strengthen[ing] electrical connections" during wire bonding, as Petitioner contends, or "improving wire bonding connection," as recited in claim 1. Petitioner also does not identify, nor do we discern, any disclosure in Jones suggesting that support substrate 32 is capable of these functions.

Petitioner next asserts that support substrate 32 shown in Jones's Figure 2 teaches the recited "support pattern . . . for improving wire bonding connection" because "[b]y providing support substrate 32 underneath insulating substrate's wiring layer 38, the bottom surface is rendered flat and thus not susceptible to bending during wire bonding." Pet. 84. Petitioner argues that "the '013 patent explains that the 'protrudent part' and bending problem does not occur when the bottom surface of the insulating substrate is flat." *Id.* (citing Ex. 1001, 2:65–3:18).

Patent Owner argues that Jones does not describe or suggest "there was a problem with substrate bending and a desire to find a solution." Prelim. Resp. 46–47(citing Ex. 2001 ¶¶ 116–117). We agree with Patent Owner's argument.

Figure 1 of Jones is reproduced below.

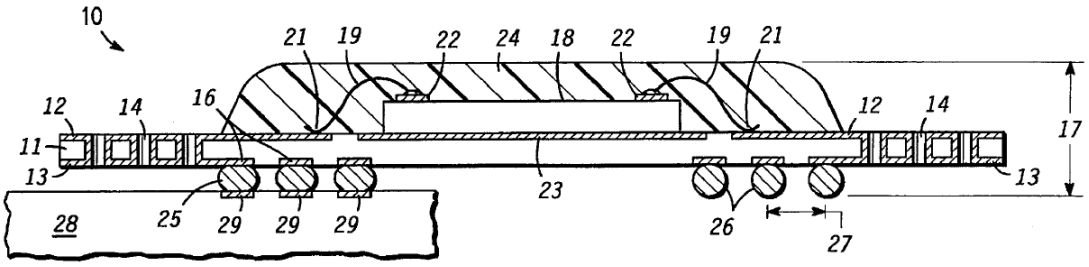


FIG. 1
-PRIOR ART-

Figure 1 of Jones illustrates a cross-sectional view of prior art BGA package 10. Ex. 1013, 1:63–64, 2:12–13.

As discussed above, Jones describes that conductive solder balls 26 are attached to BGA package 10 at the last step of the fabrication process and that, after BGA package 10 is completed, conductive solder balls 26 are "*later* connected to a *next level of assembly* or printed circuit board 28" using a standard solder reflow process. Ex. 1013, 2:41–49 (emphases added). Thus, as shown in Figure 1 of Jones, during wire bonding of BGA package 10's fabrication process, the bottom surface of insulating layer 11 would have been flat without solder balls 26. Therefore, as explained in the '013 patent (Ex. 1001, 3:19–25), the bending problem during wire bonding would not have occurred in the conventional art distinguished by Jones, and Jones's addition of support substrate 32 to already flat insulating layer 11 could not have been to prevent or reduce the bending problem that did not exist in the prior art BGA package. In other words, Jones's addition of support substrate 32 to the conventional BGA package could not have been to improve wire bonding connection by preventing or reducing any bending

problem. Nor does Jones suggest the support substrate 32 is capable of such purpose.

Similarly, Figure 2 of Jones shows that the bottom surface of insulating substrate 31 is already flat without support substrate 32 during BGA package 30's fabrication process. Petitioner does not explain why support substrate 32 is needed to render the bottom surface of the insulating substrate 31 flat when insulating substrate 31 already has a flat bottom surface. More importantly, Petitioner does not explain how the flat bottom of support substrate 32 is capable of "improving wire bonding connection," as recited in claim 1, when the bottom surface of insulating substrate 31 is already flat without support substrate 32.

As discussed above in Section II.C, under the heading "SUMMARY OF THE INVENTION," the '013 patent states that "[t]he object of *the present invention* is to provide a wiring substrate, a semiconductor device, and a package stack semiconductor device, all with *improved reliability of connection* by suppressing occurrence of inadequate electrical connection." Ex. 1001, 3:60–64 (emphases added). The '013 patent further states that

> A wiring substrate of *the present invention*, in order to achieve the foregoing object, includes an insulating substrate, a terminal section for wire bonding or flip-chip connection and a *support pattern*, provided on a surface of the other side of the surface where the terminal section is provided, and on a position corresponding to the terminal section, *for improving reliability of connection of wire bonding*.
>
> Therefore, this structure can suppress deformation of the insulating substrate *by the support pattern*, even when the terminal section is pressed in wire bonding or other connection methods. As a result, *reliability of connection in wire bonding* or other connection methods, *can be improved* than conventionally.

Id. at 3:65–4:11 (emphases added).

In view of these disclosures in the Specification and the express recitation "for improving wire bonding connection" in the claim, we determine that the limitation reciting "support pattern . . . for improving wire bonding connection" requires the recited "support pattern" to be capable of "improving wire bonding connection." *See GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1371 (Fed. Cir. 2016) ("When a patent . . . describes the features of the 'present invention' as a whole, this description limits the scope of the invention." (quoting *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007))); *see also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004) ("Statements that describe the invention as a whole are more likely to be found in certain sections of the specification, such as the Summary of the Invention.").

Petitioner does not show sufficiently that support substrate 32 of Jones meets the recited "support pattern . . . for improving wire bonding connection" because Petitioner does not explain adequately why the flat bottom of support substrate 32 is capable of "improving wire bonding connection," as required by claim 1, when the bottom surface of insulating substrate 31 is already flat without support substrate 32.

Petitioner further contends that "[e]ven if small gaps remain between the (uneven) bottom wiring layer 38 and substrate 32, the flattened bottom surface nevertheless reinforces and protects the insulating substrate during wire bonding." Pet. 84 (citing Ex. 1002 ¶¶ 329–331). However, neither Petitioner nor Dr. Suhling cites to any disclosure in Jones that there is any gap between bottom wiring layer 38 and substrate 32 or that substrate 32 "protects the insulating substrate during wire bonding." As discussed above,

Jones discloses that support substrate 32 acts as stand off during the mounting of completed BGA package 30 on a motherboard to reduce strain on solder joint between the BGA package 30 and the motherboard, *not* to "protect[] the insulating substrate during wire bonding" in the process of fabrication of BGA package 30. Ex. 1013, 2:47–49, 2:58–66, 4:21–28. Thus, Petitioner's argument is conclusory and unsupported by evidence.

For the foregoing reasons and based on the record presented, we are not persuaded that Jones's support substrate 32 teaches or suggests "a support pattern, provided on the second surface corresponding in position to the terminal section, *for improving wire bonding connection*," as recited in claim 1.

Accordingly, Petitioner has not set forth sufficient argument and supporting evidence to demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claim 1 would have been obvious over Jones in view of the general knowledge of a person of ordinary skill in the art.

3. Independent Claims 6, 8, 11, 13, 14, and 20

Petitioner acknowledges that claims 1, 6, 8, 11, 13, 14, and 20 recite identical or nearly identical "support pattern" limitations. Pet. 86–87, 88, 92, 93. For these limitations of claims 6, 8, 11, 13, 14, and 20, Petitioner cites to and relies on its analysis of claim 1 discussed above. *Id.* Thus, for the same reasons discussed above with respect to claim 1, Petitioner does not demonstrate a reasonable likelihood that it would prevail in showing that the subject matter of claims 6, 8, 11, 13, 14, and 20 would have been obvious over Jones in view of the general knowledge of a person of ordinary skill in the art.

4. Dependent Claims 2 and 4

Claims 2 and 4 depend from claim 1. Petitioner's arguments and evidence presented with respect to these dependent claims only address the additionally recited limitations of claims 2 and 4, and, therefore, do not remedy the deficiencies in Petitioner's analysis of claim 1 discussed above. *See* Pet. 93–94. Accordingly, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claims 2 and 4 are unpatentable under § 103(a) over Jones in view of the general knowledge of a person of ordinary skill in the art.

IV. CONCLUSION

For the foregoing reasons, based on the arguments and evidence presented in the Petition, we conclude that Petitioner has not demonstrated a reasonable likelihood that Petitioner would prevail in showing at least one of the challenged claims of the '013 patent is unpatentable based on any asserted ground of unpatentability. Therefore, we do not institute an *inter partes* review with respect to any of the challenged claims of the '013 patent.

V. ORDER

In consideration of the foregoing, it is

ORDERED that Petitioner's request for an *inter partes* review is *denied* as to all challenged claims of the '013 patent, and no trial is instituted.

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