

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

LS CLOUD STORAGE TECHNOLOGIES LLC,
Patent Owner.

IPR2023-00120
Patent 10,154,092 B2

Before LARRY J. HUME, MINN CHUNG, and AMBER L. HAGY,
Administrative Patent Judges.

HUME, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Google LLC (“Petitioner”)¹ filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review (“IPR”) of all claims 1–24 (“the challenged claims”) of U.S. Patent No. 10,154,092 B2 (Ex. 1001, “the ’092 patent”). LS Cloud Storage Technologies LLC (“Patent Owner”) timely filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

An *inter partes* review may not be instituted unless “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition.” 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.4.

Having reviewed the parties’ papers and the evidence of record, we determine that Petitioner has shown a reasonable likelihood it will prevail in establishing the unpatentability of at least one challenged claim. Accordingly, we institute an *inter partes* review of all challenged claims 1 through 24 of the ’092 patent, based on the grounds raised in the Petition.

II. BACKGROUND

A. Related Matters

The parties indicate that the ’092 patent has been asserted in various district court lawsuits, including: *LS Cloud Storage Technologies, LLC v.*

¹ Petitioner identifies its parent entity as XXVI Holdings Inc., which is a subsidiary of Alphabet Inc. Petitioner states that neither XXVI Holdings Inc. nor Alphabet Inc. are real parties-in-interest to this proceeding. Pet. 2, n.1.

Google LLC, No. 6:22-cv-00318 (W.D. Tex. 2022). Pet. 2; Paper 4 (Patent Owner Mandatory Notices), 2.²

After filing of the Petition and Patent Owner's Response, the '092 patent has become the subject of one other petition for *inter partes* review and Motion for Joinder, i.e., IPR2023-00733 (filed by Cisco Systems, Inc., Microsoft Corporation, Amazon.Com, Inc., Amazon Web Services, Inc., and Amazon.Com Services LLC). The Decision whether to institute *inter partes* review in IPR2023-00733 and effect joinder with this proceeding will be made in due course.

B. The '092 Patent

The '092 patent is titled "Data Sharing Using Distributed Cache in a Network of Heterogeneous Computers." Ex. 1001, code (54). The '092 patent issued December 11, 2018, from U.S. Patent Application No. 14/997,327, filed January 15, 2016, claiming benefit as a continuation application under 35 U.S.C. § 120 to a series of applications, and ultimately claiming benefit as a divisional application under 35 U.S.C. § 121 of U.S. Patent Application No. 09/236,409 filed on January 22, 1999, and issued on April 15, 2003. *Id.* at codes (21), (22), (45), (60). We note the '092 patent term appears to have expired on September 16, 2019.

² In addition, Patent Owner has asserted the '092 patent against other parties, i.e., *LS Cloud Storage Technologies, LLC v. Amazon.com, Inc. et al.*, 6:22-cv-00316 (W.D. Tex. 2022); *LS Cloud Storage Technologies, LLC v. Cisco Systems, Inc.*, 6:22-cv-00319 (W.D. Tex. 2022) (dismissed); *LS Cloud Storage Technologies, LLC v. Microsoft Corporation*, 6:22-cv-00321 (W.D. Tex. 2022); and *LS Cloud Storage Technologies, LLC v. Cisco Systems, Inc.*, 6:22-cv-00845 (W.D. Tex. 2022). See Paper 4, 2; see also Pet. 2.

The '092 patent describes a network of PCs that includes an input/output (I/O) channel adapter and network adapter, configured for management of a distributed cache memory stored in the plurality of PCs interconnected by the network. *See* Ex. 1001, code (57) (Abstr.). According to the '092 patent, the use of standard PCs serves to reduce the cost of the data storage system, and using networked PCs permits building large, high-performance data storage systems. *Id.* The '092 patent further describes:

This invention relates generally to the field of cached data storage systems and more particularly to a data storage system that permits independent access from local hosts connected via I/O channels and independent access from remote hosts and remote storage systems connected via network links. A network of PCs permits building a high-performance, scalable, data storage system using off-the-shelf components at reduced cost. A configuration manager ensures consistency of data stored in the distributed cache.

Id. at 1:18–26.

As background, the '092 patent describes the prior art as follows:

A typical data processing system generally involves a cached data storage system that connects to local host computers via I/O channels or remote host computers via network links. The purpose of the data storage system is to improve the performance of applications running on the host computer by offloading I/O processing from the host to the data storage system. The purpose of the cache memory in a data storage system is to further improve the performance of the applications by temporarily storing data buffers in the cache so that the references to those buffers can be resolved efficiently as “cache hits”. Reading data from a cache is an order of magnitude faster than reading data from a back end storage device such as a disk. Writing data to a cache is also an order of magnitude faster than writing to a disk. All writes are cache hits because data is simply copied into cache buffers that are later flushed to disks.

Id. at 1:30–45. The '092 patent also describes the need for improvements in distributed data storage systems at the time of the invention:

There is a growing demand for distributed data storage systems. In response to this demand some prior art systems have evolved into complex assemblies of two systems, one proprietary a data storage system and the other an open networking server. One such system is described in a white paper on a company web site on Internet. The industry white paper, EMC Data Manager: A high-performance, centralized open system backup/restore solution for LAN-based and Symmetrix resident data, describes two different systems, one for network attached hosts and second for channel attached hosts. The two systems are needed because of the lack of generic networking support. In related products such as Celerra File Server, product data sheets suggest using data movers for copying data between LAN-based open system storage and channel attached storage system.

However, the above systems are built from two systems, one for handling I/O channels, and another for handling open networks. Two systems are very expensive even in minimal configuration that must include two systems.

Id. at 2:42–60.

The background of the '092 patent concludes by stating that there is a need “to provide a high-performance data storage system that is assembled out of standard modules, using off-the-shelf hardware components and a standard general-purpose operating system that supports standard network software and protocols.” *Id.* at 3:30–34. Further, the background of the '092 patent identifies a need “to provide a cached data storage system that permits independent data accesses from I/O channel attached local hosts, network attached remote hosts, and network-attached remote data storage systems.” *Id.* at 3:35–38.

Against this backdrop, the '092 patent describes embodiments of a cached storage system that includes a network of personal computers (PCs) with an I/O channel adaptor and a network adaptor configured for management of a distributed cache memory stored in the network-connected PCs. *Id.*, Abstr. Figure 1 of the '092 patent is reproduced below as an aid in understanding the claimed invention.

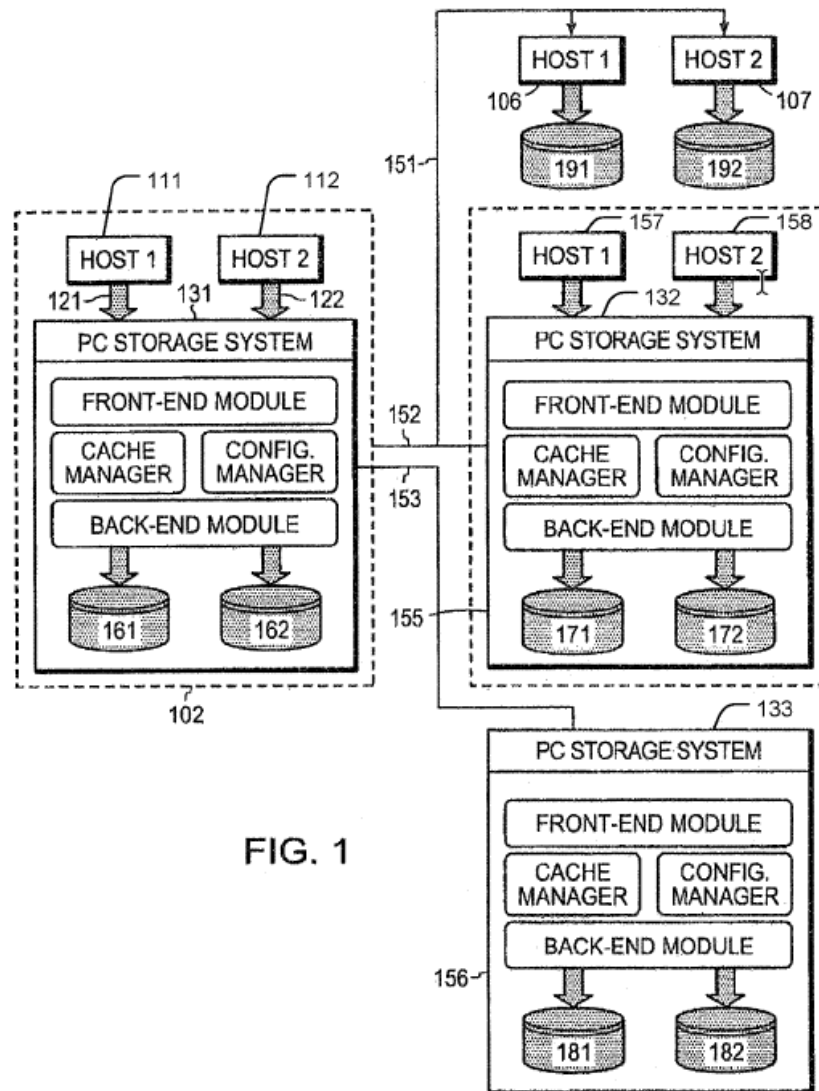


Figure 1 of the '092 patent “shows data storage systems configurations” (*id.* at 4:50) illustrating a network of data storage systems (131, 132, 133).

In the preferred embodiment shown in Figure 1 of the '092 patent, “PC data storage system 131 services a plurality of channel attached host processors 111, 112 using channels 121, 122, and a plurality of network attached host processors 106, 107 using network link 151, and a plurality of network attached data storage systems 132, 133 using network links 152, 153.” Ex. 1001, 5:10–15. In addition, “PC storage system 132 services channel attached hosts 157, 158.” *Id.* at 5:15–16. The '092 patent further describes that

Hosts 157 and 158 access a data storage system 131 indirectly via network attached data storage system 132, thereby offloading communications protocol overhead from remote hosts 157, 158. Hosts 106 and 107 directly access storage system 131 via network link 151 thereby incurring communications protocol overhead on hosts 106, 107 and therefore decreasing performance of applications running on said hosts.

Host 111 accesses remote disk 181 via local data storage system 131, network link 153, and remote data storage system 133 without incurring protocol overhead on host 111. Host 157 accesses disk 161 via data storage system 133, network link 152, and data storage system 131 without incurring protocol overhead on host 157. Host 106 directly accesses local disk 161 via network link 151 thereby incurring protocol overhead. The disks 191, 192 that are attached to hosts 106, 107 without a data storage system, cannot be accessed by outside hosts.

Id. at 5:17–34; *see also* Ex. 2001 (PO Declaration of Dr. Hassan Zeino, Ph.D, hereinafter “Zeino Declaration”) ¶¶ 27–28 (in which Dr. Zeino discusses the disclosures relating to Figure 1 of the '092 patent (citing Ex. 1001, 5:9–24, Fig. 1)).

The '092 patent describes that “[t]he presence of fast access cache memory permits front end channels and network links to operate completely independent of the back-end physical disk devices. Because of this front-

end/back-end separation, the data storage system 131 is liberated from the I/O channel and network timing dependencies.” Ex. 1001, 6:1–6. As a result, processing resources may be dedicated to increase performance through better scheduling and utilization of data transfer network protocol. *Id.* at 6:6–8.

C. Illustrative Claims

Of the challenged claims, claims 1, 13, 19, and 24 are independent, and for purposes of this Decision, claims 1, 4, 5, 10, and 13 are illustrative of the challenged claims, and are reproduced below:

Claim 1 recites:

[1.pre] An apparatus comprising:

[1.a] a first interface configured to receive input/output (I/O) traffic from a first host device via a dedicated I/O channel, the I/O traffic comprising a read command;

[1.b] a second interface configured to receive first data via a network;

[1.c] a cache memory configured to store second data;

[1.d] a storage device configured to store third data; and

[1.e] a processor coupled to the cache memory, the processor coupled to the storage device via a communication path that is distinct from the dedicated I/O channel, the processor configured to access the cache memory during processing of the I/O traffic,

[1.f] the processor further configured to perform an access operation at the storage device based on the I/O traffic.

Ex. 1001, 9:20–34 (Petitioner-provided bracketed labeling added for ease of reference); *see* Pet. 21–30.

Claim 4 recites:

4. The apparatus of claim 1, wherein the dedicated I/O channel comprises a small computer system interface (SCSI) channel.

Ex. 1001, 9:40–42.

Claim 5 recites:

5. The apparatus of claim 1, wherein the second interface comprises an Ethernet interface or an asynchronous transfer mode (ATM) interface.

Ex. 1001, 9:43–45.

Claim 10 recites:

10. The apparatus of claim 1, wherein the processor is further configured to route the read command to the cache memory or to the storage device.

Ex. 1001, 9:58–60.

Claim 13 recites:

13. [13.pre] A method comprising:

[13.a] receiving input/output (I/O) traffic from a host device via a dedicated I/O channel at a first interface, the I/O traffic comprising a write command;

[13.b] receiving first data via a network at a second interface;

[13.c] storing second data at a cache memory;

[13.d] storing third data at a storage device;

[13.e] accessing the cache memory during processing of the I/O traffic; and

[13.f] performing one or more access operations at the storage device based on the I/O traffic, the one or more access operations utilizing a communication path between a processor and the storage device, the communication path distinct from the dedicated I/O channel.

Ex. 1001, 10:6–19 (Petitioner-provided bracketed labeling added for ease of reference); *see* Pet. 51–53.

D. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds 1 through 5 of unpatentability (Pet. 4–5, 21–76):

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1–3, 7–12, 19–23	102(e)	Heil ⁴
2	10, 11	102(b)	Heil
3	1–3, 6–24	103(a)	Heil, Nakayama ⁵
4	4	103(a)	Heil, Nakayama, Gulick ⁶
5	5	103(a)	Heil, Nakayama, Berman ⁷

³ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. The ’092 patent claims benefit under 35 U.S.C. § 120 to applications filed before that date, so we refer to the pre-AIA version of the statute, but our findings and analysis would be the same under the current version of the statute.

⁴ US 6,173,374 B1, filed Feb. 11, 1998, issued Jan. 9, 2001 (Ex. 1006, “Heil”).

⁵ US 5,920,893, filed June 2, 1997, issued July 6, 1999. (Ex. 1007, “Nakayama”).

⁶ US 5,692,211, filed Sept. 11, 1995, issued Nov. 25, 1997 (Ex. 1008, “Gulick”).

⁷ US 6,118,776, filed Aug. 7, 1997, issued Sept. 12, 2000 (Ex. 1009, “Berman”).

Petitioner supports its challenge with a declaration from Dr. Paul Franzon, Ph.D. (Ex. 1004, “Franzon Declaration”).

III. ANALYSIS

A. Legal Standards

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to the patent owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

“A single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375–76 (Fed. Cir. 2005). To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001).

Further, a “reference must describe the claimed invention with sufficient precision and detail to establish that the subject matter existed in the prior art.” *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1120 (Fed. Cir. 2002). The reference does not need to use the same terminology. *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (noting that a reference anticipates if a person of skill in the art

“would at once envisage the claimed arrangement or combination” (internal quotation marks and citation omitted)). But, an ambiguous reference will not anticipate a claim. *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1284 (Fed. Cir. 2017). The dispositive question for anticipation is whether one skilled in the art would reasonably understand or infer from the reference that every claim element is disclosed. *Eli Lilly & Co. v. Los Angeles Biomedical Research Inst. at Harbor-UCLA Medical Ctr.*, 849 F.3d 1073, 1074–75 (Fed. Cir. 2017).

The legal question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). One seeking to establish obviousness based on more than one reference also must articulate sufficient reasoning with rational underpinnings to combine teachings. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Level of Ordinary Skill in the Art

Supported by the testimony of Dr. Franzon, Petitioner asserts that the level of ordinary skill in the art corresponds to a person having “a bachelor’s degree in Computer Science, Computer Engineering, or Electrical Engineering, or an equivalent course of study, as well as 2 or more years of academic or industry experience in the field of computer networking,

⁸ The current record does not include allegations or evidence of objective indicia of nonobviousness (secondary considerations).

computer architecture and storage management. . . . More education can supplement practical experience, and vice versa.” Pet. 17–18 (citing Ex. 1004 ¶¶ 34–36).

At this stage, “Patent Owner agrees to Petitioner’s proffered level of ordinary skill in the art because it comports with the technology and claims of the ’092 Patent as well as the asserted prior art.” *See* Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner’s unopposed position as to the level of ordinary skill in the art at the time of the claimed invention, as articulated above. We are satisfied that Petitioner’s proposed definition generally comports with the level of skill necessary to understand and implement the teachings of the ’092 patent and the asserted prior art. This definition is also supported by the testimony of Dr. Franzon (*see* Ex. 1004 ¶¶ 34–36), as well as a declaration from Patent Owner’s declarant, Dr. Hassan Zeino, Ph.D. *See* Ex. 2001 ¶ 24 (“Zeino Declaration”).

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), following the standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). In applying such standard, claim terms are generally given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic*

Sofamor Danek, Inc., 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

“Petitioner interprets all terms of claims 1–23 in accordance with their ordinary and customary meaning.” Pet. 18. Petitioner further states that claim 24 recites various “means for” limitations that “are means-plus-function limitations governed by 35 U.S.C. § 112[, sixth paragraph].” *Id.*

Patent Owner responds that “the terms of claims 1–4 (and all other challenged claims) of the ’092 Patent are clear on their face,” and “Patent Owner reserves the right to propose further constructions if necessary.” Prelim. Resp. 5.

However, notwithstanding the parties’ stated positions, we note claim 1 of the ’092 patent recites, *inter alia*, “a first interface configured to receive input/output (I/O) traffic from a first host device *via a dedicated I/O channel*, the I/O traffic comprising a read command.” Ex. 1001, 9:21–23 (emphasis added).

We find no express definition of “dedicated I/O channel” in the disclosure of the ’092 patent or the related prosecution history (*see generally* Ex. 1002 (File History of U.S. Patent No. 10,154,092) and Ex. 1003 (File History of U.S. Patent No. 6,549,988)). Further, Patent Owner asserts:

Heil does not disclose “a first interface configured to receive input/output (I/O) traffic from a first host device via a dedicated I/O channel.” *The channel used by the PCI bus bridge 115 and PCI bus 116.5 is used for other communications besides I/O requests, for example arbitrary communications among peer CPUs* (Heil, Col. 8, lines 8–18) and thus the PCI bus bridge 115 and PCI bus 116.5 simply **cannot be** and **cannot serve** as a dedicated I/O channel.

Prelim. Resp. 15 (*italics* added).

Patent Owner’s assertion highlights a potential claim construction dispute. Although Patent Owner highlights this potential dispute and characterizes Petitioner’s position regarding the teachings of Heil as improper, Patent Owner does not explicitly propose any construction. Prelim. Resp. 12–16; Ex. 2001 (Zeino Declaration) ¶¶ 4–5. Likewise, Petitioner does not offer any proposed construction of the phrase “dedicated I/O channel.” *See* Pet. 18–21. Thus, we are left without guidance from the parties on this issue.

Lacking guidance, we nevertheless consider whether independent claim 1 and, similarly, independent claims 13, 19, and 24, require that the recitation of “dedicated I/O channel” either be construed as (1) requiring a node-based approach using an exclusive communication channel *dedicated between two components*, e.g., a central processing unit (CPU) and a peripheral I/O device, over which dedicated input/output requests are transmitted, thus precluding sharing of the channel with other CPUs and peripheral I/O devices; or (2) as a channel that is *dedicated exclusively for a certain type of data*, i.e., I/O requests, thus encompassing load sharing configurations that share the I/O channel between multiple CPUs and I/O peripheral devices.

The only allusion provided by Patent Owner as to how “dedicated I/O channel” should be construed is found in Dr. Zeino’s declaration: “The PC data storage system 131 services a plurality of channel attached host processors 111, 112 ***using dedicated I/O channels 121, 122***, and a plurality of network attached host processors 106, 107. . . .” Ex. 2001 ¶ 27 (emphasis added); *see also* Prelim. Resp. 3–4 (relying upon the same description as Dr. Zeino). Elements 121 and 122 are illustrated in Figure 1 of the ’092 patent. *See* Ex. 1001, Fig. 1 (reproduced, *supra*).

Based on the current record, given Patent Owner’s argument cited above that Heil’s configuration does not meet the limitation “dedicated I/O channel” because of other types of data purportedly being communicated over the channel, we infer from Patent Owner’s assertion and Dr. Zeino’s statement that the second claim construction issue articulated above is relevant, i.e., whether a “dedicated I/O channel” should be interpreted as a channel that is *used exclusively for a certain type of data*, i.e., I/O requests.

We find that, in contrast to Patent Owner’s and Dr. Zeino’s assertions, the ’092 patent provides a somewhat broader description of elements 121 and 122, to wit: “The PC data storage system 131 services a plurality of channel attached host processors 111, 112 *using channels 121, 122*, and a plurality of network attached host processors 106, 107. . . .” Ex. 1001, 5:10–13 (omitting Dr. Zeino’s proffered words “*dedicated I/O*” (Ex. 2001 ¶ 27 (emphasis added))). The ’092 patent goes on to later describe channels 121 and 122 as “I/O channels.” Ex. 1001, 5:51. We have reviewed the ’092 patent and prosecution history, and find no further intrinsic evidence of record, i.e., original disclosure or arguments presented during prosecution, that would provide additional context for the “*dedicated* I/O channel” limitation.

Nonetheless, for purposes of this Decision, we need not determine whether a “dedicated I/O channel” can transmit data other than I/O requests because, as discussed in Section III.E.1 below, Petitioner shows sufficiently that Heil discloses a “dedicated I/O channel” even under the claim construction inferred from Patent Owner’s argument. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (noting that “we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”

(quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Thus, based on the current record and purposes of this Decision, we preliminarily construe a “dedicated I/O channel” as a channel that is *used exclusively for a certain type of data*, i.e., I/O requests, thus encompassing load sharing configurations that share the I/O channel between multiple CPUs and I/O peripheral devices for communication of I/O requests.

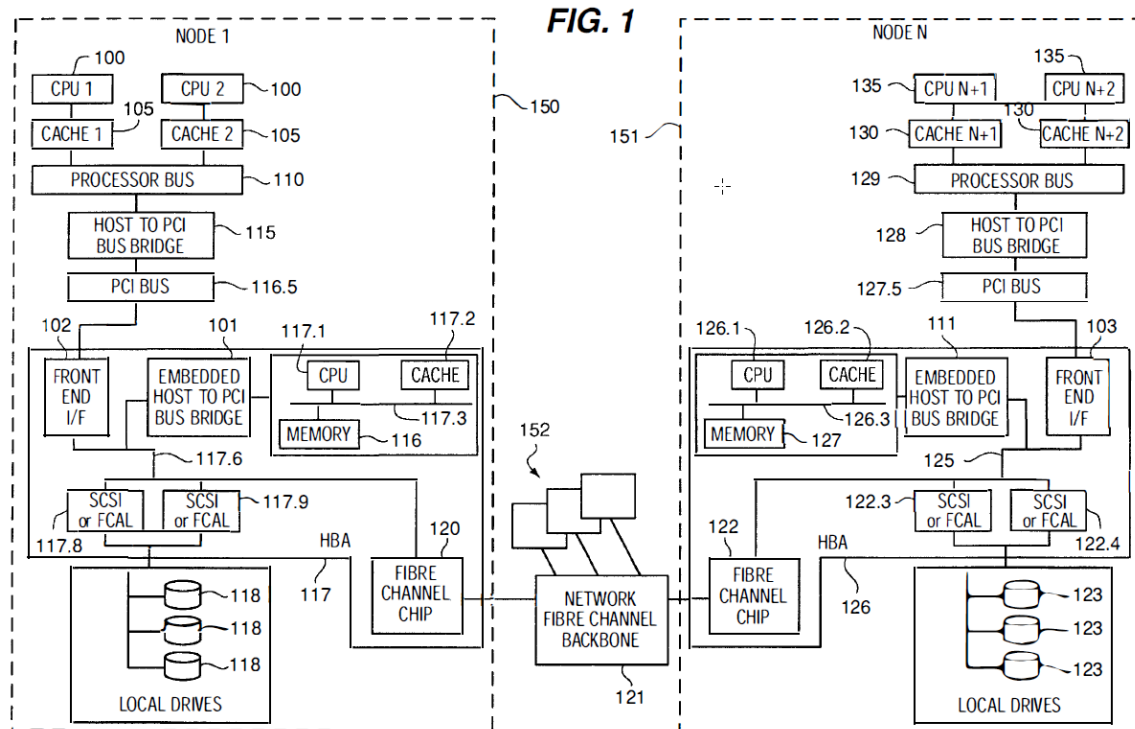
At this stage of the proceeding, based on the parties’ stated positions, we do not find it necessary to address the construction of any other claim terms or phrases. *See Nidec*, 868 F.3d at 1017.

We further note our claim construction analysis in this Decision is preliminary, and does not preclude the parties from arguing proposed constructions of the claims during trial. Indeed, the parties are hereby given notice that claim construction, in general, is an issue to be addressed at trial. Claim construction will be determined at the close of all the evidence and after any hearing. The parties are expected to assert all their claim construction arguments and evidence in the Petition, Patent Owner’s Response, Petitioner’s Reply, Patent Owner’s Sur-reply, or otherwise during trial, as permitted by our rules.

D. Summary of Asserted Prior Art References

1. Heil (Ex. 1006)

Heil describes data storage systems and an apparatus and method in which host computers may store files in a cache or disk storage. Ex. 1006, Abstr., 1:9–14, 6:34–47. Figure 1 of Heil is reproduced below.



“FIG. 1 depicts a host system in which the present invention may be advantageously applied.” *Id.* at 6:33–34.

In Figure 1, Node 1 (150) includes a host system with CPU 1 and CPU 2 (100) connected via Peripheral Component Interconnect (PCI) bus 116.5 to host bus adapter (“HBA”) 117. *Id.* at 6:34–47. Host bus adapter 117 includes cache memory 117.2 and local memory 116 and is connected to local drives 118 via Small Computer System Interface (SCSI) or fiber channel arbitrated loop (“FCAL”) interfaces 117.8 and 117.9. *Id.* at 7:9–15, 7:51–56. The host may process I/O requests locally by accessing HBA 117 via PCI bus 116.5. *Id.* at 4:51–57, 6:34–47. “Although PCI is the preferred I/O bus standard, one skilled in the art will recognize other I/O bus standards are operable within the present invention, such as EISA, MicroChannel, etc.” *Id.* at 6:61–64.

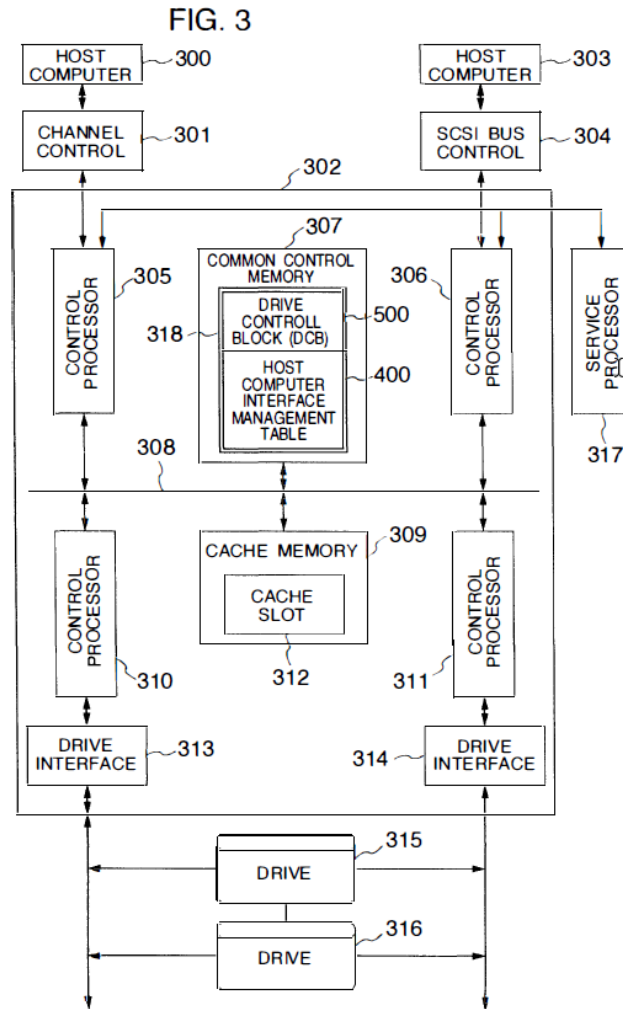
Front-end interface 102 represents a PCI-to-PCI Bus bridge that connects various peripheral I/O devices via PCI bus 117.6, e.g., local drives

118 and Fibre Channel Chip 120, to centralized system PCI bus 116.5. *Id.* at 7:1–4. “To improve I/O performance, CPU **117.1** temporarily caches disk data in cache memory **117.2** that is frequently accessed. Later, the CPU **117.1** stores the data permanently in the slower disk drive devices **118.**” *Id.* at 7:24–27. Figure 1 illustrates that one HBA services I/O requests from CPU 1 and CPU 2 100. “One skilled in the art, however, will recognize the load sharing benefits of allowing a plurality of HBAs to service the local and remote I/O requests of CPU **1** and CPU **2 100.**” *Id.* at 7:35–39.

2. *Nakayama (Ex. 1007)*

Nakayama is directed to cached data storage systems and describes an apparatus and method in which host computers provide input to a cache memory or a storage drive. Ex. 1007, Abstr., 4:52–65.

Figure 3 of Nakayama is reproduced below.



“FIG. 3 is a schematic block diagram showing the configuration of an[] embodiment of a disk subsystem of the present invention.” Ex. 1007, 3:13–15. Figure 3 shows host disk control 302, containing cache memory 309, connected via channel 301 to host computer 300 on the host side. Disk control 302 is also connected to host computer 303 via a SCSI interface, and disk control 302 is connected to magnetic storage medium drives 315 and 316 to perform read/write operations for data on drives 315/316 in response to requests from host computers 300 and 303. *Id.* at 4:39–51.

3. *Gulick (Ex. 1008)*

Gulick describes a system that includes a dedicated multimedia engine and dedicated multimedia memory coupled directly to a main memory. A data path to the main memory and multimedia memory is provided, as is a separate command path to the multimedia engine. Ex. 1008, Abstr.

Figure 1 of Gulick is reproduced below.

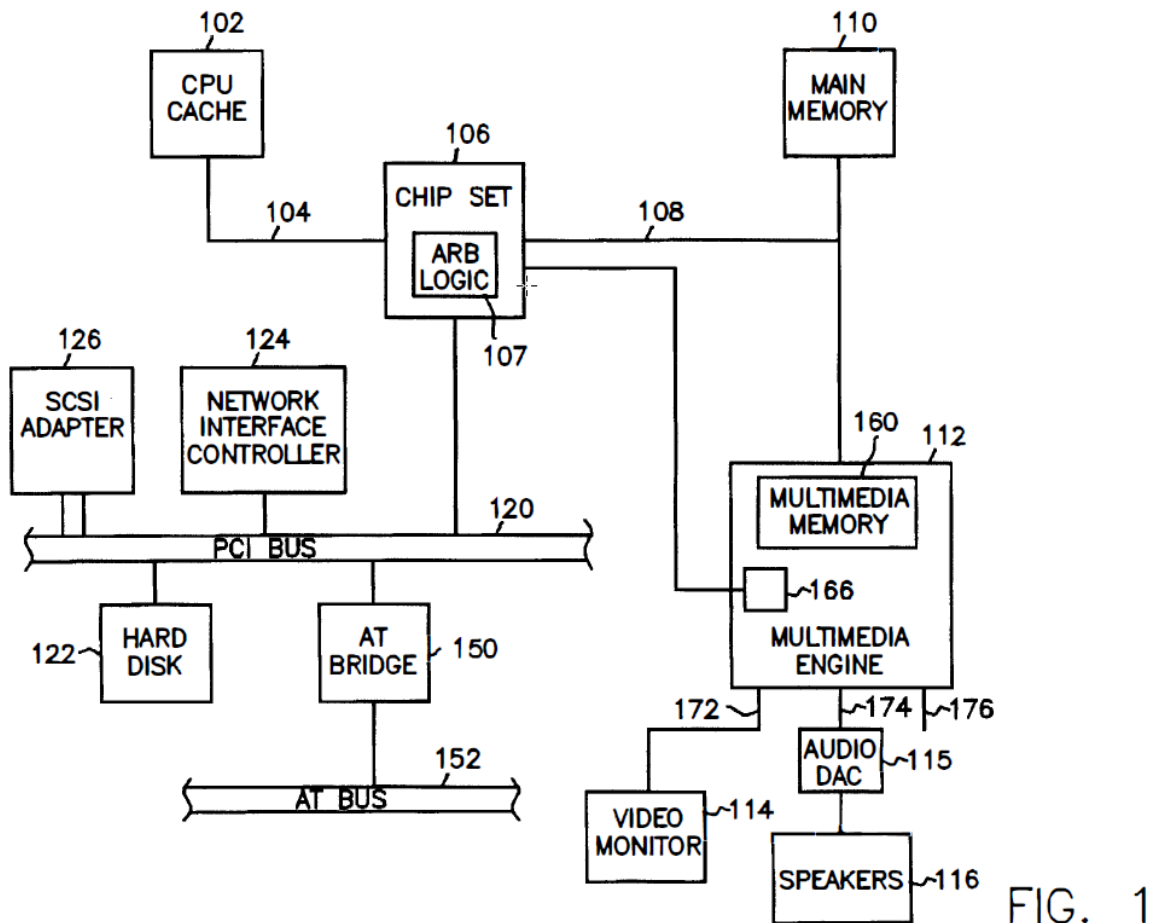


Figure 1 “is a block diagram of a computer system including a separate command path to a multimedia engine.” *Id.* at 3:45–47. Figure 1 depicts central processing unit (CPU) 102 coupled through CPU local bus 104 to a host/PCI/cache bridge or chipset 106. *Id.* at 4:61–65.

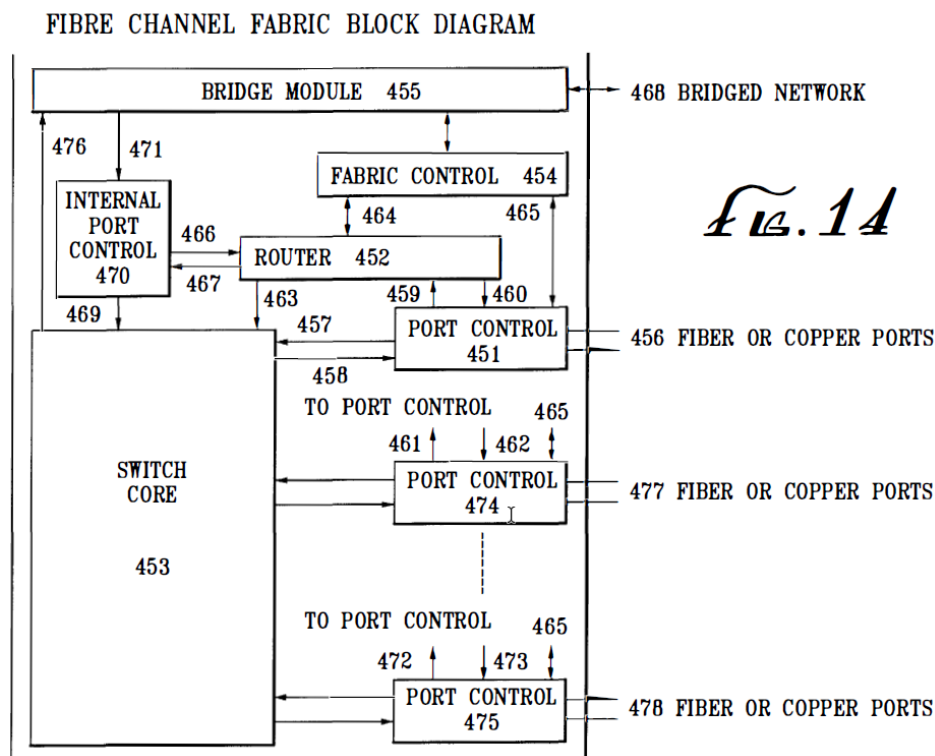
Gulick describes that, in an embodiment, PCI local bus 120 is used, but that other local buses of known types may be used. *Id.* at 5:39–41. In

addition, Gulick discloses that a number of different types of devices may be connected to PCI bus 120. *Id.* at 5:41–43. In Figure 1, hard disk 122 and network interface controller 124 are coupled to PCI bus 120, and SCSI adapter 126 may also be coupled to PCI bus 120 to connect to various SCSI devices, such as a CD-ROM drive and a tape drive (not shown). *Id.* at 5:44–51.

4. Berman (Ex. 1009)

Berman describes “Methods and apparatus for Fiber Channel interconnection . . . provided between a plurality of private loop devices through a Fiber Channel private loop device interconnect system.”

Ex. 1009, Abstr. Figure 14 of Berman is reproduced below.



Berman – Figure 14

Figure 14 of Berman “is a block diagram of a Fibre Channel Fabric.” *Id.* at 6:36. In the block diagram of Figure 14, fabric 30 is composed of fabric control module (FCM) 454, fabric router 452, multiple port control modules 451, 474, and 475, switch core module 453 and, optionally, one or more bridge router (brouter) modules 455. The Fabric Control module controls and configures the rest of the fabric but is said to not usually be involved in the normal routing of frames. *Id.* at 11:30–36. “The interface to the brouter module 455 allows the FCM to communicate through legacy networks such as ethernet and fast ethernet, depending on the brouter module.” *Id.* at 12:8–11.

Berman further describes:

Any type of private loop device, consistent with the apparatus and methods stated herein, may be utilized in conjunction with this system. Examples of private loop devices include storage devices, such as tape drives, JBODs and RAID subsystems, host systems, and other connections within a system, such as bridges, particularly SCSI to Fibre Channel bridges, routers, particularly Fibre Channel to asynchronous transfer mode systems and Fibre Channel to ethernet systems.

Id. at 3:23–31.

*E. Ground 1: Anticipation of Claims 1–3, 7–12, and 19–23
by Heil Under § 102(e)*

Petitioner contends the subject matter of challenged claims 1–3, 7–12, and 19–23 is anticipated by Heil. Pet. 21–30. Patent Owner argues that Petitioner’s showing is insufficient. Prelim. Resp. 11–18.

We have considered the parties’ arguments and the evidence presented at this stage, and we address them in the context of representative claim 1. For the reasons explained below, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that

the subject matter of claim 1 is anticipated by Heil, notwithstanding Patent Owner's arguments to the contrary.

1. Independent Claim 1⁹

[1.pre]: "An apparatus comprising:"

Petitioner contends Heil discloses the preamble. Pet. 21. According to Petitioner, "Heil discloses a data storage and communication apparatus and teaches the preamble." *Id.* (citing Ex. 1006, 1:9–14; Ex. 1004 ¶ 67).

Petitioner's assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil discloses the claim's preamble.¹⁰ At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner's showing. *See* Prelim. Resp. 12 *et seq.*

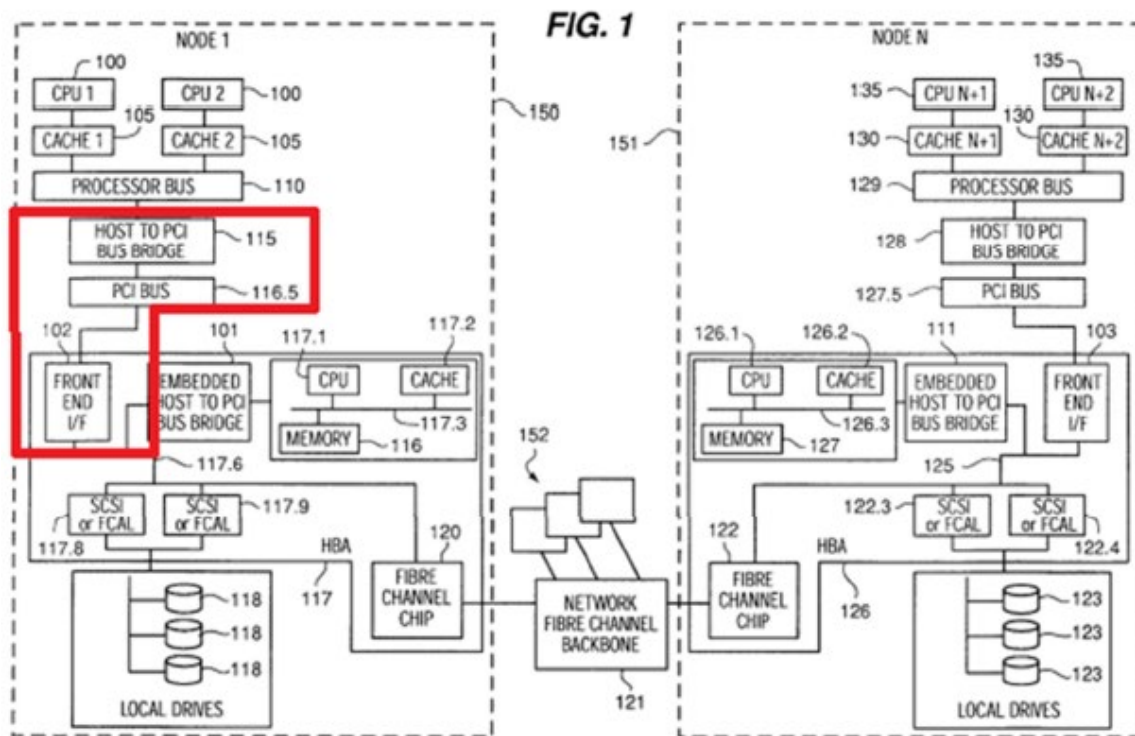
[1.a]: "a first interface configured to receive input/output (I/O) traffic from a first host device via a dedicated I/O channel, the I/O traffic comprising a read command"

Next, addressing the limitations recited in the body of the claim, Petitioner contends that Heil discloses limitation [1.a]. Pet. 21–23. According to Petitioner, Heil in Figure 1 discloses this element by describing a first interface that receives I/O traffic, i.e., I/O requests, from a host device via either Host to PCI bus bridge 115 and PCI bus 116.5, or via Front End I/F 102. Pet. 22–23 (citing Ex. 1006, 6:35–40, 7:36–37; Ex. 1004

⁹ Bracketed numbering of claim limitations is that adopted by Petitioner.

¹⁰ We need not determine whether the preamble is limiting because Petitioner has sufficiently shown that Heil discloses this aspect of the claim and Patent Owner does not rebut this assertion. *See Vivid Techs.*, 200 F.3d at 803; *see generally* Prelim. Resp. 12 *et seq.*

¶¶ 69, 71). Petitioner characterizes the first interface as alternatively reading on either PCI bus bridge 115, PCI bus 116.5, or Front End I/F 102, and that these elements serve as an interface between host bust adaptor (HBA) 117 and Node 1's host system, i.e., a first host device. Pet. 22. Petitioner's annotated Figure 1 of Heil is reproduced below to illustrate the mapping of the claimed first interface to Heil:



Heil – Fig. 1 (annotated) (Pet. 23)

Annotated Figure 1 of Heil (*see* Pet. 23; Ex. 1004 ¶ 30) illustrates Petitioner’s mapping of limitation [1.a] to Heil, as described above, in which “the first interface” is asserted as including “HOST TO PCIBUS BRIDGE” 115 connected to “PCIBUS” 116.5 and “FRONT END I/F” 102. Pet. 22.

Petitioner further asserts “[t]he channel used by the PCI bus bridge 115 and PCI bus 116.5 is a dedicated I/O channel because it is a direct, dedicated connection between the host and the HBA that carries I/O

traffic between them.” Pet. 24 (citing Ex. 1006, 6:35–40, 7:36–37; Ex. 1004 ¶ 72).

Under our preliminary claim construction of the phrase “dedicated I/O channel” adopted above, i.e., we interpret “dedicated I/O channel” as a channel that is *used exclusively for a certain type of data*, i.e., I/O requests, thus encompassing load sharing configurations that share the I/O channel between multiple CPUs and I/O peripheral devices for communication of I/O requests. *See* § III.C, *supra*.

Patent Owner’s declarant states that Petitioner “maps path 115 to 116.5 to 102 as the dedicated I/O channel of element [1.a]” (Ex. 2001 ¶ 17), and opines “[t]his mapping [cannot be made . . . because] Heil specifically notes that the indicated path (i.e., the path including elements 115, 116.5 and 102) is **not dedicated**” because Figure 1 of Heil shows “one HBA services the I/O requests from CPU1 and CPU2 100” (*id.*), thus providing “the **load sharing benefits** of allowing a plurality of HBAs to service the local and remote I/O requests of CPU 1 and CPU 2 100.” Prelim. Resp. at 14.

Relying on the Declaration of Dr. Zeino, Patent Owner states “[t]he channel used by the PCI bus bridge 115 and PCI bus 116.5 is used for other communications besides I/O requests, for example arbitrary communications among peer CPUs (Heil, Col. 8, lines 8–18) and thus the PCI bus bridge 115 and PCI bus 116.5 simply **cannot be** and **cannot serve** as a dedicated I/O channel.” Prelim. Resp. 15. “[T]he the only path to the Fibre Channel backbone 121 from the host system CPUs 100 and remote system CPUs 135 is over PCI bus bridge 115 and PCI bus 116.5, so PCI bus bridge 115 and PCI bus 116.5 are also used to allow a channel or path for each CPU to be connected to peer CPU’s.” *Id.* at 16.

We reproduce Heil column 8, lines 8–21¹¹ (referencing Heil, Fig. 1), cited by Patent Owner, below:

In the present invention, each CPU within Node 150, Nodes 152, and Node N 151 does [sic] not have direct connectivity to a peer CPU within another node. For example, CPU 1 100 does not communicate directly with CPU N+1 135 in Node N 151. Instead, Node 150, Nodes 152, and Node N 151 are connected via a network communications medium. In the preferred embodiment, a Fibre Channel backbone 121 allows each CPU to be connected to peer CPU's. One skilled in the art will recognize all node-to-node inter-processor communication can occur on this Fibre Channel backbone 121. *Alternatively, the Fibre Channel backbone 121 can be used exclusively for storage communications and inter-processor communications can occur over a separate network.*

Ex. 1006, 8:8–21 (emphasis added).

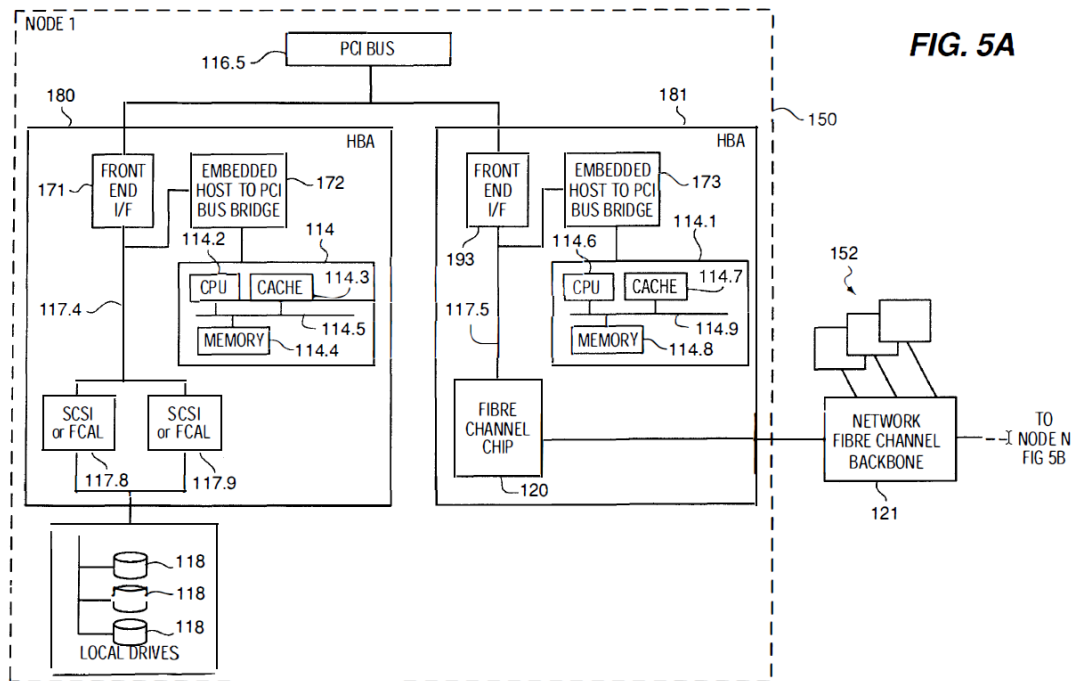
From this cited portion of Heil that refers to the functions of Fibre Channel backbone 121, it is unclear on this record whether Heil's Host to PCI Bus Bridge 115, PCI Bus 116.5, and Front End I/F 102 "cannot be" and "cannot serve" as a dedicated I/O channel, as Patent Owner contends. While Petitioner proffers the "dedicated I/O channel" as reading on Heil's Host To PCI Bus Bridge 115, PCI Bus 116.5, and Front End I/F 102 (*see* Pet. 22–23), Patent Owner's assertion appears to center on the function of Heil's network Fibre Channel Backbone 121, which is described as connecting various nodes, e.g., Node 1 150 and Node N 151, so that distributed CPUs (e.g., CPU 117.1 in Node 1 or CPU 126.1 in Node N) can access local drives (e.g., local drive 118 in Node 1 and local drive 123 in Node N) in another node via Fibre Channel Backbone 121.

¹¹ Although Patent Owner cites Heil at column 8, lines 8–18, we expand the citation to include lines 19–21 to highlight additional teachings of Heil.

We further note that Heil provides additional disclosure on the purpose and function of Fibre Channel Backbone 121.

In the preferred embodiment, each HBA in Node 1 150, Nodes 152, and Node N 151 are connected to the Fibre Channel backbone 121 via a Fibre Channel Chip such as 120, 122. The *Fibre Channel backbone 121 is used as the physical medium to “ship” the block level I/O requests among the HBAs and to exchange data associated with the shipped I/O requests.* In the preferred embodiment, one HBA has the processing power to support the local and remote storage channels of a node. In an alternative embodiment, due to design considerations, such as load balancing, at least one HBA can support the local storage channels and a separate HBA can support the remote storage channels within a node. This alternative embodiment distributes the I/O requests between the HBAs and reduces the workload on both HBAs within the node. FIG. 5A is a block diagram of such an embodiment.

Ex. 1006, 9:11–26. Figure 5A of Heil, provided below, illustrates HBA 181 being used to support accessing remote storage channels.



Heil – Fig. 5A

“As shown in FIG. 5A, Node 1 150 contains two HBAs 180 and 181. Both HBAs are connected together via PCI bus 116.5. HBA 180 processes I/O requests directed to the local drives 118. HBA181 supports the remote I/O requests. HBA 181 is connected to the network Fibre Channel backbone 121 via Fibre Channel Chip 120.” Ex. 1006, 9:27–32.

It appears that Patent Owner does not address the specific mapping of the “dedicated I/O channel” proffered by Petitioner and the additional teachings of Heil, and instead focuses only on inter-node communications between Node 1 and Node N via Fibre Channel backbone 121, for example.

In addition, Patent Owner argues that, because Heil teaches “the identified path is a **shared path** and that **load balancing and sharing** is advantageous over a dedicated path, . . . [Heil] **teaches away** from Patent Owner’s claimed invention.” Prelim. Resp. 14.

However, we note that “[t]eaching away is irrelevant to anticipation.” *Seachange International, Inc., v. C-Cor, Inc.*, 413 F.3d 1361, 1380 (Fed. Cir. 2005).

Accordingly, at this stage of the proceeding, on this record, and given our preliminary claim construction of the phrase “dedicated I/O channel,” *supra*, we find Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, for purposes of this Decision, Petitioner has shown sufficiently that Heil discloses limitation [1.a], notwithstanding Patent Owner’s arguments to the contrary.

[1.b]: “a second interface configured to receive first data via a network”

Petitioner contends “Heil discloses this limitation. Ex. 1004 ¶¶ 74–78. “Heil describes a second interface that receives first data via a network in the form of an interface between fibre channel chip 120 and network fibre channel backbone 121 that receives data from the fibre network (i.e., fibre channel backbone 121).” Pet. 24.

Petitioner’s assertions and explanations (*id.* at 24–25) are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil discloses limitation [1.b]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner’s showing. *See* Prelim. Resp. 12 *et seq.*

[1.c]: “a cache memory configured to store second data”

Petitioner contends, with reference to Figure 1 of Heil, “Heil discloses a cache memory for storing second data in the form of cache 117.2.” Pet. 26 (citing Ex. 1006, Fig. 1, 7:25–26).

Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil discloses limitation [1.c]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner’s showing. *See* Prelim. Resp. 12 *et seq.*

[1.d]: “a storage device configured to store third data ”

Petitioner contends with reference to Figure 1 of Heil, “Heil discloses a storage device memory for storing third data in the form of local

drives 118 and 123. . . . The data stored within the local drives comprises a third data.” Pet. 26–27 (citing Ex. 1006, Fig. 1, 10:14–20).

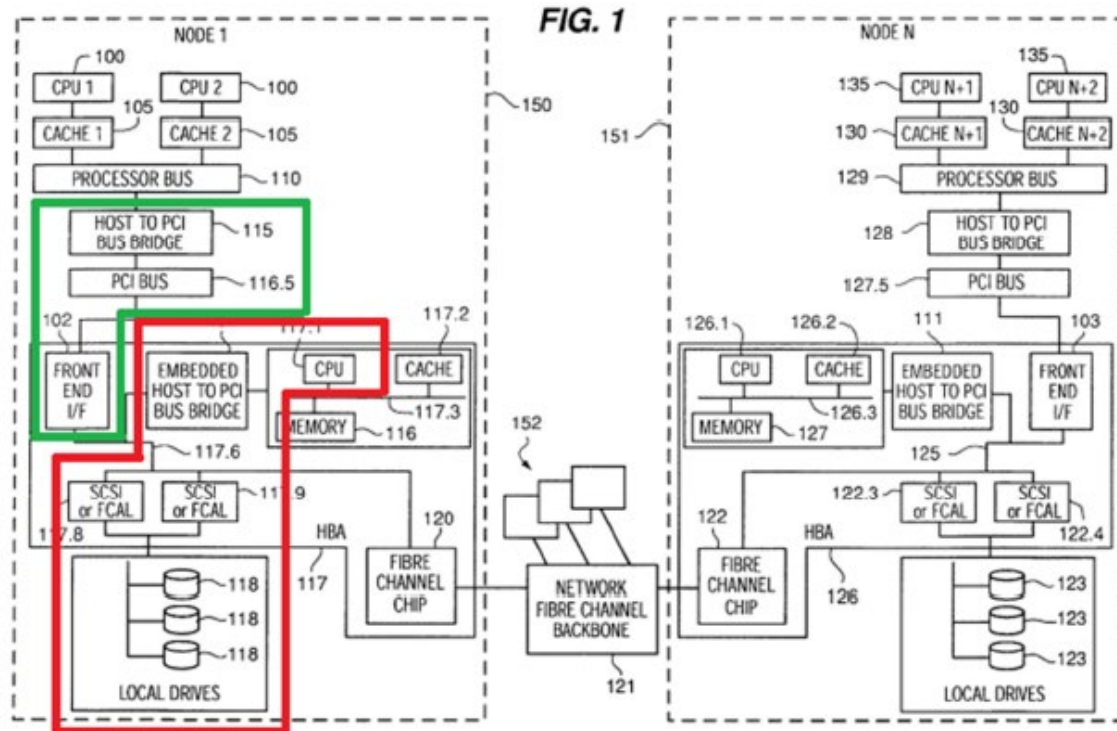
Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil discloses limitation [1.d]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner’s showing. *See* Prelim. Resp. 12 *et seq.*

[1.e]: “a processor coupled to the cache memory, the processor coupled to the storage device via a communication path that is distinct from the dedicated I/O channel, the processor configured to access the cache memory during processing of the I/O traffic”

Petitioner contends with reference to Figure 1 of Heil, “Heil discloses a processor (CPU 117.1) coupled to the cache memory (cache 117.2) and to a storage device (local drives 118).” Pet. 28 (citing Ex. 1006, Fig. 1, 7:9–11).

Heil’s Figure 1 shows that the communication path from the processor to the storage device—i.e., from the CPU 117.1 to the local drives 118 via a SCSI interface, annotated below in **red**—is distinct from the dedicated I/O channel—i.e., from the Node 1 host system to HBA 117 via a PCI bus, annotated in **green**[.]

Pet. 28; Ex. 1004 ¶ 89. Figure 1 of Heil, as annotated by Petitioner to emphasize this point with respect to limitation [1.e], is reproduced below (*see* Pet. 29) as an aid in understanding Petitioner’s mapping of this limitation to Heil:



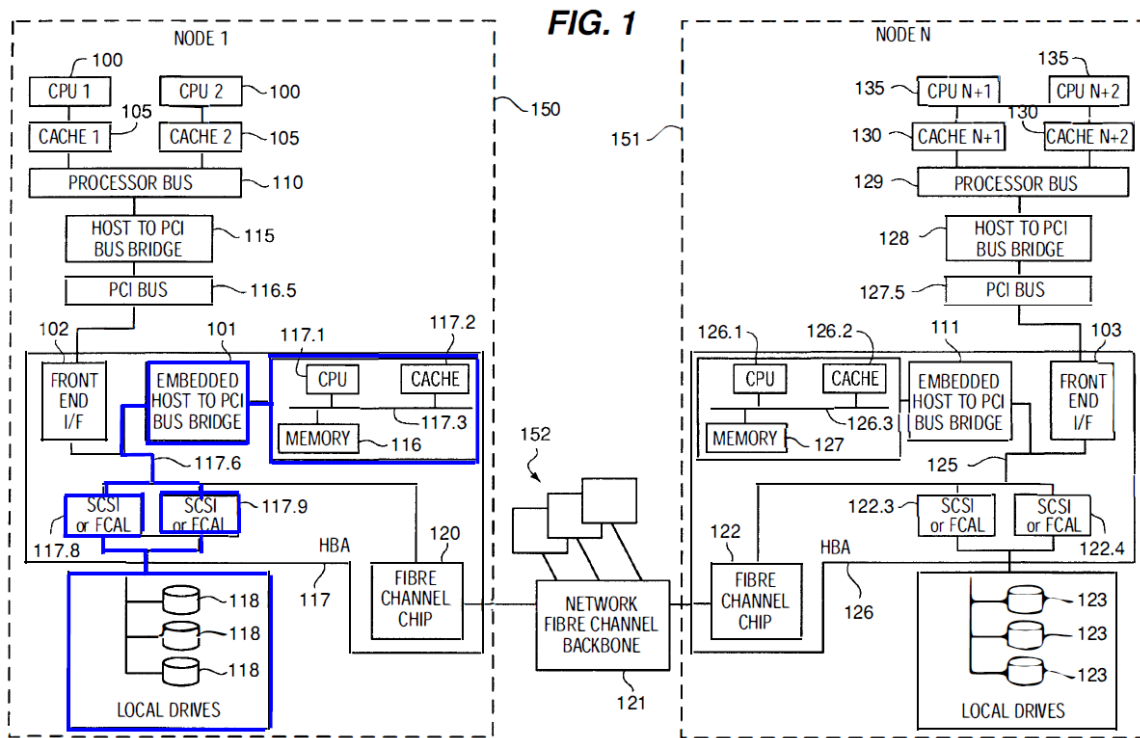
Heil – Fig. 1 (annotated) (Pet. 29)

Heil’s Figure 1, as annotated by Petitioner (*id.*), shows the communication bridge path from processor 117.1 to storage device 118 (shown in **red**), is distinct from the dedicated I/O channel shown in **green**, above. See Pet. 28–29; Ex. 1004 ¶ 89. In annotated Figure 1 above (and as seen more clearly in the Board’s annotated Figure 1, *infra*), the communication path from processor 117.1 to storage device 118 asserted by Petitioner as being distinct from the dedicated I/O channel passes through “EMBEDDED HOST TO PCI BUS BRIDGE” 101 to either HBA interface 117.8 or HBA interface 117.9 via PCI bus 117.6. See generally, Ex. 1006, 7:1–56.

Patent Owner responds, in part, by re-arguing limitation [1.a], i.e., “[i]t is clear that front-end interface 102 of Heil cannot be described as dedicated. Instead, front-end interface 102 connects to and is shared by various peripheral I/O devices, such as the local drives 118 and Fibre Channel Chip 120, to PCI bus 116.5.” Prelim. Resp.17. As for

limitation [1.e], Patent Owner contends, “front-end interface 102 connects Fibre Channel Chip 120, to PCI bus 116.5, and this connection makes front-end interface 102 part of the communication path from the processor to storage device. Thus, **the communication path from the processor to the storage device is not distinct in Heil** as stated by the Petitioner’s expert paragraph 89.” On this record, we disagree.

We provide our own annotation (in **blue**) of Heil Figure 1 below to clarify how we interpret Petitioner’s mapping of limitation [1.e] to Heil.¹²



Heil – Fig. 1 (annotated by Board)

¹² We note the panel’s annotation does not change what we understand to be Petitioner’s mapping as set forth in the Petition. Our annotated Figure 1 is provided merely to reduce the obscuration of relevant communication buses and their interconnection.

Our annotation of Heil Figure 1 is provided to clarify Petitioner’s mapping of limitation [1.e] to Heil,¹³ i.e., “Heil’s Figure 1 shows that the communication path from the processor to the storage device—i.e., from the CPU 117.1 to the local drives 118 via a SCSI interface . . . is distinct from the dedicated I/O channel—i.e., from the Node 1 host system to HBA 117 via a PCI bus.” Pet. 28.

On this record, Patent Owner asserts “front-end interface 102 connects Fibre Channel Chip 120, to PCI bus 116.5, *and this connection makes front-end interface 102 part of the communication path from the processor to storage device.* Thus, **the communication path from the processor to the storage device is not distinct in Heil.**” Prelim. Resp. 17 (*italics added*). We believe this statement is erroneous because, as seen in our annotated Figure 1 and Petitioner’s annotated Figure 1, Front End I/F 102 is ***not*** part of the communication path between CPU 117.1 and local drives 118.

Accordingly, at this stage of the proceeding, on this record, we find Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, for purposes of this Decision, Petitioner has shown sufficiently that Heil discloses limitation [1.e], notwithstanding Patent Owner’s arguments to the contrary.¹⁴

¹³ We note Petitioner’s annotation (Pet. 29) with **green** and **red** lines as shown above is somewhat unclear because Petitioner’s red lines obscure the communication path from processor 117.1 to local drives 118. Our annotation in **blue** seeks to clarify the relevant communication path by removing Petitioner’s original annotations, and replacing the colored lines with our own which we believe provide better exposition of the relevant communication paths.

¹⁴ Patent Owner again asserts that “Heil teaches away from a dedicated I[/]O channel.” Prelim. Resp. 17. We disagree because a teaching away argument is not applicable in anticipation. *See Seachange*, 413 F.3d at 1380.

[1.f]: “the processor further configured to perform an access operation at the storage device based on the I/O traffic”

Petitioner contends “Heil discloses that the processor (of the HBA) may access the storage device (the local drive) based on the I/O traffic. In response to an I/O request by CPU 100, the HBA may determine that the request may be serviced locally and retrieve the response data from the local disks.” Pet. 30 (citing Ex. 1006, 7:36–37).

Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil discloses limitation [1.f]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner’s showing. *See* Prelim. Resp. 12 *et seq.*

Conclusion

For the reasons provided above, Petitioner has sufficiently shown that Heil anticipates independent claim 1. We have considered Patent Owner’s arguments that Petitioner’s arguments are insufficient with respect to limitations [1.a] and [1.e], but at this stage and on this record, we do not agree.

Accordingly, we are persuaded that Petitioner has shown a reasonable likelihood that it would prevail in establishing that the subject matter of claim 1 is anticipated by Heil.

2. Independent/Dependent Claims 2, 3, 7–12, and 19–23

Petitioner also contends that the subject matter of independent claim 19 and dependent claims 2, 3, 7–12, and 19–23 are anticipated by Heil. *See* Pet. 31–43. Petitioner substantiates its contentions with analysis

that addresses each claim limitation and identifies supporting evidence, relying on its analysis of claim 1. *See id.*

Other than its arguments presented regarding claim 1, Patent Owner does not, at this stage, dispute Petitioner’s arguments, analysis, or evidence for dependent claims 2, 3, and 7–12. *See* Prelim. Resp. 18 (“These claims are valid because each depends from valid claim 1 and recites additional subject matter.”). Patent Owner also argues independent claim 19 is not anticipated for reasons commensurate with arguments presented with respect to independent claim 1. *See* Prelim. Resp. 18–19. Furthermore, Patent Owner argues dependent claims 20–23, depending from claim 19, are not anticipated due to their dependency from independent claim 19. Prelim. Resp. 19 (“Claims 20-23 are valid at least for the reason that each depends from valid claim 19 and recites additional subject matter.”).

These arguments are unavailing at this stage of the proceeding for the reasons explained above with respect to independent claim 1. *See supra* § III.E.1. As cited above, Patent Owner does not otherwise dispute Petitioner’s arguments, analysis, or evidence for these claims at this stage.

On this record, we are persuaded that Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenges to claims 2, 3, 7–12, and 19–23 as anticipated by Heil.

F. Ground 2: Anticipation of claims 10 and 11 by Heil Under § 102(b)

Claims 10 and 11 recite:

10. The apparatus of claim 1, wherein the processor is further configured to route the read command to the cache memory or to the storage device.

11. The apparatus of claim 1, further comprising:

configuration manager circuitry configured to route an I/O request included in the I/O traffic to the cache memory, to route the I/O request to the storage device, or to deny the I/O request;

front-end circuitry configured to process the I/O request;
and

back-end circuitry configured to perform a read operation or a write operation at the storage device based on the I/O request.

Ex. 1001, 9:58–10:3.

Petitioner asserts, using the same analysis proffered with respect to the Ground 1 challenge under 35 U.S.C. § 102(e) of claims 10 and 11 (*see* Pet. 38–40), that claims 10 and 11 are also anticipated under 35 U.S.C. § 102(b). Pet. 43–44.

With reference to the prosecution history of the '092 patent (*see* Pet. 8–11; *see also* Ex. 1002 and Ex. 1003), Petitioner contends Heil qualifies as prior art under 35 U.S.C. § 102(b) because claims 10 and 11 of the '092 patent are not entitled to the earliest effective filing date of January 22, 1999, of application 09/236,409, the earliest filed application in the '092 patent family, but instead is only entitled to the March 5, 2003, filing date of U.S. Application No. 10/382,016, the first child application of the 09/236,409 Application.

Patent Owner does not substantively rebut Petitioner's allegations, but merely states "Heil does not anticipate claims 10–11 . . . because each depends from valid claim 1 and recites additional subject matter." Prelim. Resp. 19.

Petitioner's assertions and explanations, unrebutted at this stage and on this record, appear to be consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that

Heil discloses all the limitations of claims 10 and 11. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner's showing.

However, to the extent it may become relevant at trial, we invite the parties to submit additional briefing on this matter, or otherwise further address dependent claims 10 and 11 during trial, as permitted by our rules.

Lacking Patent Owner rebuttal, on this record, we are persuaded that Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenge under Ground 2 to claims 10 and 11 under 35 U.S.C. § 102(b).

G. Ground 3: Obviousness of Claims 1–3 and 6–24 under § 103(a) over Heil and Nakayama

Petitioner contends that the subject matter of claims 1–3 and 6–24 would have been obvious over the combination of Heil and Nakayama. Pet. 44–72. Patent Owner argues that Petitioner's showing is insufficient. Prelim. Resp. 20–24.

We have considered the parties' arguments and the evidence presented at this stage, and we address them in the context of representative claim 13. For the reasons explained below, we determine that Petitioner has demonstrated a reasonable likelihood that it would prevail in showing that the subject matter of claim 13 would have been obvious over the combination of Heil and Nakayama, notwithstanding Patent Owner's arguments to the contrary.

1. Independent Claim 13

[13.pre]: “A method comprising:”

Petitioner contends Heil discloses the preamble. Pet. 51. According to Petitioner, “Heil discloses a method of data storage and teaches the preamble.” *Id.* (citing Ex. 1006, 1:9–14; *see also* Ex. 1004, ¶ 208).

Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil teaches the claim’s preamble.¹⁵ At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner’s showing. *See* Prelim. Resp. 20 *et seq.*

[13.a]: “receiving input/output (I/O) traffic from a host device via a dedicated I/O channel at a first interface, the I/O traffic comprising a write command;”

Next, addressing the limitations recited in the body of the claim, Petitioner contends that Heil discloses the portion of limitation [13.a] that recites “receiving input/output (I/O) traffic from a host device via a dedicated I/O channel at a first interface.” Pet. 51; *and see* Pet. 21–24 (discussing commensurate limitation [1.a] in claim 1). According to Petitioner, Heil in Figure 1 discloses this step by describing a first interface that receives I/O traffic, i.e., I/O requests, from a host device via either Host to PCI bus bridge 115 and PCI bus 116.5, or via Front End I/F 102. Pet. 22–

¹⁵ We need not determine whether the preamble is limiting because Petitioner has sufficiently shown that Heil discloses this aspect of the claim and Patent Owner does not rebut this assertion. *See Vivid Techs.*, 200 F.3d at 803; *see generally* Prelim. Resp. 20 *et seq.*

23 (citing Ex. 1006, 6:35–40, 7:36–37; Ex. 1004 ¶¶ 69, 71). *See* Pet. 23, 55 (both providing annotated Figure 1 of Heil); *see also* § III.E.1, *supra*.

“Nakayama discloses a similar data storage architecture as Heil in which a host computer 300 is connected via channel 301 (which may be a SCSI bus control, as seen at 304) to a disk control 302 having a cache memory 309 as shown in Nakayama’s Figure 3.” Pet. 52; *see also* § III.D.2, *supra*.

Petitioner relies upon Nakayama as teaching the claimed “write command,” and “[t]o the extent Heil describes I/O requests between its host computers and HBAs as ‘access requests’ and does not explicitly describe the access requests using the term ‘write command,’ Nakayama explicitly teaches that the host computers may provide access requests in the form of read and write requests to storage including cache memory and disk drive.” Pet. 52–53 (citing Ex. 1007, 3:66–4:25, 4:48–51, 4:61–65; Ex. 1004 ¶ 213).

Similar to limitation [1.a] of claim 1 addressed in Ground 1, above, for limitation [13.a], Petitioner relies upon the communication channel used by PCI bus bridge 115 and PCI bus 116.5 through Front End I/F 102 to teach a dedicated I/O channel in the form of a direct, dedicated connection between the host and the HBA that carries I/O traffic. Pet. 24 (citing Ex. 1006, 6:35–40, 7:36–37; Ex. 1004 ¶ 72).¹⁶

Patent Owner’s declarant asserts “Heil does not teach or suggest element[] [1.a] . . . as I have explained above. Nakayama does not cure the

¹⁶ Under our preliminary claim construction of the phrase “dedicated I/O channel,” we interpret “dedicated I/O channel” as a channel that is *used exclusively for a certain type of data*, i.e., I/O requests, thus encompassing load sharing configurations that share the I/O channel between multiple CPUs and I/O peripheral devices for communication of I/O requests. *See* § III.C, *supra*.

deficiencies of Heil with regard to these elements. . . . Heil and Nakayama do not render [13.a] . . . obvious for at least the same reasons that Heil and Nakayama do not render elements [1.a] . . . obvious.” Ex. 2001 ¶¶ 65–66.

Patent Owner contends “Heil and Nakayama do not and cannot render [element] [13.a] . . . obvious for at least the same reasons that Heil and Nakayama do not render element[] [1.a] obvious. The asserted combination of Heil and [Nakayama] is not proper and cannot be relied on by [Petitioner].” Prelim. Resp. 21.

Patent owner further argues “Heil affirmatively teaches away from a dedicated I/O channel as claimed by Patent Owner. . . . It is improper to combine references where the references teach away from their combination.” Prelim. Resp. 20 (citing Ex. 2001 ¶ 61).

With respect to limitation [1.a] under Ground 3, Patent Owner’s declarant asserts, with respect to the recited phrase “dedicated I/O channel,” that “Heil affirmatively teaches away from a dedicated I/O channel as claimed by Patent Owner. I am given to understand that it is improper to combine references where the references teach away from their combination.” Ex. 2001 ¶ 61.

Turning back to Patent Owner’s assertion under anticipation Ground 1 specifically arguing that Heil teaches away from the claimed invention, Patent Owner contends “Heil teaches use of a shared path and **teaches away from a dedicated I/O channel**, as recited in each of the independent claims of the ‘092 patent.” Prelim. Resp. 14. In this regard, Patent Owner’s declarant opines:

Heil thus teaches that the identified path is a shared path and that load balancing and sharing is advantageous over a dedicated path, and hence teaches away from Patent Owner’s claimed invention. In particular, Heil teaches use of a shared

path and teaches away from a dedicated I/O channel, as in each of the independent claims of the '092 patent. (See claim 1 element 1.A as an example). Heil does not just offer an alternative or “preferred” solution, but expressly cautions against the very solution proposed (by the claimed invention).

Ex. 2001 ¶ 46.

Our reviewing court has held “[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.”

Ricoh Co. v. Quanta Computer Inc., 550 F.3d 1325, 1332 (Fed. Cir. 2008) (citations omitted). A reference does not teach away if it merely expresses a general preference for an alternative invention from amongst options available to the ordinarily skilled artisan, and the reference does not discredit or discourage investigation into the invention claimed. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

At this stage of the proceeding, contrary to Patent Owner’s assertion, we find Heil does not teach away from the invention of claim 13 in light of our preliminary claim construction of the phrase “dedicated I/O channel” that encompasses load sharing configurations that share the I/O channel between multiple CPUs and I/O peripheral devices for communication of I/O requests, and based on Patent Owner’s argument above that Heil teaches use of a shared path. *See* §§ III.C, III.E, *supra*.

Accordingly, at this stage of the proceeding, on this record, and given our preliminary claim construction of the phrase “dedicated I/O channel,” *supra*, we find Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, for purposes of this Decision, Petitioner has shown sufficiently that the

combination of Heil and Nakayama teaches or suggests limitation [13.a], notwithstanding Patent Owner's arguments to the contrary.

[13.b]: "receiving first data via a network at a second interface"

Petitioner contends (Pet. 53) "Heil discloses element [13.b]," with reference to the analysis regarding limitation [1.b] under anticipation Ground 1. *See* Pet. 24–25; Ex. 1004 ¶¶ 74–78. "Heil describes a second interface that receives first data via a network in the form of an interface between fibre channel chip 120 and network fibre channel backbone 121 that receives data from the fibre network (i.e., fibre channel backbone 121)." Pet. 24.

Petitioner's assertions and explanations (*id.* at 24–25) are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil teaches limitation [13.b]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner's showing. *See* Prelim. Resp. 20 *et seq.*

[13.c]: "storing second data at a cache memory"

Similar to limitation [1.c] of claim 1 under anticipation Ground 1, Petitioner contends "Heil discloses element 13.c." Pet. 53 (citing analysis of element [1.c] found at Pet. 26). Petitioner further asserts "Heil in view of Nakayama renders obvious storing data (i.e., writing data) to a cache. *See* claim 6." Pet. 53 (citing Pet. 48); Ex. 1007, 6:30–38.

Petitioner's assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil teaches limitation [13.c]. At this stage, Patent

Owner does not allege any deficiencies in this aspect of Petitioner's showing. *See* Prelim. Resp. 20 *et seq.*

[13.d]: “storing third data at a storage device”

Similar to limitation [1.d] of claim 1 under anticipation Ground 1, Petitioner contends “Heil discloses element 13.d.” Pet. 53 (citing analysis of element [1.d] found at Pet. 26–27). Petitioner further asserts “Heil in view of Nakayama renders obvious storing data (i.e., writing data) to disk storage. *See* claim 6.” Pet. 53 (citing Pet. 48); Ex. 1007, 7:3–10.

Petitioner contends with reference to Figure 1 of Heil, “Heil discloses a storage device memory for storing third data in the form of local drives 118 and 123. . . . The data stored within the local drives comprises a third data.” Pet. 26–27 (citing Ex. 1006, Fig. 1, 10:14–20).

Petitioner's assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil teaches limitation [13.d]. At this stage, Patent Owner does not allege any deficiencies in this aspect of Petitioner's showing. *See* Prelim. Resp. 20 *et seq.*

[13.e]: “accessing the cache memory during processing of the I/O traffic”

Similar to a portion of limitation [1.e] of claim 1 under anticipation Ground 1, i.e., “the processor configured to access the cache memory during processing of the I/O traffic,” Petitioner contends “Heil discloses element 13.e. *See* element 1.e.” Pet. 53 (citing analysis of element [1.e] found at Pet. 27–30). Petitioner contends with reference to Figure 1 of Heil:

Heil further discloses that the processor may access cache memory while processing I/O traffic, including as a result

of processing the I/O command transmitted in the I/O traffic. Ex. 1006, 5:25–28 (“Performance is further enhanced in that each intelligent HBA can provide disk caching of the local disks under its control, and can service hits out of this cache regardless of whether the requesting host is local or remote.”), 7:24–28 (“To improve I/O performance, CPU 117.1 temporarily caches disk data in cache memory 117.2 that is frequently accessed.”); Ex. 1004, ¶ 90 (“[A person of ordinary skill in the art (POSITA)] would understand from these disclosures that the cache memory would be accessed to retrieve data responsive to the I/O request. The processor (CPU 117.1 of the HBA) may access cache memory while processing I/O traffic, including after processing an I/O command transmitted in the I/O traffic.”).

Pet. 29–30 (discussing the portion of limitation [1.e] that is commensurate with limitation [13.e]).

Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that Heil teaches limitation [1.d]. At this stage, Patent Owner does not substantively argue deficiencies in this aspect of Petitioner’s showing other than generally to assert “Petitioner argues that Heil discloses this element [13.f] and refers back to Petitioner’s arguments regarding element [1.e]. . . . [and] Heil does not teach or suggest elements [1.a] or [1.e], for the reasons provided above. In fact, Heil teaches away from these claimed features.¹⁷ Nakayama does not cure the deficiencies of Heil with regard to these elements.” See Prelim. Resp. 21.

¹⁷ We have addressed Patent Owner’s unpersuasive “teaching away” argument, *supra*. See § III.G.1 (addressing Patent Owner’s teaching away argument in connection with limitation [13.a]).

On this record, for purposes of this Decision, Petitioner has shown sufficiently that the combination of Heil and Nakayama teaches limitation [13.f], notwithstanding Patent Owner’s arguments to the contrary

[13.f]: “performing one or more access operations at the storage device based on the I/O traffic, the one or more access operations utilizing a communication path between a processor and the storage device, the communication path distinct from the dedicated I/O channel”

Petitioner asserts “Heil discloses element 13.f. See element 1.e . . . and element 1.f. . . . Heil discloses that the processor (of the HBA) may access the storage device (the local drive) based on the I/O traffic.” Pet. 53–54 (citing Pet. 27–30).

Similar to limitation [1.e], Petitioner contends:

Heil’s Figure 1 shows that the access operations at the storage device utilize a communication path from the processor to the storage device—i.e., from the CPU 117.1 to the local drives 118 via a SCSI interface, annotated below in **red**—that is distinct from the dedicated I/O channel—i.e., from the Node 1 host system to HBA 117 via a PCI bus, annotated in **green**[.]

Pet. 54; Ex. 1004 ¶ 89. Figure 1 of Heil, as annotated by Petitioner to emphasize this point with respect to limitations [1.e] and [13.e], is reproduced above. See § III.E.1 (addressing limitation [1.e]).

Heil’s Figure 1, as annotated by Petitioner (Pet. 29), shows the communication path from processor 117.1 to storage device 118 (shown in **red**), is distinct from the dedicated I/O channel shown in **green**, above. See Pet. 28–29; Ex. 1004 ¶ 89.

With respect to limitation [13.f], Patent Owner states “Heil and Nakayama do not and cannot render [13.a] and [13.f] obvious for at least the

same reasons that Heil and Nakayama do not render elements [1.a] or [1.e] obvious. The asserted combination of Heil and [Nakayama] is not proper and cannot be relied on by [Petitioner].” Prelim. Resp. 21

With respect to limitations [1.a] and [1.e], Patent Owner argues:

As shown above, Heil does not teach or suggest elements [1.a] or [1.e] Nakayama does not cure the deficiencies of Heil with regard to these elements. See EXH2001, ¶ [0061]. Petitioner does not argue that Nakayama teaches or suggests a dedicated I/O channel. As noted, Heil affirmatively teaches away from a dedicated I/O channel as claimed by Patent Owner. See EXH2001, ¶ [0061].

Prelim. Resp. 20.

We have addressed Patent Owner’s teaching away arguments above in connection with limitation [13.a].

On this record, for purposes of this Decision, Petitioner has shown sufficiently that Heil teaches limitation [13.f], notwithstanding Patent Owner’s arguments to the contrary.

Motivation to Combine Heil and Nakayama

Petitioner asserts it would have been obvious to a person of ordinary skill in the art to combine Heil and Nakayama with a reasonable expectation of success because these references are both in the same field of invention, and disclose similar architectures with respect to cache and storage. Pet. 44 (citing Ex. 1004 ¶¶ 158–163). According to Petitioner, a skilled artisan would have known that both references disclose methods of reading and writing to cache and disk storage, i.e., specific types of I/O requests, and both references recognize the important contribution of cache storage to storage technology. *Id.* Petitioner provides additional arguments concerning the motivation to combine Heil with Nakayama. *See id.* at 44–45.

Other than a general statement that “[t]he asserted combination . . . is not proper and cannot be relied on by [Petitioner],” and that Heil purportedly teaches away from limitations [13.a] and [13.f] (Prelim. Resp. 21), Patent Owner argues “Heil affirmatively teaches away from a dedicated I/O channel as claimed by Patent Owner.” Prelim. Resp. 20–21 (citing Ex. 2001 ¶ 61). On this record, as addressed above, we are not persuaded that Heil teaches away from the invention of claim 13.

Accordingly, at this stage of the proceeding, on this record, we find Petitioner’s assertions and explanations are consistent with and supported by the evidence cited by Petitioner. At this stage, as discussed above, Patent Owner repeats previous arguments, i.e., “Heil and Nakayama do not and cannot render [13.a] and [13.f] obvious for at least the same reasons that Heil and Nakayama do not render elements [1.a] or [1.e] obvious. The asserted combination of Heil and [Nakayama] is not proper and cannot be relied on by [Petitioner].” *See* Prelim. Resp. 21.

On this record, for purposes of this Decision, Petitioner has shown sufficiently that a person of ordinary skill in the art would have been motivated to combine Heil and Nakayama to arrive at the subject matter recited in claim 13.

Conclusion

For the reasons provided above, Petitioner has sufficiently shown that the combination of Heil and Nakayama renders independent claim 13 obvious. We have considered Patent Owner’s arguments that Petitioner’s arguments are insufficient with respect to limitations [13.a] and [13.f], but at this stage and on this record, we do not agree.

Accordingly, we are persuaded that Petitioner has shown a reasonable likelihood that it would prevail in establishing that the subject matter of

claim 13 would have been obvious over the combination of Heil and Nakayama.

*H. Ground 4: Obviousness of Claim 4 under § 103(a)
over Heil, Nakayama, and Gulick*

Claim 4 recites, “[t]he apparatus of claim 1, wherein the dedicated I/O channel comprises a small computer system interface (SCSI) channel.”

Ex. 1001, 9:40–42.

Petitioner contends:

It would have been obvious for a POSITA to combine Heil, Nakayama, and Gulick with a reasonable chance of success. . . . A POSITA at the time of invention would understand that PCI is a standardized format of local computer buses for attaching hardware devices to a computer and further understand that SCSI is a standard for connecting, interfacing, and transferring data between computers and peripheral devices.

Pet. 73 (citing Ex. 1004 ¶¶ 298–299).

Petitioner’s assertions and explanations (Pet. 73–75) are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that the combination of Heil, Nakayama, and Gulick teaches the limitations of claim 4. At this stage, Patent Owner alleges deficiencies in this aspect of Petitioner’s showing by reiterating arguments addressed in connection with limitations [1.a] and [1.e] of claim 1, and by stating that Gulick does not make up for these purported deficiencies, such that claim 4 is not obvious over the reference combination. *See* Prelim. Resp. 24–25. On this record, for the reasons stated above with respect to claim 1 (Ground 1) and our analysis of claim 13 (Ground 3), we are not persuaded that Petitioner’s arguments are deficient.

Accordingly, we are persuaded that Petitioner has shown a reasonable likelihood that it would prevail in establishing that the subject matter of claim 4 is obvious over the combination of Heil, Nakayama, and Gulick.

I. Ground 5: Obviousness of Claim 5 under § 103(a) over Heil, Nakayama, and Berman

Claim 5 recites, “[t]he apparatus of claim 1, wherein the second interface comprises an Ethernet interface or an asynchronous transfer mode (ATM) interface.” Ex. 1001, 9:43–45.

Petitioner contends, “It would have been obvious for a POSITA to combine Heil, Nakayama, and Berman with a reasonable chance of success. . . . A POSITA would have known that it is desirable to interface fibre channels such as Heil’s with Ethernet.” Pet. 75 (citing Ex. 1004 ¶¶ 309–310).

Petitioner’s assertions and explanations (*id.* at 75–76) are consistent with and supported by the evidence cited by Petitioner. On this record, Petitioner has shown sufficiently that the combination of Heil, Nakayama, and Berman teaches the limitations of claim 5.

At this stage, Patent Owner alleges deficiencies in this aspect of Petitioner’s showing by reiterating arguments addressed in connection with limitations [1.a] and [1.e] of claim 1, and by stating that Nakayama and Berman do not make up for the purported deficiencies of Heil, such that claim 5 is not obvious over the reference combination. *See* Prelim. Resp. 25. On this record, for the reasons stated above with respect to claim 1 (Ground 1) and our analysis of claim 13 (Ground 3), we are not persuaded that Petitioner’s arguments are deficient.

Accordingly, we are persuaded that Petitioner has shown a reasonable likelihood that it would prevail in establishing that the subject matter of claim 5 is obvious over the combination of Heil, Nakayama, and Berman.

IV. CONCLUSION

As explained above, we determine that Petitioner has established a reasonable likelihood of prevailing in its challenge to at least one claim of the '092 patent. Thus, we institute an *inter partes* review of all challenged claims on all asserted grounds.

Our factual findings, conclusions of law, and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. Our final decision as to the patentability of challenged claims will be based on the record developed during trial, including any response timely filed by Patent Owner. Any arguments not raised by Patent Owner in a timely filed response may be deemed waived.

V. ORDER

It is:

ORDERED that an *inter partes* review is instituted on all of the challenged claims, i.e., claims 1–24 of the '092 patent, on all corresponding grounds of unpatentability as specified in the Petition and identified in the Table in Section II.D. of this Decision; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '092 patent shall commence on the entry date of this Decision, and notice is hereby given of the institution of a trial.

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