AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	2/8/2022	District of Delaware

PLAINTIFF	DEFENDANT
Sentient Sensors, LLC	Xilinx Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 6,938,177 B1	8/30/2005	Sentient Sensors, LLC
2			
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In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

XILINX 1010

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas, Austin Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:16-cv-1280-SS	12/7/2016	Western District of Texas, Austin Division

PLAINTIFF	DEFENDANT
Blemel Technologies LLC	National Instruments Corporation

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 see attached		
2 6,938,177		
3		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Jeannette J. Clack	Amanda Deichert	DEC 08 2016

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the District of Delaware on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	10/4/2019	for the District of Delaware

PLAINTIFF	DEFENDANT
SENTIENT SENSORS, LLC	CYPRESS SEMICONDUCTOR CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 6,938,177 B1	8/30/2005	Kenneth Blemel
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In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
Dismissed - see attached

CLERK	(BY) DEPUTY CLERK	DATE
John A. Cerino	/s/ Mark D. Buckson, Jr.	9/2/2021

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
	10/4/2019	for the District of Delaware

PLAINTIFF	DEFENDANT
SENTIENT SENSORS, LLC	CYPRESS SEMICONDUCTOR CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 6,938,177 B1	8/30/2005	Kenneth Blemel
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of TEXAS (Marshall) on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:18-cv-00121	3/30/2018	Eastern District of TEXAS (Marshall)

PLAINTIFF	DEFENDANT
Sentient Sensors, LLC	MICROSEMI CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,938,177	8/30/2005	Sentient Sensors, LLC
2			
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
ORDERED that all of Plaintiff's claims against Defendants are dismissed with prejudice.

CLERK	(BY) DEPUTY CLERK	DATE
David A. O'Toole	ch	**4/17/19**

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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of TEXAS (Marshall) on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:18-cv-00121	3/30/2018	Eastern District of TEXAS (Marshall)

PLAINTIFF	DEFENDANT
Sentient Sensors, LLC	MICROSEMI CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,938,177	8/30/2005	Sentient Sensors, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

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Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of TEXAS (Marshall) on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:18-cv-00121	3/30/2018	Eastern District of TEXAS (Marshall)

PLAINTIFF	DEFENDANT
Sentient Sensors, LLC	MICROSEMI CORPORATION

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,938,177	8/30/2005	Sentient Sensors, LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:16-cv-1280-SS	12/7/2016	Western District of Texas, Austin Division

PLAINTIFF	DEFENDANT
Blemel Technologies LLC	National Instruments Corporation

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Jeannette J. Clack	Amanda Deichert	DEC 08 2016

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AO 120 (Rev. 08/10)

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:15cv134	2/3/2015	Eastern District of Texas, Marshall Division

PLAINTIFF	DEFENDANT
Blemel Technologies LLC	National Instruments Corporation

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,938,177	8/30/2005	Sentient Sensors LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

MICHAEL E. JONES
JOHN F. BUFE
JAMES L. HEDRICK
E. GLENN THAMES, JR.
ALLEN F. GARDNER
D. TIMOTHY SIMPSON
RONALD D. STUTES
J. MATT ROWAN
PATRICK C. CLUTTER, IV
DANIEL A. NOTEWARE, JR.
HA H. KUMMERFELD
PATRICK C. BELL

OF COUNSEL:
JOHN H. MINTON
RANDALL L. ROBERTS
HON. DIANE V. DeVASTO
DOUGLAS R. McSWANE, JR.

CHARLES F. POTTER
1909-1999

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TYLER, TEXAS
75702

TELEPHONE
903.597.8311

FACSIMILE
903.593.0846

WWW.POTTERMINTON.COM

February 3, 2015

Mail Stop 8
Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

RE: Civil Action No. 2:15cv134; *Blemel Technologies LLC v. National Instruments Corporation;* In the US District Court for the Eastern District of Texas, Marshall Division

Dear Sir or Madam:

Please find enclosed patent form A120, the Report on the Filing of an Action regarding a Patent for the above referenced matter, 2:15cv134.

Please contact our office should you have any questions or concerns.

With kindest regards, I am

Very truly yours,

Jo Vallery, Litigation Case Manager for
Michael E. Jones

/jv
Enc.

{A07/09727/0001/W1272566.1 }

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,177 B1
DATED : August 30, 2005
INVENTOR(S) : Blemel

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [57], **ABSTRACT**,
Lines 2-3, "incorporate" should be -- incorporates --.

Column 1,
Line 7, "tis" should be -- this --.
Line 14, "multi-hip" should be -- multi-chip --.
Line 39, "output" should be -- outputs --.
Line 49, "bee" should be -- been --.

Column 2,
Line 5, "multilayer" should be -- multi-layer --.
Line 60, "feature" should be -- features --.

Column 3,
Line 41, "embodiment" should be -- embodied --.
Line 47, "input" should be -- inputs --.

Column 5,
Line 34, "converts" should be -- converters --.
Line 43, "sale" should be -- scale --.
Line 57, "a synchronous" should be -- asynchronous --.

Column 6,
Line 22, "nonvolatile" should be -- non-volatile --.
Lines 26 and 32, "preened" should be -- preferred --.
Line 48, "he" should be -- the --.

Column 7,
Line 17, "cryst" should be -- crystal --.
Line 33, "to" should be -- timing --.
Line 38, "intended" should be -- integrated --.

Column 8,
Line 2, "FGA" should be -- FPGA --.

Column 9,
Line 22, "digital" should be -- digitized --.
Line 32, after "to" delete "of".
Line 34, "microlight" should be -- micro-light --.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,177 B1
DATED : August 30, 2005
INVENTOR(S) : Blemel

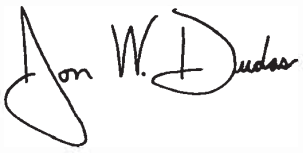
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 11,
Line 1, "digita" should be -- digital --.

Column 12,
Line 16, after "portion of" insert -- the gates in --.
Line 18, "conducing" should be -- conducting --.
Line 37, "potion" should be -- portion --.

Signed and Sealed this

Twenty-fourth Day of January, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

10/028556

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SHEPPARD MULLIN
SHEPPARD MULLIN RICHTER & HAMPTON LLP
ATTORNEYS AT LAW

48th Floor | 333 South Hope Street | Los Angeles, CA 90071-1448
213-620-1780 office | 213-620-1398 fax | www.sheppardmullin.com

Certificate

FACSIMILE COVER SHEET

NOV 17 2005

*** THIS FACSIMILE TRANSMISSION WILL NOT BE MAILED ***

of Correction

Date: November 11, 2005	File Number: 097Y-084435	
Total number of pages: (including 1-page cover sheet) 3	If all pages are not received, please call Sheppard Mullin at 213-620-1780, ext. 2155	

TO:	Facsimile No.	Telephone No.
U.S. Patent and Trademark Office	(571) 273-8300	

Rec'd 1:10

From: James R. Brueggemann, Esquire Direct Dial: 213-617-4156

Re: Transmittal of Certificate of Correction

MESSAGE: Please see attached.

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on November 11, 2005.

James R. Brueggemann, Esquire

Transmittal of Certificate of Correction (2 pages)
Inventors: Kenneth Blemel
Title: MULTI-CHIP MODULE SMART CONTROLLER...
Patent No.: 6,938,177 Issued: August 30, 2005
Our Docket No.: 097Y-084435 **Date Faxed: 11/11/05**
Client: Sentient Sensors
Atty/Sec.: BrueggemannKemp

NOTE: THIS MESSAGE IS INTENDED ONLY FOR THE USE OF THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED, AND MAY CONTAIN INFORMATION THAT IS PRIVILEGED, CONFIDENTIAL AND EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAW. IF THE READER OF THIS MESSAGE IS NOT THE INTENDED RECIPIENT, OR THE EMPLOYEE OR AGENT RESPONSIBLE FOR DELIVERING THE MESSAGE TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT ANY DISSEMINATION, DISTRIBUTION OR COPYING OF THIS COMMUNICATION IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS COMMUNICATION IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE TO US AT THE ABOVE ADDRESS VIA THE U.S. POSTAL SERVICE. THANK YOU.

NOV 18 2005

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : **6,938,177**
DATED : **August 30, 2005**
INVENTOR(S) : **Kenneth Blemel**

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, in the Abstract, "incorporate" should be -- incorporates --.

At column 1, line 7, "tis" should be --this --.

, line 14, "multi-hip" should be -- multi-chip --.

, line 39, "output" should be -- outputs --.

, line 49, "bee" should be -- been --.

At column 2, line 5, "multilayer" should be --multi-layer --.

, line 60, "feature" should be -- features --.

At column 3, line 41, "embodiment" should be -- embodied --.

, line 47, "input" should be -- inputs --.

At column 5, line 34, "converts" should be -- converters --.

, line 43, "sale" should be -- scale --.

, line 57, " a synchronous" should be -- asynchronous --.

At column 6, line 22, "nonvolatile" should be -- non-volatile --.

MAILING ADDRESS OF SENDER (Please do not use customer number

PATENT NO. 6,938,177

James R. Brueggemann, Esquire
Sheppard, Mullin, Richter & Hampton LLP
333 South Hope Street, 48th Floor
Los Angeles, California 90071
(213) 620-1780

No. of additional copies

PAGE 2/3 * RCVD AT 11/11/2005 4:10:18 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:213 620 1398 * DURATION (mm-ss):01-06

NOV 18 2005

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NOV 11 2005

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,177
DATED : August 30, 2005
INVENTOR(S) : Kenneth Blemel

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

, line 26, "preened" should be -- preferred --.

, line 32, "preened" should be -- preferred --.

, line 48, "he" should be -- the --.

At column 7, line 17, "cryst" should be -- crystal --.

, line 33, " to" should be -- timing --.

, line 38, "intended" should be -- integrated --.

At column 8, line 2, "FGA" should be -- FPGA --.

At column 9, line 22, "digital" should be -- digitized --.

, line 32, after "to" please delete -- of --.

, line 34, "microlight" should be -- micro-light --.

At column 11, line 1, "digita" should be -- digital --.

At column 12, line 16, after "portion of" please insert -- the gates in --.

, line 18, "conducing" should be -- conducting --.

, line 37, "potion" should be -- portion --.

MAILING ADDRESS OF SENDER (Please do not use customer number

James R. Brueggemann, Esquire
Sheppard, Mullin, Richter & Hampton LLP
333 South Hope Street, 48th Floor
Los Angeles, California 90071
(213) 620-1780

PATENT NO. 6,938,177

No. of additional copies

P1S/REV03

NOV 18 2005

OIPE
APR 15 2005
PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/14/2005

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles, CA 90071

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

Brian D. Martin, Esquire	(Depositor's name)
Brian D. Martin	(Signature)
April 15, 2005	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

TITLE OF INVENTION: MULTI-CHIP MODULE SMART CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$0	$700	06/14/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
STOYNOV, STEFAN	2116	713-500000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sheppard, Mullin,
2 Richter & Hampton LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

04/18/2005 MBIZUNE2 00000011 191853 10028556
01 FC:2501 700.00 DA

(A) NAME OF ASSIGNEE: Sentient Sensors LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Albuquerque, New Mexico

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 19-1853 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Brian D. Martin Date April 15, 2005

Typed or printed name Brian D. Martin, Esquire Registration No. 47,771

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PAGE 2/3 * RCVD AT 4/15/2005 2:49:01 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-2/1 * DNIS:7464000 * CSID:213 620 1398 * DURATION (mm-ss):01-28

PTO/SB/21 (09-04)
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APR 15 2005
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SHEPPARD MULLIN
SHEPPARD MULLIN RICHTER & HAMPTON LLP
ATTORNEYS AT LAW

48th Floor | 333 South Hope Street | Los Angeles, CA 90071-1448
213-620-1780 *office* | 213-620-1398 *fax* | *www.sheppardmullin.com*

FACSIMILE COVER SHEET

*** THIS FACSIMILE TRANSMISSION WILL NOT BE MAILED ****

Date: April 15,2005

File Number: 097Y-084435

Total number of pages: (including 1-page cover sheet) 3

If all pages are not received, please call Sheppard Mullin at 213-620-1780, ext. 2155

TO:	Facsimile No.	Telephone No.
U.S. Patent and Trademark Office	(703) 746-4000	

From: Brian D. Martin Direct Dial: 213-617-5415

Re: Transmittal of Issue Fee

MESSAGE: Please see attached.

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on **April 15, 2005**.

Brian D. Martin, Esquire

Transmittal of Issue Fee (in duplicate)
Applicant: Kenneth Blemel
Title: MULTI-CHIP MODULE SMART CONTROLLER
Serial No: 10/028,556 Filed: December 19, 2001
Examiner: Stefan Stoynov Group Art Unit: 2116
Fees: $700.00 authorized to be charged to Deposit Account
Our Docket No.: 097Y-084435 **Date Faxed: 04/15/05**
Client: Sentient Sensors **Date Due: 06/14/05**
Atty/Secy: Martin/Kemp

NOTE: THIS MESSAGE IS INTENDED ONLY FOR THE USE OF THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED, AND MAY CONTAIN INFORMATION THAT IS PRIVILEGED, CONFIDENTIAL AND EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAW. IF THE READER OF THIS MESSAGE IS NOT THE INTENDED RECIPIENT, OR THE EMPLOYEE OR AGENT RESPONSIBLE FOR DELIVERING THE MESSAGE TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT ANY DISSEMINATION, DISTRIBUTION OR COPYING OF THIS COMMUNICATION IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS COMMUNICATION IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE TO US AT THE ABOVE ADDRESS VIA THE U.S. POSTAL SERVICE. THANK YOU.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/14/2005

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles, CA 90071

EXAMINER	
STOYNOV, STEFAN	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/14/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

TITLE OF INVENTION: MULTI-CHIP MODULE SMART CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$0	$700	06/14/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax **(703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 03/14/2005

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles, CA 90071

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

TITLE OF INVENTION: MULTI-CHIP MODULE SMART CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$0	$700	06/14/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
STOYNOV, STEFAN	2116	713-500000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

7590 03/14/2005

EXAMINER
STOYNOV, STEFAN

ART UNIT	PAPER NUMBER
2116	

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles, CA 90071

DATE MAILED: 03/14/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 658 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 658 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 12/04) Approved for use through 04/30/2007.

Notice of Allowability	Application No.	Applicant(s)	
	10/028,556	BLEMEL, KENNETH	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *25 February 2005*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *19 December 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 03/04/2002
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

PATENT & TRADEMARK OFFICE
MAR 04 2002

COPY OF PAPERS ORIGINALLY FILED

Docket Number (Optional)	Application Number
97Y-8[redacted]	10/028,556
Applicant(s)	
Kenneth Blemel	
Filing Date	**Group Art Unit**
12/19/2001	2814

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SS	A	6,148,399	11/14/2000	Lyke	~~713~~	~~32~~	~~10/26/1998~~

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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JUN 18 2002

EXAMINER	DATE CONSIDERED
Stephen Stagnaro	3/9/2005

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/028,556	BLEMEL, KENNETH	
	Examiner	Art Unit	
	Stefan Stoynov	2116	SS

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
713	500	710	69						
INTERNATIONAL CLASSIFICATION		716	16						
G 06F	1/04								
G 06F	13/12								
H 03K	17/693								
	/								
	/								

Stefan Stoynov 03/09/2005
(Assistant Examiner) (Date)

(Legal Instruments Examiner) (Date)

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
(Primary Examiner) 10 Mar 05 (Date)

Total Claims Allowed: 20

O.G. Print Claim(s)	O.G. Print Fig.
1	1

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
11	2		32		62		92		122		152		182
1	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
6	5		35		65		95		125		155		185
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	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
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	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
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18	25		55		85		115		145		175		205
19	26		56		86		116		146		176		206
20	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/028,556	BLEMEL, KENNETH	
	Examiner	Art Unit	
	Stefan Stoynov	2116	SS

SEARCHED			
Class	Subclass	Date	Examiner
UPDATED	SEARCH	3/9/2005	SS

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
713	**500**	**3/9/2005**	**SS**
710	69	3/9/2005	SS
716	16	3/9/2005	SS

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Bib Data Sheet

CONFIRMATION NO. 2328

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/028,556	12/19/2001 RULE	713	2116	97Y-84435

APPLICANTS

Kenneth Blemel, Albuquerque, NM;

** CONTINUING DATA ********** SS

** FOREIGN APPLICATIONS ********** SS

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 01/23/2002

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☒ no 35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature SS Initials	NM	3	13	3

ADDRESS
John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles , CA
90071

TITLE
Multi-chip module smart controller

FILING FEE	FEES: Authority has been given in Paper
RECEIVED 670	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:

- ☐ All Fees
- ☐ 1.16 Fees (Filing)
- ☐ 1.17 Fees (Processing Ext. of time)
- ☐ 1.18 Fees (Issue)
- ☐ Other _____
- ☐ Credit

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	21264	(field adj programmable adj gate adj array$1) or FPGA$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:24
L2	548948	signal$1 near2 process$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:25
L3	37634	signal$1 near2 rout$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:26
L4	426992	signal$1 near2 (rout$3 or (re adj direct$3) or redirect$3 or switch$3 or direct$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:28
L5	4705	1 same 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:28
L6	3682	1 with 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:28
L7	83	5 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:53
L8	11	6 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 10:53
L9	18	("5999990").URPN.	USPAT	OR	OFF	2005/03/09 10:39
L12	25	("5574930").URPN.	USPAT	OR	OFF	2005/03/09 11:15
L13	13237	(real adj time) near3 clock$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:05

L14	2617	(date adj2 time) near2 stamp$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:06
L15	397414	((non adj volatile) near2 memory) or nvram or ROM orPROM or EPROM or (flash adj memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:07
L16	67	13 same 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:07
L17	47	13 with 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:08
L18	4	16 same 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:08
L19	1	17 with 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:10
L20	1263	13 same reset$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:10
L21	544	13 with reset$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:11
L22	10	20 same 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:12
L23	3	21 same 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:11

L24	0	22 same 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:11
L25	346	reset$5 near6 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:13
L26	1	25 same 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:14
L27	73661	power near6 converter$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:14
L28	60	27 same 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:14
L29	30	27 with 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:15
L30	22	28 same (internal$2 or embedded or inside or within)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:16
L31	2	29 with (internal$2 or embedded or inside or within)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:16
L32	281	implement$3 near6 (power adj converter$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:17
L33	0	32 same 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/09 12:17

PATENT
097Y-084435

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/028,556	Confirmation No. 2328
Applicant	:	Kenneth Blemel	
Filed	:	December 19, 2001	
TC/A.U.	:	2116	
Examiner	:	Stefan Stoynov	
Docket No.	:	097Y-084435	
Customer No.	:	30764	

February 25, 2005

AMENDMENT

VIA FACSIMILE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Non-final Office Action mailed December 8, 2004. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begin on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

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FACSIMILE COVER SHEET

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Date: February 25, 2005

File Number: 097Y-084435

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From: Brian D. Martin Direct Dial: 213-617-5415

Re: Transmittal of Amendment

MESSAGE: Please see attached.

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on **February 25, 2005**

Brian D. Martin, Esquire

Amendment
Amendment Transmittal Letter
Applicant: Kenneth Blemel
Title: MULTI-CHIP MODULE SMART CONTROLLER...
Serial No: 10/028,556 Filed: December 19, 2001
Examiner: Stefan Stoynov Group Art Unit: 2116
Fee: $300.00 authorized to be charged to Deposit Acct.
Our Docket No.: 097Y-084435 **Date Faxed: 02/25/05**
Client: Sentient **Date Due: 03/08/05**
Atty/Secy: Martin/Kemp

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W02-LA:1BDM1\70806933.1

AMENDMENT TRANSMITTAL LETTER (Small Entity) Applicant(s): Kenneth Blemel					Docket No. 097Y-084435
Application No. 10/028,556	Filing Date December 19, 2001	Examiner Stefan Stoynov	Customer No. 30764	Group Art Unit 2116	Confirmation No. 2328

Invention: **MULTI-CHIP MODULE SMART CONTROLLER HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION AND BUILT IN FIELD PROGRAMMABLE GATE ARRAY FOR PARALLEL PROCESSES**

COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

☒ Applicant claims small entity status. See 37 CFR 1.27

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT		RATE	ADDITIONAL FEE
TOTAL CLAIMS	20	-	20	=	0	x	$25.00	$0.00
INDEP. CLAIMS	6	-	3	=	3	x	$100.00	$300.00
Multiple Dependent Claims (check if applicable) ☐								$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT								$300.00

☐ No additional fee is required for amendment.

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Signature

Dated: **February 25, 2005**

Brian D. Martin, Esquire
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1, 4, and 7-11 have been canceled. Claims 3, 5, 6, and 13 have been amended to be written in independent form. Also, claim 13 has been amended to correct a typographical error. Dependent claims 2 and 12 have been amended to depend from amended independent claims 6 and 13, respectively. In addition, dependent claim 12 has been amended to correct antecedent basis.

New claims 14-27 have been added. Support for new claims 14, 15, 18, 21, and 25 is found, *inter alia*, in originally filed independent claim 7. Support for new claims 16 and 19 is found, *inter alia*, in originally filed claim 2. Support for new claims 17 and 20 is found, *inter alia*, in originally filed claim 10. Support for new independent claim 22 is found, *inter alia*, in originally filed claims 1, 2, 3, and 6, and in the specification on page 15, lines 9-11, page 18, lines 9-12, and page 21, lines 15-17. Support for new claims 23. 24, and 27 is found, *inter alia*, in originally filed claims 5, 6, and 13, respectively. Support for new claim 26 is found, *inter alia*, in originally filed claim 8. No new matter has been added.

Listing of Claims:

Claims 1 (canceled)

Claim 2 (amended): The ~~multi-chip module~~ instrument controller of claim [[1]]6, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog.

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Claim 3 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 1, wherein~~comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

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wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the ~~multi-chip~~ instrument controller.

Claim 4 (canceled)

Claim 5 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 1, further~~ comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor;

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a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor; and

a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

Claim 6 (amended): [[The]]An ~~multi-chip module~~ instrument controller ~~of claim 5,~~comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and

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a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claims 7-11 (canceled)

Claim 12 (amended): The method for conducting multiple parallel ~~monitoring and control functions~~processing using a single ~~multi-chip module~~ instrument controller as in claim [[11]]13, further comprising the additional step of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations.

Claim 13 (amended): [[The]]A method for conducting multiple parallel ~~monitoring and control functions~~processing using a single ~~multi-chip module~~ instrument controller ~~as in claim 11, further comprising the step of~~having a processor and a field programmable array, the method comprising:

receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths (thereby generating digital inputs);

providing a first portion of the digital inputs to the processor;

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providing a remaining portion of the digital inputs to the field programmable gate array;

performing digital signal processing on the first portion of the digital inputs utilizing the processor;

receiving the remaining portion of the digital inputs at the field programmable gate array and configuring a first portion of the gates in the field programmable gate array to perform digital signal processing on the remaining portion of the digital inputs, thereby conducting multiple parallel processing using a single instrument controller; and

configuring a ~~section~~second portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claim 14 (new): The instrument controller according of claim 3, whereir a third portion of the gates in the field programmable gate array is configured to activate the instrument controller from a deactivated state, or to deactivate the instrument controller from an active state.

Claim 15 (new): The instrument controller of claim 3, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

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Claim 16 (new): The instrument controller of claim 3, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

Claim 17 (new): The instrument controller of claim 3, wherein a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Claim 18 (new): The instrument controller of claim 5, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 19 (new): The instrument controller of claim 5, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

Claim 20 (new): The instrument controller of claim 5, wherein a portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

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Claim 21 (new): The instrument controller of claim 6, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 22 (new): A stand-alone instrument controller comprising:

a plurality of gates arranged in a field programmable gate array having multiple portions of gates, the multiple portions of gates including:

a first portion of the gates in the field programmable gate array is configured to perform signal processing,

a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, and

a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter;

a microprocessor coupled to the plurality of gates, and configured to operate independently or under the control of the plurality of gates;

a non-volatile memory storage system with non-volatile storage components for programs and data storage coupled to both the microprocessor and the plurality of gates;

a large volatile memory storage system coupled to the microprocessor with volatile storage components having a memory size that is comparable to, or larger than, an address space operated upon by the microprocessor;

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a plurality of analog-to-digital converters for receiving a plurality of analog inputs and digitizing the analog inputs, thereby providing digital inputs for use in the instrument controller; and

a plurality of analog outputs where each analog output is controlled by an independent digital-to-analog converter, and each independent digital-to-analog converter is configured to convert from one of at least two possible depths to analog.

Claim 23 (new): The stand-alone instrument controller of claim 22, further comprising a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

Claim 24 (new): The stand-alone instrument controller of claim 22, wherein the internal embedded power converter is configured to receive an input voltage level and to generate each operating and reference voltage needed within the instrument controller.

Claim 25 (new): The stand-alone instrument controller of claim 22, wherein the microprocessor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

Claim 26 (new): The stand-alone instrument controller of claim 22, further comprising at least two internal oscillators coupled to the microprocessor for providing clock signals for low-frequency and high-frequency operations.

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Claim 27 (new): A method for conducting multiple parallel processing using a single instrument controller having a field programmable array, the method comprising:

configuring a portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving at least one input voltage level and generating each operating and reference voltage needed for activation, operation, and deactivation of the instrument controller.

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REMARKS/ARGUMENTS

In the Non-final Office Action mailed December 9, 2004, claims 1-6 and 11-13 were examined, and claims 7-10 were withdrawn from consideration. In the Office Action, the Examiner rejected, and objected to, the claims as follows:

- Claim 4 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly indefinite, and was objected to as allegedly having improper dependent form.

- Claims 1, 2, 11, and 12 were rejected under 35 U.S.C. § 103(a), as allegedly obvious over U.S. Patent No. 6,148,399 to Lyke ("the Lyke patent") in view of U.S. Patent No. 5,892,962 to Cloutier ("the Cloutier patent") and U.S. Patent Application Publication No. 2002/0129191 to DaCosta ("the DaCosta publication").

- Claims 3, 5, 6, and 13 were objected to as being dependent upon a rejected base claim, but indicated to be allowable if rewritten in independent form.

Applicant has cancelled rejected claims 1, 4, and 7-11, has amended allowable claims 3, 5, 6, and 13 to be in independent form, and has amended dependent claims 2 and 12 to depend from allowable claims 6 and 13, respectively. Applicant has added new claims 14-27. Accordingly, Applicant respectfully requests the removal the objections, and traverses the rejection to dependent claims 2 and 12.

The Invention

Before addressing the specific claim limitations, it will be helpful first to briefly summarize embodiments of the invention that are covered by the pending claims.

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The present invention resides in a new and improved stand-alone, compact, low-power electronic instrument controller. The core elements of the present invention include the following: a microprocessor, a static random access memory, a non-volatile memory, a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion. Preferably, the present invention supports the following: multiple analog inputs, with at least four analog inputs to a high precision digitizer, analog outputs, adjustable analog signal paths, serial communications ports, interrupts, and digital discrete I/O.

In a preferred embodiment, the present invention supports the following types of functionality: (1) in-situ reprogramming of the microprocessor's operational software; (2) in-situ reprogrammation of the FPGA's operational software programs, with adaptive parallel program codes; (3) individualization of the serial codes, embedded descriptions of design specification, past history, maintenance, etc.; (4) storage of configuration information for setting properties of functional units; (5) a real-time crystal oscillator controlled clock; and (6) creative power management options for discontinuous (going from powered operation to non-powered) operation effected through state preservation and recovery.

The instrument controller of the present invention offers enhanced power management and functional flexibility, more specifically, the instrument controller offers variable analog-to-digital conversion bit depths, along with higher bit depths for some applications. Also, the present invention eliminates the need for a resistive ASIC. Instead, the present invention adds a separately controllable FPGA that acts as a parallel processor with an internal clock or separate external clock. The FPGA preferably includes more than thirty thousand gates and adds a freely reconfigurable, and separately programmable, multi-purpose digital system that can run independent of the microprocessor. Also, the present invention incorporates a microprocessor with a processing speed of up to 33 MHz.

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The Election of Claims 1-6 and 11-13

On page 2 of the Office Action, the Examiner requested affirmation of the provisional election of claims 1-6 and 11-13. Applicant affirms the election with traverse to prosecute the invention of claims 1-6 and 11-13.

The Rejection of Claim 4 Under 35 U.S.C. § 112, Second Paragraph

On page 3 of the Office Action, dependent claim 4 was rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Also, on page 6 of the Office Action, dependent claim 4 was objected to, as allegedly being of improper dependent form. Applicant has canceled dependent claim 4, and, as such, Applicant believes the rejection of, and objection to, dependent claim 4 are moot.

The Rejection of Claims 1, 2, 11, and 12 Based on the Lyke Patent, the Clotier Patent, and the DaCosta Publication

On pages 3-6 of the Office Action, independent claims 1 and 11, and dependent claims 2 and 12, were rejected under 35 U.S.C. § 103(a), as allegedly obvious over the Lyke patent in view of the Clotier patent and the DaCosta publication. Applicant has canceled independent claims 1 and 11, and amended claims 2 and 12 to depend from allowable claims 6 and 13, respectively. Thus, Applicant believes this rejection to claims 1, 2, 11, and 12 is moot.

Allowable Subject Matter

On page 7 of the Office Action, the Examiner indicated that dependent claims 3, 5, 6, and 13 "would be allowable if rewritten in independent form . . ." Applicant has amended dependent claims 3, 5, 6, and 13 so as to be written in independent form. Accordingly, Applicant believes amended independent claims 3, 5, 6, and 13 to be allowable, and respectfully requests removal of this objection.

PAGE 16/18 * RCVD AT 2/25/2005 3:49:28 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:213 620 1398 * DURATION (mm-ss):05-00

New Claims 14-27

Applicant has added new claims 14-27 to offer additional permutations of patent protection. As previously noted, support for new dependent claims 14, 15, 18, 21, and 25 is found, *inter alia*, in originally filed independent claim 7. Support for new dependent claims 16 and 19 is found, *inter alia*, in originally filed dependent claim 2. Support for new dependent claims 17 and 20 is found, *inter alia*, in originally filed dependent claim 10. Support for new independent claim 22 is found, *inter alia*, in originally filed claims 1, 2, 3, and 6, and in the specification on page 15, lines 9-11, page 18, lines 9-12, and page 21, lines 15-17. Support for new claims 23, 24, and 27 is found, *inter alia*, in originally filed dependent claims 5, 6, and 13, respectively. Support for new dependent claim 26 is found, *inter alia*, in originally filed dependent claim 8. No new matter has been added.

Applicant believes that new dependent claims 14-21 are allowable because each of those claims depends from allowable amended independent claim 3, 5, or 6. Also, Applicant believes that new independent claim 22 and new dependent claims 23-26, all of which depend from independent claim 22, are allowable because they include the following claim features: "a first portion of the gates in the field programmable gate array is configured to perform signal processing, a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, and a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter . . . ," which the Examiner, on page 7 of the Office Action, stated were reasons for the allowability of claims 3, 6, and 13. Similarly, Applicant believes that new independent claim 27 is allowable because it includes the following claim features: "configuring a portion of the gates in the field programmable gate array to operate as an internal embedded power converter . . . ," which the Examiner, on page 7 of the Office Action, stated was a reason for the allowability of claims 6 and 13.

PAGE 17/18 * RCVD AT 2/25/2005 3:49:28 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:213 620 1398 * DURATION (mm-ss):05-00

Conclusion

This application should now be in condition for a favorable action. Applicant respectfully requests entry of the Amendment and an early allowance of all claims herein. If for any reason the Examiner finds the application other than in allowance, the Examiner is requested to call the undersigned attorney at the below-listed telephone number to discuss the steps necessary for placing the application in condition for allowance. If there are any fees due in connection with the filing of this Amendment, please charge the fees to our Deposit Account No. 19-1853.

Respectfully submitted,
SHEPPARD, MULLIN, RICHTER & HAMPTON LLP

By: _____
Brian D. Martin
Registration No. 47,771

333 South Hope Street, 48th Floor
Los Angeles, California 90071
(213) 620-1780

PAGE 18/18 * RCVD AT 2/25/2005 3:49:28 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/7 * DNIS:8729306 * CSID:213 620 1398 * DURATION (mm-ss):05-00

PATENT
097Y-084435

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/028,556	Confirmation No. 2328
Applicant	:	Kenneth Blemel	
Filed	:	December 19, 2001	
TC/A.U.	:	2116	
Examiner	:	Stefan Stoynov	
Docket No.	:	097Y-084435	
Customer No.	:	30764	

February 25, 2005

AMENDMENT

VIA FACSIMILE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Non-final Office Action mailed December 8, 2004. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begin on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

SHEPPARD MULLIN
SHEPPARD MULLIN RICHTER & HAMPTON LLP
ATTORNEYS AT LAW

48th Floor | 333 South Hope Street | Los Angeles, CA 90071-1448
213-620-1780 office | 213-620-1398 fax | www.sheppardmullin.com

FACSIMILE COVER SHEET

*** THIS FACSIMILE TRANSMISSION WILL NOT BE MAILED ***

Date: February 25, 2005

File Number: 097Y-084435

Total number of pages: (including 1-page cover sheet) 18

If all pages are not received, please call Sheppard Mullin at 213-620-1780, ext. 2155

TO:	Facsimile No.	Telephone No.
U.S. Patent and Trademark Office	(703) 872-9306	

From: Brian D. Martin Direct Dial: 213-617-5415

Re: Transmittal of Amendment

MESSAGE: Please see attached.

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on **February 25, 2005**

Brian D. Martin, Esquire

Amendment
Amendment Transmittal Letter
Applicant: Kenneth Blemel
Title: MULTI-CHIP MODULE SMART CONTROLLER...
Serial No: 10/028,556 Filed: December 19, 2001
Examiner: Stefan Stoynov Group Art Unit: 2116
Fee: $300.00 authorized to be charged to Deposit Acct.
Our Docket No.: 097Y-084435 **Date Faxed: 02/25/05**
Client: Sentient **Date Due: 03/08/05**
Atty/Secy: Martin/Kemp

NOTE: THIS MESSAGE IS INTENDED ONLY FOR THE USE OF THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED, AND MAY CONTAIN INFORMATION THAT IS PRIVILEGED, CONFIDENTIAL AND EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAW. IF THE READER OF THIS MESSAGE IS NOT THE INTENDED RECIPIENT, OR THE EMPLOYEE OR AGENT RESPONSIBLE FOR DELIVERING THE MESSAGE TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT ANY DISSEMINATION, DISTRIBUTION OR COPYING OF THIS COMMUNICATION IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS COMMUNICATION IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE TO US AT THE ABOVE ADDRESS VIA THE U.S. POSTAL SERVICE. THANK YOU.

W02-LA:1BDM1\70806933.1

AMENDMENT TRANSMITTAL LETTER (Small Entity)					Docket No.
Applicant(s): Kenneth Blemel					097Y-084435
Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/028,556	December 19, 2001	Stefan Stoynov	30764	2116	2328

Invention: **MULTI-CHIP MODULE SMART CONTROLLER HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION AND BUILT IN FIELD PROGRAMMABLE GATE ARRAY FOR PARALLEL PROCESSES**

COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

☒ Applicant claims small entity status. See 37 CFR 1.27

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT		RATE	ADDITIONAL FEE
TOTAL CLAIMS	20	-	20	=	0	x	$25.00	$0.00
INDEP. CLAIMS	6	-	3	=	3	x	$100.00	$300.00
Multiple Dependent Claims (check if applicable) ☐								$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT								$300.00

☐ No additional fee is required for amendment.

☒ Please charge Deposit Account No. **19-1853** in the amount of **$300.00**

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **19-1853**

- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.

☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Signature

Dated: **February 25, 2005**

Brian D. Martin, Esquire
Registration No. 47,771
Sheppard, Mullin, Richter & Hampton LLP
333 South Hope Street, 48th Floor
Los Angeles, California 90071
(213) 620-1780

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(Date)

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

cc:

P11SMALLREVC0

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number
10/638,556
BTY-8443K

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	13	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	13 minus 20=	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL	370	OR	TOTAL	

2/25/03 DCW

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 20	Minus	** 20	=
Independent	* 6	Minus	*** 3	= 3
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
~~X$9=~~		OR	X$18=	
~~X42~~	30	OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE	30	OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT
097Y-084435

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/028,556	Confirmation No. 2328
Applicant	:	Kenneth Blemel	
Filed	:	December 19, 2001	
TC/A.U.	:	2116	
Examiner	:	Stefan Stoynov	
Docket No.	:	097Y-084435	
Customer No.	:	30764	

February 25, 2005

AMENDMENT

VIA FACSIMILE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Non-final Office Action mailed December 8, 2004. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that be gin on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

03/03/2005 CCURTIS 00000001 191853 10028556
01 FC:2201 300.00 DA

AMENDMENT TRANSMITTAL LETTER (Small Entity) Applicant(s): Kenneth Blemel				Docket No. 097Y-084435
Application No. 10/028,556	Filing Date December 19, 2001	Examiner Stefan Stoynov	Customer No. / Group Art Unit 30764 / 2116	Confirmation No. 2328

Invention: **MULTI-CHIP MODULE SMART CONTROLLER HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION AND BUILT IN FIELD PROGRAMMABLE GATE ARRAY FOR PARALLEL PROCESSES**

COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

☒ Applicant claims small entity status. See 37 CFR 1.27

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	20	-	20	=	0	x $25.00	$0.00
INDEP. CLAIMS	6	-	3	=	3	x $100.00	$300.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$300.00

☐ No additional fee is required for amendment.

☒ Please charge Deposit Account No. 19-1853 in the amount of $300.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-1853

- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.

☐ Payment by credit card. Form PTO-2038 is attached.

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Signature

Dated: February 25, 2005

Brian D. Martin, Esquire
Registration No. 47,771
Sheppard, Mullin, Richter & Hampton LLP
333 South Hope Street, 48th Floor
Los Angeles, California 90071
(213) 620-1780

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(Date)

Signature of Person Mailing Correspondence

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CC:

P11SMALL.REV03

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,556	12/19/2001	Kenneth Blemel	97Y-84435	2328

7590 12/08/2004

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles, CA 90071

EXAMINER	
STOYNOV, STEFAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/028,556	BLEMEL, KENNETH	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,11 and 12* is/are rejected.

7)☒ Claim(s) *3,5,6 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6 and 11-13, drawn to multi-chip module instrument controller, classified in class 713, subclass 500.

II. Claims 7-10, drawn to multi-chip module instrument controller, classified in class 713, subclass 323.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as multi-chip module instrument controller with power management providing automatic activation/deactivation of processor based on an external signal. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with James Brueggemann on 11/24/2004 a provisional election was made with traverse to prosecute the invention of I, claims 1-6 and 11-13. Affirmation of this election must be made by applicant in replying to this Office action. Claims 7-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "microprocessor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyke in view of Clotier and DaCosta.

Re claim 1, Lyke discloses a multi-chip module instrument controller (column 1, lines 58-62, Fig. 1) comprising a non-volatile memory storage component for program and data storage (column 3, line 66, column 4, lines 14 and 15, Fig.1); a large volatile memory storage component for additional program and data storage (column 4, lines 35-37, Fig. 1); a processor coupled to both said non-volatile memory storage (Fig. 1) said processor capable of high-frequency and low-frequency operations (column 4, lines 42-44); at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations (column 4, lines 42-44, Fig. 1); a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to processor (column 3, lines 28-33, Fig. 1).

Lyke fails to disclose an embedded memory for storing an initialization program and a field programmable gate array coupled to the processor for parallel processing.

DaCosta teaches embedded CPU registers (paragraph 0028, lines 1-5, paragraph 0029, lines 12-14, FIG. 2) for storing operating system software (paragraph 0034, lines 2-5) that enables the processor to start processing without first copying the application software into RAM. In DaCosta, the use of embedded non-volatile CPU registers provides for fast bootup and shutdown with information preservation when the system is powered down (paragraph 0015, lines 1-15, paragraph 30, lines 4-7). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to incorporate the embedded registers and bootup sequence, as suggested by

DaCosta for the multi-chip module instrument controller disclosed by Lyke in order to store an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory.

Cloutier teaches a multiprocessor based on a multidimensional array of field programmable gate arrays (FPGAs) (column 2, lines 9-13, FIG. 1) adapted to function as a parallel processor (column 2, lines 65-67). In Cloutier, the multiprocessor provides improved data processing for applications requiring large number of operations (column 1, line 32-35). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to use the FPGA-based processing elements, as suggested by Cloutier for the multi-chip module instrument controller disclosed by Lyke in order to run independent processes in parallel with the processor.

Re claim 2, Lyke discloses the multi-chip instrument controller, further comprising a plurality of analog outputs, each being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog (column 3, lines 63-65).

Re claim 11, Lyke discloses a method using multi-chip module instrument controller (Fig.1) receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths (thereby generating digital inputs) (column 3, lines 28-33), providing the first portion of said digital inputs to said processor (Fig. 1), performing digital signal processing on said first portion of said digital inputs utilizing the processor (Fig. 1).

Lyke fails to disclose multiple parallel signal processing utilizing both processor and a field programmable gate array.

Cloutier teaches a multiprocessor based on a multidimensional array of field programmable gate arrays (FPGAs) (column 2, lines 9-13, FIG. 1) adapted to function as a parallel processor (column 2, lines 65-67). In Cloutier, the multiprocessor provides improved data processing for applications requiring large number of operations (column 1, line 32-35). It would have been obvious to one of the ordinary skill in the art at the time of applicant's invention to use the FPGA-based architecture, as suggested by Cloutier for the method disclosed by Lyke in order to achieve multiple signal processing.

Re claim12, Lyke discloses the method as per claim 11, further comprising the additional steps of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations (column 4, lines 42-44, Fig. 1).

Claim Objections

Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 4 includes every limitations of the parent claim 1.

Allowable Subject Matter

Claims 3, 5, 6, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 3, the prior art fails to disclose or suggest "first portion of the gates configured to perform signal processing; and second portion of the gates configured to operate as a signal distribution matrix".

Re claim 5, the prior art fails to disclose or suggest "resettable digital real-time quartz controlled clock for accurate date and time stamping of date and time stamping of data before it is stored in the non-volatile memory".

Re claims 6 and 13, the prior art fails to disclose or suggest "a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



THANH DU

***
SS

Notice of References Cited	Application/Control No. 10/028,556	Applicant(s)/Patent Under Reexamination BLEMEL, KENNETH	
	Examiner Stefan Stoynov	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,148,399	11-2000	Lyke, James C.	712/10
	B	US-5,892,962	04-1999	Cloutier, Jocelyn	712/16
	C	US-2002/0129191	09-2002	DaCosta, Behram Mario	711/103
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Bib Data Sheet

CONFIRMATION NO. 2328

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/028,556	12/19/2001 RULE	257	2814	97Y-84435

APPLICANTS

Kenneth Blemel, Albuquerque, NM;

** CONTINUING DATA ********** SS

** FOREIGN APPLICATIONS ********** SS

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 01/23/2002

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☒ no 35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	NM	3	13	3

ADDRESS

John Carr, Esq.
Sheppard Mullin Richter & Hampton
333 S. Hope St., 48th Floor
Los Angeles ,CA 90071

TITLE

Multi-chip module smart controller

FILING FEE RECEIVED		
370	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/028,556	BLEMEL, KENNETH	
Examiner	**Art Unit**	
Stefan Stoynov	2116	SS

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	12/1/04
	1	√
	2	√
	3	O
	4	√
	5	O
	6	O
	7	N
	8	N
	9	N
	10	N
	11	√
	12	√
	13	O
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Claim		Date
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Claim		Date
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/028,556	BLEMEL, KENNETH	
Examiner	**Art Unit**	
Stefan Stoynov	2116	SS

SEARCHED			
Class	Subclass	Date	Examiner
710		12/1/2004	SS
711		12/1/2004	SS
712		12/1/2004	SS
713	500	12/1/2004	SS
716		12/1/2004	SS

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST search including US-PGPUB, USPAT, EPO, JPO, DERWENT, IBM_TDB	12/1/2004	SS

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3637049	(simultaneous$2 or concurrent$2 or (in adj parallel) or parallel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:28
L2	214297	(execut$3 or run$4) near3 (process$2 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:29
L3	16372	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:30
L4	13654	1 with 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:30
L5	9	4 with 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:31
L6	0	5 and "710"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:31
L7	0	5 and "712"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:31
L8	1	5 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:32
L9	62504	(non adj volatile) adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:22
L10	1237710	(processor$1 or microprocessor$1 or (micro adj processor$1) or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:50

L11	5468402	(embedded or within or inside)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:25
L12	35541	11 adj2 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:36
L13	150	12 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:44
L14	11	13 and "711"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 11:36
L15	3	("5761697" | "6122704" | "6330977").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 11:42
L16	7	("5586081" | "5764945" | "5860083" | "6026465" | "6091640" | "6320782" | "6385688").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 11:43
L23	2	("4839640" | "5758359").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:26
L24	9	("5504760" | "5586073" | "5592003" | "5768191" | "5822248" | "5867428" | "5905676" | "5996108" | "6134141").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:27
L25	7	("5012163" | "5623281" | "5726718" | "5880702" | "6040876" | "6052491" | "6215913").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:29
L26	3	("5761697" | "6122704" | "6330977").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:31
L27	7	("5586081" | "5764945" | "5860083" | "6026465" | "6091640" | "6320782" | "6385688").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:32
L28	5	("4751961" | "5363904" | "5561461" | "5782296" | "6577231").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:36
L29	15	("3946613" | "4086488" | "4476721" | "4571995" | "4577512" | "4696189" | "4757463" | "5044770" | "5089979" | "5347476" | "5354200" | "5365462" | "5375073" | "5377128" | "5686831").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 12:37

L30	16	("5826166").URPN.	USPAT	OR	OFF	2004/11/29 12:39
L32	1	("5822225").URPN.	USPAT	OR	OFF	2004/11/29 12:43
L33	8	12 adj2 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:46
L34	38	9 adj2 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:46
L35	813808	(processor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:50
L36	21740	11 adj2 35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:53
L37	12	9 adj2 36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:56
L38	71	9 with 36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:56
L39	15	9 near2 36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 12:56
L40	2618579	(autonomous$2 or independent$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:27
L41	288641	(initializ$5 or startup or (start adj up))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:47

L42	5033267	(program$1 or code or function$1 or routine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:29
L43	26953	41 near2 42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:29
L44	2	43 with 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:31
L45	0	44 and "771"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:32
L46	1041	40 near3 41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:32
L47	0	46 with 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:33
L48	2	46 with 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:34
L49	0	46 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:34
L50	1043	memory adj2 36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:40
L51	19	9 with 50	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:40

L52	7	("5586081" | "5764945" | "5860083" | "6026465" | "6091640" | "6320782" | "6385688").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 13:42
L53	285	(non adj volatile) adj register$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:53
L54	4	11 adj2 53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:55
L55	5	53 near2 35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 13:56
L56	23	("5041886" | "5450363" | "5515317" | "5526364" | "5537354" | "5600605" | "5615159" | "5619461" | "5666321" | "5675540" | "5677885" | "5751039" | "5787457" | "5825782" | "5933434" | "5936903" | "5995438" | "6026465" | "6028798" | "6073204" | "6097637" | "6137133" | "6141247").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 13:58
L57	729	9 with cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:14
L58	253	9 near2 cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:15
L59	113	9 adj2 cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:22
L60	54	9 adj cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:08

L61	86	57 with processor$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:14
L62	44	58 with processor$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:15
L63	5339697	(within or inside)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:25
L64	17889	63 adj2 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:27
L65	855	memory adj2 64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:27
L66	406	memory adj 64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:28
L67	10588	63 adj processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:27
L68	232	memory adj 67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:32
L69	7	9 adj 67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:28
L70	1	68 with 41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:33

L71	8	("5371876" | "5479639" | "5530847" | "5579522" | "5692190" | "6122732" | "6128732" | "6158000").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 14:32
L72	28	65 with 41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:34
L73	62	BIOS adj 63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:42
L74	2	73 with processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:42
L75	2630	(initializ$5 or startup or (start adj up)) adj2 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:48
L76	32	75 with self	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:53
L77	2878	initializ$5 adj program	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:54
L78	308	stor$3 near2 77	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:00
L79	2	78 with 67	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:56
L80	2	78 with 64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:57

L81	2893	embedded adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:59
L82	0	81 with 78	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:58
L83	0	81 same 78	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:58
L84	21611	internal adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:59
L85	893	84 near2 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 14:59
L86	0	85 with 77	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:00
L87	3281	stor$3 near2 BIOS	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:00
L88	0	85 with 87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:00
L89	0	85 same 87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:00
L90	1	85 same 77	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:01

L93	1032	start$3 adj processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:02
L94	9	93 with self	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:02
L95	10	("5408624" | "5410703" | "5500806" | "5761530" | "5771064" | "5805880" | "5841991" | "5905896" | "5922072" | "5938766").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 15:05
L96	3	(self adj power$2) adj processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:09
L97	1	("6128392").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 15:08
L98	386459	(initializ$5 or startup or (start adj up) or boot$3 or (boot$3 adj up))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:46
L99	15623	98 with (quick$2 or immediat$4 or fast)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:58
L100	0	99 with (without near3 ((non adj volatile) adj memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:48
L101	0	99 with ("without" near3 ((non adj volatile) adj memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:49
L102	282	enabl$4 near3 (processor or microprocessor or cpu) near3 98	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:57
L103	4	102 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:51

L104	17	("4787032" | "4942606" | "4959860" | "4984213" | "5128995" | "5136713" | "5226122" | "5257377" | "5295064" | "5345424" | "5388267" | "5390324" | "5410706" | "5426775" | "5452339" | "5557777" | "5764995").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 15:53
L105	7065	98 adj2 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:58
L106	97	105 with (quick$2 or immediat$4 or fast)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 15:58
L107	1	106 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:01
L108	4	("5872967").URPN.	USPAT	OR	OFF	2004/11/29 15:59
L109	2826	(startup or (start adj up) or BIOS) near2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:02
L110	707	109 with (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:02
L111	93	110 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:02
L112	20	111 with 98	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:03
L113	382	(enab$4 or allow$3) near3 (processor or microprocessor or CPU) near3 (startup or (start adj up) or initializ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:08

L114	11	113 with (quick$2 or immediat$4 or fast)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:13
L115	631	BIOS near2 instruction$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:16
L116	26925	(within or incide) adj2 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:14
L117	2	115 with 116	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:14
L118	248	BIOS near2 register$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:16
L119	0	118 with 116	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:17
L120	946	(autonomous$2 or independent$2) near3 (starup or (start adj up) or initializ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:19
L121	35	120 near3 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:21
L122	2	(self adj boot$3) near3 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:24
L123	0	120 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:24

L124	15274	(processor or microprocessor or CPU) near3 (satrup or (start adj up) or initializ$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:35
L125	7	("5410706" | "5596713" | "5748940" | "5872967" | "5892943" | "5918048" | "6473856").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 16:30
L126	196	124 with self	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:33
L127	37	126 with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:34
L128	206	124 with (quick$2 or immediat$4 or fast)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:36
L129	1	128 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:35
L130	0	128 with (autonomous$2 or independent$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:40
L131	8992	(initializ$5 or satrup or (start adj up)) adj2 (program or code or instruction$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:42
L133	164136	(stor$3 or kept or located) near3 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:49
L134	117	131 with 133	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:49

L135	5	134 with (within or inside)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:50
L136	2365058	(fast or instant$2 or immediat$4 or quick$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:52
L137	8083	136 near3 98	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:53
L138	286	137 with (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:53
L139	20	(enabl$3 or allow$3) with 138	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 16:54
L140	3023	internal near2 cache	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:02
L141	1	140 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:02
L142	2778	(fast or quick) adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:08
L143	56952	(internal$2 or inside or within) near2 (processor or microprocessor or CPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:08
L144	64	142 with 143	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:13

L145	0	144 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:09
L146	0	144 with (initializ$5 or satrup or (start adj up))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:10
L147	53164	((physically adj integrated) or integtared or included or within or inside) near2 (processor or microprocessor or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:14
L148	3958	memory near2 147	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:15
L149	58	148 with 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:15
L150	11	(non adj volatile) adj local adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/29 17:22
L151	20	("4752870" | "5109484" | "5146568" | "5280627" | "5331634" | "5367688" | "5404527" | "5504903" | "5603056" | "5613123" | "5652886" | "5657448" | "5668992" | "5727207" | "5790788" | "5838907" | "5980078" | "6012088" | "6012100" | "6105122").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/29 17:23

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	flash$3 adj bounc$3 adj ball$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:23
L2	514	flash$3 near4 ball$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:26
L3	8	2 with bounc$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:23
L4	4	2 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:45
L7	71	((light or solar) adj power$2) near3 calculator$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:33
L8	4	autonomous$2 near2 startup	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:37
L9	2	autonomous$2 adj startup	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:37
L10	73	autonomous$2 adj start$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:38
L11	6	10 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:43
L12	2879	embedded adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:49

L14	618	12 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:43
L15	0	14 with 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:44
L16	0	14 with 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:44
L17	0	14 same 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:44
L18	52069	(initializ$5 or start$3) near4 (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:47
L19	0	18 with 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:46
L20	10513	(initializ$5 near3 program)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:48
L21	2	20 with 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:48
L22	6062	embedded near2 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:49
L23	6	22 with 20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 07:50
L24	13	("4947477").URPN.	USPAT	OR	OFF	2004/11/24 07:51

L25	9483	embedded near3 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:00
L26	2366	L25 with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:00
L28	1	26 with 20	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:01
L29	17726	(multi adj chip adj module$1) or MCM$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:02
L30	0	29 with 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:03
L31	0	29 same 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:04
L32	53781	(application adj specific adj integrated adj circuit$1) or ASIC$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:04
L33	74	32 with 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:20
L37	656	instrument$5 adj controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:20
L38	0	37 with 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:22

L39	7	22 with 18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 08:22
L40	5	("5974528").URPN.	USPAT	OR	OFF	2004/11/24 08:28
L41	13	("5293424" | "5442704" | "5644781" | "5682027" | "5687345" | "5771191" | "5828911" | "5881295" | "5905921" | "5923838" | "5974528" | "6038635" | "6075941").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:34
L42	1952	((on adj chip) or (single adj chip)) adj2 (microcomputer$1 or (micro adj computer))	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:38
L43	13307	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:38
L44	0	42 with 43	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:38
L45	0	42 same 43	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:38
L46	2070	((on adj chip) or (single adj chip)) near2 (microcomputer$1 or (micro adj computer))	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:40
L47	0	46 same 43	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/24 08:40

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2879	embedded adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:31
L2	62244	(non adj volatile) adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:32
L3	957084	(processor or microprocessor or (micro adj processor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:32
L4	10046213	(includ$3 or hav$3 or compris$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:34
L5	134720	3 near1 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:40
L6	14	5 near1 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:39
L7	157	5 near1 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:40
L8	144	5 adj 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:40
L9	51941	3 adj 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:41
L10	45	9 adj 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/24 16:41

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	94625	((cut$4 adj off) or (shut$4 adj off) or (turn$3 adj off) or deactivat$4 or suspend$3) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:48
L2	4815	L1 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:48
L3	109	L2 same ((zero or no) near2 power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:50
L11	63	L2 with ((zero or no) near2 power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:00
L12	1	((discontinuous$2 or irregular$2) near4 (power adj operation$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:02
L13	0	(discontinuous$2 near4 (power adj operation$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:03
L14	642	(discontinuous$2 near3 power)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:04
L15	90169	((cut$4 adj off) or (shut$4 adj off) or (turn$3 adj off) or deactivat$4) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:04
L16	42569	((turn$3 adj on) or restart$3 or activat$4) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:04
L17	6	14 with (L15 or L16)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:04

L22	5169	((power$3 adj down) or powerdown or (zero adj power) or unpower$2) near2 (mode or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:16
L23	14163	automatic$4 near3 (enter$3 or exit$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:15
L24	17	23 with 22	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:16
L25	742	((zero adj power) or unpower$2) near2 (mode or state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:16
L26	0	23 with 25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:16
L27	1	23 same 25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:17
L29	7	(zero adj power) adj sleep	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:50
L30	30833	solar near3 energy	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:51
L31	22843	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near4 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:54
L32	2	31 with 30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:56

L33	293	solar near4 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:09
L34	7	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) same 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:20
L35	17	("5228644").URPN.	USPAT	OR	OFF	2004/11/23 15:04
L36	7	(solar adj power$2) near2 (processor or microprocessor or CPU)	USPAT	OR	OFF	2004/11/23 15:08
L37	29	(solar adj power$2) near3 controller	USPAT	OR	OFF	2004/11/23 15:08
L38	0	29 same (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:09
L39	271	nuclear near4 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:10
L40	5	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) same 39	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:13
L41	70187	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near3 (insrument or device)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:16
L42	2	41 same 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:14
L44	90899	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near3 (insrument or device or controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:41
L45	3	44 same 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:18

L46	62634	solar near3 (cell$1 or batter$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:19
L47	585	46 with (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:26
L48	23	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) same 47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:39
L49	25947	solar adj energy	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:25
L50	14	(processor$1 or microprocessor$1 or CPU$1) near4 49	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:26
L51	2204159	(energy or power) not electric$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:58
L52	125	51 with 47	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:05
L53	20031	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near3 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:41
L54	677	51 with 53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:46
L55	8	54 with automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:42

L56	0	54 with solar	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:45
L57	198324	(processor$1 or microprocessor$1 or CPU$1) near3 us$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:08
L58	3852	57 with 51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:52
L59	2	58 same 49	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:52
L60	794	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near4 (processor$1 or microprocessor$1 or CPU$1) with 51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:16
L61	32	60 same automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:55
L62	742622	energy not electric$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:59
L63	60	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near4 (processor$1 or microprocessor$1 or CPU$1) with 62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:10
L66	548	non adj2 (electric$3 adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:09
L67	0	66 with 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:08

L68	0	(processor$1 or microprocessor$1 or CPU$1) with 66	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:08
L69	3526786	(power or energy) not (electrical adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:17
L70	1911	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) near4 (processor$1 or microprocessor$1 or CPU$1) with 69	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:24
L71	52788	(different near3 (power or energy)) not (electrical adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:19
L72	6	71 with 70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:18
L73	37483	(solar near3 (power or energy)) not (electrical adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:20
L74	2	73 with 70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:21
L75	10067	(alternative near3 (power or energy)) not (electrical adj (power or energy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:20
L76	0	75 with 70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:21
L77	2	75 same 70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:21

L78	3	73 same 70	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:21
L79	9483	embedded near3 (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:34
L80	68	(activat$4 or reactivat$4 or (wak$3 adj up) or awaken$2) with 79	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:25
L82	1679	((zero adj power) or suspend) adj (state or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:34
L84	4	"4341230".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:41
L85	2	"4702140".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 16:41
L86	10	("4702140").URPN.	USPAT	OR	OFF	2004/11/23 16:41
S1	90169	((cut$4 adj off) or (shut$4 adj off) or (turn$3 adj off) or deactivat$4) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:55
S2	42569	((turn$3 adj on) or restart$3 or activat$4) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:56
S3	99573	(power$3 adj down) or (shut$4 adj down)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 14:11
S4	46680	(power$3 adj up) or (power$3 adj on)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 11:42

S5	9618	(S1 or S3) with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:32
S6	8259	(S2 or S4) with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 11:44
S7	789	S5 with (complet$3 or entir$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:03
S8	11508	zero near2 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:15
S9	21478	no adj power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 11:49
S10	3	(S8 or S9) with S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 11:53
S11	9	(S8 or S9) same S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 11:53
S12	33	("5511205").URPN.	USPAT	OR	OFF	2004/11/23 11:58
S13	6	("5050172").URPN.	USPAT	OR	OFF	2004/11/23 12:06
S14	57	("4279020").URPN.	USPAT	OR	OFF	2004/11/23 12:07
S15	1679	((zero adj power) or suspend) adj (state or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:16
S16	90	S5 same S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:17

S17	51	S5 with S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:46
S18	20	S7 same S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:19
S19	8	S7 with S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:19
S20	191	(suspend$3 adj2 resum$3) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:32
S21	1126	(activat$3 adj2 deactivat$3) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:32
S22	94	(S20 or S21) with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:00
S23	1	S22 with automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:34
S24	4	S22 same S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:37
S25	114850	(external or outside) near3 signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:39
S26	324	S6 with automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:39

S27	1	S25 same S26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:40
S28	34563	automatic$4 near4 (resum$3 or restart$3 or (start$3 adj again) or activat$4 or reactivat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:44
S29	2378	S28 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:44
S30	83	S29 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:45
S31	1	S30 with S25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:46
S32	94625	((cut$4 adj off) or (shut$4 adj off) or (turn$3 adj off) or deactivat$4 or suspend$3) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:55
S33	45682	((turn$3 adj on) or restart$3 or activat$4 or resum$3) near4 power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 12:56
S34	4815	S32 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 13:00
S35	2528	S33 with (processor$1 or microprocessor$1 or CPU$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/23 15:08

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	216878	(independent$2 or separat$2 or (stand adj1 alone)) near3 (process$2 or task$1 or operation$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:00
L2	10913	(execut$3 or run$4 or complet$3) near5 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:00
L3	106397	(simultaneous$2 or concurrent$2 or (in adj1 parrallel)) near4 (process$3 or microprocess$3 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:04
L4	16274	((field adj programmable adj gate adj array) or FPGA)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:06
L5	10913	1 with 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:06
L6	8	5 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:13
L7	0	5 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:07
L10	46	3 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:23
L11	0	2 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:23
L12	8	2 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:24

L13	184	1 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:24
L14	75	1 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:25
L15	4816	(implement$3 or design$3 or us$3 or hav$3) near3 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:46
L16	726	15 with (process$2 or coprocess$2 or (co adj1 process$2))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:48
L17	0	16 same 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:49
L18	0	16 same 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:49
L19	31	16 same 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:56
L20	251	15 with ((digital adj signal adj process$3) or DSP$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:57
L21	0	20 same 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:57
L22	0	20 same 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:57

L23	3	20 same 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 08:58
L24	28	15 with ((signal adj distribut$3 adj matri$3) or (switch$3 adj matri$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:04
L25	764	(signal adj2 condition$3 adj2 filter$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:04
L26	0	15 with 25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:05
L27	0	4 with 25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:05
L28	1455	(cross adj1 bar adj switch$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:06
L29	6	15 with 28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:07
L31	181551	(((analog-to-digital) or (A adj1 D)) adj conver$3) or ADC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:20
L32	99605	(((digital-to-analog) or (D adj1 A)) adj conver$3) or DAC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:20
L33	48	(31 or 32) with 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:27

L34	510387	(multi adj chip module) or MCM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:30
L35	492	(instrument adj controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:31
L36	60	(smart adj control adj system$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:31
L37	128	(space adj based) near3 (device$1 or module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:32
L38	41370	(application adj specific adj integrated adj circuit) or ASIC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:33
L39	172	(tightly near3 coupl$3) with 34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:48
L40	1	39 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:34
L41	16	35 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:38
L42	1	35 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:35
L43	0	36 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:38

L44	1	37 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:38
L45	6123	38 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:44
L46	1126	38 same 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:39
L47	924	38 with 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:39
L48	26	47 with 34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:40
L49	0	47 with 39	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:40
L50	0	37 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:46
L51	1	37 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:47
L52	1	39 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:48
L53	8281	34 near3 design	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:50

L54	63	53 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:50
L55	35	53 with 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:58
L56	1658	(discontinuous$2 or irregular$2) near4 (power or (power adj operation))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 09:59
L57	780	((zero adj power) or unpower$2) near2 (state$1 or mode$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:00
L58	0	56 with 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:00
L59	0	56 same 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:01
L60	28645	automatic$4 near4 (activat$3 or deactivat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:01
L61	899	(processor$1 or microprocessor$1 or CPU$1) with 60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:02
L62	92404	(external or outside) near2 signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:03
L63	1	61 with 62	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:04

L64	0	61 same 56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:05
L65	0	61 same 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:05
L66	0	60 same 56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:05
L67	1	60 same 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:06
L68	0	37 same 56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:07
L69	0	37 same 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:07
L70	1	35 same 56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:08
L71	0	35 same 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 10:08

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	22588	(independent$2 or (stand adj alone)) near4 (execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:14
S2	4690	S1 with (process$2 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:55
S3	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:56
S4	10	S2 same S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:56
S5	739	instrument$5 adj controller$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:09
S6	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:09
S7	2	S5 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:12
S8	56135	microcontroller$1 or (micro adj controller$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S9	1623	S8 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S10	22588	(independent$2 or (stand adj alone)) near4 (execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13

S11	4690	S10 with (process$2 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S12	244720	(processor$1 or microprocessor$1 or CPU$1) near4 (coupl$3 or connect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:16
S13	386	S12 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:16
S14	21	S9 same S13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:19
S15	6358	(implement$3 or (based adj on)) with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:20
S16	1462	((digital adj signal adj process$3) or DSP$1) with S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:22
S17	0	S16 same S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:23
S18	169353	(((analog adj to adj digital) or (A adj D)) adj convert$3) or ADC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:27
S19	92482	(((digital adj to adj analog) or (D adj A)) adj convert$3) or DAC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:28
S21	26215	(S18 or S19) near4 (coupl$3 or connect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:31

S22	44	S21 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:34
S23	689	signal adj condition$3 adj2 filter$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:34
S24	1	S23 same S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:35
S25	2813	(monitor$3 or control$4) near5 S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:36
S26	164	S25 same (S18 or S19)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:38
S27	63	S25 with (S18 or S19)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:38
S28	22285	motor adj controller$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S29	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S30	6358	(implement$3 or (based adj on)) with S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S31	4	S28 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:18

S32	134091	(simultaneous$2 or concurrent$2 or (in adj paralell)) near5 (process$3 or execut$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:25
S33	147347	(simultaneous$2 or concurrent$2 or (in adj paralell)) near5 (process$3 or execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:27
S34	2601175	(independent$2 or autonomous$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:32
S35	62	S34 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:30
S36	171069	(process$2 or task$1) near3 execut$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S37	3958	S34 with S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S38	0	S37 with S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S39	2	S37 same S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:46
S40	9119	coprocessor or (co adj processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:47
S41	32	S40 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:51

S42	526	controller with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:53
S43	17705	(multi adj chip adj module$1) or MCM$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:54
S44	9	S43 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:56
S45	1	S33 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:59

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	211	(zero adj power$2) near3 state$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:17
L12	7	(processor$1 or microprocessor$1 or CPU$1) with 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:15
L13	6566	automatic$2 near4 (activat$3 or deactivat$3)	USPAT	OR	OFF	2004/11/22 17:06
L14	187	(processor$1 or microprocessor$1 or CPU$1) with 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:37
L15	56786	(external or outside) adj2 signal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:25
L16	0	15 with 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:25
L17	13	14 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:29
L18	50	external adj activat$3 adj signal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:31
L19	324	13 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:33
L20	21	19 same (processor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:35

L22	100	sonar adj2 energy	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:05
L24	2	(processor$1 or microprocessor$1 or CPU$1) with 22	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:40
L25	3	("5309408").URPN.	USPAT	OR	OFF	2004/11/22 16:38
L26	114	automatic$3 near4 (wake adj up)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:41
L27	3	26 with processor$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:41
L28	40988	(activat$2 or deactivat$2) near3 (state$1 or mode$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:51
L29	1027	28 with (prcessor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:50
L30	47	29 with automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:47
L31	20	30 same signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:49
L32	13447	energy near2 conserv$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:50
L33	170	32 with (prcessor$1 or microprocessor$1 or CPU$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:50

L34	68	33 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:52
L35	4	34 with automatic$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:52
L36	420	unpower$2 near3 state$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:02
L37	19	(processor$1 or microprocessor$1 or CPU$1) with 36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:07
L38	27392	solar adj2 energy	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:05
L39	1	13 with 38	USPAT	OR	OFF	2004/11/22 17:06
L40	75	(processor$1 or microprocessor$1 or CPU$1) with 38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:11
L41	20	40 with power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:09
L42	68396	device near3 activat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:16
L43	16	42 with 38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 17:16
S1	22588	(independent$2 or (stand adj alone)) near4 (execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:14

S2	4690	S1 with (process$2 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:55
S3	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:56
S4	10	S2 same S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 13:56
S5	739	instrument$5 adj controller$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:09
S6	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:09
S7	2	S5 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:12
S8	56135	microcontroller$1 or (micro adj controller$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S9	1623	S8 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S10	22588	(independent$2 or (stand adj alone)) near4 (execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13
S11	4690	S10 with (process$2 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:13

S12	244720	(processor$1 or microprocessor$1 or CPU$1) near4 (coupl$3 or connect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 16:17
S13	386	S12 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:16
S14	21	S9 same S13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:19
S15	6358	(implement$3 or (based adj on)) with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:20
S16	1462	((digital adj signal adj process$3) or DSP$1) with S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:22
S17	0	S16 same S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:23
S18	169353	(((analog adj to adj digital) or (A adj D)) adj convert$3) or ADC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:27
S19	92482	(((digital adj to adj analog) or (D adj A)) adj convert$3) or DAC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:28
S21	26215	(S18 or S19) near4 (coupl$3 or connect$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:31
S22	44	S21 with S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:34

S23	689	signal adj condition$3 adj2 filter$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:34
S24	1	S23 same S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:35
S25	2813	(monitor$3 or control$4) near5 S6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:36
S26	164	S25 same (S18 or S19)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:38
S27	63	S25 with (S18 or S19)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 14:38
S28	22285	motor adj controller$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S29	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S30	6358	(implement$3 or (based adj on)) with S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:15
S31	4	S28 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:18
S32	134091	(simultaneous$2 or concurrent$2 or (in adj paralell)) near5 (process$3 or execut$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:25

S33	147347	(simultaneous$2 or concurrent$2 or (in adj paralell)) near5 (process$3 or execut$3 or run$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:27
S34	2601175	(independent$2 or autonomous$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:32
S35	62	S34 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:30
S36	171069	(process$2 or task$1) near3 execut$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S37	3958	S34 with S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S38	0	S37 with S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:34
S39	2	S37 same S29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:46
S40	9119	coprocessor or (co adj processor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:47
S41	32	S40 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:51
S42	526	controller with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:53

S43	17705	(multi adj chip adj module$1) or MCM$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:54
S44	9	S43 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:56
S45	1	S33 with S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/22 15:59

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	13656	(multi adj1 chip adj1 module) or MCM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 12:57
S2	2496	(advanced adj instrument adj controller) or AIC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 12:57
S3	16274	(field adj programmable adj gate adj array) or FPGA	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:26
S4	23	S1 near5 S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:15
S5	35	S1 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:08
S6	2	S2 near5 S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:09
S7	4	S2 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:09
S8	3	("4887239" | "5365591" | "5369314").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/19 13:10
S9	1	("6081896").URPN.	USPAT	OR	OFF	2004/11/19 13:11
S10	6	("5563928" | "5678057" | "5761516" | "5973376" | "6049748" | "6061260").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/19 13:11
S11	165834	(parallel or (in adj parallel) or simultaneous$2 or concurrent$2) near3 (process$4 or execut$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:06

S12	34541	S11 with (processor$1 or CPU$1 or microprocessor$1 or coprocessor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:21
S13	62	S12 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:22
S14	1	S13 same S1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:22
S15	1	S13 same S2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:22
S16	169387	microcomputer or (micro adj computer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:37
S17	202	S16 near5 S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:50
S18	3	S17 same S1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:45
S20	264	S16 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:59
S21	0	S20 same S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 13:52
S22	122	S11 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:00

S23	38054	(application adj specific adj integerated adj circuit) or ASIC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:15
S24	5256	S23 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:17
S25	3	S24 with S12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:19
S26	5	S24 with S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:19
S27	9	S2 with S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:45
S28	3212	independent$2 near3 S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:50
S29	0	idependent$2 adj3 S11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:52
S30	13992	independent$2 near2 (run$4 or execut$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:06
S31	244	S30 with ((parallel or (in adj parallel) or simultaneous$2 or concurrent$2) near3 (process$2 or task$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 14:57
S32	3	S30 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:02

S33	310716	(run$4 or execut$3) near3 (process$3 or task$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:06
S34	3275	independent$2 near2 S33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:24
S35	527	S34 with (parallel or (in adj parallel) or simultaneous$2 or concurrent$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:09
S36	2	S35 same S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:10
S37	48094	implement$3 near3 (processor$1 or microprocessor$1 or CPU$1 or coprocessor$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:21
S38	440	S37 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:18
S39	237	S38 with S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:20
S40	0	S39 with parallel	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:21
S41	347	implement$3 near3 coprocessor$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:22
S42	9	S41 with S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:22

S43	7	S34 with coprocessor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:24
S44	2652	implement$3 near4 ((field adj programmable adj gate adj array) or FPGA)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:26
S45	15	S44 with coprocess$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/11/19 15:27

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Kenneth Blemel	Examiner: Not Assigned
	Group Art Unit: 2814
Serial No.: 10/028,556	
Filed: December 19, 2001	
For: Multi-Chip Module Smart Controller	February 21, 2002

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TC 2800 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
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Washington, DC 20231

Sir:

In accordance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants submit the enclosed copies of references that might be deemed material to the examination of the above-identified application. The documents are identified on the attached form PTO-A820, "Information Disclosure Citation."

Applicants respectfully request that the identified documents be considered in the examination of this application, and that their consideration be made of written record in the application file.

Respectfully submitted,

By _____
John Carr, Reg. No. 42,390

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97Y-8	10/028,556
Applicant(s)	
Kenneth Blemel	
Filing Date	**Group Art Unit**
12/19/2001	2814

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A	6,148,399	11/14/2000	Lyke	713	32	10/26/1998

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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12/19/01 H064 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Small Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
97Y-84435
Total Pages in this Submission
42

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

Multi-Chip Module Smart Controller Having Variable Analog-To-Digital Conversion and Built in Field Programmable Gate Array for Parallel Processes

and invented by:

Kenneth Blemel

11002 U.S. PTO 10/028556 12/19/01

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 32 pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☒ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL (Small Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. 97Y-84435
	Total Pages in this Submission 42

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal b. ☐ Informal Number of Sheets 3

4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche

7. ☐ Genetic Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & documents)*

9. ☐ 37 CFR 3.73(b) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing
   ☐ First Class ☒ Express Mail *(Specify Label No.):* EL 727855210 US

UTILITY PATENT APPLICATION TRANSMITTAL (Small Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. 97Y-84435
	Total Pages in this Submission 42

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Small Entity Statement(s) - Specify Number of Statements Submitted: _____

17. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

18. ☒ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

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	Total Pages in this Submission 42

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	13	- 20 =	0	x $9.00	$0.00
Indep. Claims	3	- 3 =	0	x $42.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$370.00
OTHER FEE *(specify purpose)*	Assignment Recordation Fee				$40.00
				TOTAL FILING FEE	$410.00

☒ A check in the amount of **$370.00** to cover the filing fee is enclosed.

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Dated: **December 19, 2001**



Signature

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CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Kenneth Blemel**			Docket No. **97Y-84435**
Serial No.	Filing Date **12/19/01**	Examiner	Group Art Unit

Invention: **MULTI-CHIP MODULE SMART CONTROLLER HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION AND BUILT IN FIELD PROGRAMMABLE GATE ARRAY FOR PARALLEL PROCESSES**

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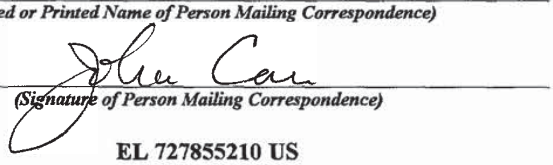
Utility Patent Application

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P06A/REV02

UTILITY APPLICATION

OF

KENNETH BLEMEL

FOR

UNITED STATES PATENT

ON

MULTI-CHIP MODULE SMART CONTROLLER

HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION

AND

BUILT IN FIELD PROGRAMMABLE GATE ARRAY

FOR PARALLEL PROCESSES

Sheets of Drawings: 3

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Multi-Chip Module Smart Controller

Statement of Government Interest

1. The terms and conditions of the Cooperative Research and Development Agreement under which this invention was created entitle the Government of the United States to a non-exclusive royalty free right to practice and use the invention which is the subject of this patent.

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Field of the Invention

2. The present invention generally relates to multi-chip modules (MCM). More specifically, the present invention relates to an MCM capable of running multiple processes and having non-volatile storage for numerous monitoring/controlling applications.

Description of the Prior Art

3. United States Letters Patent No. 6,148,399 is directed toward an Advanced Instrument Controller (AIC). The AIC was developed by Mr. James Lyke while employed at the US Air Force Research Laboratory (AFRL). The original purpose of the AIC was to improve over prior art space-based experimental test devices and modules which previouslyused separate board-mounted payload,

control, and data acquisition circuit boards that were generally bulky, high power consuming, and expensive.

4. The design in U.S. Patent No. 6,148,399 is based on an 8-bit 8051 25MHz processor which may be clocked at two different frequencies, 12Mhz and 10Mhz, by either one of two different internal voltage controlled oscillator circuits for high-frequency and for low frequency operation. The internal oscillators provide only relative speed clocking as the clock speed is significantly affected by thermal conditions. The AIC in U.S. Patent No. 6,148,399 provides 10 bit analog-to-digital (A/D) conversion and 12 bit digital to analog (D/A) conversion for analog outputs. Moreover, the invention disclosed in U.S. Patent No. 6,148,339 requires separate power conversion circuitry to provide variable and continuous power levels, even for the low-speed clocks.

5. The invention in U.S. Patent No. 6,148,399 combines controller and data acquisition functions of conventional test modules into a single, tightly coupled MCM design. Prior to the invention of the AIC, many MCM design proposals for space-based test devices had been proposed and/or developed; however, designs approaching the functional capability of the AIC would have been very large and unwieldy because tightly coupled MCMs were unknown in the art.

6. Tightly coupled MCMs refer to MCMs whose components possess one or more of the following features: (1) more input/output (I/O) terminal contacts than is normally consistent with a discrete implementation, (2) lower capacitive drive in output circuits than is normally consistent with a discrete implementation, (3) I/O terminals in locations inconsistent with standard integrated circuits (ICs), (4) I/O circuitry with reduced or eliminated electrostatic discharge protection structures.

7. By tightly coupling the MCM, more complex interactions between the components within the design are possible, thereby providing greater functional capability than would have been possible using a single integrated circuit. In other words, a tightly coupled MCM is built like a hybrid microcircuit but possesses a highly integrated behavior more consistent with "system-on-a-chip" or monolithic IC designs. The result is that Lyke's invention greatly reduced size, weight, and power consumption over discrete implementations ("discrete" referring to an arrangement of several individually packaged ICs built onto a circuit board or other presumably multi-layer wiring medium). Accordingly, the invention in U.S. Patent 6,148,399 combines in a small MCM a number of functions which could not have previously been executed using a single integrated circuit.

8. However, there are several limitations to the design in U.S. Patent No. 6,148,399. First, the AIC is not capable of performing parallel independent processes.

Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

9. Additionally, the AIC in U.S. Patent No. 6,148,399 performs all A/D conversion at a 10 bit digitizing depth and does not offer variable conversion as may be required by different processes. For example, it may be preferred that some processes execute at a higher bit depth of 14 bits while some may be able to execute at a lower bit depth of 10 bits and still ensure accuracy. The AIC of U.S. Patent No. 6,148,399 uses a constant bit depth of 10 bits for its A/D conversion so all processes are executed at the same bit depth. Accordingly, what is needed is an MCM design capable of performing A/D conversion at different bit depths such that multiple parallel processes which require different bit depths can be executed in an independent fashion.

Summary of the Invention

10. The present invention is embodied in a stand-alone, compact, low-power electronics instrument controller which utilizes an MCM design. However, an electronics instrument controller designed in accordance with the present invention

has less complexity, includes enhanced power management, and offers more functional flexibility than prior art controllers. This is because an electronics instrument controller designed in accordance with the invention includes a significant improvement in functionality and circuitry design over prior art MCM controllers, such as the AIC in U.S. Patent No. 6,148,399. For example, the present invention improves on the digitizing precision and offers variable A/D conversion bit depths, with higher bit depths for some applications. Additionally, the circuitry design of the present invention eliminates the need for a resistive ASIC. Instead, the present invention adds a separately controllable FPGA that acts as a parallel processor with internal or separate external clock. The FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system which can run independent of the microprocessor. Finally, the present invention incorporates a microprocessor with significant processing improvements over the processor used in the AIC patent, including an increased processing speed of up to 33Mhz.

11. The present invention uniquely combines inherent core and I/O features, design methodology, and operating principles to create an electronics building block having numerous monitoring/controlling applications. Along with its increased functionality and unique circuit design, the primary characteristics of the present invention are its compact size, light weight , low power consumption, and

compatibility with robust application regimes. The core elements of the present invention include a microprocessor, static random access memory (single- or multi-ported), non-volatile memory (e.g., flash or EEPROM), a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion. Preferably, the present invention supports multiple analog inputs (to either 14 bit or 12 bit digitizers), with at least four analog inputs to a high precision (xx bit) digitizer, analog outputs (from a digital representation), adjustable analog signal paths (variable gain, offset, impedance, signal filtration properties), serial communications ports, interrupts, and digital discrete I/O.

12. In a preferred embodiment, the present invention supports the following types of functionality: (1) in-situ reprogramming of the microprocessor's operational software (program code); (2) in-situ reprogrammation of the FPGA's operational software programs with adaptive parallel program codes, (3) individualization of the serial codes, embedded descriptions of design specification, past history, maintenance, etc. ; (4) storage of configuration information for setting properties of functional units; (5) a real-time crystal oscillator controlled clock, and (6) creative power management options for discontinuous (going from powered operation to non-powered) operation effected through state preservation and recovery.

Brief Description of the Drawings

FIG. 1 is a functional schematic block diagram of a preferred embodiment of the MCM Controller of the present invention;

FIG. 2 is a functional block diagram that illustrates the concept of utilizing the FPGA to reroute external inputs and execute multiple processes; and

FIG. 3 is a functional block diagram that illustrates the operational concepts for the embedded smart power convertor utilized in a preferred embodiment of the present invention.

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Detailed Description of Preferred Embodiments

13. The present invention is embodient in a tightly coupled smart control system which uses a multi-chip module (MCM) instrument controller which uniquely combines conventional high-density interconnects patterned in an overlay of MCM substrates.

14. Preferably, the MCM of the present invention is capable of receiving multiple analog inputs and offers variable A/D conversion, including at least four high speed precision differential digitizers for enhanced performance. Additionally, the present invention incorporates a stand alone FPGA based parallel processor which

can be configured to run under control of a microprocessor or independently. The invention embodies many additional features that make it possible in some cases to use no additional pre-scaling, timing, and other supplemental electronics. As such, the invention is similar to a "system-on-a-chip" and appears similar to a chip in size, weight, and physical configuration, but through a tightly coupled MCM implementation, transcends the functional capability of a single integrated circuit.

Overall Functional Elements and Configuration

15. In a preferred embodiment, the invention combines a microprocessor, a large Field Programmable Gate Array (FPGA), high speed precision A/D converters, D/A converters for producing analog outputs, and both volatile and non-volatile memory storage systems. Preferably, the invention includes an embedded smart power conversion system. The invention combines all of these elements on a single tightly coupled MCM to achieve its stand-alone capabilities. These capabilities include ultra-low power requirements, extremely small size and weight, versatile functionality, and the ability to operate in extreme environments.

FIG. 1 is a schematic block diagram which illustrates a preferred embodiment of the present invention. As shown, the invention is comprised of a microprocessor 110 having a plurality of I/O ports, including analog inputs/outputs and digital serial inputs/outputs. The microprocessor 110 is preferably clocked by a system

clock signal SYS CLK which is generated by either an on-module voltage controlled oscillator (VCO) 115 or an external clock 120. In a preferred embodiment, the present invention actually includes two different on-module VCOs for generating a high frequency clock signal and a low frequency clock signal. The high frequency clock signal will be used during a high frequency operation mode and the low frequency clock signal will be used during the low frequency operation mode.

16. The microprocessor is preferably coupled to volatile and non-volatile memory components. In a preferred embodiment, the non-volatile data storage component 130 is a large 256 Mbit EEPROM, and the volatile memory component is a large static RAM.

17. The microprocessor is preferably configured to receive a plurality of analog inputs. As shown in FIG. 1, at least eight analog inputs are received through an eight channel multiplexer 140 and digitized using high resolution A/D converters 145 (equal to or greater than 12 bits). Additionally, the present invention further includes at least four parallel high precision digitizers 150a-d which are capable of receiving analog inputs directly and digitizing these inputs at a higher bit depth (ex. 14 bits) without the need for separate resistors and capacitors for signal conditioning. The high precision digitizers 150a-d are designed and implemented to operate with dual electronic circuit configuration whereby one digitizer provides an

alternating period of time to allow for high speed yet stable signal acquisition and digitizing of signals.

18. The microprocessor is further coupled to a fully programmable field gate array (FPGA) 170. In a preferred embodiment, the FPGA is comprised of at least 30,000 gates which may operate either under control of the microprocessor (for example as a co-processor) or, may be operated independently. The FPGA provides the ability to use internal parallel processing. For example, the FPGA could be performing signal processing while acting as a cross-bar switching device to select analog or digital signals, and performing signal conditioning and filtering at the same time. As shown, the FPGA may be clocked using the same on-board VCO as the microprocessor; or it may be clocked separately via an external clock 175. Alternatively, where no clock is used, the FPGA will operate at gate speeds.

19. A preferred embodiment of the present invention further includes at least four 12 bit digital-to-analog (D/A) converters 180 for providing analog output signals.

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Microprocessor

20. In a preferred embodiment, the microprocessor of the present invention preferably includes an embedded memory that enables the startup of processing without first loading a program from the non-volatile memory. This improves on the prior art systems which can only operate after a program is first loaded from non-volatile memory. Moreover, the improvement provides a totally unpowered ready state, reduces power consumption when idle, and provides an abbreviated time to activation by retaining the active program in non volatile memory thereby eliminating need for loading of the initiating program.

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21. Additionally, because the microprocessor of the present invention has an autonomous startup capability on activation it can operate without need for control of an internal or external clock. This means the present invention can function with discontinuous applied power whereas prior art controllers can only go into a sleep mode that requires power to the internal capacitive oscillating circuit. This means the present invention is able to display history-dependent behavior and be put to zero-power sleep for extended periods of time to be awakened by application of power from another device. This also means the invention can turn itself off completely allowing for wakeup on activation by the next input of power (e.g. from solar energy).

Interfaces

22. As described earlier herein, the present invention has multiple I/O including a plurality of digital and analog inputs. Additionally, the present invention provides for variable A/D conversion of these analog inputs and different bit depths. In a preferred embodiment, the invention includes an internal 10 bit analog-to-digital (A/D) converter with a 12 channel multiplexer front end. In a preferred embodiment at least four of the twelve input channels have differential amplifier inputs. The amplifiers are preferably low power operational amplifiers, which may be shut down under program control when not in use. In shutdown mode each op amp draws no current. The amplifiers are configured to permit sensors which use the 4-20 milliamp interface convention to be used directly with the present invention without the need for a specialized ASIC for signal conditioning of the input.

23. In a preferred embodiment, the invention also includes multiple (at least four) high precision analog-to-digital (A/D) converters operating in alternating fashion to avoid aliasing of signals. These high precision A/D converters are configured to operate at high speeds, providing significantly more conversions per second. They also provide higher precision (i.e. 14 bits) for advanced applications such as digital signal processing.

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24. The invention further includes a 12 bit precision analog-to-digital (A/D) converter that is serially multiplexed over the an individual or multiple (at least 8) input channels. Each channel preferably has a fixed window for operation corresponding to zero and full scale digital readings, with the inputs defaulting to one of the fixed window values. Accordingly, such a typical default window might be 0-4.096V for input range where a channel receiving a -2V signal would be represented as 0V at the input, and a 10V signal would be represented as 4.096V.

25. In most applications, it is important for a controller to have a large number of serial interfaces. Most conventional controllers have few, if any, serial interfaces and it is often necessary to add additional hardware to allow for more serial interfaces. In a preferred embodiment of the current invention, a large number of serial interface are preferably readily accommodated without the need for additional hardware. Accordingly, in a preferred embodiment, the present invention includes a number of both asynchronous serial ports (e.g., RS-232/RS-422) as well as synchronous (e.g., clocked) serial ports. Preferably, the voltage levels of the serial ports default to CMOS-compatible levels; however, the present invention includes an adaptive I/O module which allows these voltage levels to be adjusted. For example, the RS-232 ports could be adjusted to +/-4V instead of (0,3.3V) levels.

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26. In a preferred embodiment, the invention has more than 10 externally available discrete signal channels. These channels are bi-directional lines having pull-up or pull-down characteristics that can be externally set. When used as outputs, these channels are set to CMOS level; however, a subset of the lines can be passed through an adaptive I/O function to adjust the levels to any two other desired voltage levels.

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Memory Storage Components

27. The present invention further includes a combination of large volatile and non-volatile memory storage components. These memory storage components are preferably customized and tightly coupled within the MCM for maximum performance.

28. In a preferred embodiment, the non-volatile memory storage components include at least two non-volatile memory units each with a minimum of 256K bytes of non-volatile memory space, preferably FLASH or EEPROM based. In addition, the invention allows for the coupling and addressing of an external data storage unit, such as a FLASH memory card or EEPROM memory. The non-volatile memory is used for both program storage and data storage, which can be changed repetitively, limited only by the fatigue mechanism associated with the non-volatile device. In a preferred embodiment, the non-volatile data storage allows for data

time stamping with the digital value of an accurate internal clock. Accordingly, the digital output from the real time date/time clock 165 can be used to provide accurate date time stamping of data. In a preferred embodiment, the present invention powers down the non-volatile components when power consumption needs to be minimized, so that the effects of non-optimized drivers (those not designed with tightly coupled methodologies) that consume high amounts of power can be negated.

29. In a preferred embodiment, the present invention further includes a volatile static random access memory (SRAM) 155 with storage contents comparable to or larger than the address space that the CPU operates upon. Unlike prior art controllers, such as that in U.S. Patent No. 6,148,399, where some components such as the SRAM are always powered, the present invention is able to totally shut down all electronics to achieve a zero power state. The present invention is able to reinstate activity upon an activating event or upon receipt of an external activation signal. Preferably, the SRAM contains a shadow copy of the program memory.

30. The present invention preferably utilizes a large static random access memory (SRAM) for the volatile memory. The volatile memory can all be used to store programs and large amounts of data (greater than 2 megabits).

31. The ability to exploit non-volatile data storage allows the present invention to preserve the context of key operations by periodically storing state information and intermediate results from algorithms executed by the microprocessor and/or the FPGA. The existence of this state information is tested upon reset, especially after power is interrupted, to determine where the last left operation (a simple form of rollback). The non-volatile storage also allows serialization, for specific calibration parameter storage (e.g., monitor the non-linearity of its own analog inputs and store the necessary corrective coefficients in memory), and for history-depending operations such as data logging. It is possible to also store particular design specifications, usage/maintenance history for recall during diagnosis, maintenance, and repair of the present invention. The non-volatile memory of the present invention may also be used to program reconfigurable logic (e.g. the FPGA) and interconnect devices.

Internal Clocking

32. In a preferred embodiment, the present invention includes at least three internal oscillators 115a, 115b, and 115c, and one real time quartz clock. Two of the oscillators are used to produce internal clock signals which clock the microprocessor. In a preferred embodiment, one oscillator generates a high-frequency clock signal which is used to clock the microprocessor for high frequency operations. The other oscillator generates a low-frequency clock signal for low-

frequency operations, respectively. The distinction between the high-frequency and low-frequency oscillators is important, as it is necessary for power preservation to maintain an independent oscillator that operates at a lower frequency. The third oscillator generates a clock signal which is used for the individually programmable FPGA. In order to offer accurate speed and performance at high-G applications or applications where both extreme cold and discontinuous operation are present, the present invention preferably utilizes non-crystal based oscillators for effective operation. Alternatively, crystal oscillators may be used. The present invention also permits external oscillators for cases where synchronization or more precise timing is important. In all cases, the low frequency clock signal is independently generated to minimize power consumption in divider networks and fast-switching drivers. In a preferred embodiment, the high-frequency oscillator operates at 25 MHz and the low-frequency oscillator operates at 200 Hz for high and low frequency operations, respectively. The third oscillator is preferably a 33MHz oscillator which is used to control the FPGA (which otherwise would operate at the speed required to complete gate transitions). Alternatively, the FPGA may be clocked from an external clock signal. In this embodiment, only two oscillators are necessary.

33. In a preferred embodiment, the present invention further includes a resettable digital real time quartz controlled clock for precision timing. The

resettable digital real time quartz controlled clock provides for accurate date and time stamping of recorded data.

Field Programmable Gate Array

34. The design of the present invention eliminates the need for an analog application-specific integrated circuit (ASIC). Instead, present invention utilizes an independently operable and programmable FPGA which is used to implement many of the key instrumentation functions of an ASIC. In a preferred embodiment, the FPGA is a large (greater than 30,000 gate) Field Programmable Gate Array which operates either under control of the microprocessor (for example as a co-processor) or, can be operated independently. The FPGA provides the ability to use internal parallel processing. For example, the FPGA could be performing signal processing while acting as a cross-bar switching device to select analog or digital signals, and performing signal conditioning and filtering at the same time. This can be extended to re-route almost all external conductors and selected internal conductors, whether power or signal bearing. The FPGA can be switched off to consume no power during sleep and restarted by the external signal or by the processor program when the processor is reactivated.

35. The combination of the FPGA and microprocessor provides built in test capability not inherent in prior art control systems, which utilize a single

microprocessor and specialized ASIC. More specifically, the FPGA can be programmed to monitor the functionality of the microprocessor, the analog-to-digital conversion operations, and the digital-to-analog conversion operations. Alternatively, the microprocessor can be used to perform built in self test on the FPGA.

36. The invention provides for either external or internal input of a clock signal from a high speed oscillator for controlled sequencing of multiple processors formed in the FPGA for parallel processing. Otherwise, if no clock signal is provided, then the FPGA operates at gate ripple speed. By operating the FPGA at higher speeds, the present invention improves on the speed of operations and digital calculations and enables the FPGA to act as a mathematical co-processor.

37. The FPGA utilized in a preferred embodiment of the present invention has the ability to be reprogrammed from non-volatile memory, by the microcontroller, or through a serial port. This enables the parallel activities of the FPGA to be constructed "on the fly" and personalized with a variety of unique programs and data, such as serial codes, calibration coefficients, or a reduced "traveler" containing process history. Accordingly, the FPGA of the present invention has the ability to be dynamically configured as a processor with extended mathematical or logical precision (e.g. 32 bit or 64 bit).

38. The present invention can use the parallel processing of the FPGA to re-route a subset of its external interconnections through the use of switch matrices. FIG. 2 illustrates the concept of utilizing the FPGA to reroute a subset of the external inputs in order to perform parallel processes. As shown, gates X1, X2 and X3 are configured to route the input at node A to anyone of three independent processes A1-A3. The processes are independent configurations of a subset of gates within the FPGA. Switches Y1, Y2 and Y3 are configured to selectively route the outputs from these processes to the output node B. When the analog functions represented by A1-A3 are identical, then a form of functional redundancy is achieved, giving an increased fault tolerance to the signal monitoring function. When the analog functions A1-A3 differ, then different analog processing functions are selectively applied to the analog signal being monitored.

39. The parallel processing internal to the FPGA eliminates the unreliability of switches built from discrete or micro-electromechanical systems (MEMS) technology. Preferably, the FPGA can be configured in numerous gate array patterns. Additionally, FPGA switching is far superior to prewired solid state switches for near-static reconfiguration of digital and analog signal lines. The FPGA provides lower series resistance, flexibility, lower signal variability, ability to swing above and below rails without attenuation, lower noise, and non-volatility. Using the FPGA, the present invention is endowed with important capabilities, including

the re-location of I/O due to wiring errors.

Internal Embedded Power Conversion

40. As described earlier, a preferred embodiment of the present invention includes an internal embedded power conversion module which greatly extends robustness of the design, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog control, this capability allows the present invention to not only maintain its internally correct operating power supply under external variation, but this capability permits the present invention to maintain interface integrity. This internal embedded power convertor performs two key functions: generation of each operating and reference voltage needed within the module and regulation and filtering of power supply irregularities over a very wide voltage range.

41. In a preferred embodiment, subsets of gates in the FPGA can be used to provide power conversion, thereby forming an internal embedded power conversion module without requiring any additional circuitry. FIG. 3 is a functional block diagram which illustrates the internal power conversion concept. As shown in FIG. 3, a first stage in the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG). A number of second stages convert from the fixed VREG to several power voltages consumed internal to the module.

These second stage voltages provide for the supply of internal digital power, internal analog power, and a series of reference voltages. Many topologies known in the art of power convertor design may be applied, whether switching based, linear based, or a combination of the two.

Applications and Functionality

42. The present invention can be applied and/or used in numerous applications. Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management, security systems, miniature weapons computers, space probe central control processor, beacon processor, and jet engine control. The invention may also be used on the manufacturing floor for smart, discontinuous low-level sensing, test equipment probes, embedded credit card processors, wearable computers, or remote data logging.

43. The inclusion of the FPGA in the design of the present invention provides a simultaneous parallel processing capability that can be implemented as a mathematical coprocessor and still perform as a digital signal processor (DSP) of multiple analog signals simultaneously digitized by the ADC, all the while switching input lines to the ADC.

44. The present invention has been designed especially for managing multiple sensors, both discrete and continuous. Because of the fast and high precision ADC included in a preferred embodiment, the FPGA can perform vibration signature analysis and harmonic analysis using DSP algorithms. This capability is used in determining the health and condition of transmissions, engines and other rotating equipment. Used in a wired system, the invention is able to perform DSP analysis of the wiring and the items connected to the wiring. The invention can determine the condition of power signals as well as digital signals and can be used with micro-light sources to determine the health of fiber optic carriers.

45. In a preferred embodiment, the present invention can implement a bi-directional scheme for extending the operating voltage range of discrete drivers through a smart-signal concept. For outputs, one of two charge pumps are selected by the CMOS-level I/O in the CPU. These charge pumps are programmable in voltage and can be set to a large range of values. In this manner, a (0V, 3.3V) discrete can be transformed into a (-4V, +5V) signal, as an example. For inputs, an agile analog gain and offset scheme can be employed. In this case, the gain and offset coefficients are selected and implemented by DACs such that the output voltages are converted to the (0V, V.sub.dd) range.

46. The foregoing description details certain preferred embodiments of the present invention and describes the best mode contemplated. It will be appreciated, however, that the invention can be practiced in many ways and is not intended to be limited or restricted in any fashion except as defined in the claims which follow, and any equivalents thereto.

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CLAIMS

What is claimed is:

1. A multi-chip module instrument controller comprising:

a non-volatile memory storage component for program and data storage;

a large volatile memory storage component for additional program and data storage;

a processor coupled to both said non-volatile memory storage component and said large volatile memory storage components, said processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

a plurality of gates arranged in a field programmable gate array, said gate array coupled to said processor and configured to run independent processes in parallel with said processor; and

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to said processor.

2. The multi-chip module instrument controller of claim 1, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog.

3. The multi-chip module instrument controller of claim 1, wherein:

a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the multi-chip module instrument controller.

4. The multi-chip module instrument controller of claim 1, wherein the microprocessor includes an embedded memory that enables the startup of processing without first loading a program from the non-volatile memory.

5. The multi-chip module instrument controller of claim 1, further comprising a resettable digital real-time quartz controlled clock for accurate date and time stamping of data before it is stored in the non-volatile memory.

6. The multi-chip module instrument controller of claim 5, wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

7. A multi-chip module instrument controller comprising:

a processor configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power; and

a plurality of gates arranged in a field programmable gate array, said gate array coupled to said processor and configured to run independent processes in parallel with said processor.

8. The multi-chip module instrument controller of claim 7, further comprising:

a non-volatile memory storage component coupled to said processor for program and data storage;

at least two internal oscillators coupled to the processor for providing clock signals for low-frequency and high-frequency operations;

a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to said processor.

9. The multi-chip module instrument controller of claim 8, further comprising a plurality of analog outputs each output being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

10. The multi-chip module instrument controller of claim 8, wherein a portion of the gates in the field programmable gate array is configured to operate as an

internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

11. A method for conducting multiple parallel signal processing using a single multi-chip module instrument controller having a processor and a field programmable array, said method comprising:

receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths (thereby generating digital inputs),

providing a first portion of said digital inputs to said processor,

providing a remaining portion of said digital inputs to said field programmable gate array;

performing digital signal processing on said first portion of said digital inputs utilizing the processor; and

receiving the remaining portion of the digital inputs at the field programmable gate array and configuring a first portion of the gates in the field programmable gate array to perform digital signal processing on the remaining portion of said digital inputs, thereby conducting multiple parallel signal processing using a single multi-chip module instrument controller.

12. The method for conducting multiple parallel monitoring and control functions using a single multi-chip module instrument controller as in claim 11, further comprising the additional step of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations.

13. The method for conducting multiple parallel monitoring and control functions using a single multi-chip module instrument controller as in claim 11, further comprising the step of configuring a section portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

ABSTRACT

A multi-chip module instrument controller having various interface and operational capabilities. The controller incorporates a microprocessor and both volatile and non-volatile memories. The controller includes variable analog-to-digital conversion bit depths, with higher bit depths for some applications. Additionally, the controller includes a separately controllable field programmable gate array that acts as a parallel processor with internal or separate external clock. The FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.

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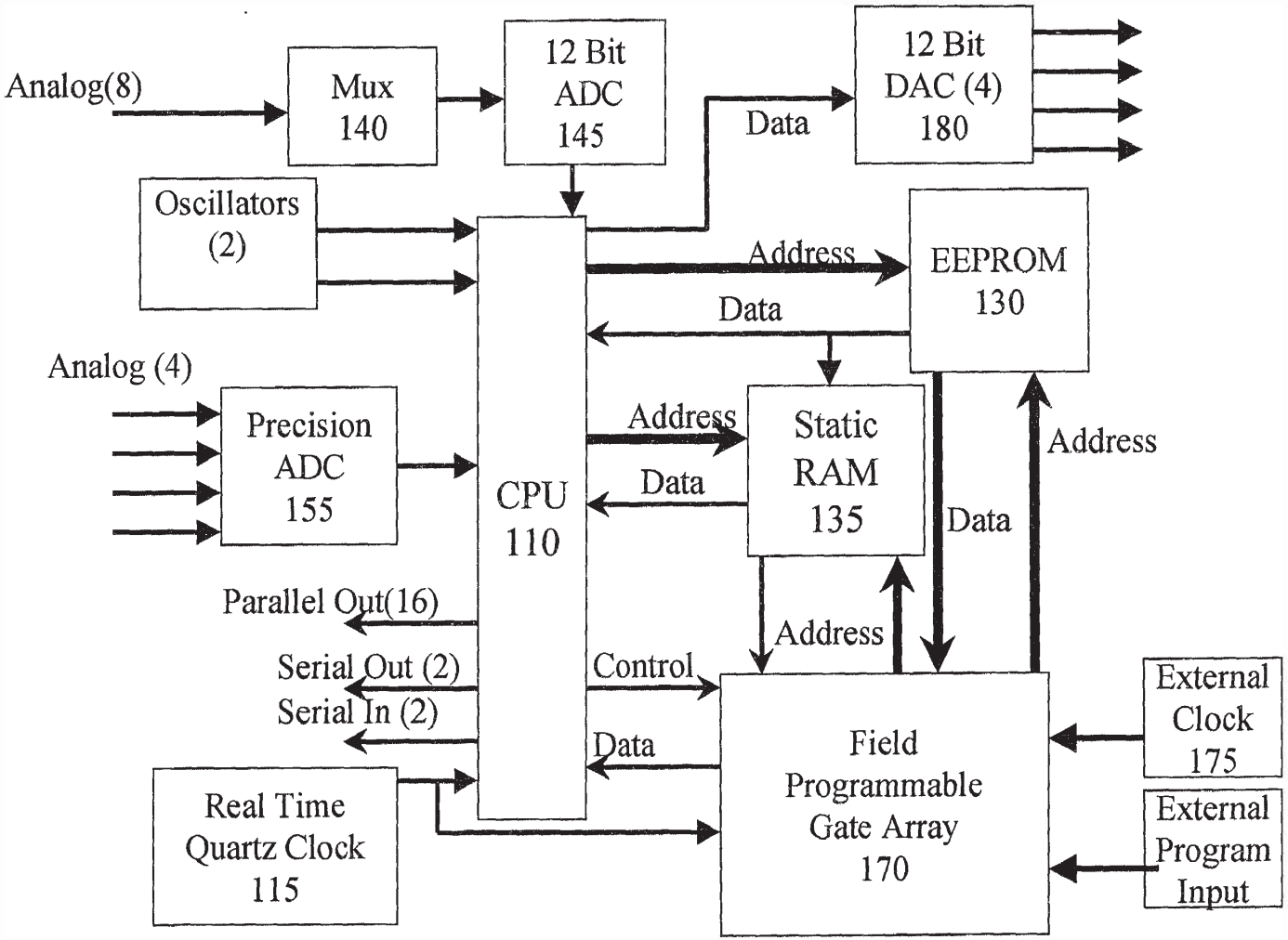


Fig. 1

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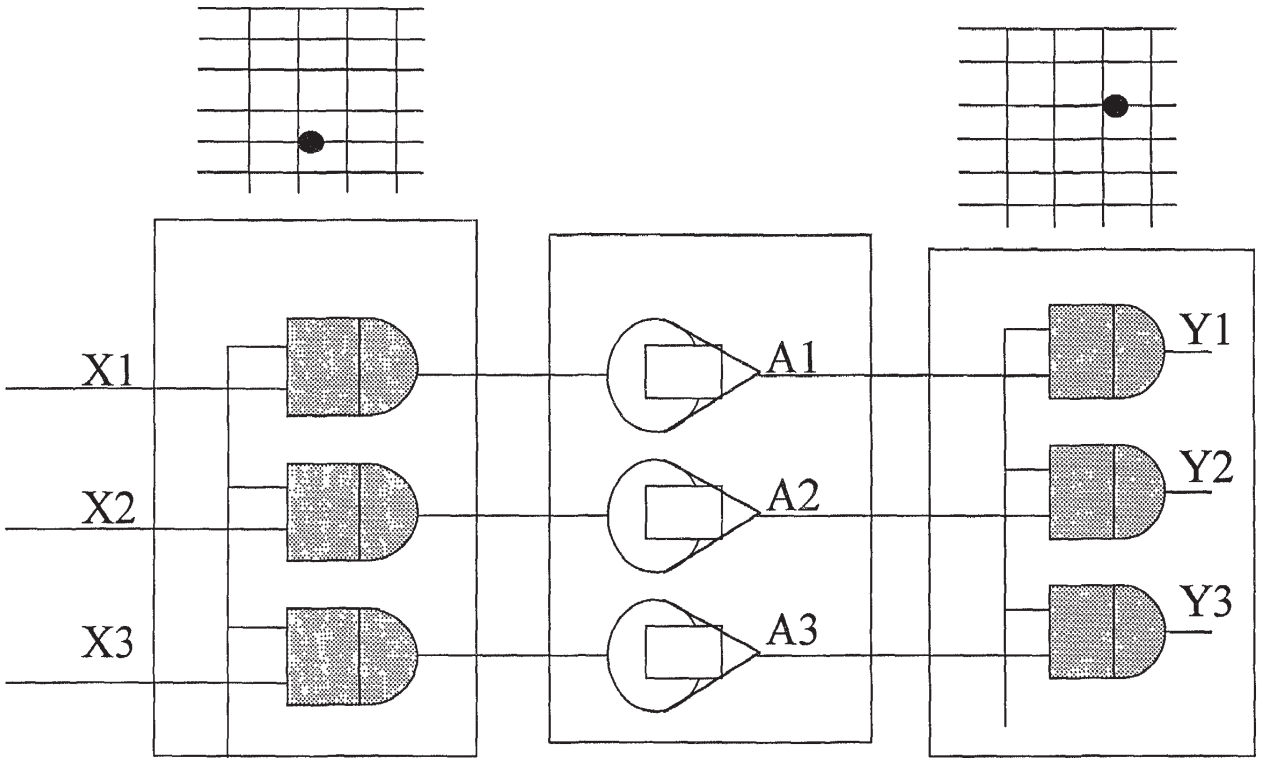


Fig. 2

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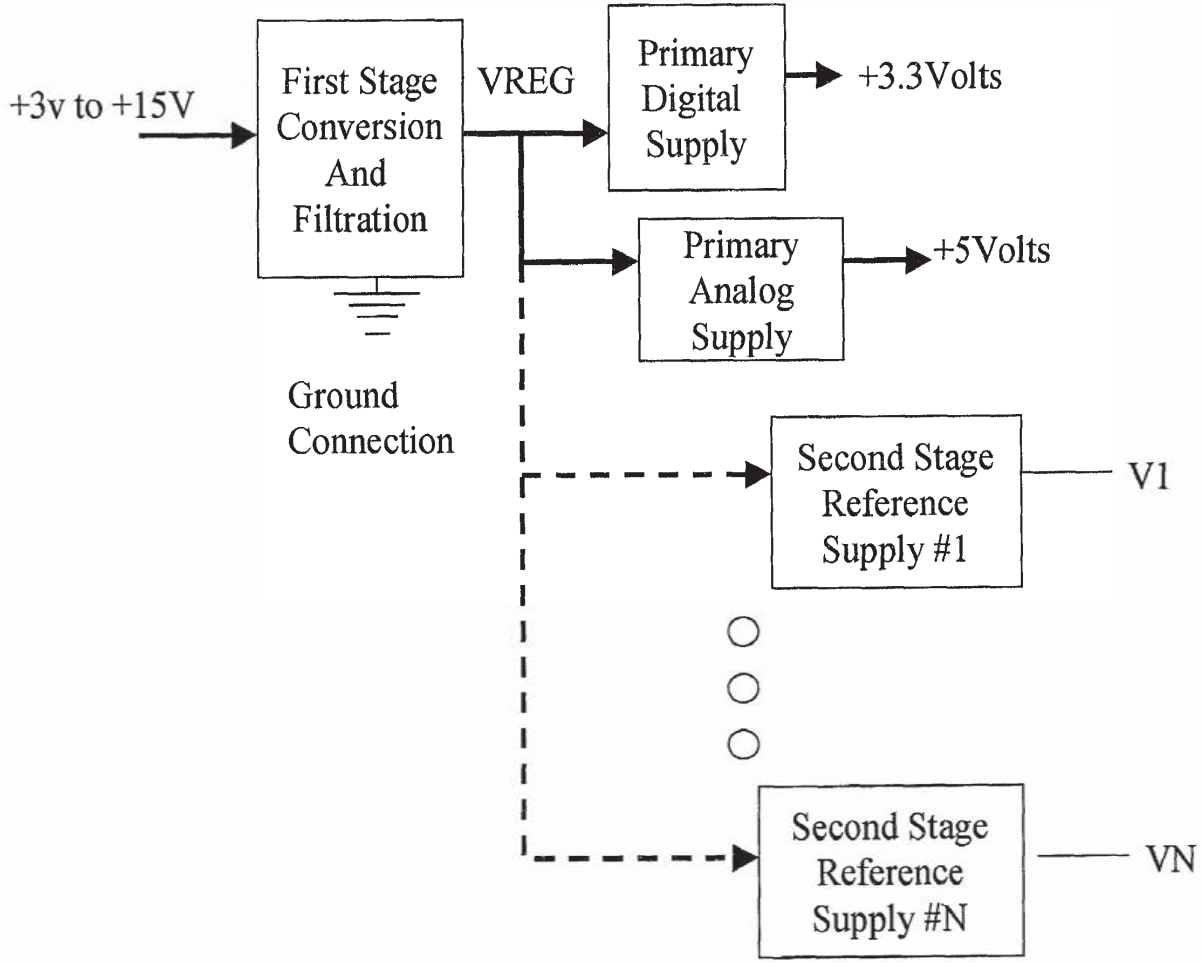

+3v to +15V
First Stage Conversion And Filtration
VREG
Primary Digital Supply
+3.3Volts
Primary Analog Supply
+5Volts
Ground Connection
Second Stage Reference Supply #1
V1
Second Stage Reference Supply #N
VN

Fig. 3

Express Mail Label No. EL 727855210 US

Docket No.
97Y-84435

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MULTI-CHIP MODULE SMART CONTROLLER HAVING VARIABLE ANALOG-TO-DIGITAL CONVERSION AND BUILT IN FIELD PROGRAMMABLE GATE ARRAY FOR PARALLEL PROCESSES

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Sole or first inventor's signature Kenneth L. Blemel Date December 19, 2001
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Albuquerque, New Mexico 87112

Full name of second inventor, if any
Second inventor's signature Date
Residence
Citizenship
Post Office Address

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

12/31/2001 JBALINAN 00000121 10028556
01 FC:201 370.00 OP

PTO-1556
(5/87)

*U.S. GPO: 2000-468-987/39595

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 97Y - 8443

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	13	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	13 minus 20=	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL	370	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/01)

☆U.S.GPO 2001 482-124 / 59197

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

CLAIMS ONLY

SERIAL NO.	FILING DATE
10/028,556	12-18-01
APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
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TOTAL DEP.	10					
TOTAL CLAIMS	13					

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TOTAL IND.		⬇		⬇		⬇
TOTAL DEP.						
TOTAL CLAIMS						

*MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

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*U.S. GPO: 1998-443-593/89152