DSP96002

32-BIT GENERAL PURPOSE FLOATING-POINT DUAL-PORT PROCESSOR

The DSP96002 is designed to support intensive graphic image and numeric processing. It is a dual-port, low-power, general purpose floating-point processor. The DSP includes 1024 words of data RAM (equally divided into X data and Y data memory), 1024 words of full-speed on-chip Program RAM, two data ROMs, a dual-channel Direct Memory Access (DMA) controller, special on-chip bootstrap hardware, and On-Chip Emulation (OnCE™) debug circuitry. The Central Processing Unit (CPU) consists of three 32-bit execution units operating in parallel. The DSP96002 has two identical memory expansion ports with control lines to facilitate interfacing SRAMs, DRAMs (operating in their fast access modes), and Video RAMs (VRAMs). Each port can be configured as a Host Interface (HI), which facilitates easy interface with other processors for multiprocessor applications. Linear arrays of DSP96002s can be implemented without glue logic. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The high speed of the DSP96002 makes it well-suited for high bandwidth and numerically intensive applications that require floating-point processing and access to large memory subsystems.

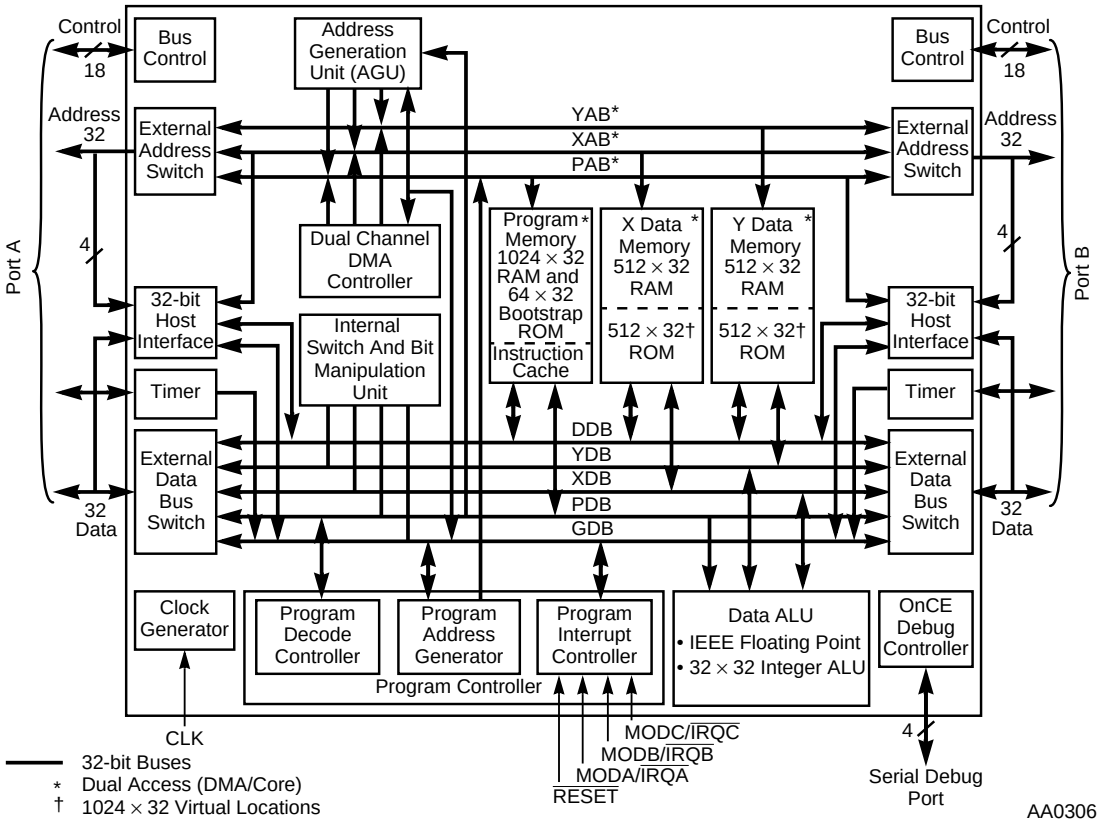

Figure 1 Block Diagram

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FOR TECHNICAL ASSISTANCE:

Telephone: 1-800-521-6274

Email: dsphelp@dsp.sps.mot.com

Internet: http://www.motorola-dsp.com

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

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FEATURES

- Digital signal processing core
  - Efficient 32-bit DSP engine
  - Conforms to IEEE 754-1985 standard for single precision (32-bit) and single extended precision (44-bit) arithmetic
  - Up to 30 Million Instructions Per Second (MIPS) at 60 MHz
  - Parallel operation of Data ALU, Address Generation Unit (AGU), and program controller within the CPU allow more processing per instruction cycle
  - Single-cycle 32×32 bit parallel multiplier
  - Highly parallel instruction set with unique DSP addressing modes
  - Nested hardware DO loops
  - Instruction cache extended to operate as 4 K byte (1 K word)
  - Fast auto-return interrupts
  - Address buses:
    - One 32-bit unidirectional internal X memory Address Bus (XAB)
    - One 32-bit unidirectional internal Y memory Address Bus (YAB)
    - One 32-bit internal Program Address Bus (PAB)
    - Two 32-bit external address buses
  - Data buses:
    - One 32-bit bidirectional internal X memory Data Bus (XDB)
    - One 32-bit bidirectional internal Y memory Data Bus (YDB)
    - One 32-bit bidirectional internal Global memory Data Bus (GDB)
    - One 32-bit bidirectional internal DMA Data Bus (DDB)
    - One 32-bit bidirectional internal Program Data Bus (PDB)
    - Two 32-bit external data buses
  - MCU-like instruction set mnemonics make programming easier
- Memory
  - On-chip 1024×32-bit Program RAM
  - Two independent on-chip 512×32-bit data RAMs
  - Two independent on-chip 512×32-bit data ROMs (1024×32-bit virtual memory)
  - On-chip 64×32-bit bootstrap ROM

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- Off-chip expansion to 2×2^{32} 32-bit words of data memory
- Off-chip expansion to 2^{32} 32-bit words of program memory

• Miscellaneous features

- Two expansion ports assignable to X data, Y data, or program memory spaces or a combination thereof, effectively doubling off-chip bus bandwidth.
- Host interface circuitry on each port provides a flexible slave interface to Direct Memory Access (DMA) controllers and external processors for easy design of multimaster systems
- Write strobe pins support interface to external SRAMs without additional logic
- Two programmable timers/counters
- Three external interrupt/mode control lines
- One external reset line for hardware reset
- 4-pin OnCE port for unobtrusive, processor speed-independent debugging
- HCMOS design for operating frequencies from 60 MHz down to DC
- 223-pin plastic Pin Grid Array (PGA) package or 240-pin Ceramic Quad Flat Pack (CQFP) package
- 5.0 V power supply

PRODUCT DOCUMENTATION

The two manuals listed in **Table 1** are required for a complete description of the DSP96002 and are necessary to design properly with the device. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 Additional Documentation

Document Name	Description	Order Number
DSP96002 User's Manual	Detailed description of the DSP96002 core processor and peripherals	DSP96002UM/AD
DSP96002 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP96002/D

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SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

SIGNAL GROUPINGS

The input and output signals of the DSP96002 are organized into eight functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**.

Table 1-1 DSP96002 Functional Signal Groupings

Functional Group	Detailed Description
Power (V_{CCN} and V_{CCQ})	**Table 1-2**
Ground (GND_N and GND_Q)	**Table 1-3**
Clock (CLK)	**Table 1-4**
Interrupt and Mode Control	**Table 1-5**
Port A (Address, Data, and Control)	**Table 1-6**
Port B (Address, Data, and Control)	**Table 1-6**
Timer/Event Counters	**Table 1-7**
OnCE Port	**Table 1-8**

Figure 1-1 is a diagram of DSP96002 signals by functional group.

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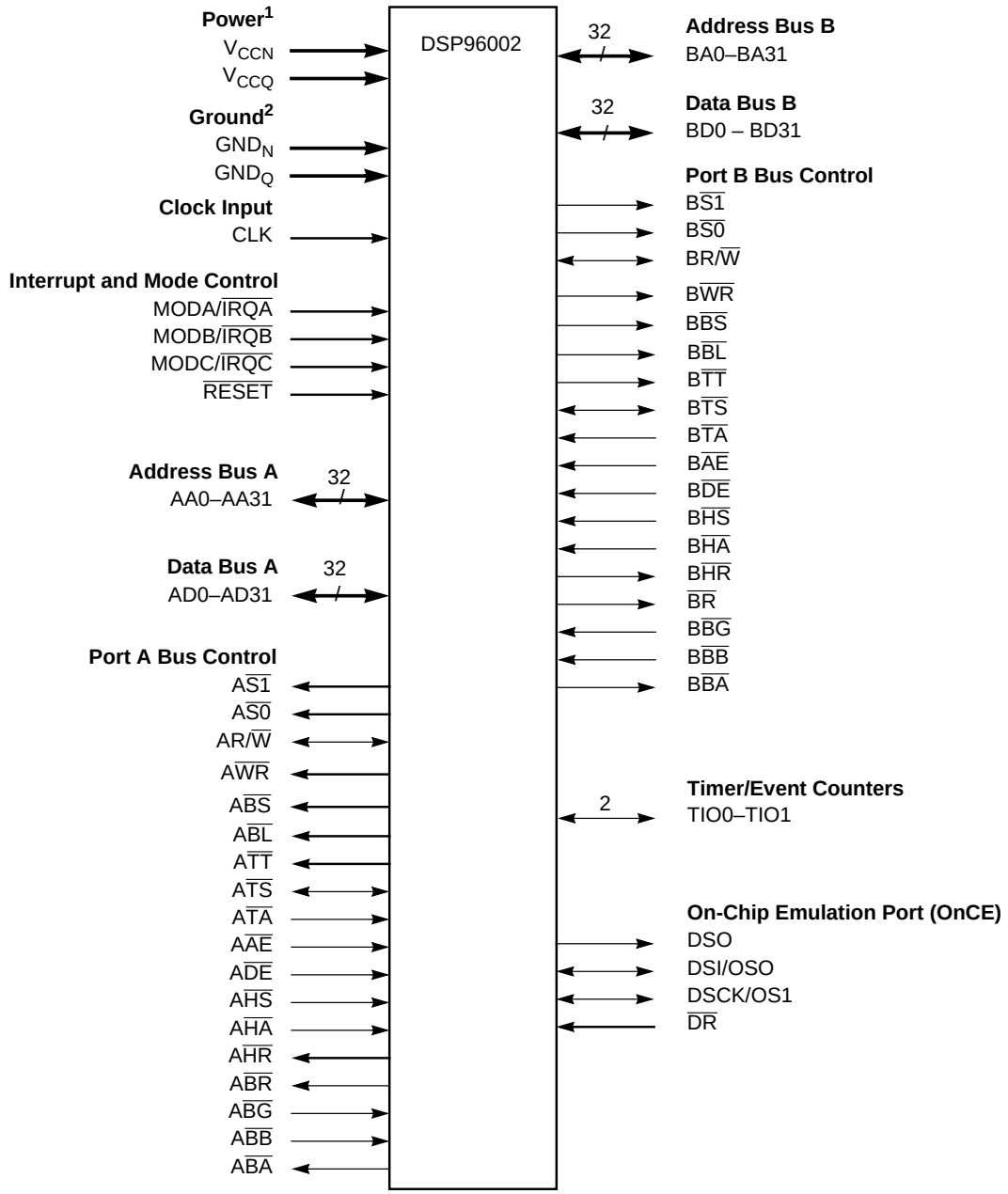

Note: 1. Number of power input pins is package dependent. See **Section 3**.
2. Number of ground connections is package dependent. See **Section 3**.

Figure 1-1 Functional Group Pin Allocations

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POWER

Table 1-2 Power Inputs

Power Name	Description
V_{CCN}	**Normal Power** —V_{CCN} inputs are V_{CC} provided for general use with the DSP96002 peripheral circuits. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCQ}	**Quiet Power—**V_{CCQ} inputs provide isolated power for the internal processing logic. The voltage should be well-regulated, and the input should be provided with an extremely low impedance path to the V_{CC} power rail. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
Note: The number of available power connecctions is package-dependent. See **Section 3** for a detailed description of individual package pinouts.	

GROUND

Table 1-3 Grounds

Ground Name	Description
GND_N	**Normal Ground** —GND_P connections provide a ground return for the DSP96002 peripheral circuits. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_Q	**Quiet Ground** —GND_Q is an isolated ground for the internal processing logic. The connection should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
Note: The number of available ground connecctions is package-dependent. See **Section 3** for a detailed description of individual package pinouts.	

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CLOCK

Table 1-4 Clock Signal

Signal Name	Type	State During Reset	Signal Description
CLK	Input	Input	**Clock Input**—CLK is a high frequency processor clock input. The frequency is twice the instruction rate. As shown in **Figure 1-2**, an internal phase generator divides CLK into four phases (t_0, t_1, t_2 and t_3), which is the basic instruction execution cycle. Additional t_w phases are optionally generated to insert Wait States (WS) into instruction execution. A Wait State is formed by pairing a t_2 and t_w phase. CLK should be continuous with a 46–54% duty cycle.

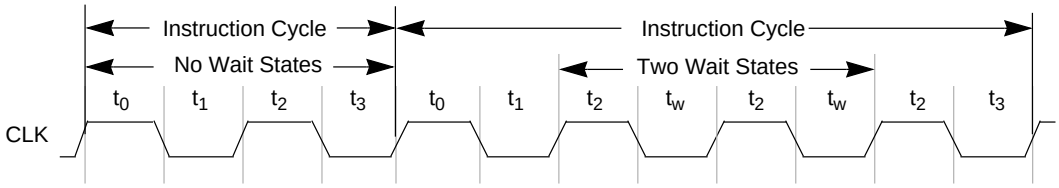

Figure 1-2 Clock Input and Instruction Cycle Timing

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INTERRUPT AND MODE CONTROL

Table 1-5 Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Input	**Reset**—This input is a direct hardware reset of the processor. When $\overline{\text{RESET}}$ is asserted low, the signal is internally synchronized to the input clock (CLK), the DSP is placed in the Reset state, and the internal phase generator is reset. A Schmitt trigger input is used for noise immunity and allows a slowly rising input (such as a capacitor charging) to reliably reset the chip. If $\overline{\text{RESET}}$ is deasserted synchronous to the input clock (CLK), exact start-up timing is guaranteed, allowing multiple processors to start-up synchronously and operate together in "lock-step." When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODA, MODB and MODC pins.
MODA / $\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A**—This input is internally synchronized to the input clock (CLK). MODA / $\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB and MODC select one of eight initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ pin is deasserted. If $\overline{\text{IRQA}}$ is asserted synchronous to the input clock (CLK), multiple processors can be resynchronized by using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.
MODB / $\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B**—This input is internally synchronized to the input clock (CLK). MODB / $\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB and MODC select one of eight initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ pin is deasserted. If $\overline{\text{IRQB}}$ is asserted synchronous to the input clock (CLK), multiple processors can be resynchronized by using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the Wait state.

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Table 1-5 Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
MODC / $\overline{\text{IRQC}}$	Input	Input	**Mode Select C/External Interrupt Request C—**This input is internally synchronized to the input clock (CLK). MODC / $\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB and MODC select one of eight initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ pin is deasserted. If $\overline{\text{IRQC}}$ is asserted synchronous to the input clock (CLK), multiple processors can be resynchronized by using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the Wait state.

PORT A AND PORT B

Port A and Port B are identical in pinout and function. The following pin descriptions apply to both ports. Each port may be a bus master and each port has a slave Host Interface which can be accessed on demand.

Table 1-6 Port A and Port B

Signal Name	Type	State During Reset	Signal Description
AA0–AA31 BA0–BA31	Input or Output	Tri-stated	**Address Bus—**A0–A31 specify the address for external program and data memory accesses. If there is no external bus activity, A0–A31 remain at their previous values. The Address Enable ($\overline{\text{AE}}$) input acts as an output enable control for A0–A31. A0–A31 are stable whenever the transfer strobe $\overline{\text{TS}}$ is asserted and may change only when $\overline{\text{TS}}$ is deasserted. The signal direction depends on whether the DSP is the bus master: • **Bus Master**—A0–A31 are tri-state, active high outputs. • **Not a Bus Master**—A2–A5 are active high inputs used to select the Host Interface register. Lines A0–A1 and A6–A31 are tri-stated. As inputs, A2–A5 may change asynchronously relative to the input clock (CLK).

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
AD0–AD31 BD0–BD31	Input/ Output	Tri-stated	**Data Bus**—D0–D31 are tri-state, active high, bidirectional input/outputs whether the DSP is a bus master or not. The Data Enable ($\overline{DE}$) input acts as an output enable control for D0–D31. As a bus master, the data lines are controlled by the CPU instruction execution or the DMA controller. D0–D31 are also the Host Interface data lines. If there is no external bus activity, D0–D31 are tri-stated.
A$\overline{S0}$–A$\overline{S1}$ B$\overline{S0}$–B$\overline{S1}$	Output	Tri-stated	**Space Select—**These signals can be viewed in different ways, depending on how the external memories are mapped. They support splitting memory spaces among ports, and mapping multiple memory spaces into the same physical memory locations. $\overline{S0}$ and $\overline{S1}$ are outputs when the DSP is the bus master and tri-stated when the DSP is not a bus master. Timing is the same as the address lines A0–A31.
AR/$\overline{W}$ BR/$\overline{W}$	Input or Output	Tri-stated	**Read/Write—**R/$\overline{W}$ is a an output when the DSP is the bus master and an input when not a bus master. Bus master timing is the same as the DSP96002 address lines, giving an "early write" signal for DRAM interfacing. R/$\overline{W}$ is high for a read access and low for a write access. The R/$\overline{W}$ pin is also the Host Interface read/write input. As an input, R/$\overline{W}$ may change asynchronously relative to the input clock. R/$\overline{W}$ goes high if the external bus is not used during an instruction cycle.
A$\overline{WR}$ B$\overline{WR}$	Output	Tri-stated	**Write Strobe** —$\overline{WR}$ is an output when the DSP is the bus master and tri-stated when it is not a bus master. $\overline{WR}$ supports a glueless interface to external SRAMs. $\overline{WR}$ is asserted during external memory write cycles to indicate that the address lines A0–A32, S1, S0, $\overline{BS}$, $\overline{BL}$, and R/$\overline{W}$ are stable. The output data goes to the data bus after $\overline{WR}$ is asserted. $\overline{WR}$ requires a weak external pull-up resistor and can be connected directly to the $\overline{WE}$ pin of a Static RAM.
A$\overline{BS}$ B$\overline{BS}$	Output	Tri-stated	**Bus Strobe—**$\overline{BS}$ is an output when the DSP is the bus master and tri-stated when it is not a bus master. Bus strobe is asserted at the start of a bus cycle (providing an "early bus start" signal for DRAM interfacing) and deasserted at the end of the bus cycle. The early negation provides an "early bus end" signal useful for external bus control. If the external bus is not used during an instruction cycle, $\overline{BS}$ remains deasserted until the next external bus cycle.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{TT}$ B$\overline{TT}$	Output	Tri-stated	**Transfer Type**—$\overline{TT}$ is an output when the DSP is the bus master and tri-stated when it is not a bus master. When the DSP is the bus master, $\overline{TT}$ is controlled by an on-chip page circuit. $\overline{TT}$ is asserted when a fast access memory mode (Page, Static Column, Nibble or Serial Shift Register) is detected. If the external bus is not used during an instruction cycle, or a fault is detected by the page circuit during an external access, $\overline{TT}$ remains deasserted. The parameters of the page circuit fault detection are user programmable.
A$\overline{TS}$ B$\overline{TS}$	Input or Output	Tri-stated	**Transfer Strobe—**$\overline{TS}$ is an output when the DSP is the bus master and an input when it is not a bus master. When the DSP is the bus master, $\overline{TS}$ is asserted to indicate that the address lines A0–A31, S1, S0, $\overline{BS}$, $\overline{BL}$ and R/$\overline{W}$ are stable and that a bus read or bus write transfer is taking place. During a read cycle, input data is latched inside the DSP96002 on the rising edge of $\overline{TS}$. During a write cycle, output data is placed on the data bus after $\overline{TS}$ is asserted. Therefore, $\overline{TS}$ can be used as an output enable control for external data bus buffers if they are present. If the external bus is not used during an instruction cycle, $\overline{TS}$ remains deasserted until the next external bus cycle. An external flip-flop can delay $\overline{TS}$, if required, for slow devices or more address decoding time. The $\overline{TS}$ pin is also the Host Interface transfer strobe input used to enable the data bus output drivers during host read operations and to latch data inside the Host Interface during host write operations. As an input, $\overline{TS}$ may change asynchronously relative to the input clock. Write data is latched inside the Host Interface on the rising edge of $\overline{TS}$. When the DSP is the bus master, the combination of $\overline{BS}$ and $\overline{TS}$ can be decoded externally to determine the status of the current bus cycle and to generate hardware strobes useful for latching address and data signals.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{\text{TA}}$ B$\overline{\text{TA}}$	Input	Input, ignored during reset	**Transfer Acknowledge—** The $\overline{\text{TA}}$ input is a synchronous "DTACK" function that can extend an external bus cycle indefinitely. $\overline{\text{TA}}$ must be asserted and deasserted synchronously to the input clock (CLK) for proper operation. $\overline{\text{TA}}$ is sampled on the falling edge of the input clock (CLK). Any number of wait states (0, 1, 2, …, infinity) may be inserted by keeping $\overline{\text{TA}}$ deasserted. In a typical operation, $\overline{\text{TA}}$ is first deasserted at the start of a bus cycle, then is asserted to enable completion of the bus cycle, and finally is deasserted before the next bus cycle.The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronously to CLK. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the Bus Control Register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. If $\overline{\text{TA}}$ is tied low (asserted) and no wait states are specified in the BCR, zero wait states will be inserted into external bus cycles. Note: If the DSP96002 is the bus master and there is no external bus activity or the DSP96002 is not the bus master, then the $\overline{\text{TA}}$ input is ignored by the core.
A$\overline{\text{AE}}$ B$\overline{\text{AE}}$	Input	Input, ignored during reset	**Address Enable—**$\overline{\text{AE}}$ is an input that must be asserted and deasserted synchronous to the input clock (CLK) for proper operation. If the DSP is the bus master, $\overline{\text{AE}}$ is asserted to enable the A0–A31 address output drivers. If $\overline{\text{AE}}$ is deasserted, the address output drivers are tri-stated. If the DSP is not a bus master, the address output drivers are tri-stated regardless of whether $\overline{\text{AE}}$ is asserted or deasserted. The function of $\overline{\text{AE}}$ is to allow implementation of multiplexed bus systems. An example of such an implementation is a multiplexed address1 / address2 bus used with dual port memories, such as dynamic VRAMs. Note: There must be at least one undriven CLK period between enables for multiplexed buses to allow one bus to tri-state before another bus is enabled. External control is responsible for this timing. For non-multiplexed systems, $\overline{\text{AE}}$ should be tied low.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{DE}$ B$\overline{DE}$	Input	Input, ignored during reset	**Data Enable**—$\overline{DE}$ is an input that must be asserted and deasserted synchronous to the input clock (CLK) for proper operation. If a bus master or the Host Interface is being read, $\overline{DE}$ is asserted to enable the D0–D31 data bus output drivers. If $\overline{DE}$ is deasserted, the data bus output drivers are tri-stated. If not a bus master, the data bus output drivers are tri-stated regardless of whether $\overline{DE}$ is asserted or deasserted. Read-only bus cycles may be performed even though $\overline{DE}$ is deasserted. The function of $\overline{DE}$ is to allow multiplexed bus systems to be implemented. An example is a multiplexed data1 / data2 bus used for long word transfers with one 32-bit wide memory. Note: There must be at least one undriven CLK period between enables for multiplexed buses to allow one bus to tri-state before another bus is enabled. External control is responsible for this timing. For non-multiplexed systems, $\overline{DE}$ should be asserted (tied low).
A$\overline{HS}$ B$\overline{HS}$	Input	Input	**Host Select—**$\overline{HS}$ is an input that may change asynchronous to the input clock. $\overline{HS}$ is asserted low to enable selection of the Host Interface functions by the address lines A2–A5. If $\overline{TS}$ is asserted when $\overline{HS}$ is asserted, a data transfer with the Host Interface will take place. Note: Both $\overline{HS}$ and $\overline{HA}$ must be tied high to disable the Host Interface. When $\overline{HA}$ is asserted, $\overline{HS}$ is ignored.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{\text{HA}}$ B$\overline{\text{HA}}$	Input	Input	**Host Acknowledge**—$\overline{\text{HA}}$ is an input that may change asynchronously to the input clock. $\overline{\text{HA}}$ is used to acknowledge either an interrupt request or a DMA request by the Host Interface. When the Host Interface is not in DMA mode, asserting $\overline{\text{TS}}$ when $\overline{\text{HA}}$ and $\overline{\text{HR}}$ are asserted will enable the contents of the Host Interface Interrupt Vector Register (IVR) onto the data bus outputs D0–D31. This provides an interrupt acknowledge capability compatible with MC68000 family processors. If the Host Interface is in DMA mode, $\overline{\text{HA}}$ is used as a DMA transfer acknowledge input and it is asserted by an external device to transfer data between the Host Interface registers and an external device. In DMA read mode, $\overline{\text{HA}}$ is asserted to read the Host Interface RX register on the data bus outputs D0–D31. In DMA Write mode, $\overline{\text{HA}}$ is asserted to strobe external data into the Host Interface TX register. Write data is latched into the TX register on the rising edge of $\overline{\text{HA}}$.
A$\overline{\text{HR}}$ B$\overline{\text{HR}}$	Output	Driven high	**Host Request**—$\overline{\text{HR}}$ is an output that is never tri-stated. The host request $\overline{\text{HR}}$ is asserted to indicate that the Host Interface is requesting service—either an interrupt request or a DMA request—from an external device. The $\overline{\text{HR}}$ output may be connected to interrupt request input $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, or $\overline{\text{IRQC}}$ of another DSP96002. The on-chip DMA Controller channel of the other DSP96002 can select the interrupt request input as a DMA transfer request input.
A$\overline{\text{BR}}$ B$\overline{\text{BR}}$	Output	Driven high	**Bus Request**—$\overline{\text{BR}}$ is an output that is never tri-stated. $\overline{\text{BR}}$ is asserted when the CPU or DMA is requesting bus mastership. $\overline{\text{BR}}$ is deasserted when the CPU or DMA no longer needs the bus. $\overline{\text{BR}}$ may be asserted or deasserted independent of whether the DSP96002 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP96002 is the bus master (see the description of bus “parking” in the $\overline{\text{BA}}$ pin description). The RH bit in the Bus Control Register allows $\overline{\text{BR}}$ to be asserted under software control even though the CPU or DMA does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator, which controls the priority, parking, and tenure of each DSP96002 on the same external bus. $\overline{\text{BR}}$ is only affected by CPU or DMA requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the Bus Slave state.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{BG}$ $\overline{BBG}$	Input	Input, ignored during reset	**Bus Grant**—$\overline{BG}$ is an input that must be asserted / deasserted synchronous to the input clock (CLK) for proper operation. $\overline{BG}$ is asserted by an external bus arbitration circuit indicating the DSP96002 has become the pending bus master. When $\overline{BG}$ is asserted, the DSP96002 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction, which requires more than one external bus cycle for execution. Note: Indivisible read-modify-write instructions (BSET, BCLR, BCHG) will not give up bus mastership until the end of the current instruction. $\overline{BG}$ is ignored during hardware reset.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{BA}$ B$\overline{BA}$	Output	Tri-stated	**Bus Acknowledge**—$\overline{BA}$ is an open drain output. When deasserting $\overline{BA}$, the DSP96002 drives $\overline{BA}$ high during half a CLK cycle and then disables the active pull-up. In this way, only a weak external pull-up resistor is required to hold the line high. $\overline{BA}$ may be directly connected to $\overline{BB}$ in order to obtain the same functionality as the MC68040 $\overline{BB}$ pin. When $\overline{BG}$ is asserted, the DSP96002 becomes the pending bus master. It waits until $\overline{BB}$ is negated by the previous bus master, indicating that the previous bus master is off the bus. The pending bus master asserts $\overline{BA}$ to become the current bus master. $\overline{BA}$ is asserted when either the CPU or the DMA has taken the bus and is the bus master. While $\overline{BA}$ is asserted, the DSP96002 is the owner of the bus (the bus master). When $\overline{BA}$ is deasserted, the DSP96002 is a bus slave. $\overline{BA}$ may be used as a tri-state enable control for external address, data, and bus control signal buffers. Note: A current bus master may keep $\overline{BA}$ asserted after ceasing bus activity, regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to use the bus repeatedly without re-arbitration until some other device wants the bus. The current bus master keeps $\overline{BA}$ asserted during indivisible read-modify-write bus cycles, regardless of whether $\overline{BG}$ has been deasserted by the external bus arbitration unit. This form of “bus locking” allows the current bus master to perform atomic operations on shared variables in multitasking and multiprocessor systems. Current instructions that perform indivisible read-modify-write bus cycles are BCLR, BCHG and BSET.

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Table 1-6 Port A and Port B (Continued)

Signal Name	Type	State During Reset	Signal Description
A$\overline{BB}$ $\overline{BBB}$	Input	Input	**Bus Busy—**$\overline{BB}$ is an input that must be asserted and deasserted synchronous to the input clock (CLK) for proper operation. $\overline{BB}$ is deasserted when there is no bus master on the external bus. In multiple DSP96002 systems, all $\overline{BB}$ inputs are tied together and are driven by the logical AND of all $\overline{BA}$ outputs. $\overline{BB}$ is asserted when a pending bus master becomes the current bus master (directly or indirectly by $\overline{BA}$ assertion). $\overline{BB}$ is deasserted by the current bus master (directly or indirectly by $\overline{BA}$ deassertion) to indicate that it is off the bus and is no longer the bus master. The pending bus master monitors the $\overline{BB}$ signal until it is deasserted. Then the pending bus master asserts $\overline{BA}$ to become the current bus master, which asserts $\overline{BB}$ directly or indirectly. Note: Use of pull-up resistors is recommended.
A$\overline{BL}$ B$\overline{BL}$	Output	Driven high	**Bus Lock—**$\overline{BL}$ is an output that is never tri-stated. Asserted at the start of an external indivisible Read-Modify-Write (RMW) bus cycle (providing an “early bus start” signal for DRAM interfacing) and deasserted at the end of the write bus cycle, $\overline{BL}$ remains asserted between the read and write bus cycles of the read-modify-write bus sequence. $\overline{BL}$ can be used to indicate that special memory timing (such as RMW timing for DRAMs) may be used or to “resource lock” an external multi-port memory for secure semaphore updates. The early negation provides an “early bus end” signal useful for external bus control. If the external bus is not used during an instruction cycle, $\overline{BL}$ remains deasserted until the next external indivisible read-modify-write bus cycle. $\overline{BL}$ also remains deasserted if the external bus cycle is not an indivisible read-modify-write bus cycle or if there is an internal RMW bus cycle. The only instructions that automatically assert $\overline{BL}$ are a BSET, BCLR or BCHG instruction, which accesses external memory. $\overline{BL}$ can also be asserted by setting the LH bit in the BCR.

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TIMER/EVENT COUNTER

Table 1-7 Timer / Event Counters

Signal Name	Type	State During Reset	Signal Description
TIO0–TIO1	Input or Output	Input	**Timer/Event Counter** —The bidirectional TIO signal connects to the on-chip Timer / Event Counter. When TIO is used as an input, the module is functioning as an external event counter or is measuring external pulse width / signal period. When TIO is used as an output, the module is functioning as a timer, and TIO becomes the timer pulse. When the TIO pin is not used by the timer module, it can be used as a General Purpose Input / Output (GPIO) pin. The timer can use internal or external clocking and can interrupt the processor after a number of events specified by a user program, or it can signal an external device after counting internal events. The timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurs. When the timer is disabled, the TIO pin becomes tri-stated. To prevent undesired spikes from occurring, the TIO pin should be pulled up or down when it is not in use.

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OnCE PORT

Table 1-8 On-Chip Emulation Port (OnCE) Signals

Signal Name	Signal Type	State during Reset	Signal Description
DSI/OS0	Output	Low Output	**Debug Serial Input/Chip Status 0—**Serial data or commands are provided to the OnCE controller through the DSI/OS0 signal when it is an input. The data received on the DSI signal will be recognized only when the DSP has entered the Debug mode of operation. Data is latched on the falling edge of the DSCK serial clock. Data is always shifted into the OnCE serial port Most Significant Bit (MSB) first. When the DSI/OS0 signal is an output, it works in conjunction with the OS1 signal to provide chip status information. The DSI/OS0 signal is an output when the processor is not in Debug mode. When switching from output to input, the signal is tri-stated. Note: If the OnCE interface is in use, an external pull-down resistor should be attached to this pin. If the OnCE interface is not in use, the resistor is not required.
DSCK/OS1	Output	Low Output	**Debug Serial Clock/Chip Status 1—**The DSCK/OS1 signal supplies the serial clock to the OnCE when it is an input. The serial clock provides pulses required to shift data into and out of the OnCE serial port. (Data is clocked into the OnCE on the falling edge and is clocked out of the OnCE serial port on the rising edge.) The debug serial clock frequency must be no greater than $^{1}/_{8}$ of the processor clock frequency. When switching from input to output, the signal is tri-stated. When it is an output, this signal works with the OS0 signal to provide information about the chip status. The DSCK/OS1 signal is an output when the chip is not in Debug mode. Note: If the OnCE interface is in use, an external pull-down resistor should be attached to this pin. If the OnCE interface is not in use, the resistor is not required.

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Table 1-8 On-Chip Emulation Port (OnCE) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
DSO	Output	Output, pulled high	**Debug Serial Output—**Data contained in one of the OnCE controller registers is provided through the DSO output signal, as specified by the last command received from the external command controller. Data is always shifted out the OnCE serial port MSB first. Data is clocked out of the OnCE serial port on the rising edge of DSCK. The DSO signal also provides acknowledge pulses to the external command controller. When the chip enters the Debug mode, the DSO signal will be pulsed low to indicate (acknowledge) that the OnCE is waiting for commands. After the OnCE receives a read command, the DSO signal will be pulsed low to indicate that the requested data is available and the OnCE serial port is ready to receive clocks in order to deliver the data. After the OnCE receives a write command, the DSO signal will be pulsed low to indicate that the OnCE serial port is ready to receive the data to be written; after the data is written, another acknowledge pulse will be provided.
$\overline{\text{DR}}$	Input	Input	**Debug Request—**The Debug Request input ($\overline{\text{DR}}$) allows the user to enter the Debug mode of operation from the external command controller. When $\overline{\text{DR}}$ is asserted, it causes the DSP to finish the current instruction being executed, save the instruction pipeline information, enter the Debug mode, and wait for commands to be entered from the DSI line. While in Debug mode, the $\overline{\text{DR}}$ signal lets the user reset the OnCE controller by asserting it and deasserting it after receiving acknowledge. It may be necessary to reset the OnCE controller in cases where synchronization between the OnCE controller and external circuitry is lost. $\overline{\text{DR}}$ must be deasserted after the OnCE responds with an acknowledge on the DSO signal and before sending the first OnCE command. Asserting $\overline{\text{DR}}$ will cause the chip to exit the Stop or Wait state. Having $\overline{\text{DR}}$ asserted during the deassertion of $\overline{\text{RESET}}$ will cause the DSP to enter Debug mode. Note: If the OnCE interface is not in use, attach an external pull-up resistor to the $\overline{\text{DR}}$ input.

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SECTION 2

SPECIFICATIONS

INTRODUCTION

The digital signal processor (DSP) is fabricated using high-density Complementary Metal Oxide Semiconductor (CMOS) with Transistor-Transistor-Logic (TTL) compatible inputs and outputs. This section covers the maximum ratings, thermal characteristics, and electrical characteristics of the DSP96002.

Note: Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

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Table 2-1 Maximum Electrical Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0	V
All Input Voltages	V_{in}	GND – 0.5 to V_{CC} + 0.5	V
Current Drain per Pin excluding V_{CC} and V_{SS}[1]	I	10	mA
Operating Temperature Range	T_J	–40 to +100	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Note: GND = 0 VDC			

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	PGA Value	CQFP Value	Unit
Junction to Ambient[1]	$R_{\theta JA}$ or θ_{JA}	22	31	°C / W
Junction to Case[2]	$R_{\theta JC}$ or θ_{JC}	5.7	1.6	°C / W
Thermal characterization parameter	ψ_{JT}	5.2	1.0	°C / W

Note:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection. SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043, (415) 964-5111.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

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DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics

Characteristic[1]		Symbol	Min	Typical	Max	Unit
Supply Voltage,	+10% at 33.3 MHz +5% at 40 MHz +5% at 60 MHz	V_{CC}	4.5 4.75 4.75	5.0 5.0 5.0	5.5 5.25 5.25	V V V
Input High Voltage	Except CLK, $\overline{\text{RESET}}$ MODA, MODB,MODC	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	Except CLK, MODA, MODB, MODC	V_{IL}	–0.5	—	0.8	V
Input High Voltage	CLK	V_{IHC}	4.0	—	V_{CC}	V
Input Low Voltage	CLK	V_{ILC}	–0.5	—	0.6	V
Input High Voltage	$\overline{\text{RESET}}$	V_{IHR}	2.5	—	V_{CC}	V
Input High Voltage	MODA, MODB, MODC	V_{IHM}	3.5	—	V_{CC}	V
Input Low Voltage	MODA, MODB, MODC	V_{ILM}	–0.5	—	2.0	V
Input Leakage Current	—	I_{in}	–10	—	10	µA
Tri-State (Off-State) Input Current	@2.4 V / 0.5 V	I_{TSI}	–10	—	10	µA
Output High Voltage	I_{OH} = –10 µA	V_{OHC}	V_{CC} – 0.1	—	—	V
Output High Voltage	I_{OH} = –0.4 mA	V_{OH}	2.4	—	—	V
Output Low Voltage	I_{OL} = 10 µA	V_{OLC}	—	—	0.1	V

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Table 2-3 DC Electrical Characteristics (Continued)

Characteristic[1]		Symbol	Min	Typical	Max	Unit
Output Low Voltage	I_{OL} = 3.2 mA	V_{OL}	—	—	0.4	V
Power Dissipation	f = 33.3 MHz[2,3] f = 40 MHz[2,3] f = 60 MHz[2,3]	P_D	— — —	1.0 1.25 1.75	— — —	W
Total Supply Current	5 V, 33.3 MHz Wait Mode[2,3] Stop Mode[2,3] 5 V, 40 MHz Wait Mode[2,3] Stop Mode[2,3] 5 V, 60 MHz Wait Mode[2,3] Stop Mode[2,3]	I_{DD} I_{DDW} I_{DDS} I_{DD} I_{DDW} I_{DDS} I_{DD} I_{DDW} I_{DDS}	— — — — — — — — —	200 18 80 250 20 100 350 22 300	350 26 400 400 34 500 500 40 600	mA mA µA mA mA µA mA mA µA
Input Capacitance[4]	—	C_{in}	—	10	—	pF

Note:
1. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
2. P_D is measured for $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$V. with no DC loads. CLK is driven by a 50% duty-cycle oscillator.
3. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
4. Input capacitance is not tested in production.

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AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in this section are tested with the following values:

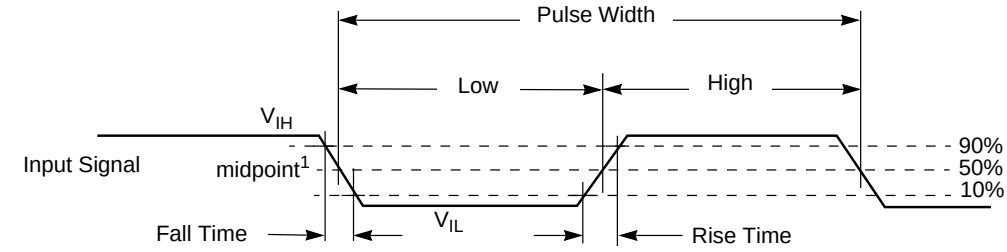
V_{IL} maximum of 0.5 V

V_{IH} minimum of 2.4 V for all pins[1]

Note: 1. CLK, $\overline{RESET}$, MODA, MODB, and MODC are tested using the input levels described in **DC Electrical Characteristics** on page 2-3.

AC timing specifications that are referenced to a device input signal are measured in production with respect to the V_{IH} / V_{IL} levels of the respective input signal's transition.

AC timing specifications that are referenced to a device's output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively. For load capacitances greater than 50pF, the drive capability of the output pins derates linearly at 1.5 ns per 20 pF of additional capacitance from 50 pF to 200 pF of loading, and at 2 ns per 20 pF of additional capacitance for loads greater than 200 pF.



Note: 1. The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$

Figure 2-1 Signal Measurement Reference

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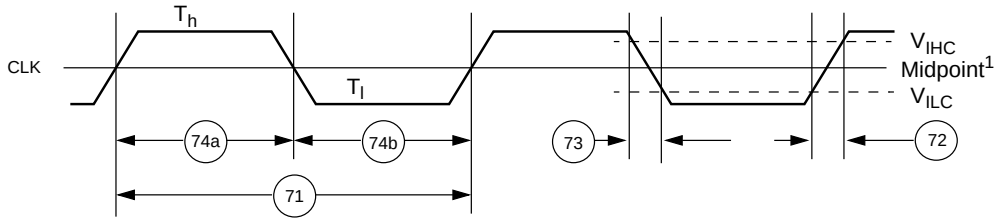
Clock Operation

The DSP96002 system clock is derived from a crystal or an external system clock signal. The clock input is an active high input, high frequency processor clock. The frequency is twice the instruction rate. An internal phase generator divides CLK into four phases (t_0, t_1, t_2 and t_3), which is the basic instruction execution cycle. Additional t_w phases are optionally generated to insert Wait States (WS) into instruction execution. A wait state is formed by pairing a t_2 and t_w phase. CLK should be continuous with a 46–54% duty cycle.

Table 2-4 Clock Operation

No.[1]	Characteristic[2]	Symb.	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
			Min	Max	Min	Max	Min	Max	
	Instruction Cycle Time = $2T_C$ = 4T Instruction Cycle Time = $2T_C$ = 4T	I_{cyc}	60	—	50	—	33.3	—	ns
	Wait State = T_C = 2T Wait State = T_C = 2T	WS	30	—	25	—	16.7	—	ns
71	CLK Cycle Time CLK Cycle Time	T_c	30	—	25	—	16.7	—	ns
72	CLK Rise Time		—	4	—	4	—	4	ns
73	CLK Fall Time		—	4	—	4	—	4	ns
74a	CLK High	T_h	14	16	11.5	13.5	7.7	9.5	ns
74b	CLK Low	T_l	14	16	11.5	13.5	7.7	9.5	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. 46%–54% Duty Cycle
4. 46.7%–53.3% Duty Cycle



Note: 1. The midpoint is 0.5 (V_{CC} – GND).

Figure 2-2 CLK Timing Diagram

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Arbitration Bus Timing

Table 2-5 Arbitration Bus Timing

No.[1]	Characteristic[2]	33.3 MHz		40 MHz		60 MHz		Unit
		Min	Max	Min	Max	Min	Max	
1	CLK High to $\overline{BR}$ Asserted / Deasserted	2	14	2	12	2	10	ns
2	$\overline{BG}$ Valid to CLK High (Setup)	6	—	5	—	5	—	ns
3	CLK High to $\overline{BG}$ Invalid (Hold)	2	—	2	—	2	—	ns
4	CLK High to $\overline{BA}$ Asserted / Deasserted	2	14	2	12	2	10	ns
5	$\overline{BB}$ Valid to CLK High (Setup)	6	—	5	—	4	—	ns
6	CLK High to $\overline{BB}$ Invalid (Hold)	2	—	2	—	2	—	ns
7	CLK High to A0–A31, S0–S1, R/$\overline{W}$, $\overline{BS}$, $\overline{TT}$, and $\overline{BL}$ Active	2	10	2	8	2	7	ns
8	A0–A31, S0–S1, R/$\overline{W}$, $\overline{BS}$, and $\overline{TT}$ tri-state to $\overline{BA}$ Deasserted	0	—	0	—	0	—	ns
9	CLK High to A0–A31, S0–S1, R/$\overline{W}$, $\overline{BS}$, and $\overline{TS}$ tri-state	2	12	2	10	2	8	ns
9a	CLK Low to $\overline{BA}$ tri-state	2	12	2	10	2	8	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C

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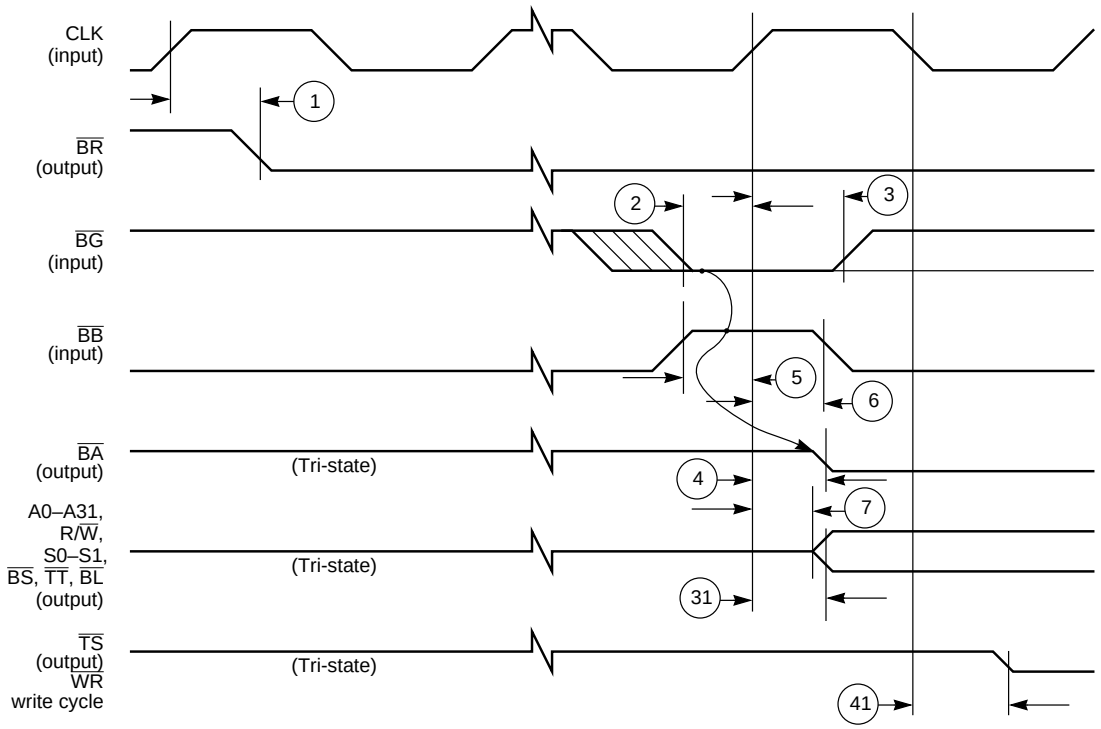

Figure 2-3 Bus Acquisition Timing

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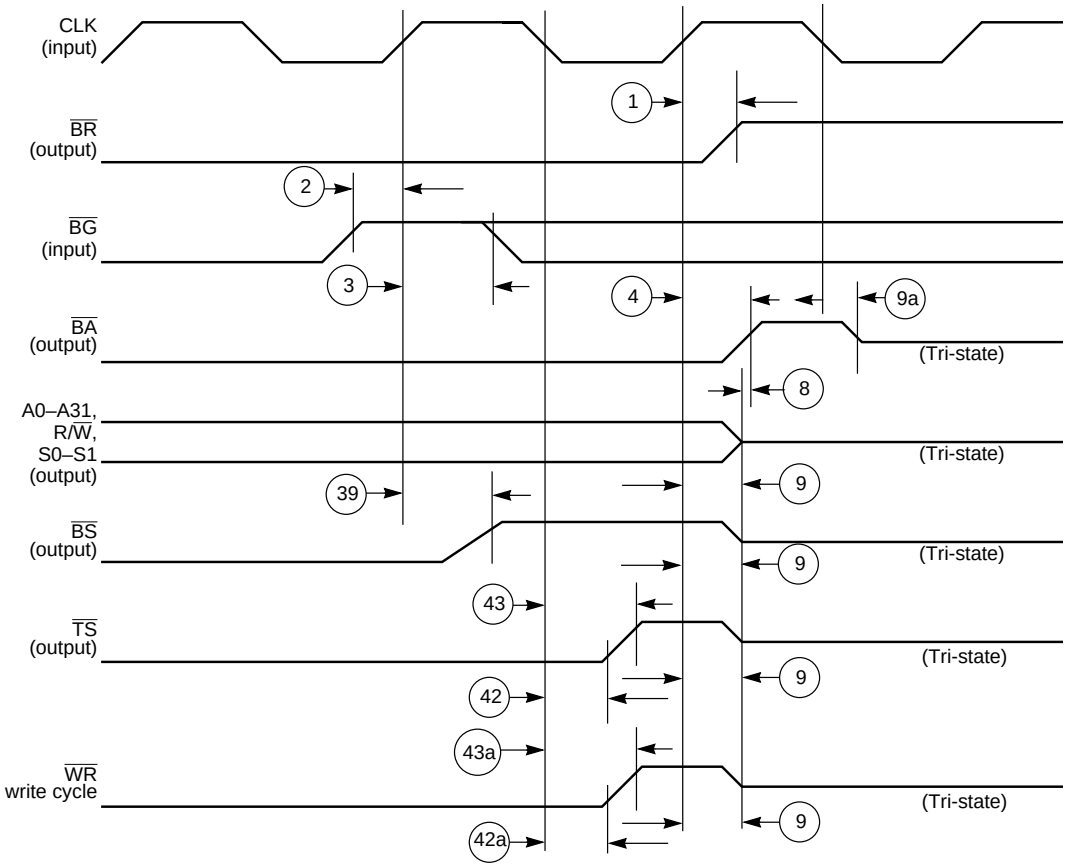

Figure 2-4 Bus Release Timing

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External Bus Relative Timing

Table 2-6 External Bus Relative Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
10	A0–A31, S0–S1, R/$\overline{W}$ Valid to $\overline{TS}$ Asserted Expression:	10[5]	16[6]	7.5[5]	13.5[6]	4.0[5]	9.5[6]	ns
11	A0–A31, S0–S1, R/$\overline{W}$ Valid to $\overline{TS}$ Deasserted	42[7]	—	33.5[8]	—	25.0[8]	—	ns
12	$\overline{TS}$ Width Asserted	30[9]	—	25[9]	—	17[9]	—	ns
12a	$\overline{WR}$ Width Asserted	27[27]	—	22[27]	—	15[27]	—	ns
13	$\overline{TS}$ Deasserted to R/$\overline{W}$, A0–A31 Invalid	6[10]	—	6.5[11]	—	6.5[11]	—	ns
13a	$\overline{WR}$ Deasserted to R/$\overline{W}$, A0–A31 Invalid	6	—	3.5	—	2.5	—	ns
14	$\overline{TS}$ Width Deasserted	21[12]	—	18[13]	—	1[613]	—	ns
14a	$\overline{WR}$ Width Deasserted	18	—	15	—	10	—	ns
15	$\overline{TS}$ Asserted to D0–D31 Valid (Write Cycle)	—	20[14]	—	17.5[14]	—	15[14]	ns
16	D0–D31 Valid to $\overline{TS}$ Deasserted (Write Cycle)	12[15]	—	8.5[16]	—	6[16]	—	ns
16a	D0–D31 Valid to $\overline{WR}$ Deasserted (Write Cycle)	12[28]	—	10[29]	—	6.5[29]	—	ns
17	$\overline{TS}$ Deasserted to D0–D31 Invalid (Write Cycle)	6[10]	—	6.5[11]	—	6.5[11]	—	ns
17a	$\overline{WR}$ Deasserted to D0–D31 Invalid (Write Cycle)	6	—	3.5	—	2.5	—	ns
18	$\overline{TS}$ Asserted to D0–D31 Active (Write Cycle)	10[17]	—	10[18]	—	7.7[18]	—	ns
19	$\overline{TS}$ Deasserted to D0–D31 Tri–state (Write Cycle)	—	16[19]	—	13.5[19]	—	11[19]	ns

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Table 2-6 External Bus Relative Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
19a	$\overline{WR}$ Deasserted to D0–D31 Three-state (Write Cycle)	—	16[19]	—	13.5[19]	—	11[19]	ns
20	$\overline{TS}$ Deasserted to D0–D31 Active (Write Cycle)	35[20]	—	31.5[21]	—	26.5[21]	—	ns
21	$\overline{TS}$ Asserted to D0–D31 Valid (Read Cycle)	—	21[22]	—	17.5[23]	—	14[23]	ns
22	$\overline{TS}$ Deasserted to D0–D31 Invalid (Hold) (Read Cycle)	0	—	0	—	0	—	ns
23	A0–A31, S0–S1, R/$\overline{W}$ Valid to D0–D31 Valid (Read Cycle)[24]	—	32[25]	—	26.5[26]	—	21[26]	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND= 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3% and no wait states
4. Assuming duty cycle in the range 46%–54% and no wait states
5. T_h–4
6. T_h
7. $(WS + 1)T_c + T_h$–2
8. $(WS + 1)T_c + T_h – 3$
9. $(WS + 1)T_c$
10. $T_l – 8$
11. $T_l – 5$
12. $T_c – 9$
13. $T_c – 7$
14. $T_l + 4$
15. $(WS)T_c + T_h – 2$
16. $(WS)T_c + T_h – 3$
17. $T_l – 4$
18. $T_l – 1.5$
19. T_l
20. $T_c + T_l – 9$
21. $T_c + T_l – 5$
22. $(WS + 1)T_c – 9$
23. $(WS + 1)T_c – 7.5$
24. Using T_h minimum
25. $(WS + 1)T_c + T_h – 12$
26. $(WS + 1)T_c + T_h – 10$
27. $T_c – 3$
28. $T_h – 2$
29. $T_h – 1.5$

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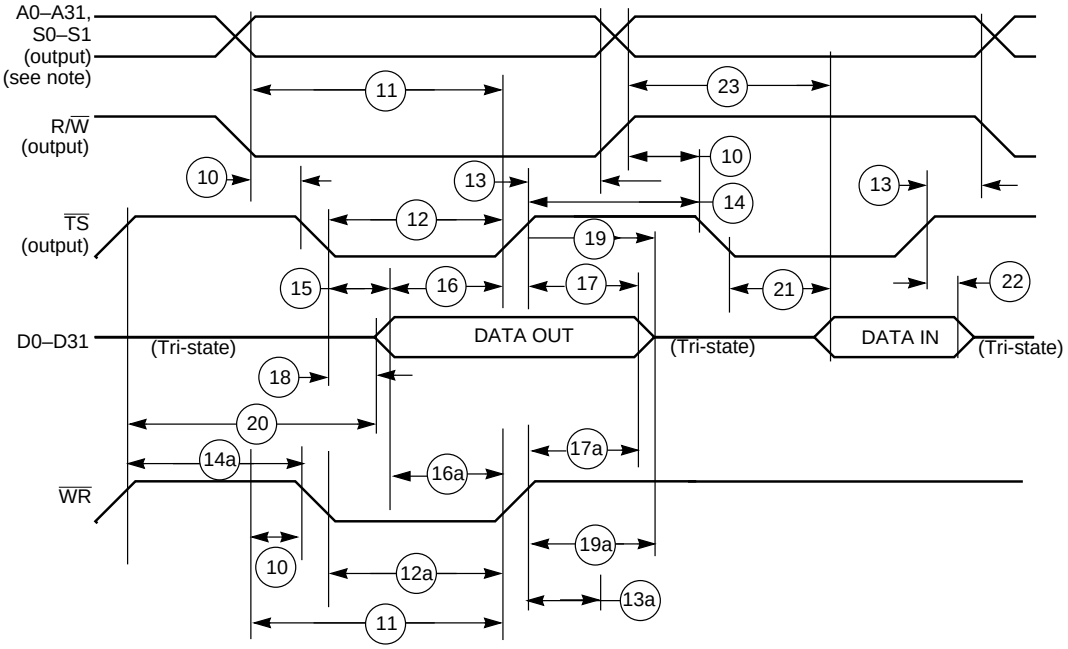

Note: During Read-Modify-Write instructions, A0–A31, S0–S1 do not change.

Figure 2-5 External Bus Relative Timing

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External Bus Synchronous Timing

Table 2-7 External Bus Synchronous Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
31	CLK High to A0–A31, S0–S1, R/$\overline{W}$ Valid and $\overline{TT}$, $\overline{BS}$, $\overline{BL}$ Asserted	2	14	2	12	2	10	ns
32	CLK High to A0–A31, S0–S1, R/$\overline{W}$ Invalid	2	—	1.5	—	1.5	—	ns
33	CLK High to D0–D31 Valid (Write Cycle)	2	14	2	12	2	10	ns
34	CLK High to D0–D31 Invalid (Write Cycle)	2	—	1.5	—	1.5	—	ns
35	CLK High to D0–D31 Active (Write Cycle)	2	—	1.5	—	1.5	—	ns
36	CLK High to D0–D31 Three-state (Write Cycle)	—	12	—	10	—	8.5	ns
37	D0–D31 Valid to CLK Low (Setup) (Read Cycle)	0	—	0	—	0	—	ns
38	CLK Low to D0–D31 Invalid (Hold) (Read Cycle)	11	—	9	—	7	—	ns
39	CLK High to $\overline{TT}$, $\overline{BS}$, $\overline{BL}$ Deasserted	2	14	2	12	2	10	ns
40	$\overline{BS}$, $\overline{TT}$ Width Deasserted	25[6]	—	21[7]	—	16.5[7]	—	ns
41	CLK Low to $\overline{TS}$ Asserted	2	11	1.5	9.5	1.5	8	ns
41a	CLK High $\overline{TS}$ tri-state	2	11	1.5	9.5	1.5	8	ns
42	$\overline{TS}$ Hold Time from CLK Low	2	—	1.5	—	1.0	—	ns
42a	$\overline{WR}$ Hold Time from CLK Low	1.5	—	1.5	—	1.0	—	ns
43	CLK Low to $\overline{TS}$ Deasserted	—	16	—	13	—	9	ns
43a	CLK Low to $\overline{WR}$ Deasserted	—	19	—	16	—	13	ns
44	$\overline{TS}$ Deasserted to $\overline{BS}$ Asserted (Two Successive Bus Cycles)	7[8]	—	6.5[9]	—	6.5[9]	—	ns
44a	$\overline{WR}$ Deasserted to $\overline{BS}$ Asserted (Two Successive Bus Cycles)	—	6	—	3.5	—	3.	ns

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Table 2-7 External Bus Synchronous Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
45	$\overline{BS}$ Asserted to $\overline{TA}$ Asserted[5.]	—	15[10]	—	12.5[11]	—	9.5[11]	ns
46	$\overline{TA}$ Valid to CLK High (Setup)[5.]	3	—	3	—	3	—	ns
47	CLK High to $\overline{TA}$ Invalid (Hold)	8	—	7	—	6	—	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3% and no wait states
4. Assuming duty cycle in the range 46%–54% and no wait states
5. Timing 45 or timing 46 should be satisfied.
6. T_c–5
7. T_c–4
8. T_l–7
9. T_l–5
10. T_c–15
11. T_c–12.5

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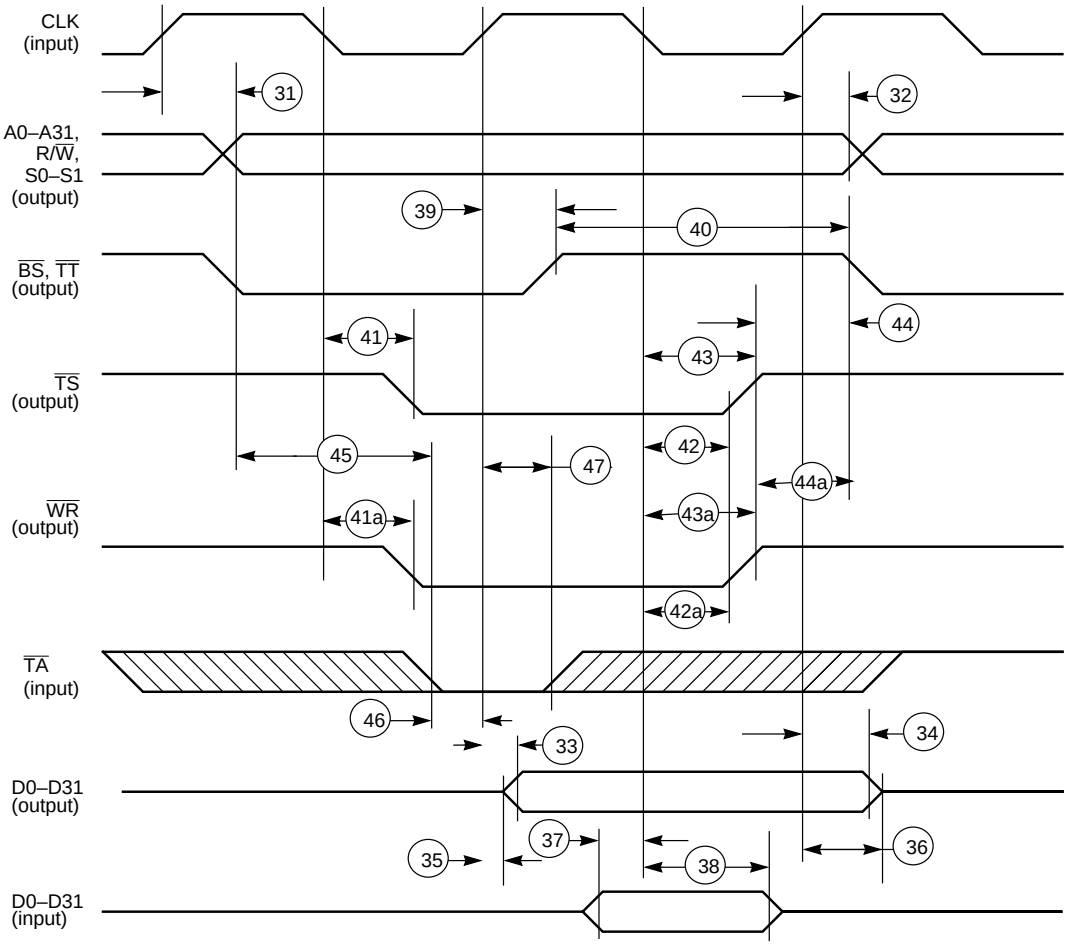

Figure 2-6 External Bus Synchronous Timing—No Wait States

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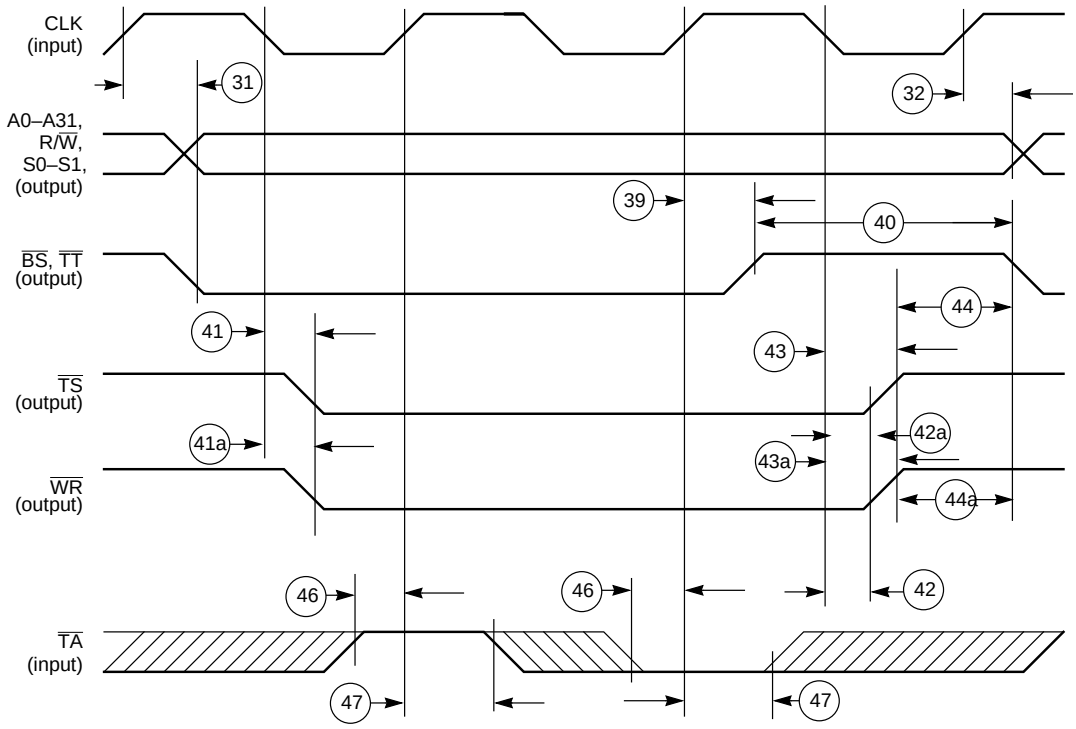

Figure 2-7 External Bus Synchronous Timing—One Wait State

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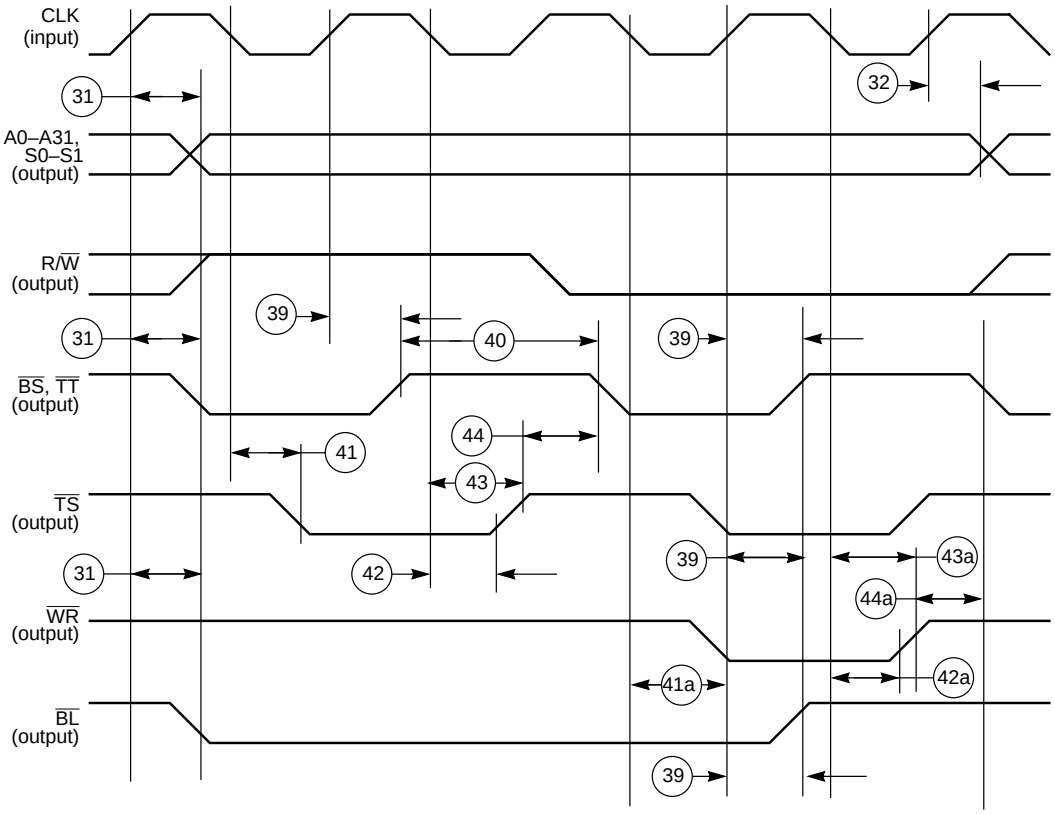

Figure 2-8 Read-Modify-Write Cycle Timing—No Wait States

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Multiplexed Bus Timing

Table 2-8 Multiplexed Bus Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
51	$\overline{AE}$ Asserted to CLK Low[5]	8	14[6]	6.5	11.5[6]	5.5	9[6]	ns
52	$\overline{AE}$ Asserted to A0–A31 Valid	2	14	2	12	2	10	ns
53	$\overline{AE}$ Deasserted to A0–A31 tri-state	2	12	2	10	1.5	8	ns
54	$\overline{AE}$ Deasserted to A0–A31 Invalid	2	—	2	—	1.5	—	ns
55	$\overline{AE}$ Asserted to CLK High[7]	0	12[8]	0	9.5[9]	0	7[9]	ns
56	$\overline{AE}$ Asserted to A0–A31 Active	1	—	1	—	1	—	ns
57	CLK High to A0–A31 Active	2	—	1.5	—	1.5	—	ns
61	$\overline{DE}$ Asserted to CLK Low[5, 10]	8	14[6]	6.5	11.5[6]	5.5	9[6]	ns
62	$\overline{DE}$ Asserted to D0–D31 Valid	14	2	2	12	2	10	ns
63	$\overline{DE}$ Deasserted to D0–D31 Tri-state	2	12	2	10	1.5	8	ns
64	$\overline{DE}$ Deasserted to D0–D31 Invalid	2	—	2	—	1.5	—	ns
65	$\overline{DE}$ Asserted to CLK High[7, 10]	0	12[8]	0	9.5[9]	0	7[9]	ns
66	$\overline{DE}$ Asserted to D0–D31 Active	1	—	1	—	1	—	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3%
4. Assuming duty cycle in the range 46%–54%
5. T_h minimum
6. T_h
7. T_l minimum
8. T_l–4
9. T_l–2
10. For Host Interface data output, only timings 62, 63, 64, and 66 apply.

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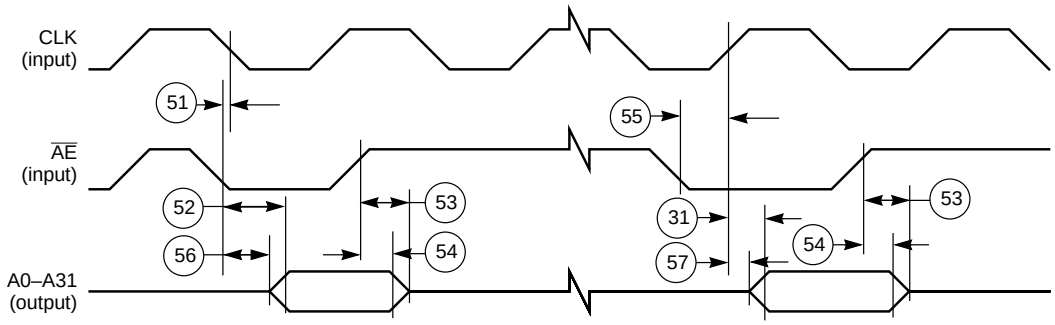

Figure 2-9 Address Bus Enable/Disable Timing

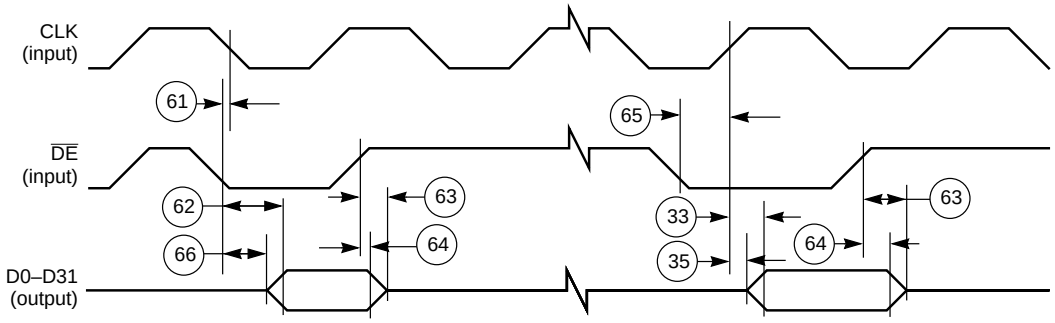

Figure 2-10 Data Bus Enable/Disable Timing

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Host Timing

Table 2-9 Host Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
101	A2–A5, R/$\overline{W}$ Valid to $\overline{TS}$ Asserted (Setup)	10	—	7	—	5	—	ns
102	$\overline{TS}$ Deasserted to A2–A5, R/$\overline{W}$ Invalid (Hold)	0	—	0	—	0	—	ns
103	$\overline{TS}$ Asserted to D0–D31 Out Valid $\overline{TS}$ Asserted to D0–D31 Out Valid[5]	— —	18[6] 100	— —	16 88	— —	13.5 74	ns ns
104	$\overline{TS}$, $\overline{HA}$ Deasserted to D0–D31 Out Invalid (Hold)	2	—	2	—	2	—	ns
105	$\overline{TS}$, $\overline{HA}$ Asserted to D0–D31 Out Active	3	—	3	—	3	—	ns
106	$\overline{TS}$, $\overline{HA}$ Deasserted to D0–D31 Tri-state	—	18	—	16	—	14	ns
107	A2–A5, R/$\overline{W}$ Valid to D0–D31 Valid to D0–D31 Out Valid A2–A5, R/$\overline{W}$ Valid to D0–D31 Valid to D0–D31 Out Valid[5]	— —	30[6] 100	— —	25 88	— —	20 74	ns ns
108	$\overline{HS}$, $\overline{HA}$ Asserted to D0–D31 Out Valid (Access Time) $\overline{HS}$, $\overline{HA}$ Asserted to D0–D31 Out Valid[5]	—	21[6]	—	20	—	17	ns
109	D0–D31 In Valid to $\overline{TS}$, $\overline{HA}$ Deasserted (Setup)	8	—	6	—	5	—	ns
110	$\overline{TS}$, $\overline{HA}$ Deasserted to D0–D31 In Invalid (Hold)	5	—	4	—	3.5	—	ns
111	$\overline{TS}$ Width Asserted[5]	16	—	14	—	12	—	ns
112	$\overline{TS}$ Width Deasserted Between Consecutive TX Writes[8] $\overline{TS}$, $\overline{HA}$ Width Deasserted (Others)[11]	— —	79 12	— —	64.5 10	— —	51.5 9	ns ns
113	$\overline{HS}$ Asserted to $\overline{TS}$ Deasserted	24	—	21	—	17	—	ns
114	$\overline{HS}$ Hold Time After $\overline{TS}$ Deasserted	0	—	0	—	0	—	ns

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Table 2-9 Host Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
115	$\overline{HS}$, $\overline{HA}$ Deasserted to $\overline{TS}$ Asserted (Setup)	1	—	0	—	0	—	ns
118	$\overline{HA}$ Width Asserted (DMA Mode)	24	—	21	—	18	—	ns
120	CLK Low to $\overline{HR}$ Asserted	—	14	—	12	—	10	ns
121	$\overline{TS}$, $\overline{HA}$ Asserted to $\overline{HR}$ Deasserted	—	30	—	25	—	21	ns
122	CLK Low to $\overline{HR}$ Asserted After $\overline{TS}$ Deassertion[12]	60	—	50	—	40	—	ns
123	$\overline{TS}$, $\overline{HA}$ Deasserted to CLK Low (Setup)[14]	13	30	11	25	9.5	20	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3%
4. Assuming duty cycle in the range 46%–54%
5. When reading status (ICS register), the status data is guaranteed to be stable.
6. $2T_c + 40$
7. $2T_c + 38$
8. Assuming both TX and HRX empty
9. $2T_c + T_l + 5$
10. $2T_c + T_l + 3$
11. Both $\overline{TS}$ and $\overline{HA}$ must be deasserted in case of mixed DMA / non-DMA accesses (i.e., after any access this recovery time must be respected before a new access.)
12. When $\overline{TS}$ deassertion was in respect to timing 123
13. $2T_c$
14. When timing 123 is respected, timing 122 is guaranteed to be respected. Timing 123 is not required for correct operation.
15. T_c

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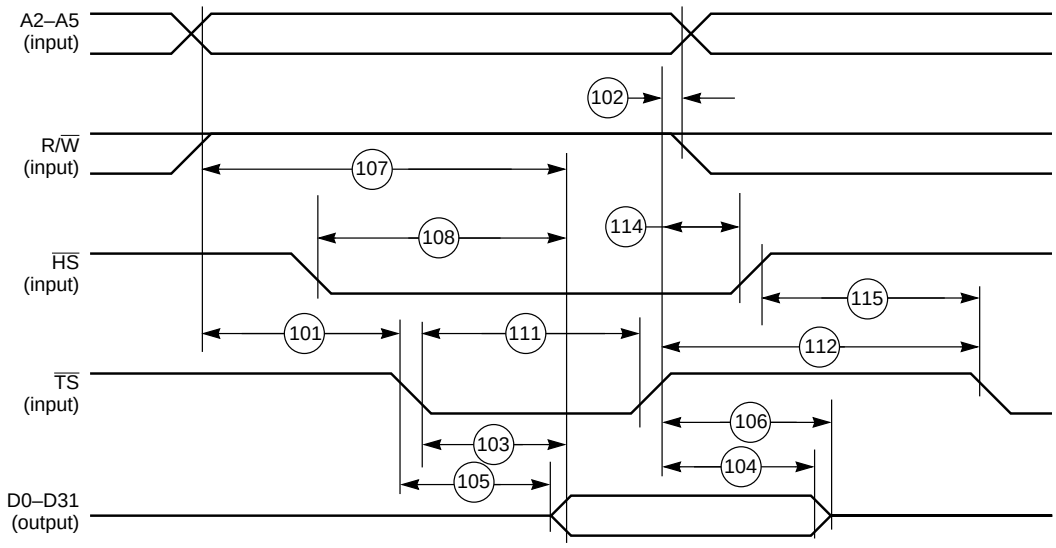

Figure 2-11 Host Read Cycle Timing (Non-DMA Mode)

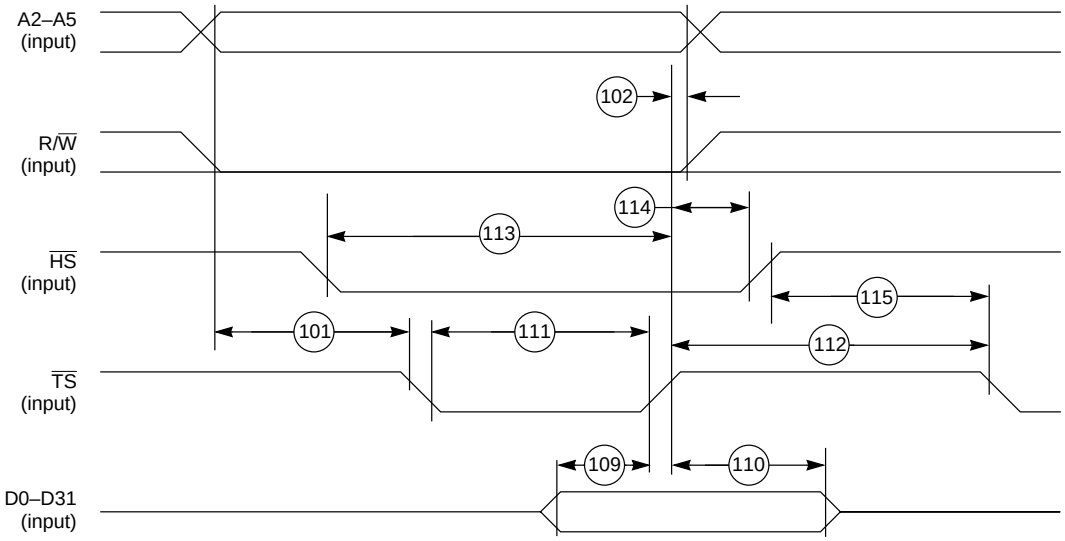

Figure 2-12 Host Write Cycle Timing (Non-DMA Mode)

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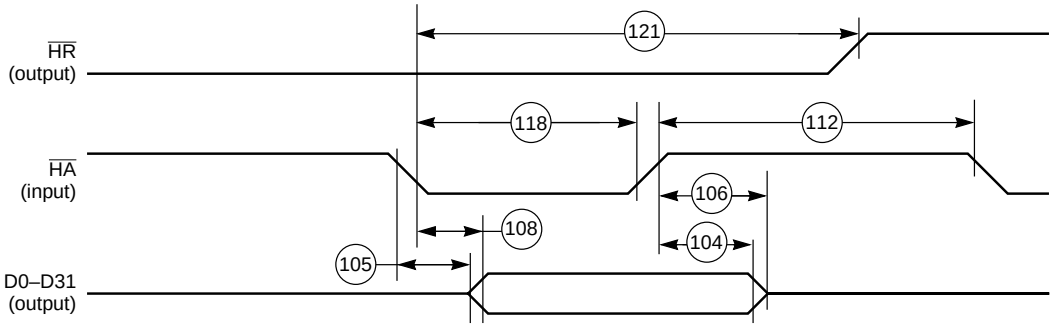

Figure 2-13 Host Read Cycle Timing (DMA Mode)

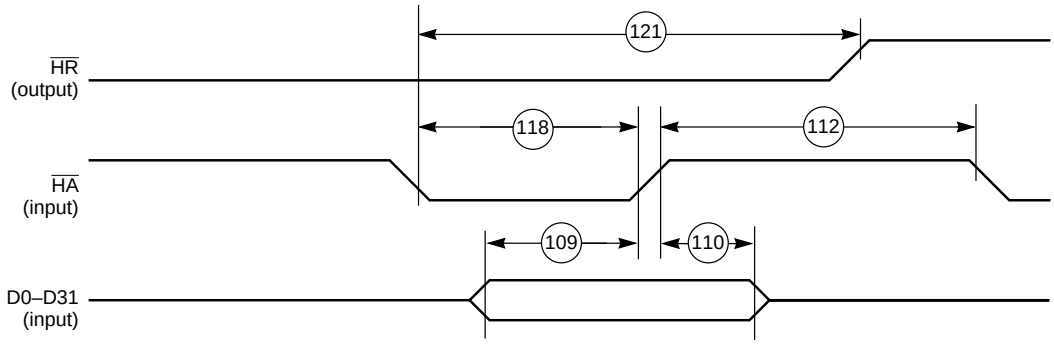

Figure 2-14 Host Write Cycle Timing (DMA Mode)

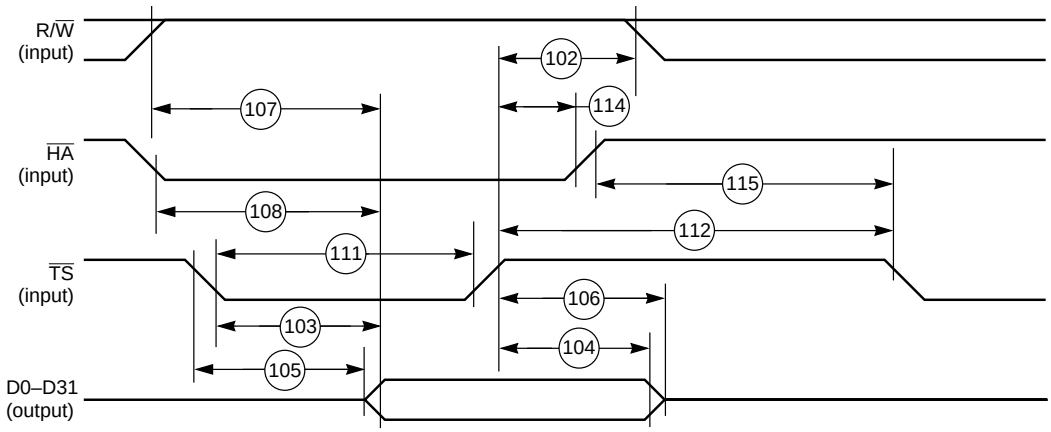

Figure 2-15 Host Interrupt Vector Register (IVR) Read Timing (Non-DMA Mode)

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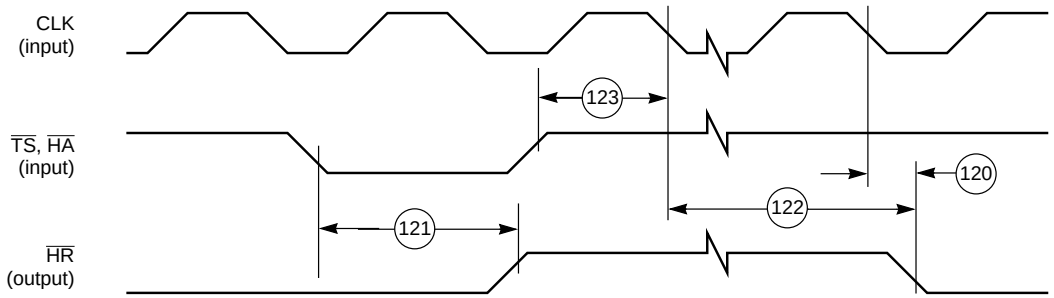

Figure 2-16 Host Request Timing

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OnCE Timing

Table 2-10 OnCE Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
130	DSCK Low	40	—	40	—	40	—	ns
131	DSCK High	40	—	40	—	35	—	ns
132	DSCK Cycle Time	240	—	200	—	160	—	ns
133	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Asserted	152[5]	—	126[6]	—	105[6]	—	ns
134	DSCK High to DSO Valid	51	—	42	—	34	—	ns
135	DSCK High to DSO Invalid	6	—	5	—	4	—	ns
136	DSI Valid to DSCK Low (Setup)	17	—	15	—	13	—	ns
137	DSCK Low to DSI Invalid (Hold)	6	—	5	—	4	—	ns
138	Last DSCK Low to OS0–OS1, $\overline{ACK}$ Active	74[7]	—	61.5[7]	—	50[7]	—	ns
139	DSO ($\overline{ACK}$) Asserted to First DSCK High[8]	81[9]	—	67.5[10]	—	54[10]	—	ns
140	DSO ($\overline{ACK}$) Width Asserted	40[11]	68[12]	33.5[13]	57[14]	27	46	ns
141	DSO ($\overline{ACK}$) Asserted to OS0–OS1 Tri-state	—	0	—	0	—	0	ns
142	OS0–OS1 Valid to CLK High	10[15]	—	8[16]	—	7	—	ns
143	CLK High to OS0–OS1 Invalid	4	—	3	—	2	—	ns
144	Last DSCK Low of Read Register to First DSCK High of Next Command[19]	222[17]	—	185.5[18]	—	148[18]	—	ns
145	Last DSCK Low to DSO Invalid (Hold)	6	—	5	—	4	—	ns
146	DSCK Rise and Fall Times		60		60		50	ns

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Table 2-10 OnCE Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3%
4. Assuming duty cycle in the range 46%–54%

5. $5T_c + 2$
6. $5T_c + 1$
7. $2T_c + T_l$
8. T_l maximum.
9. $2T_c + T_l + 5$
10. $2T_c + T_l + 4$
11. $T_c + T_l – 4$
12. $2T_c + 8$
13. $T_c + T_l – 3$
14. $2T_c + 7$
15. $T_c – 20$
16. $T_c – 17$
17. $6T_c + T_h + 26$
18. $6T_c + T_h + 22$
19. T_h maximum

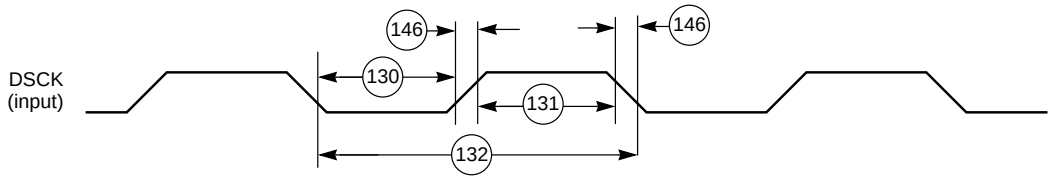

Figure 2-17 OnCE Serial Clock Timing

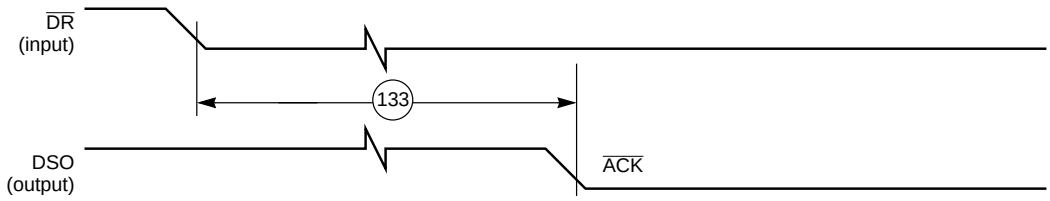

Figure 2-18 OnCE Acknowledge Timing

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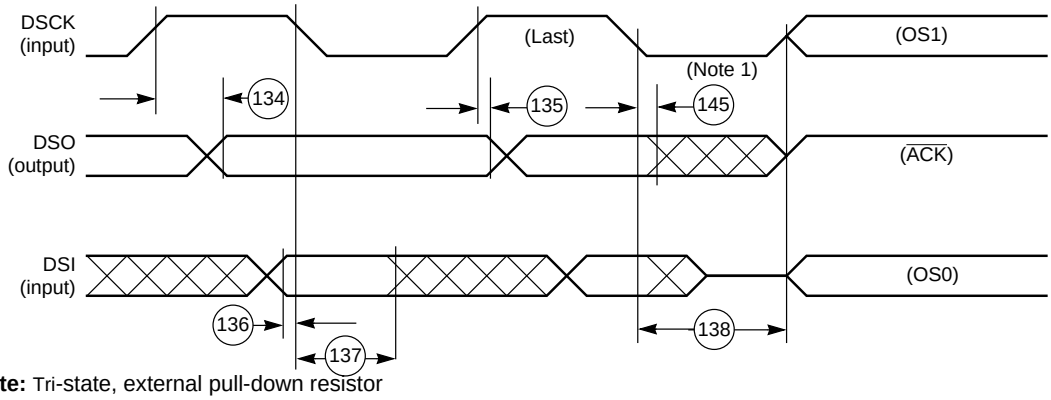
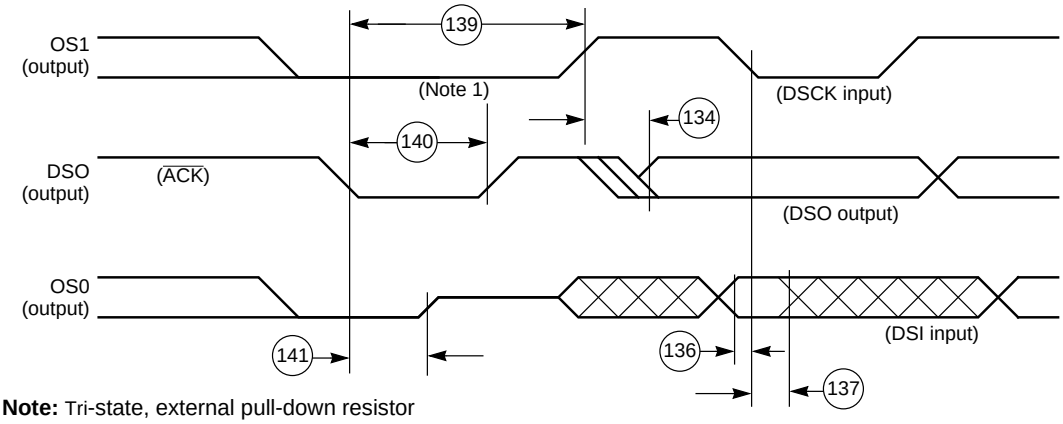


Note: Tri-state, external pull-down resistor

Figure 2-19 OnCE Data I/O to Status Timing



Note: Tri-state, external pull-down resistor

Figure 2-20 OnCE Status to Data I/O Timing

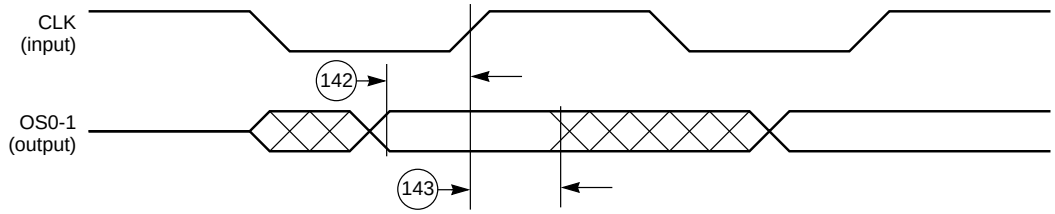


Figure 2-21 OnCE CLK to Status Timing

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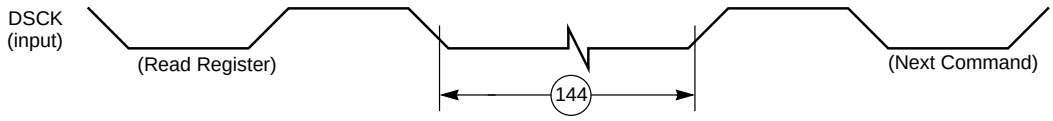

Figure 2-22 OnCE DSCK Next Command After Read Register Timing

Reset, Mode Select, Interrupt Timing

Table 2-11 Reset, Mode Select, Interrupt Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
160	$\overline{\text{RESET}}$ Asserted to D0–D31, A0–A31, S0–S1, R/$\overline{\text{W}}$, $\overline{\text{BS}}$, $\overline{\text{TT}}$, $\overline{\text{TS}}$, $\overline{\text{BA}}$ Three-state	—	70[9]	—	60[10]	—	50	ns
161	$\overline{\text{RESET}}$ Asserted to $\overline{\text{BL}}$, $\overline{\text{BR}}$, $\overline{\text{HR}}$ Deasserted	—	100[11]	—	85[12]	—	60	ns
162	$\overline{\text{RESET}}$ Width Asserted[5]	600[13]	—	500[13]	—	400[13]	—	ns
163	Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Access	300[14]	365[15]	250[14]	305[16]	200[14]	245[16]	ns
164	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to CLK High	6	25[17]	5	20[17]	4	16[17]	ns
165	Synchronous Reset Delay from CLK High to First External Access[7]	242[18]	254[19]	202[18]	212[20]	162[18]	170	ns
166	Mode Select Setup Time	50	—	50	—	40	—	ns
167	Mode Select Hold Time	0	—	0	—	0	—	ns
168	Edge-Triggered Interrupt Request Width	10	—	10	—	10	—	ns
169	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, or $\overline{\text{IRQC}}$ assertion to External Memory Access Out Valid Caused by First Interrupt Instruction Execution[6]	284[21]	—	236.5[21]	—	189[21]	—	ns

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Table 2-11 Reset, Mode Select, Interrupt Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
170	Delay from A0–A31, S0–S1, R/$\overline{W}$, $\overline{BS}$, and $\overline{TT}$ Valid Caused by First Interrupt Instruction Execution to $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$ Deassertion[8]	—	30[22]	—	25[23]	—	20[23]	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3% and no wait states
4. Assuming duty cycle in the range 46%–54%% and no wait states
5. Assuming stable CLK and V_{CC}
6. Assuming a single-cycle MOVE instruction in the first vector location, interrupting a stream of one-word, single-cycle instructions
7. Assuming $\overline{BG}$ asserted and $\overline{BB}$ deasserted
8. This timing is necessary to prevent multiple interrupt service when the interrupt request is a level-sensitive fast interrupt. To avoid this restriction, Edge-triggered mode is recommended when using fast interrupts and long interrupts are recommended when using Level-sensitive mode

9. $T_c + 40$
10. $T_c + 35$
11. $2T_c + 40$
12. $2T_c + 35$
13. $20T_c$
14. $10T_c$
15. $11T_c + 35$
16. $11T_c + 30$
17. $T_c – 5$
18. $8T_c + 2$
19. $8T_c + 14$
20. $8T_c + 12$
21. $9T_c$ + Tl
22. $(WS + 2)T_c – 30$
23. $(WS + 2)T_c – 25$

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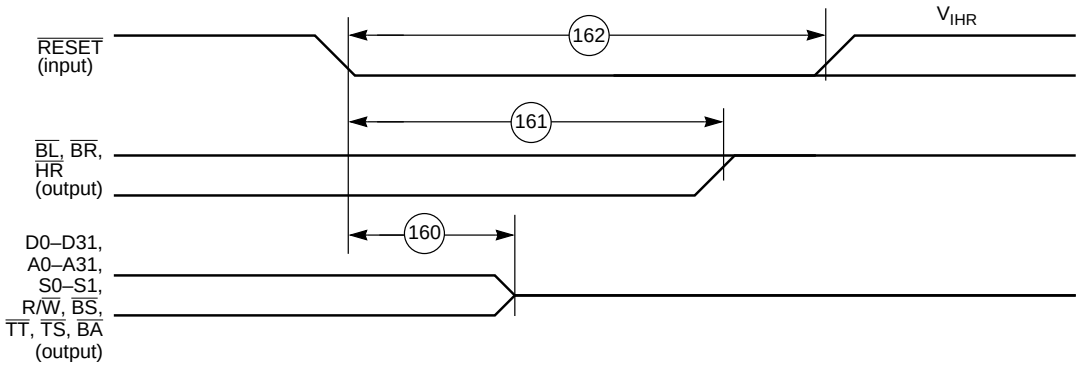

Figure 2-23 Reset Entry Timing

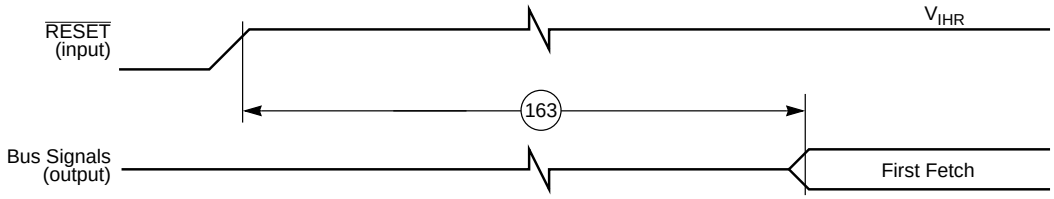

Figure 2-24 Asynchronous Reset Exit Timing

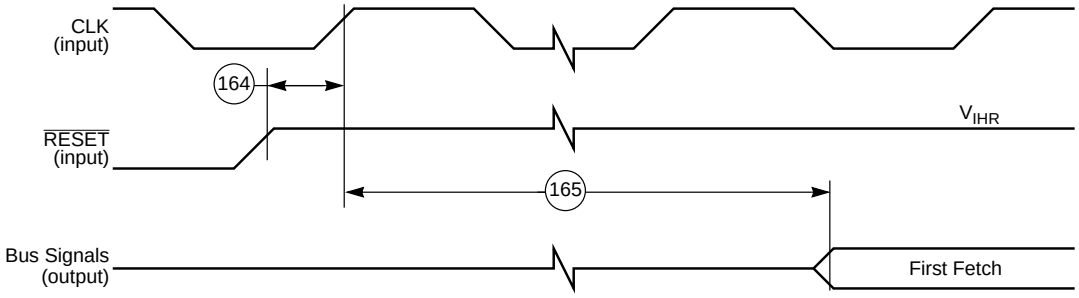

Figure 2-25 Synchronous Reset Exit Timing

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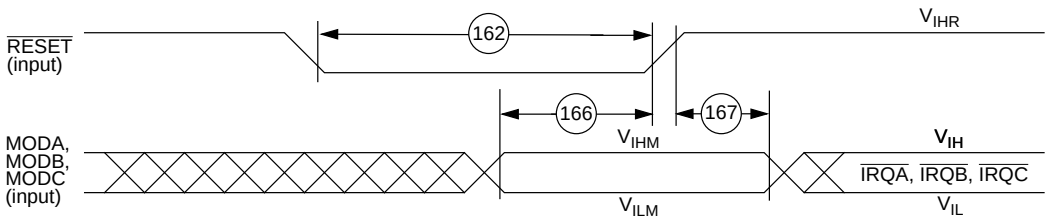
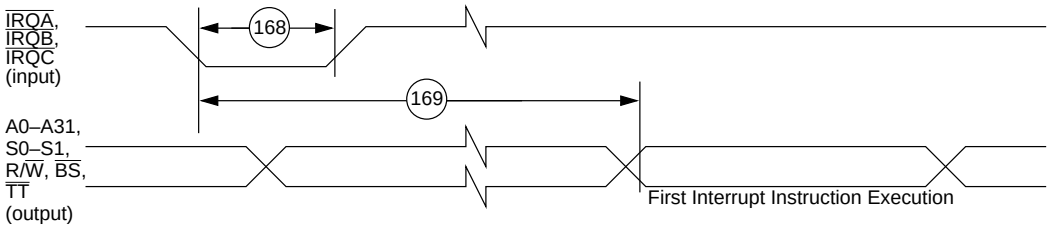


Figure 2-26 Operating Mode Select Timing



Note: Reset, Mode Select, Interrupt Figure 5

Figure 2-27 External Edge-Triggered Interrupt Timing

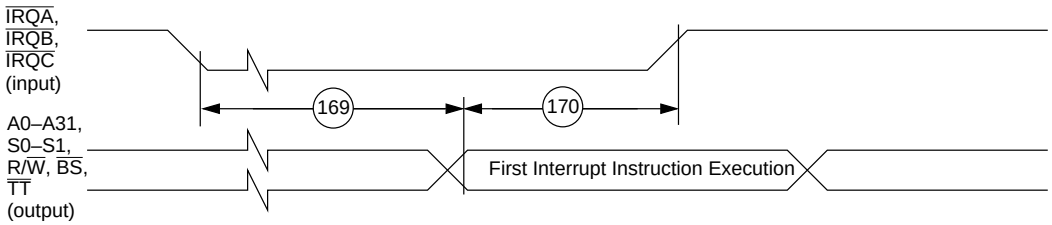


Figure 2-28 External Level-Sensitive Interrupt Timing

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WAIT, STOP, DMA Request Timing

Table 2-12 WAIT, STOP, DMA Request Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
180	$\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$ Asserted to CLK Low (Setup Time for Synchronous Recovery from WAIT State)	12	30	10	25	8	17	ns
181	CLK Low to External Memory Access Valid (First Interrupt Instruction Fetch After Synchronous Recovery from WAIT State)[5]	406[7]	420[8]	338.5[7]	350.5[9]	271[7]	281[9]	ns
182	$\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$ Width Asserted (Recovery from WAIT State)	35[10]	—	30[10]	—	20[10]	—	ns
183	$\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$ Asserted to External Memory Access Valid (First Interrupt Instruction Fetch After Asynchronous Recovery from WAIT State)[5]	406[7]	466[11]	338.5[7]	388.5[12]	271[7]	311	ns
184	$\overline{IRQA}$ Asserted to CLK Low (Setup Time for Synchronous Recovery from STOP State)	8	30[13]	7	25[13]	5.5	20[13]	ns
185	CLK Low to External Memory Access Valid (First Instruction Fetch After Synchronous Recovery from STOP State)[5]	376[14]	390[15]	313.5[14]	325.5[16]	251[14]	261	ns
186	$\overline{IRQA}$ Width Asserted (Recovery from Stop State)	35[22]	—	30[22]	—	25[22]	—	ns
187	$\overline{IRQA}$ Asserted to External Memory Access Valid (First Instruction Fetch After Asynchronous Recovery from STOP State)[5])	376[14]	436[17]	313.5[14]	363.5[18]	251[14]	291	ns
188	$\overline{DR}$ Asserted to CLK Low (Setup Time for Synchronous Recovery from WAIT or STOP State)	8	30[13]	7	25[13]	5.5	20[13]	ns

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Table 2-12 WAIT, STOP, DMA Request Timing (Continued)

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
189	CLK Low to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) • After Synchronous Recovery from STOP State • After Synchronous Recovery from WAIT State	 540[19] 510[20]	 — —	 450[19] 425[20]	 — —	 305[19] 290[20]	 — —	 ns ns
190	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) • After Asynchronous Recovery from STOP State • After Asynchronous Recovery from WAIT State	 540[19] 510[20]	 — —	 450[19] 425[20]	 — —	 305[19] 290[20]	 — —	 ns ns
191	DMA Request Asserted to CLK Low (Setup)[6]	6	—	5	—	5	—	ns
192	CLK Low to DMA Request Invalid (Hold)[6]	2	—	2	—	1.5	—	ns
193	CLK Low to External DMA Access Valid	76[21]	—	63.5[21]	—	50[21]	—	ns
194	$\overline{DR}$ Assertion Width • To recover from WAIT / STOP • To recover from WAIT / STOP and enter Debug Mode	 35[22] 420[25]	 300[23] —	 29[24] 350[25]	 250[23] —	 23[24] 235[25]	 200[23] —	 ns ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, GND = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, GND = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3% and no wait states.
4. Assuming duty cycle in the range 46%–54%% and no wait states.
5. Assuming bus ownership.
6. $\overline{IRQ}$ pin internally defined as DMA request.

7. 13Tc + Tl + 2
8. 13Tc + Tl + 14
9. 13Tc + Tl + 12
10. Tc + 5
11. 14Tc + Tl + 30
12. 14Tc + Tl + 25
13. Tc
14. 12Tc + Tl + 2
15. 12Tc + Tl + 14
16. 12Tc + Tl + 12
17. 13Tc + Tl + 30
18. 13Tc + Tl + 25
19. 18Tc
20. 17Tc
21. 2Tc + Tl + 2
22. Tc + 5
23. 10Tc
24. Tc + 4
25. 14Tc

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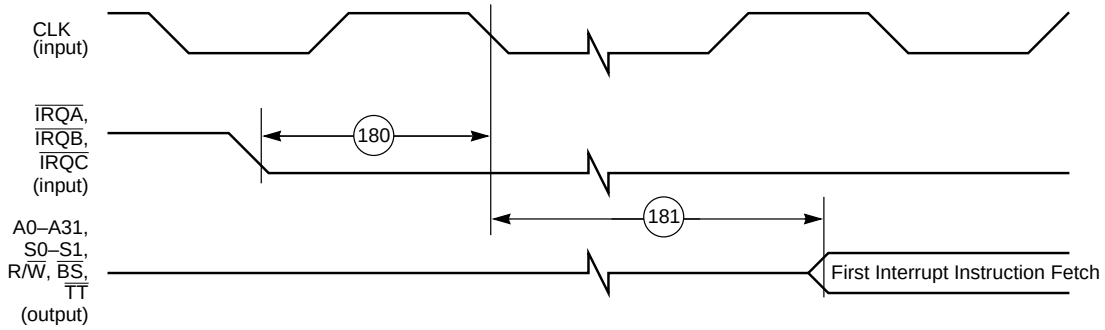

Figure 2-29 Recovery from WAIT State Using Synchronous Interrupt Timing

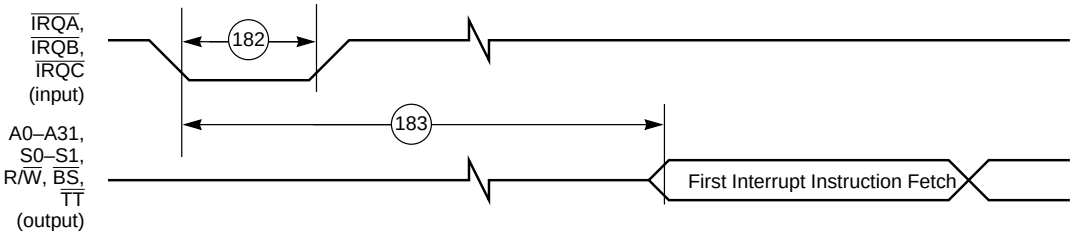

Figure 2-30 Recovery from WAIT State Using Asynchronous Interrupt Timing

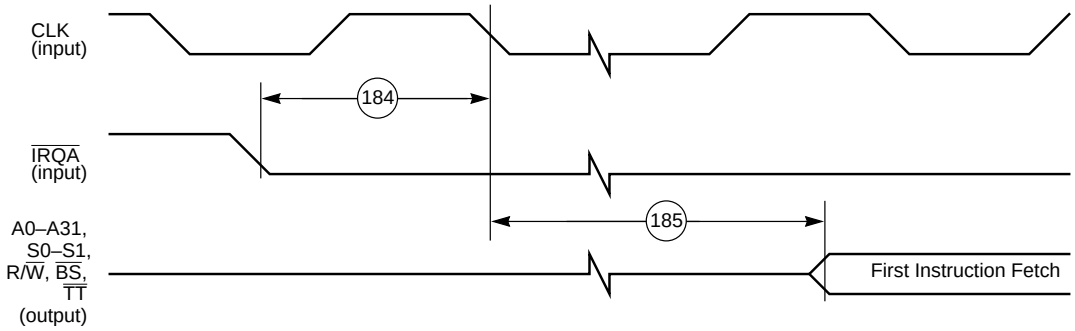

Figure 2-31 Recovery from STOP State Using Synchronous Interrupt Timing

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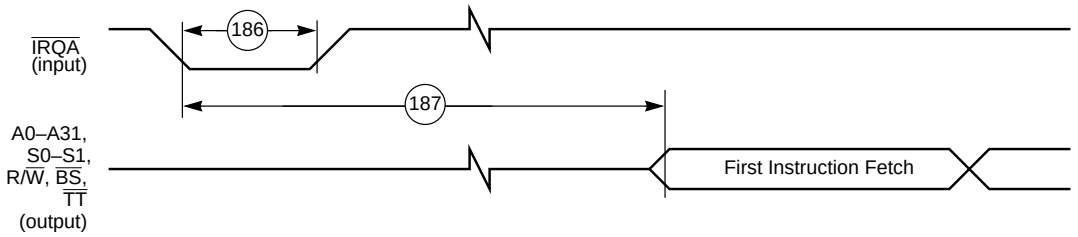

Figure 2-32 Recovery from STOP State Using Asynchronous Interrupt Timing

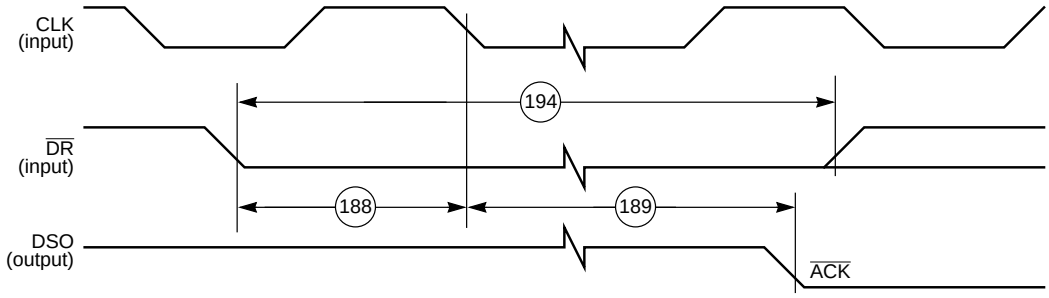

Figure 2-33 Recovery from WAIT/STOP State Using Synchronous DR Timing

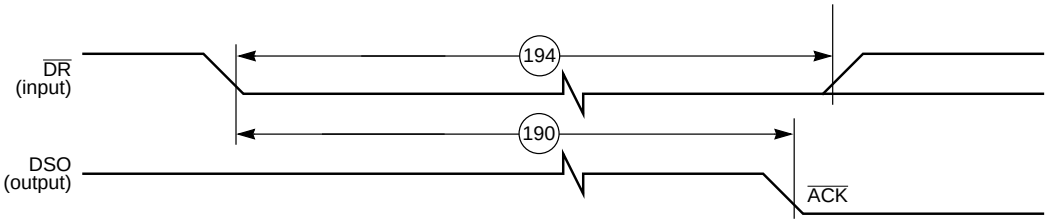

Figure 2-34 Recovery from WAIT/STOP State Using Asynchronous DR Timing

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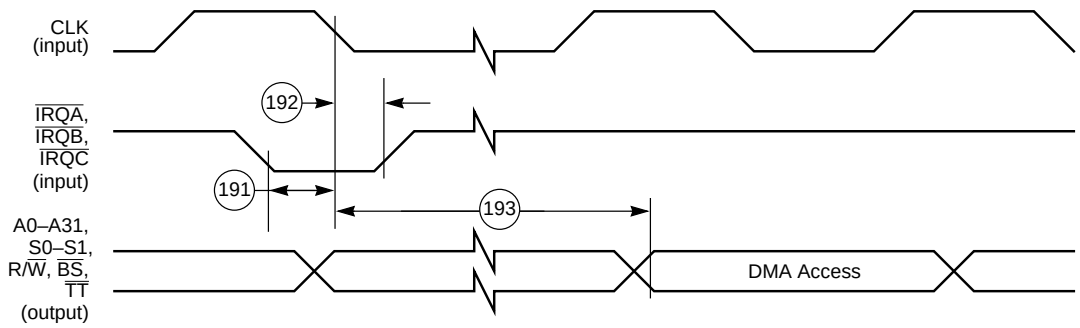

Figure 2-35 External DMA Request Timing

Timer/Event Counter

Table 2-13 Timer Timing

No.[1]	Characteristic[2]	33.3 MHz[3]		40 MHz[4]		60 MHz[4]		Unit
		Min	Max	Min	Max	Min	Max	
260	TIO Low	$2T_c$	—	$2T_c$	—	$2T_c$	—	ns
261	TIO High	$2T_c$	—	$2T_c$	—	$2T_c$	—	ns
262	CKOUT to TIO (output) assertion	2	18	2	15	2	12	ns
263	CKOUT to TIO (output) deassertion	2	18	2	15	2	12	ns

Note:
1. The numbers in this column are shown as circled numbers in the following figures.
2. DC Electrical Characteristics:
   at 33.3 MHz: V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V DC, T_J = –40°C to 100°C
   at 40 or 60 MHz: V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V DC, T_J = –40°C to 100°C
3. Assuming duty cycle in the range 46.7%–53.3% and no wait states.
4. Assuming duty cycle in the range 46%–54%% and no wait states.

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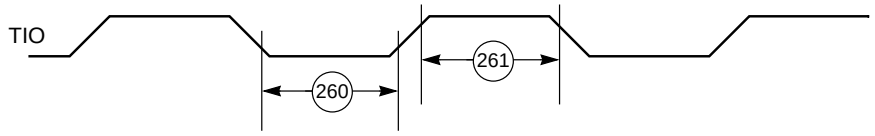

Figure 2-36 TIO Timer Event Input Restrictions

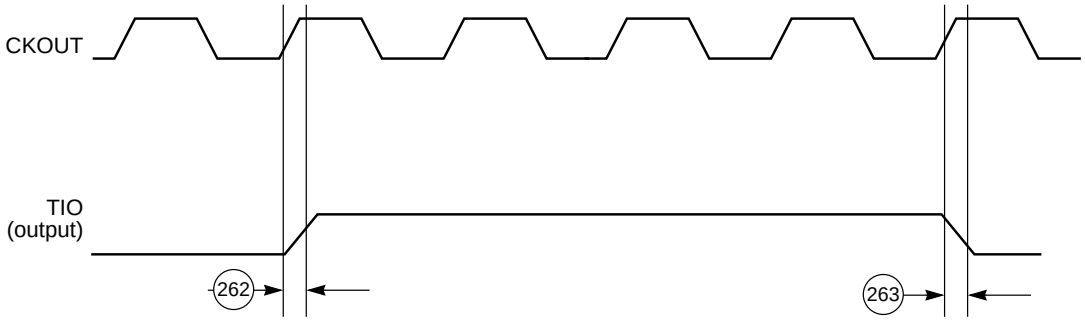

Figure 2-37 External Pulse Generation

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SECTION 3

PACKAGING

This section contains package and pin-out information for the DSP96002. There are two package options: 223-pin Pin Grid Array (PGA) or 240-pin Ceramic Quad Flat Pack (CQFP).

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PGA PACKAGE

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	BA23	BA27	BA29	BA31	$\overline{IRQA}$	$A\overline{BB}$	$A\overline{BR}$	TIO0	AR/$\overline{W}$	AS0	$A\overline{TS}$	$A\overline{AE}$	AA02	AA04	AA07	AA10	AA13	AA16	A
B	BA20	BA25	BA28	BA30	$\overline{IRQB}$	$A\overline{BG}$	$A\overline{BA}$	$B\overline{TT}$	AS1	$A\overline{BS}$	AA00	AA03	AA06	AA09	AA11	AA14	AA18	AA20	B
C	BA17	BA21	BA26	GND_N	$\overline{IRQC}$	$\overline{RES}$	$A\overline{BL}$	$A\overline{TT}$	$A\overline{WR}$	AA01	AA05	AA08	AA12	AA15	AA17	AA19	AA21	AA23	C
D	BA15	BA18	BA24		GND_N	GND_N	GND_N	V_{CCN}	V_{CCN}	V_{CCQ}	GND_Q	V_{CCN}	GND_N	GND_N	GND_N	AA22	AA25	AA26	D
E	BA13	BA16	BA22	GND_N											GND_N	AA24	AA28	AA29	E
F	BA12	BA14	BA19	GND_N											GND_N	AA27	AA30	AD31	F
G	BA09	BA10	V_{CCN}	V_{CCN}											GND_N	AA31	AD30	AD29	G
H	BA08	CLK	BA11	V_{CCQ}											V_{CCN}	AD28	AD27	AD26	H
J	$A\overline{TA}$	$B\overline{TA}$	BA07	GND_Q											GND_Q	AD24	AD25	AD23	J
K	BA04	BA05	BA06	V_{CCN}											GND_Q	AD20	AD21	AD22	K
L	BA03	BA01	BA02	V_{CCN}											V_{CCQ}	AD16	AD18	AD19	L
M	BA00	BS1	BS0	GND_N											V_{CCN}	V_{CCN}	$A\overline{DE}$	AD17	M
N	$B\overline{AE}$	TIO1	$B\overline{WR}$	GND_N											GND_N	AD11	AD14	AD15	N
P	BR/$\overline{W}$	$B\overline{TS}$	$B\overline{BL}$	GND_N											GND_N	AD07	AD12	AD13	P
R	$B\overline{BS}$	$B\overline{BR}$	$B\overline{BB}$	GND_N	GND_N	GND_N	V_{CCN}	GND_Q	V_{CCQ}	V_{CCQ}	V_{CCN}	GND_N	GND_N	GND_N	GND_N	AD05	AD09	AD10	R
T	$B\overline{BG}$	$B\overline{BA}$	$A\overline{HR}$	$\overline{DR}$	$A\overline{HS}$	BD31	GND_N	BD26	BD22	BD17	BD14	BD11	BD07	BD04	BD01	AD02	AD06	AD08	T
U	$B\overline{HR}$	DSCK	NC(1)	$A\overline{HA}$	$B\overline{DE}$	BD29	BD27	BD24	BD21	BD18	BD15	BD12	BD09	BD06	BD03	BD00	AD03	AD04	U
V	DSO	DSI	$B\overline{HA}$	$B\overline{HS}$	BD30	BD28	BD25	BD23	BD20	BD19	BD16	BD13	BD10	BD08	BD05	BD02	AD00	AD01	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

DSP96002

Top View

Figure 3-1 Top View of the DSP96002 223-pin PGA Package

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
V	DSO	DSI	$\overline{BHA}$	$\overline{BHS}$	BD30	BD28	BD25	BD23	BD20	BD19	BD16	BD13	BD10	BD08	BD05	BD02	AD00	AD01	V
U	$\overline{BHR}$	DSCK	NC(1)	$\overline{AHA}$	$\overline{BDE}$	BD29	BD27	BD24	BD21	BD18	BD15	BD12	BD09	BD06	BD03	BD00	AD03	AD04	U
T	$\overline{BBG}$	$\overline{BBA}$	$\overline{AHR}$	$\overline{DR}$	$\overline{AHS}$	BD31	GND_N	BD26	BD22	BD17	BD14	BD11	BD07	BD04	BD01	AD02	AD06	AD08	T
R	$\overline{BBS}$	$\overline{BBR}$	$\overline{BBB}$	GND_N	GND_N	GND_N	V_{CCN}	GND_Q	V_{CCQ}	V_{CCQ}	V_{CCN}	GND_N	GND_N	GND_N	GND_N	AD05	AD09	AD10	R
P	BR/$\overline{W}$	$\overline{BTS}$	$\overline{BBL}$	GND_N											GND_N	AD07	AD12	AD13	P
N	$\overline{BAE}$	TIO1	$\overline{BWR}$	GND_N											GND_N	AD11	AD14	AD15	N
M	BA00	BS1	BS0	GND_N											V_{CCN}	V_{CCN}	$\overline{ADE}$	AD17	M
L	BA03	BA01	BA02	V_{CCN}											V_{CCQ}	AD16	AD18	AD19	L
K	BA04	BA05	BA06	V_{CCN}											GND_Q	AD20	AD21	AD22	K
J	$\overline{ATA}$	$\overline{BTA}$	BA07	GND_Q											GND_Q	AD24	AD25	AD23	J
H	BA08	CLK	BA11	V_{CCQ}											V_{CCN}	AD28	AD27	AD26	H
G	BA09	BA10	V_{CCN}	V_{CCN}											GND_N	AA31	AD30	AD29	G
F	BA12	BA14	BA19	GND_N											GND_N	AA27	AA30	AD31	F
E	BA13	BA16	BA22	GND_N											GND_N	AA24	AA28	AA29	E
D	BA15	BA18	BA24		GND_N	GND_N	GND_N	V_{CCN}	V_{CCN}	V_{CCQ}	GND_Q	V_{CCN}	GND_N	GND_N	GND_N	AA22	AA25	AA26	D
C	BA17	BA21	BA26	GNDN	$\overline{IRQC}$	$\overline{RES}$	$\overline{ABL}$	$\overline{ATT}$	$\overline{AWR}$	AA01	AA05	AA08	AA12	AA15	AA17	AA19	AA21	AA23	C
B	BA20	BA25	BA28	BA30	$\overline{IRQB}$	$\overline{ABG}$	$\overline{ABA}$	$\overline{BTT}$	AS1	$\overline{ABS}$	AA00	AA03	AA06	AA09	AA11	AA14	AA18	AA20	B
A	BA23	BA27	BA29	BA31	$\overline{IRQA}$	$\overline{ABB}$	$\overline{ABR}$	TIO0	AR/$\overline{W}$	AS0	$\overline{ATS}$	$\overline{AAE}$	AA02	AA04	AA07	AA10	AA13	AA16	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

DSP96002

Bottom View

Figure 3-2 Bottom View of the DSP96002 223-pin PGA Package

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package

Pin Number	Signal Type	Signal Name
A1	Input/Output	BA23
A2	Input/Output	BA27
A3	Input/Output	BA29
A4	Input/Output	BA31
A5	Input	MODA/$\overline{\text{IRQA}}$
A6	Input	A$\overline{\text{BB}}$
A7	Output	A$\overline{\text{BR}}$
A8	Input/Output	TIO0
A9	Input/Output	AR/$\overline{\text{W}}$
A10	Output	AS0
A11	Input/Output	A$\overline{\text{TS}}$
A12	Input	A$\overline{\text{AE}}$
A13	Input/Output	AA02
A14	Input/Output	AA04
A15	Input/Output	AA07
A16	Input/Output	AA10
A17	Input/Output	AA13
A18	Input/Output	AA16
B1	Input/Output	BA20
B2	Input/Output	BA25
B3	Input/Output	BA28
B4	Input/Output	BA30
B5	Input	MODB/$\overline{\text{IRQB}}$
B6	Input	A$\overline{\text{BG}}$
B7	Output	A$\overline{\text{BA}}$
B8	Output	B$\overline{\text{TT}}$
B9	Output	AS1
B10	Output	A$\overline{\text{BS}}$
B11	Input/Output	AA00
B12	Input/Output	AA03
B13	Input/Output	AA06
B14	Input/Output	AA09
B15	Input/Output	AA11
B16	Input/Output	AA14
B17	Input/Output	AA18

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
B18	Input/Output	AA20
C1	Input/Output	BA17
C2	Input/Output	BA21
C3	Input/Output	BA26
C4	Input	GND_N
C5	Input	MODC/$\overline{IRQC}$
C6	Input	$\overline{RESET}$
C7	Output	A$\overline{BL}$
C8	Output	A$\overline{TT}$
C9	Output	A$\overline{WR}$
C10	Input/Output	AA01
C11	Input/Output	AA05
C12	Input/Output	AA08
C13	Input/Output	AA12
C14	Input/Output	AA15
C15	Input/Output	AA17
C16	Input/Output	AA19
C17	Input/Output	AA21
C18	Input/Output	AA23
D1	Input/Output	BA15
D2	Input/Output	BA18
D3	Input/Output	BA24
D5	Input	GND_N
D6	Input	GND_N
D7	Input	GND_N
D8	Input	V_{CCN}
D9	Input	V_{CCN}
D10	Input	V_{CCQ}
D11	Input	GND_N
D12	Input	V_{CCN}
D13	Input	GND_N
D14	Input	GND_N
D15	Input	GND_N
D16	Input/Output	AA22
D17	Input/Output	AA25
D18	Input/Output	AA26

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
E1	Input/Output	BA13
E2	Input/Output	BA16
E3	Input/Output	BA22
E4	Input	GND_N
E15	Input	GND_N
E16	Input/Output	AA24
E17	Input/Output	AA28
E18	Input/Output	AA29
F1	Input/Output	BA12
F2	Input/Output	BA14
F3	Input/Output	BA19
F4	Input	GND_N
F15	Input	GND_N
F16	Input/Output	AA27
F17	Input/Output	AA30
F18	Input/Output	AD31
G1	Input/Output	BA09
G2	Input/Output	BA10
G3	Input	V_{CCN}
G4	Input	V_{CCN}
G15	Input	GND_N
G16	Input/Output	AA31
G17	Input/Output	AD30
G18	Input/Output	AD29
H1	Input/Output	BA08
H2	Input	CLK
H3	Input/Output	BA11
H4	Input	V_{CCQ}
H15	Input	V_{CCN}
H16	Input/Output	AD28
H17	Input/Output	AD27
H18	Input/Output	AD26
J1	Input	$A\overline{TA}$
J2	Input	$B\overline{TA}$
J3	Input/Output	BA07
J4	Input	GND_Q

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
J15	Input	GND_Q
J16	Input/Output	AD24
J17	Input/Output	AD25
J18	Input/Output	AD23
K1	Input/Output	BA04
K2	Input/Output	BA05
K3	Input/Output	BA06
K4	Input	V_{CCN}
K15	Input	GND_Q
K16	Input/Output	AD20
K17	Input/Output	AD21
K18	Input/Output	AD22
L1	Input/Output	BA03
L2	Input/Output	BA01
L3	Input/Output	BA02
L4	Input	V_{CCN}
L15	Input	V_{CCQ}
L16	Input/Output	AD16
L17	Input/Output	AD18
L18	Input/Output	AD19
M1	Input/Output	BA00
M2	Output	BS1
M3	Output	BS0
M4	Input	GND_N
M15	Input	V_{CCN}
M16	Input	V_{CCN}
M17	Input	$A\overline{DE}$
M18	Input/Output	AD17
N1	Input	$B\overline{AE}$
N2	Output	TIO1
N3	Input/Output	$B\overline{WR}$
N4	Input	GND_N
N15	Input	GND_N
N16	Input/Output	AD11
N17	Input/Output	AD14
N18	Input/Output	AD15

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
P1	Input/Output	BR/$\overline{W}$
P2	Input/Output	B$\overline{TS}$
P3	Output	B$\overline{BL}$
P4	Input	GND_N
P15	Input	GND_N
P16	Input/Output	AD07
P17	Input/Output	AD12
P18	Input/Output	AD13
R1	Output	B$\overline{BS}$
R2	Output	B$\overline{BR}$
R3	Input	B$\overline{BB}$
R4	Input	GND_N
R5	Input	GND_N
R6	Input	GND_N
R7	Input	V_{CCN}
R8	Input	GND_Q
R9	Input	V_{CCQ}
R10	Input	V_{CCQ}
R11	Input	V_{CCN}
R12	Input	GND_N
R13	Input	GND_N
R14	Input	GND_N
R15	Input	GND_N
R16	Input/Output	AD05
R17	Input/Output	AD09
R18	Input/Output	AD10
T1	Input	B$\overline{BG}$
T2	Output	B$\overline{BA}$
T3	Output	A$\overline{HR}$
T4	Input	$\overline{DR}$
T5	Input	A$\overline{HS}$
T6	Input/Output	BD31
T7	Input	GND_N
T8	Input/Output	BD26
T9	Input/Output	BD22
T10	Input/Output	BD17

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Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
T11	Input/Output	BD14
T12	Input/Output	BD11
T13	Input/Output	BD07
T14	Input/Output	BD04
T15	Input/Output	BD01
T16	Input/Output	AD02
T17	Input/Output	AD06
T18	Input/Output	AD08
U1	Output	$B\overline{HR}$
U2	Input/Output	DSCK/OS1
U3	N/A	NC[1]
U4	Input	$A\overline{HA}$
U5	Input	$B\overline{DE}$
U6	Input/Output	BD29
U7	Input/Output	BD27
U8	Input/Output	BD24
U9	Input/Output	BD21
U10	Input/Output	BD18
U11	Input/Output	BD15
U12	Input/Output	BD12
U13	Input/Output	BD09
U14	Input/Output	BD06
U15	Input/Output	BD03
U16	Input/Output	BD00
U17	Input/Output	AD03
U18	Input/Output	AD04
V1	Output	DSO
V2	Input/Output	DSI/OS0
V3	Input	$B\overline{HA}$
V4	Input	$B\overline{HS}$
V5	Input/Output	BD30
V6	Input/Output	BD28
V7	Input/Output	BD25
V8	Input/Output	BD23

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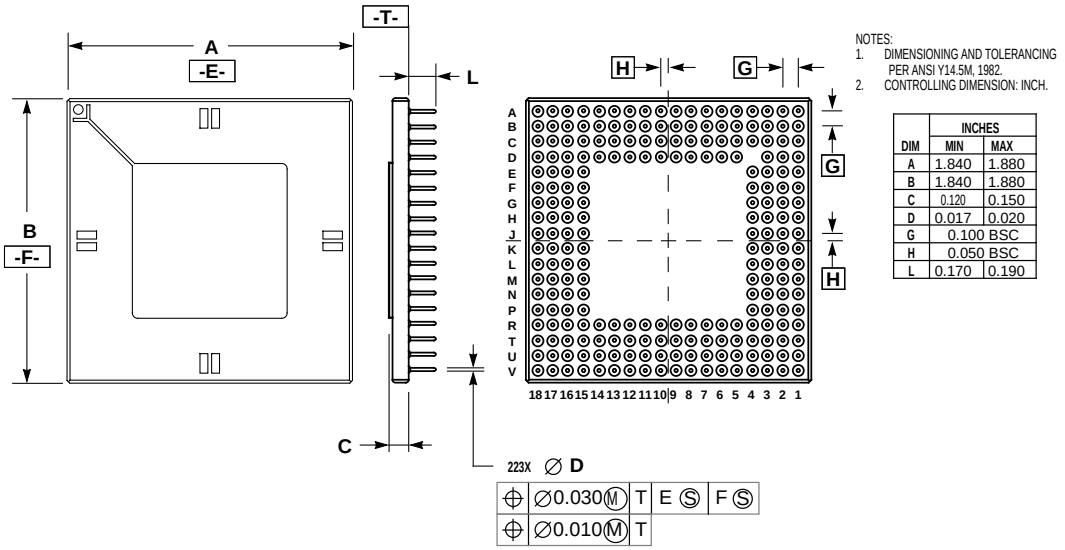
Table 3-1 DSP96002 Pin List, 223-pin PGA Package (Continued)

Pin Number	Signal Type	Signal Name
V9	Input/Output	BD20
V10	Input/Output	BD19
V11	Input/Output	BD16
V12	Input/Output	BD13
V13	Input/Output	BD10
V14	Input/Output	BD08
V15	Input/Output	BD05
V16	Input/Output	BD02
V17	Input/Output	AD00
V18	Input/Output	AD01



DIM	INCHES MIN	INCHES MAX
A	1.840	1.880
B	1.840	1.880
C	0.120	0.150
D	0.017	0.020
G	0.100 BSC	
H	0.050 BSC	
L	0.170	0.190

CASE 860C-02
ISSUE A

Figure 3-3 DSP96002 Mechanical Information, 223-pin PGA Package

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CQFP PACKAGE

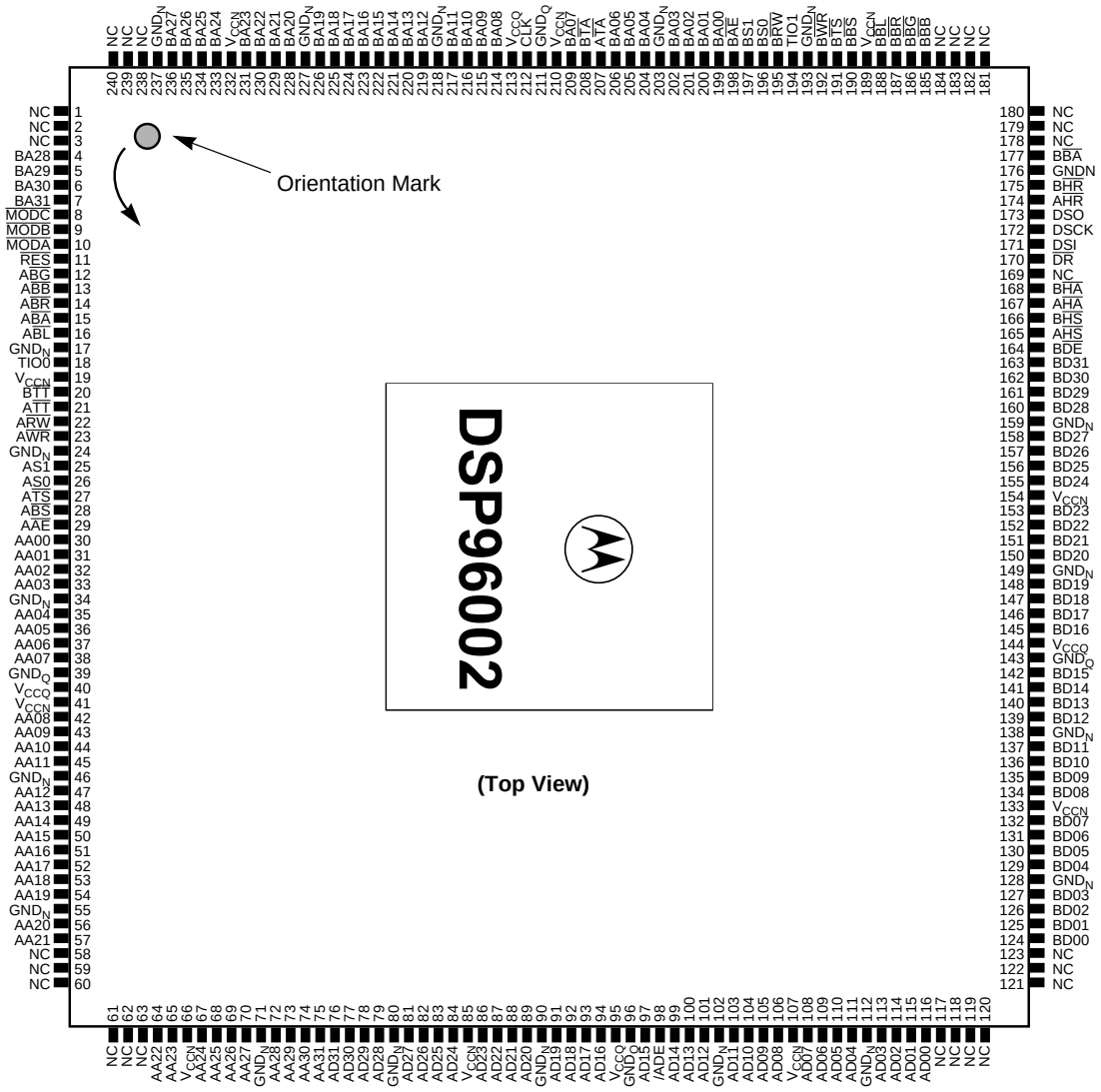

Figure 3-4 Top View of the DSP96002 240-pin CQFP Package

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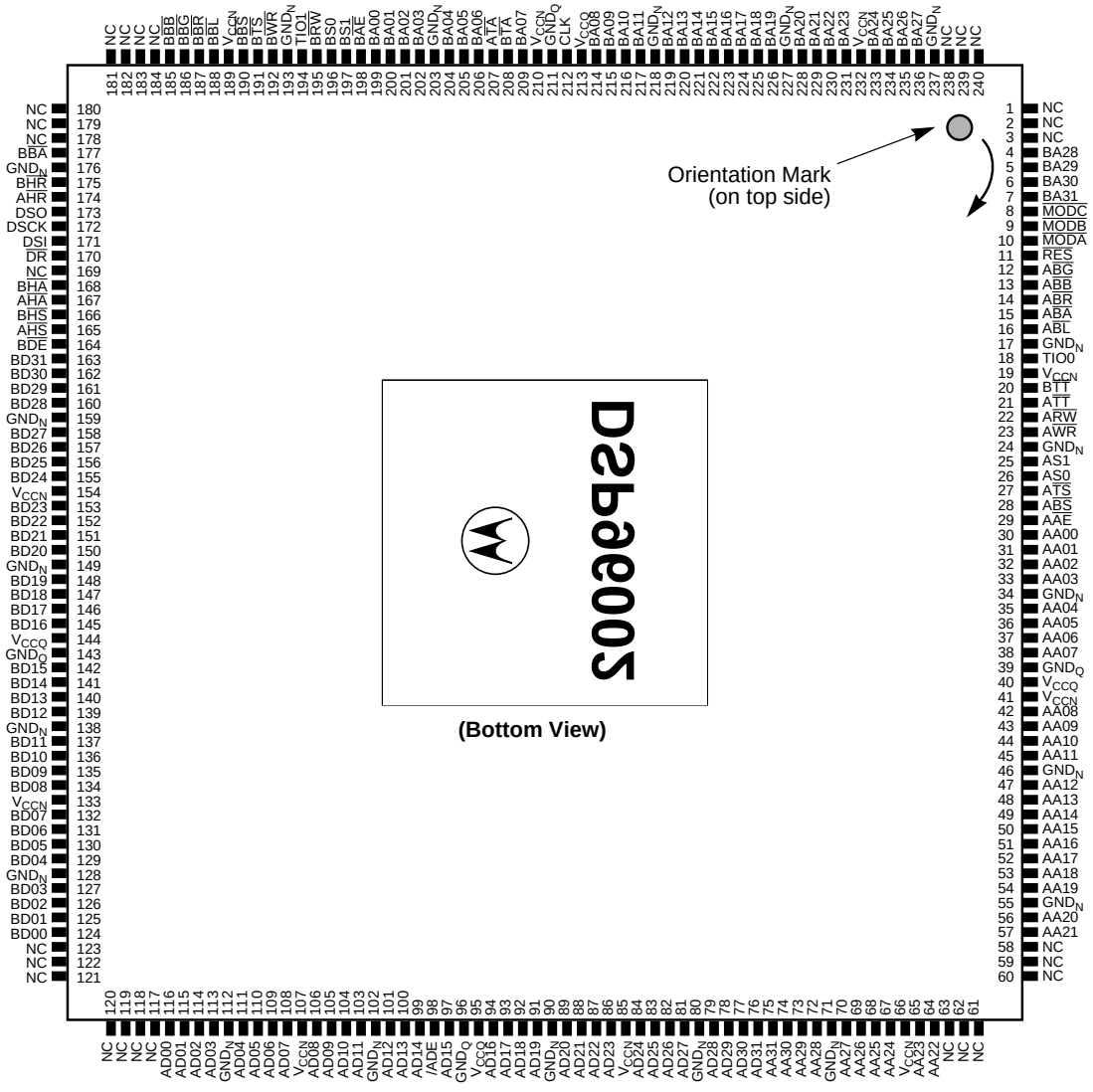

Figure 3-5 Bottom View of the DSP96002 240-pin CQFP Package

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package

Pin Number	Signal Type	Signal Name
1	N/A	NC
2	N/A	NC
3	N/A	NC
4	Input/Output	BA28
5	Input/Output	BA29
6	Input/Output	BA30
7	Input/Output	BA31
8	Input	$\overline{IRQC}$/MODC
9	Input	$\overline{IRQB}$/MODB
10	Input	$\overline{IRQA}$/MODA
11	Input	$\overline{RESET}$
12	Input	A$\overline{BG}$
13	Input	A$\overline{BB}$
14	Output	A$\overline{BR}$
15	Output	A$\overline{BA}$
16	Output	A$\overline{BL}$
17	Input	GND_N
18	Input/Output	TIO0
19	Input	V_{CCN}
20	Output	B$\overline{TT}$
21	Output	A$\overline{TT}$
22	Output	AR/$\overline{W}$
23	Output	A$\overline{WR}$
24	Input	GND_N
25	Output	AS1
26	Output	AS0
27	Input/Output	A$\overline{TS}$
28	Output	A$\overline{BS}$
29	Input	A$\overline{AE}$
30	Input/Output	AA00
31	Input/Output	AA01
32	Input/Output	AA02
33	Input/Output	AA03
34	Input	GND_N

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
35	Input/Output	AA04
36	Input/Output	AA05
37	Input/Output	AA06
38	Input/Output	AA07
39	Input	GND_Q
40	Input	V_{CCQ}
41	Input	V_{CCN}
42	Input/Output	AA08
43	Input/Output	AA09
44	Input/Output	AA10
45	Input/Output	AA11
46	Input	GND_N
47	Input/Output	AA12
48	Input/Output	AA13
49	Input/Output	AA14
50	Input/Output	AA15
51	Input/Output	AA16
52	Input/Output	AA17
53	Input/Output	AA18
54	Input/Output	AA19
55	Input	GND_N
56	Input/Output	AA20
57	Input/Output	AA21
58	N/A	NC
59	N/A	NC
60	N/A	NC
61	N/A	NC
62	N/A	NC
63	N/A	NC
64	Input/Output	AA22
65	Input/Output	AA23
66	Input	V_{CCN}
67	Input/Output	AA24
68	Input/Output	AA25
69	Input/Output	AA26

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
70	Input/Output	AA27
71	Input	GND_N
72	Input/Output	AA28
73	Input/Output	AA29
74	Input/Output	AA30
75	Input/Output	AA31
76	Input/Output	AD31
77	Input/Output	AD30
78	Input/Output	AD29
79	Input/Output	AD28
80	Input	GND_N
81	Input/Output	AD27
82	Input/Output	AD26
83	Input/Output	AD25
84	Input/Output	AD24
85	Input	V_{CCN}
86	Input/Output	AD23
87	Input/Output	AD22
88	Input/Output	AD21
89	Input/Output	AD20
90	Input	GND_N
91	Input/Output	AD19
92	Input/Output	AD18
93	Input/Output	AD17
94	Input/Output	AD16
95	Input	V_{CCQ}
96	Input	GND_Q
97	Input/Output	AD15
98	Input	$\overline{ADE}$
99	Input/Output	AD14
100	Input/Output	AD13
101	Input/Output	AD12
102	Input	GND_N
103	Input/Output	AD11

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
104	Input/Output	AD10
105	Input/Output	AD09
106	Input/Output	AD08
107	Input	V_{CCN}
108	Input/Output	AD07
109	Input/Output	AD06
110	Input/Output	AD05
111	Input/Output	AD04
112	Input	GND_N
113	Input/Output	AD03
114	Input/Output	AD02
115	Input/Output	AD01
116	Input/Output	AD00
117	N/A	NC
118	N/A	NC
119	N/A	NC
120	N/A	NC
121	N/A	NC
122	N/A	NC
123	N/A	NC
124	Input/Output	BD00
125	Input/Output	BD01
126	Input/Output	BD02
127	Input/Output	BD03
128	Input	GND_N
129	Input/Output	BD04
130	Input/Output	BD05
131	Input/Output	BD06
132	Input/Output	BD07
133	Input	V_{CCN}
134	Input/Output	BD08
135	Input/Output	BD09
136	Input/Output	BD10
137	Input/Output	BD11
138	Input	GND_N
139	Input/Output	BD12

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
140	Input/Output	BD13
141	Input/Output	BD14
142	Input/Output	BD15
143	Input	GND_Q
144	Input	V_{CCQ}
145	Input/Output	BD16
146	Input/Output	BD17
147	Input/Output	BD18
148	Input/Output	BD19
149	Input	GND_N
150	Input/Output	BD20
151	Input/Output	BD21
152	Input/Output	BD22
153	Input/Output	BD23
154	Input	V_{CCN}
155	Input/Output	BD24
156	Input/Output	BD25
157	Input/Output	BD26
158	Input/Output	BD27
159	Input	GND_N
160	Input/Output	BD28
161	Input/Output	BD29
162	Input/Output	BD30
163	Input/Output	BD31
164	Input	$B\overline{DE}$
165	Input	$A\overline{HS}$
166	Input	$B\overline{HS}$
167	Input	$A\overline{HA}$
168	Input	$B\overline{HA}$
169	N/A	NC
170	Input	$\overline{DR}$
171	Input/Output	DSI/OS0
172	Input/Output	DSK/OS1
173	Output	DSO
174	Output	$A\overline{HR}$
175	Output	$B\overline{HR}$

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
176	Input	GND_N
177	Output	$B\overline{BA}$
178	N/A	NC
179	N/A	NC
180	N/A	NC
181	N/A	NC
182	N/A	NC
183	N/A	NC
184	N/A	NC
185	Input	$B\overline{BB}$
186	Input	$B\overline{BG}$
187	Output	$B\overline{BR}$
188	Output	$B\overline{BL}$
189	Input	V_{CCN}
190	Output	$B\overline{BS}$
191	Input/Output	$B\overline{TS}$
192	Output	$B\overline{WR}$
193	Input	GND_N
194	Input/Output	TIO1
195	Output	$BR/\overline{W}$
196	Output	BS0
197	Output	BS1
198	Input	$B\overline{AE}$
199	Output	BA00
200	Output	BA01
201	Output	BA02
202	Output	BA03
203	Input	GND_N
204	Output	BA04
205	Output	BA05
206	Output	BA06
207	Input	$A\overline{TA}$
208	Input	$B\overline{TA}$
209	Output	BA07
210	Input	V_{CCN}

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Table 3-2 DSP96002 Pin List, 240-pin CQFP Package (Continued)

Pin Number	Signal Type	Signal Name
211	Input	GND_Q
212	Input	CLK
213	Input	V_{CCQ}
214	Output	BA08
215	Output	BA09
216	Output	BA10
217	Output	BA11
218	Input	GND_N
219	Output	BA12
220	Output	BA13
221	Output	BA14
222	Output	BA15
223	Output	BA16
224	Output	BA17
225	Output	BA18
226	Output	BA19
227	Input	GND_N
228	Output	BA20
229	Output	BA21
230	Output	BA22
231	Output	BA23
232	Input	V_{CCN}
233	Output	BA24
234	Output	BA25
235	Output	BA26
236	Output	BA27
237	Input	GND_N
238	N/A	NC
239	N/A	NC
240	N/A	NC

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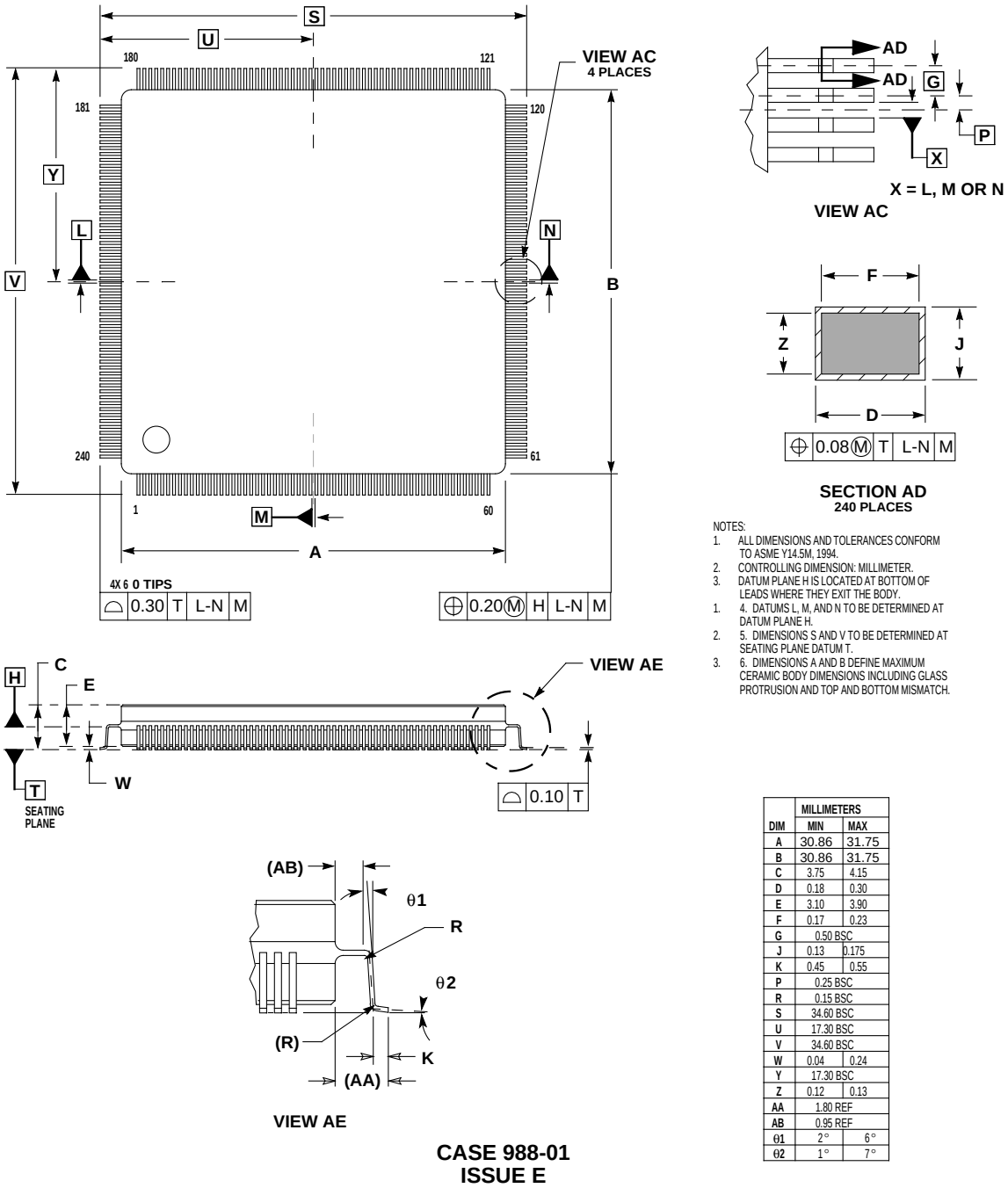

NOTES:
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEADS WHERE THEY EXIT THE BODY.
1. 4. DATUMS L, M, AND N TO BE DETERMINED AT DATUM PLANE H.
2. 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE DATUM T.
3. 6. DIMENSIONS A AND B DEFINE MAXIMUM CERAMIC BODY DIMENSIONS INCLUDING GLASS PROTRUSION AND TOP AND BOTTOM MISMATCH.

	MILLIMETERS	
DIM	MIN	MAX
A	30.86	31.75
B	30.86	31.75
C	3.75	4.15
D	0.18	0.30
E	3.10	3.90
F	0.17	0.23
G	0.50 BSC	
J	0.13	0.175
K	0.45	0.55
P	0.25 BSC	
R	0.15 BSC	
S	34.60 BSC	
U	17.30 BSC	
V	34.60 BSC	
W	0.04	0.24
Y	17.30 BSC	
Z	0.12	0.13
AA	1.80 REF	
AB	0.95 REF	
θ1	2°	6°
θ2	1°	7°

Figure 3-6 DSP96002 Mechanical Information, 240-pin CQFP Package

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PACKAGE AND PIN-OUT INFORMATION

Complete mechanical information regarding DSP96002 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The mechanical drawings for the 223-pin PGA package are referenced as 860C-02.

The mechanical drawings for the 240-pin CQFP package are referenced as 988-01.

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SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C / W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C / W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C / W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

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The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T) / P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T) / P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface, and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

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ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP, and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5” per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses, as well as the $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{TA}$, $\overline{TS}$, $\overline{BG}$, $\overline{HS}$, and $\overline{HA}$ pins. Maximum PCB trace lengths on the order of 6" are recommended.
- Consider all device loads, as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{CCPLL} and V_{SSPLL} pins.

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POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. Some of the factors that affect current consumption are described in this section. Most of the current consumed by CMOS devices is Alternating Current (AC), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the formula:

Equation 3: $I = C \times V \times f$

where: C = node / pin capacitance
V = voltage swing
f = frequency of node / pin toggle

Example 4-1 Current Consumption

For an I / O pin loaded with 50 pF capacitance, operating at 5.5 V, and with a 60 MHz clock, toggling at its maximum possible rate (30 MHz), the current consumption is:

Equation 4: $I = 50 \times 10^{-12} \times 5.5 \times 30 \times 10^{6} = 8.25\ \text{mA}$

The Maximum Internal Current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The Typical Internal Current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.
- Disable unused pin activity.

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POWER-UP CONSIDERATIONS

To power-up the device properly, ensure that the following conditions are met:

- Stable power is applied to the device according to the specifications in **Table 2-3** (DC Electrical Characteristics).
- The external clock oscillator is active and stable.
- $\overline{\text{RESET}}$ is asserted according to the specifications in **Table 2-7** (Reset, Stop, Mode Select, and Interrupt Timing).

Care should be taken to ensure that the maximum ratings for all input voltages obey the restrictions on **Table 2-1** (Maximum Ratings), at all phases of the power-up procedure. This may be achieved by powering the external clock, hardware reset, and mode selection circuits from the same power supply that is connected to the power supply pins of the chip.

At the beginning of the hardware reset procedure, the device might consume significantly more current than the specified typical supply current. This is because of contentions among the internal nodes being affected by the hardware reset signal until they reach their final hardware reset state.

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SECTION 5

ORDERING INFORMATION

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 5-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP96002	5 V	Pin Grid Array (PGA)	223	60	DSP96002RC60
				40	DSP96002RC40
				33	DSP96002RC33
		Ceramic Quad Flat Pack (CQFP)	240	60	DSP96002FE60
				40	DSP96002FE40

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APPENDIX A

BOOTSTRAP CODE FOR DSP96002

```
; BOOTSTRAP CODE FOR DSP96002 - © Copyright 1988 Motorola Inc.
;
; Host algorithm  / AND / external bus method.
;
; This is the Bootstrap program contained in the DSP96002. This program
; can load the internal program memory from one of 4 external sources.
; The program reads the OMR bits MA and MB to decide which external
; source to access.
; If MB:MA = 0X - load from 4,096 consecutive byte-wide P: memory
; locations (starting at P:$FFFF0000).
; If MB:MA = 10 - load internal PRAM thru Host Interface in Port A.
; If MB:MA = 11 - load internal PRAM thru Host Interface in Port B.
BOOT            EQU     $FFFF0000; The location in P: memory
          ; where the external byte-wide
          ; EPROM is expected to be mapped
M_HCRA          EQU     $FFFFFFEC; Port A Host Control Register
M_HSRA          EQU     $FFFFFFED; Port A Host Status Register
M_HRXA          EQU     $FFFFFFEF; Port A Host Rec. Data Register
M_HCRB          EQU     $FFFFFFE4; Port B Host Control Register
M_HSRB          EQU     $FFFFFFE5; Port B Host Status Register
M_HRXB          EQU     $FFFFFFE7; Port B Host Rec. Data Register
          ORG     PL:$0; bootstrap code starts at P:$0
START           MOVE    #BOOT,R1; R1 = External P: address of
                     ; bootstrap byte-wide ROM
          MOVEI   #0,R0        ; R0 = starting P: address of
          ; internal memory where program
          ; will begin loading.
; If this program is entered by changing the OMR to bootstrap mode,
; make certain that registers M0 and M1 have been set to $FFFFFFFF.
; Make sure the appropriate BCR register is set to $xxxxxxFx since
; EPROMs are slow.
; Make sure that the Port Selection Register is set to permit program
; memory accesses thru the required memory expansion port (Port A or B).
;
; The first routine will load 4,096 bytes from the external P memory
; space beginning at P:$FFFF0000 (bits 7-0).  These will be condensed
; into 1,024 32-bit words and stored in contiguous internal PRAM memory
; locations starting at P:$0.  Note that the first routine loads data
; starting with the least significant byte of P:$0 first.
; The Port Selection Register is not set by this program. It is set
; by HW Reset.
```


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```
; The second routine loads the internal PRAM using the Host
; Interface logic.
; If HF1=0, it will load 4,096 bytes from the external host processor.
; These will be condensed into 1,024 32-bit words and stored in
; contiguous internal PRAM memory locations starting at P:$0.  Note that
; the routine loads data starting with the least significant byte of
; P:$0 first.
; If HF1=1, it will load 1,024 32-bit words from the external host
; processor.
; If the host processor only wants to load a portion of the P memory,
; and start execution of the loaded program, the Host Interface
; bootstrap load program routine may be killed by setting HF0 = 0.
;
  INLOOP         DO      #1024,_LOOP1; Load 1,024 instruction words
; This is the context switch
                 JSET    #1,OMR,_HOSTLD; Perform load from Host
          ; Interface if MB=1.
; This is the first routine. It loads from external P: memory.
                 DO      #4,_LOOP2; Get 4 bytes into D0.L
          LSR     #8,D0; Shift previous byte down
          MOVEM   P:(R1)+,D1.L; Get byte from ext. P mem.
          LSL     #24,D1; Shift into upper byte
          OR      D1,D0; concatenate
  _LOOP2  JMP     <_STORE; Then put the word in P memory
;
; This is the second routine. It loads thru the Host Interface.
  _HOSTLD        JSET    #0,OMR,_HOSTB; Port A or Port B?
; Boot thru Host Interface in Port A
  _HOSTA         BCLR    #5,X:M_HCRA; Enable Port A Host Interface
          MOVE    #M_HSRA,R2; R2 points to HSRA
          MOVE    #M_HRXA,R3; R3 points to HRXA
          JMP     <_HOSTR; go to host routine
; Boot thru Host Interface in Port B
  _HOSTB         BCLR    #5,X:M_HCRB; Enable Port B Host Interface
          MOVE    #M_HSRB,R2; R2 points to HSRB
          MOVE    #M_HRXB,R3; R3 points to HRXB
```

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```
; Host load routine
_HOSTR
_LBL11          JCLR    #3,X:(R2),_LBL22; if HF0=1, stop loading data.
          ENDDO     ; Must terminate the do loops
          JMP     <_BOOTEND

_LBL22    JCLR    #0,X:(R2),_LBL11; Wait for HRDF to go high
                    ; (meaning data is present).
          JCLR    #4,X:(R2),_LBL33; 8-bit source?
          MOVE    X:(R3),D0.L; Get 32-bit word from host
          JMP     <_STORE

_LBL33    DO      #4,_LOOP4; Get 4 bytes into D0.L
          LSR     #8,D0; Shift previous byte down

_LBL1     JCLR    #3,X:(R2),_LBL2; if HF0=1, stop loading data.
          ENDDO     ; Must terminate the do loops
          ENDDO
          JMP     <_BOOTEND
_LBL2     JCLR    #0,X:(R2),_LBL1; Wait for HRDF to go high
                    ; (meaning data is present).
          MOVE    X:(R3),D1.L; Get byte from host
          LSL     #24,D1; Shift into upper byte
          OR      D1,D0; concatenate
_LOOP4

_STORE    MOVEM   D0.L,P:(R0)+ ; Store 32-bit result in P mem.

_LOOP1              ; and go get another 32-bit word

; This is the exit handler that returns execution to internal PRAM
_BOOTEND  ANDI    #$F9,OMR     ; Set the operating mode to 00x
                    ; (and trigger an exit from
                    ; bootstrap mode).
          ANDI    #$0,CCR; Clear CCR as if HW RESET.
                    ; Also delay needed for
                    ; Op. Mode change.
          JMP     <$0; Start fetching from PRAM.
; DSP96002 bootstrap program size = 50 words
```


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APPENDIX B

X AND Y MEMORY ROM TABLES

Table B-1 X Memory ROM Contents (full cycle of cosine values)

xr:$00000400=	$3f800000	$3f7ffec4	$3f7ffb11	$3f7ff4e6
xr:$00000404=	$3f7fec43	$3f7fe129	$3f7fd397	$3f7fc38f
xr:$00000408=	$3f7fb10f	$3f7f9c18	$3f7f84ab	$3f7f6ac7
xr:$0000040c=	$3f7f4e6d	$3f7f2f9d	$3f7f0e58	$3f7eea9d
xr:$00000410=	$3f7ec46d	$3f7e9bc9	$3f7e70b0	$3f7e4323
xr:$00000414=	$3f7e1324	$3f7de0b1	$3f7dabcc	$3f7d7474
xr:$00000418=	$3f7d3aac	$3f7cfe73	$3f7cbfc9	$3f7c7eb0
xr:$0000041c=	$3f7c3b28	$3f7bf531	$3f7baccd	$3f7b61fc
xr:$00000420=	$3f7b14be	$3f7ac516	$3f7a7302	$3f7a1e84
xr:$00000424=	$3f79c79d	$3f796e4e	$3f791298	$3f78b47b
xr:$00000428=	$3f7853f8	$3f77f110	$3f778bc5	$3f772417
xr:$0000042c=	$3f76ba07	$3f764d97	$3f75dec6	$3f756d97
xr:$00000430=	$3f74fa0b	$3f748422	$3f740bdd	$3f73913f
xr:$00000434=	$3f731447	$3f7294f8	$3f721352	$3f718f57
xr:$00000438=	$3f710908	$3f708066	$3f6ff573	$3f6f6830
xr:$0000043c=	$3f6ed89e	$3f6e46be	$3f6db293	$3f6d1c1d
xr:$00000440=	$3f6c835e	$3f6be858	$3f6b4b0c	$3f6aab7b
xr:$00000444=	$3f6a09a7	$3f696591	$3f68bf3c	$3f6816a8
xr:$00000448=	$3f676bd8	$3f66becc	$3f660f88	$3f655e0b
xr:$0000044c=	$3f64aa59	$3f63f473	$3f633c5a	$3f628210
xr:$00000450=	$3f61c598	$3f6106f2	$3f604621	$3f5f8327
xr:$00000454=	$3f5ebe05	$3f5df6be	$3f5d2d53	$3f5c61c7
xr:$00000458=	$3f5b941a	$3f5ac450	$3f59f26a	$3f591e6a
xr:$0000045c=	$3f584853	$3f577026	$3f5695e5	$3f55b993
xr:$00000460=	$3f54db31	$3f53fac3	$3f531849	$3f5233c6
xr:$00000464=	$3f514d3d	$3f5064af	$3f4f7a1f	$3f4e8d90
xr:$00000468=	$3f4d9f02	$3f4cae79	$3f4bbbf8	$3f4ac77f
xr:$0000046c=	$3f49d112	$3f48d8b3	$3f47de65	$3f46e22a
xr:$00000470=	$3f45e403	$3f44e3f5	$3f43e200	$3f42de29
xr:$00000474=	$3f41d870	$3f40d0da	$3f3fc767	$3f3ebc1b

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$00000478=	$3f3daef9	$3f3ca003	$3f3b8f3b	$3f3a7ca4
xr:$0000047c=	$3f396842	$3f385216	$3f373a23	$3f36206c
xr:$00000480=	$3f3504f3	$3f33e7bc	$3f32c8c9	$3f31a81d
xr:$00000484=	$3f3085bb	$3f2f61a5	$3f2e3bde	$3f2d1469
xr:$00000488=	$3f2beb4a	$3f2ac082	$3f299415	$3f286605
xr:$0000048c=	$3f273656	$3f26050a	$3f24d225	$3f239da9
xr:$00000490=	$3f226799	$3f212ff9	$3f1ff6cb	$3f1ebc12
xr:$00000494=	$3f1d7fd1	$3f1c420c	$3f1b02c6	$3f19c200
xr:$00000498=	$3f187fc0	$3f173c07	$3f15f6d9	$3f14b039
xr:$0000049c=	$3f13682a	$3f121eb0	$3f10d3cd	$3f0f8784
xr:$000004a0=	$3f0e39da	$3f0cead0	$3f0b9a6b	$3f0a48ad
xr:$000004a4=	$3f08f59b	$3f07a136	$3f064b82	$3f04f484
xr:$000004a8=	$3f039c3d	$3f0242b1	$3f00e7e4	$3eff17b2
xr:$000004ac=	$3efc5d27	$3ef9a02d	$3ef6e0cb	$3ef41f07
xr:$000004b0=	$3ef15aea	$3eee9479	$3eebcbbb	$3ee900b7
xr:$000004b4=	$3ee63375	$3ee363fa	$3ee0924f	$3eddbe79
xr:$000004b8=	$3edae880	$3ed8106b	$3ed53641	$3ed25a09
xr:$000004bc=	$3ecf7bca	$3ecc9b8b	$3ec9b953	$3ec6d529
xr:$000004c0=	$3ec3ef15	$3ec1071e	$3ebe1d4a	$3ebb31a0
xr:$000004c4=	$3eb8442a	$3eb554ec	$3eb263ef	$3eaf713a
xr:$000004c8=	$3eac7cd4	$3ea986c4	$3ea68f12	$3ea395c5
xr:$000004cc=	$3ea09ae5	$3e9d9e78	$3e9aa086	$3e97a117
xr:$000004d0=	$3e94a031	$3e919ddd	$3e8e9a22	$3e8b9507
xr:$000004d4=	$3e888e93	$3e8586ce	$3e827dc0	$3e7ee6e1
xr:$000004d8=	$3e78cfcc	$3e72b651	$3e6c9a7f	$3e667c66
xr:$000004dc=	$3e605c13	$3e5a3997	$3e541501	$3e4dee60
xr:$000004e0=	$3e47c5c2	$3e419b37	$3e3b6ecf	$3e354098
xr:$000004e4=	$3e2f10a2	$3e28defc	$3e22abb6	$3e1c76de
xr:$000004e8=	$3e164083	$3e1008b7	$3e09cf86	$3e039502
xr:$000004ec=	$3dfab273	$3dee3876	$3de1bc2e	$3dd53db9
xr:$000004f0=	$3dc8bd36	$3dbc3ac3	$3dafb680	$3da3308c
xr:$000004f4=	$3d96a905	$3d8a200a	$3d7b2b74	$3d621469
xr:$000004f8=	$3d48fb30	$3d2fe007	$3d16c32c	$3cfb49ba
xr:$000004fc=	$3cc90ab0	$3c96c9b6	$3c490e90	$3bc90f88
xr:$00000500=	$248d4000	$bbc90f88	$bc490e90	$bc96c9b6
xr:$00000504=	$bcc90ab0	$bcfb49ba	$bd16c32c	$bd2fe007
xr:$00000508=	$bd48fb30	$bd621469	$bd7b2b74	$bd8a200a

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$0000050c=	$bd96a905	$bda3308c	$bdafb680	$bdbc3ac3
xr:$00000510=	$bdc8bd36	$bdd53db9	$bde1bc2e	$bdee3876
xr:$00000514=	$bdfab273	$be039502	$be09cf86	$be1008b7
xr:$00000518=	$be164083	$be1c76de	$be22abb6	$be28defc
xr:$0000051c=	$be2f10a2	$be354098	$be3b6ecf	$be419b37
xr:$00000520=	$be47c5c2	$be4dee60	$be541501	$be5a3997
xr:$00000524=	$be605c13	$be667c66	$be6c9a7f	$be72b651
xr:$00000528=	$be78cfcc	$be7ee6e1	$be827dc0	$be8586ce
xr:$0000052c=	$be888e93	$be8b9507	$be8e9a22	$be919ddd
xr:$00000530=	$be94a031	$be97a117	$be9aa086	$be9d9e78
xr:$00000534=	$bea09ae5	$bea395c5	$bea68f12	$bea986c4
xr:$00000538=	$beac7cd4	$beaf713a	$beb263ef	$beb554ec
xr:$0000053c=	$beb8442a	$bebb31a0	$bebe1d4a	$bec1071e
xr:$00000540=	$bec3ef15	$bec6d529	$bec9b953	$becc9b8b
xr:$00000544=	$becf7bca	$bed25a09	$bed53641	$bed8106b
xr:$00000548=	$bedae880	$beddbe79	$bee0924f	$bee363fa
xr:$0000054c=	$bee63375	$bee900b7	$beebcbbb	$beee9479
xr:$00000550=	$bef15aea	$bef41f07	$bef6e0cb	$bef9a02d
xr:$00000554=	$befc5d27	$beff17b2	$bf00e7e4	$bf0242b1
xr:$00000558=	$bf039c3d	$bf04f484	$bf064b82	$bf07a136
xr:$0000055c=	$bf08f59b	$bf0a48ad	$bf0b9a6b	$bf0cead0
xr:$00000560=	$bf0e39da	$bf0f8784	$bf10d3cd	$bf121eb0
xr:$00000564=	$bf13682a	$bf14b039	$bf15f6d9	$bf173c07
xr:$00000568=	$bf187fc0	$bf19c200	$bf1b02c6	$bf1c420c
xr:$0000056c=	$bf1d7fd1	$bf1ebc12	$bf1ff6cb	$bf212ff9
xr:$00000570=	$bf226799	$bf239da9	$bf24d225	$bf26050a
xr:$00000574=	$bf273656	$bf286605	$bf299415	$bf2ac082
xr:$00000578=	$bf2beb4a	$bf2d1469	$bf2e3bde	$bf2f61a5
xr:$0000057c=	$bf3085bb	$bf31a81d	$bf32c8c9	$bf33e7bc
xr:$00000580=	$bf3504f3	$bf36206c	$bf373a23	$bf385216
xr:$00000584=	$bf396842	$bf3a7ca4	$bf3b8f3b	$bf3ca003
xr:$00000588=	$bf3daef9	$bf3ebc1b	$bf3fc767	$bf40d0da
xr:$0000058c=	$bf41d870	$bf42de29	$bf43e200	$bf44e3f5
xr:$00000590=	$bf45e403	$bf46e22a	$bf47de65	$bf48d8b3
xr:$00000594=	$bf49d112	$bf4ac77f	$bf4bbbf8	$bf4cae79
xr:$00000598=	$bf4d9f02	$bf4e8d90	$bf4f7a1f	$bf5064af
xr:$0000059c=	$bf514d3d	$bf5233c6	$bf531849	$bf53fac3

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$000005a0=	$bf54db31	$bf55b993	$bf5695e5	$bf577026
xr:$000005a4=	$bf584853	$bf591e6a	$bf59f26a	$bf5ac450
xr:$000005a8=	$bf5b941a	$bf5c61c7	$bf5d2d53	$bf5df6be
xr:$000005ac=	$bf5ebe05	$bf5f8327	$bf604621	$bf6106f2
xr:$000005b0=	$bf61c598	$bf628210	$bf633c5a	$bf63f473
xr:$000005b4=	$bf64aa59	$bf655e0b	$bf660f88	$bf66becc
xr:$000005b8=	$bf676bd8	$bf6816a8	$bf68bf3c	$bf696591
xr:$000005bc=	$bf6a09a7	$bf6aab7b	$bf6b4b0c	$bf6be858
xr:$000005c0=	$bf6c835e	$bf6d1c1d	$bf6db293	$bf6e46be
xr:$000005c4=	$bf6ed89e	$bf6f6830	$bf6ff573	$bf708066
xr:$000005c8=	$bf710908	$bf718f57	$bf721352	$bf7294f8
xr:$000005cc=	$bf731447	$bf73913f	$bf740bdd	$bf748422
xr:$000005d0=	$bf74fa0b	$bf756d97	$bf75dec6	$bf764d97
xr:$000005d4=	$bf76ba07	$bf772417	$bf778bc5	$bf77f110
xr:$000005d8=	$bf7853f8	$bf78b47b	$bf791298	$bf796e4e
xr:$000005dc=	$bf79c79d	$bf7a1e84	$bf7a7302	$bf7ac516
xr:$000005e0=	$bf7b14be	$bf7b61fc	$bf7baccd	$bf7bf531
xr:$000005e4=	$bf7c3b28	$bf7c7eb0	$bf7cbfc9	$bf7cfe73
xr:$000005e8=	$bf7d3aac	$bf7d7474	$bf7dabcc	$bf7de0b1
xr:$000005ec=	$bf7e1324	$bf7e4323	$bf7e70b0	$bf7e9bc9
xr:$000005f0=	$bf7ec46d	$bf7eea9d	$bf7f0e58	$bf7f2f9d
xr:$000005f4=	$bf7f4e6d	$bf7f6ac7	$bf7f84ab	$bf7f9c18
xr:$000005f8=	$bf7fb10f	$bf7fc38f	$bf7fd397	$bf7fe129
xr:$000005fc=	$bf7fec43	$bf7ff4e6	$bf7ffb11	$bf7ffec4
xr:$00000600=	$bf800000	$bf7ffec4	$bf7ffb11	$bf7ff4e6
xr:$00000604=	$bf7fec43	$bf7fe129	$bf7fd397	$bf7fc38f
xr:$00000608=	$bf7fb10f	$bf7f9c18	$bf7f84ab	$bf7f6ac7
xr:$0000060c=	$bf7f4e6d	$bf7f2f9d	$bf7f0e58	$bf7eea9d
xr:$00000610=	$bf7ec46d	$bf7e9bc9	$bf7e70b0	$bf7e4323
xr:$00000614=	$bf7e1324	$bf7de0b1	$bf7dabcc	$bf7d7474
xr:$00000618=	$bf7d3aac	$bf7cfe73	$bf7cbfc9	$bf7c7eb0
xr:$0000061c=	$bf7c3b28	$bf7bf531	$bf7baccd	$bf7b61fc
xr:$00000620=	$bf7b14be	$bf7ac516	$bf7a7302	$bf7a1e84
xr:$00000624=	$bf79c79d	$bf796e4e	$bf791298	$bf78b47b
xr:$00000628=	$bf7853f8	$bf77f110	$bf778bc5	$bf772417
xr:$0000062c=	$bf76ba07	$bf764d97	$bf75dec6	$bf756d97
xr:$00000630=	$bf74fa0b	$bf748422	$bf740bdd	$bf73913f

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$00000634=	$bf731447	$bf7294f8	$bf721352	$bf718f57
xr:$00000638=	$bf710908	$bf708066	$bf6ff573	$bf6f6830
xr:$0000063c=	$bf6ed89e	$bf6e46be	$bf6db293	$bf6d1c1d
xr:$00000640=	$bf6c835e	$bf6be858	$bf6b4b0c	$bf6aab7b
xr:$00000644=	$bf6a09a7	$bf696591	$bf68bf3c	$bf6816a8
xr:$00000648=	$bf676bd8	$bf66becc	$bf660f88	$bf655e0b
xr:$0000064c=	$bf64aa59	$bf63f473	$bf633c5a	$bf628210
xr:$00000650=	$bf61c598	$bf6106f2	$bf604621	$bf5f8327
xr:$00000654=	$bf5ebe05	$bf5df6be	$bf5d2d53	$bf5c61c7
xr:$00000658=	$bf5b941a	$bf5ac450	$bf59f26a	$bf591e6a
xr:$0000065c=	$bf584853	$bf577026	$bf5695e5	$bf55b993
xr:$00000660=	$bf54db31	$bf53fac3	$bf531849	$bf5233c6
xr:$00000664=	$bf514d3d	$bf5064af	$bf4f7a1f	$bf4e8d90
xr:$00000668=	$bf4d9f02	$bf4cae79	$bf4bbbf8	$bf4ac77f
xr:$0000066c=	$bf49d112	$bf48d8b3	$bf47de65	$bf46e22a
xr:$00000670=	$bf45e403	$bf44e3f5	$bf43e200	$bf42de29
xr:$00000674=	$bf41d870	$bf40d0da	$bf3fc767	$bf3ebc1b
xr:$00000678=	$bf3daef9	$bf3ca003	$bf3b8f3b	$bf3a7ca4
xr:$0000067c=	$bf396842	$bf385216	$bf373a23	$bf36206c
xr:$00000680=	$bf3504f3	$bf33e7bc	$bf32c8c9	$bf31a81d
xr:$00000684=	$bf3085bb	$bf2f61a5	$bf2e3bde	$bf2d1469
xr:$00000688=	$bf2beb4a	$bf2ac082	$bf299415	$bf286605
xr:$0000068c=	$bf273656	$bf26050a	$bf24d225	$bf239da9
xr:$00000690=	$bf226799	$bf212ff9	$bf1ff6cb	$bf1ebc12
xr:$00000694=	$bf1d7fd1	$bf1c420c	$bf1b02c6	$bf19c200
xr:$00000698=	$bf187fc0	$bf173c07	$bf15f6d9	$bf14b039
xr:$0000069c=	$bf13682a	$bf121eb0	$bf10d3cd	$bf0f8784
xr:$000006a0=	$bf0e39da	$bf0cead0	$bf0b9a6b	$bf0a48ad
xr:$000006a4=	$bf08f59b	$bf07a136	$bf064b82	$bf04f484
xr:$000006a8=	$bf039c3d	$bf0242b1	$bf00e7e4	$beff17b2
xr:$000006ac=	$befc5d27	$bef9a02d	$bef6e0cb	$bef41f07
xr:$000006b0=	$bef15aea	$beee9479	$beebcbbb	$bee900b7
xr:$000006b4=	$bee63375	$bee363fa	$bee0924f	$beddbe79
xr:$000006b8=	$bedae880	$bed8106b	$bed53641	$bed25a09
xr:$000006bc=	$becf7bca	$becc9b8b	$bec9b953	$bec6d529
xr:$000006c0=	$bec3ef15	$bec1071e	$bebe1d4a	$bebb31a0
xr:$000006c4=	$beb8442a	$beb554ec	$beb263ef	$beaf713a

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$000006c8=	$beac7cd4	$bea986c4	$bea68f12	$bea395c5
xr:$000006cc=	$bea09ae5	$be9d9e78	$be9aa086	$be97a117
xr:$000006d0=	$be94a031	$be919ddd	$be8e9a22	$be8b9507
xr:$000006d4=	$be888e93	$be8586ce	$be827dc0	$be7ee6e1
xr:$000006d8=	$be78cfcc	$be72b651	$be6c9a7f	$be667c66
xr:$000006dc=	$be605c13	$be5a3997	$be541501	$be4dee60
xr:$000006e0=	$be47c5c2	$be419b37	$be3b6ecf	$be354098
xr:$000006e4=	$be2f10a2	$be28defc	$be22abb6	$be1c76de
xr:$000006e8=	$be164083	$be1008b7	$be09cf86	$be039502
xr:$000006ec=	$bdfab273	$bdee3876	$bde1bc2e	$bdd53db9
xr:$000006f0=	$bdc8bd36	$bdbc3ac3	$bdafb680	$bda3308c
xr:$000006f4=	$bd96a905	$bd8a200a	$bd7b2b74	$bd621469
xr:$000006f8=	$bd48fb30	$bd2fe007	$bd16c32c	$bcfb49ba
xr:$000006fc=	$bcc90ab0	$bc96c9b6	$bc490e90	$bbc90f88
xr:$00000700=	$a48d4000	$3bc90f88	$3c490e90	$3c96c9b6
xr:$00000704=	$3cc90ab0	$3cfb49ba	$3d16c32c	$3d2fe007
xr:$00000708=	$3d48fb30	$3d621469	$3d7b2b74	$3d8a200a
xr:$0000070c=	$3d96a905	$3da3308c	$3dafb680	$3dbc3ac3
xr:$00000710=	$3dc8bd36	$3dd53db9	$3de1bc2e	$3dee3876
xr:$00000714=	$3dfab273	$3e039502	$3e09cf86	$3e1008b7
xr:$00000718=	$3e164083	$3e1c76de	$3e22abb6	$3e28defc
xr:$0000071c=	$3e2f10a2	$3e354098	$3e3b6ecf	$3e419b37
xr:$00000720=	$3e47c5c2	$3e4dee60	$3e541501	$3e5a3997
xr:$00000724=	$3e605c13	$3e667c66	$3e6c9a7f	$3e72b651
xr:$00000728=	$3e78cfcc	$3e7ee6e1	$3e827dc0	$3e8586ce
xr:$0000072c=	$3e888e93	$3e8b9507	$3e8e9a22	$3e919ddd
xr:$00000730=	$3e94a031	$3e97a117	$3e9aa086	$3e9d9e78
xr:$00000734=	$3ea09ae5	$3ea395c5	$3ea68f12	$3ea986c4
xr:$00000738=	$3eac7cd4	$3eaf713a	$3eb263ef	$3eb554ec
xr:$0000073c=	$3eb8442a	$3ebb31a0	$3ebe1d4a	$3ec1071e
xr:$00000740=	$3ec3ef15	$3ec6d529	$3ec9b953	$3ecc9b8b
xr:$00000744=	$3ecf7bca	$3ed25a09	$3ed53641	$3ed8106b
xr:$00000748=	$3edae880	$3eddbe79	$3ee0924f	$3ee363fa
xr:$0000074c=	$3ee63375	$3ee900b7	$3eebcbbb	$3eee9479
xr:$00000750=	$3ef15aea	$3ef41f07	$3ef6e0cb	$3ef9a02d
xr:$00000754=	$3efc5d27	$3eff17b2	$3f00e7e4	$3f0242b1
xr:$00000758=	$3f039c3d	$3f04f484	$3f064b82	$3f07a136

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$0000075c=	$3f08f59b	$3f0a48ad	$3f0b9a6b	$3f0cead0
xr:$00000760=	$3f0e39da	$3f0f8784	$3f10d3cd	$3f121eb0
xr:$00000764=	$3f13682a	$3f14b039	$3f15f6d9	$3f173c07
xr:$00000768=	$3f187fc0	$3f19c200	$3f1b02c6	$3f1c420c
xr:$0000076c=	$3f1d7fd1	$3f1ebc12	$3f1ff6cb	$3f212ff9
xr:$00000770=	$3f226799	$3f239da9	$3f24d225	$3f26050a
xr:$00000774=	$3f273656	$3f286605	$3f299415	$3f2ac082
xr:$00000778=	$3f2beb4a	$3f2d1469	$3f2e3bde	$3f2f61a5
xr:$0000077c=	$3f3085bb	$3f31a81d	$3f32c8c9	$3f33e7bc
xr:$00000780=	$3f3504f3	$3f36206c	$3f373a23	$3f385216
xr:$00000784=	$3f396842	$3f3a7ca4	$3f3b8f3b	$3f3ca003
xr:$00000788=	$3f3daef9	$3f3ebc1b	$3f3fc767	$3f40d0da
xr:$0000078c=	$3f41d870	$3f42de29	$3f43e200	$3f44e3f5
xr:$00000790=	$3f45e403	$3f46e22a	$3f47de65	$3f48d8b3
xr:$00000794=	$3f49d112	$3f4ac77f	$3f4bbbf8	$3f4cae79
xr:$00000798=	$3f4d9f02	$3f4e8d90	$3f4f7a1f	$3f5064af
xr:$0000079c=	$3f514d3d	$3f5233c6	$3f531849	$3f53fac3
xr:$000007a0=	$3f54db31	$3f55b993	$3f5695e5	$3f577026
xr:$000007a4=	$3f584853	$3f591e6a	$3f59f26a	$3f5ac450
xr:$000007a8=	$3f5b941a	$3f5c61c7	$3f5d2d53	$3f5df6be
xr:$000007ac=	$3f5ebe05	$3f5f8327	$3f604621	$3f6106f2
xr:$000007b0=	$3f61c598	$3f628210	$3f633c5a	$3f63f473
xr:$000007b4=	$3f64aa59	$3f655e0b	$3f660f88	$3f66becc
xr:$000007b8=	$3f676bd8	$3f6816a8	$3f68bf3c	$3f696591
xr:$000007bc=	$3f6a09a7	$3f6aab7b	$3f6b4b0c	$3f6be858
xr:$000007c0=	$3f6c835e	$3f6d1c1d	$3f6db293	$3f6e46be
xr:$000007c4=	$3f6ed89e	$3f6f6830	$3f6ff573	$3f708066
xr:$000007c8=	$3f710908	$3f718f57	$3f721352	$3f7294f8
xr:$000007cc=	$3f731447	$3f73913f	$3f740bdd	$3f748422
xr:$000007d0=	$3f74fa0b	$3f756d97	$3f75dec6	$3f764d97
xr:$000007d4=	$3f76ba07	$3f772417	$3f778bc5	$3f77f110
xr:$000007d8=	$3f7853f8	$3f78b47b	$3f791298	$3f796e4e
xr:$000007dc=	$3f79c79d	$3f7a1e84	$3f7a7302	$3f7ac516
xr:$000007e0=	$3f7b14be	$3f7b61fc	$3f7baccd	$3f7bf531
xr:$000007e4=	$3f7c3b28	$3f7c7eb0	$3f7cbfc9	$3f7cfe73
xr:$000007e8=	$3f7d3aac	$3f7d7474	$3f7dabcc	$3f7de0b1
xr:$000007ec=	$3f7e1324	$3f7e4323	$3f7e70b0	$3f7e9bc9

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Table B-1 X Memory ROM Contents (full cycle of cosine values) (Continued)

xr:$000007f0=	$3f7ec46d	$3f7eea9d	$3f7f0e58	$3f7f2f9d
xr:$000007f4=	$3f7f4e6d	$3f7f6ac7	$3f7f84ab	$3f7f9c18
xr:$000007f8=	$3f7fb10f	$3f7fc38f	$3f7fd397	$3f7fe129
xr:$000007fc=	$3f7fec43	$3f7ff4e6	$3f7ffb11	$3f7ffec4

Table B-2 Y Memory ROM Contents (full cycle of sine values)

yr:$00000400=	$00000000	$3bc90f88	$3c490e90	$3c96c9b6
yr:$00000404=	$3cc90ab0	$3cfb49ba	$3d16c32c	$3d2fe007
yr:$00000408=	$3d48fb30	$3d621469	$3d7b2b74	$3d8a200a
yr:$0000040c=	$3d96a905	$3da3308c	$3dafb680	$3dbc3ac3
yr:$00000410=	$3dc8bd36	$3dd53db9	$3de1bc2e	$3dee3876
yr:$00000414=	$3dfab273	$3e039502	$3e09cf86	$3e1008b7
yr:$00000418=	$3e164083	$3e1c76de	$3e22abb6	$3e28defc
yr:$0000041c=	$3e2f10a2	$3e354098	$3e3b6ecf	$3e419b37
yr:$00000420=	$3e47c5c2	$3e4dee60	$3e541501	$3e5a3997
yr:$00000424=	$3e605c13	$3e667c66	$3e6c9a7f	$3e72b651
yr:$00000428=	$3e78cfcc	$3e7ee6e1	$3e827dc0	$3e8586ce
yr:$0000042c=	$3e888e93	$3e8b9507	$3e8e9a22	$3e919ddd
yr:$00000430=	$3e94a031	$3e97a117	$3e9aa086	$3e9d9e78
yr:$00000434=	$3ea09ae5	$3ea395c5	$3ea68f12	$3ea986c4
yr:$00000438=	$3eac7cd4	$3eaf713a	$3eb263ef	$3eb554ec
yr:$0000043c=	$3eb8442a	$3ebb31a0	$3ebe1d4a	$3ec1071e
yr:$00000440=	$3ec3ef15	$3ec6d529	$3ec9b953	$3ecc9b8b
yr:$00000444=	$3ecf7bca	$3ed25a09	$3ed53641	$3ed8106b
yr:$00000448=	$3edae880	$3eddbe79	$3ee0924f	$3ee363fa
yr:$0000044c=	$3ee63375	$3ee900b7	$3eebcbbb	$3eee9479
yr:$00000450=	$3ef15aea	$3ef41f07	$3ef6e0cb	$3ef9a02d
yr:$00000454=	$3efc5d27	$3eff17b2	$3f00e7e4	$3f0242b1
yr:$00000458=	$3f039c3d	$3f04f484	$3f064b82	$3f07a136
yr:$0000045c=	$3f08f59b	$3f0a48ad	$3f0b9a6b	$3f0cead0
yr:$00000460=	$3f0e39da	$3f0f8784	$3f10d3cd	$3f121eb0
yr:$00000464=	$3f13682a	$3f14b039	$3f15f6d9	$3f173c07
yr:$00000468=	$3f187fc0	$3f19c200	$3f1b02c6	$3f1c420c
yr:$0000046c=	$3f1d7fd1	$3f1ebc12	$3f1ff6cb	$3f212ff9
yr:$00000470=	$3f226799	$3f239da9	$3f24d225	$3f26050a
yr:$00000474=	$3f273656	$3f286605	$3f299415	$3f2ac082

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$00000478=	$3f2beb4a	$3f2d1469	$3f2e3bde	$3f2f61a5
yr:$0000047c=	$3f3085bb	$3f31a81d	$3f32c8c9	$3f33e7bc
yr:$00000480=	$3f3504f3	$3f36206c	$3f373a23	$3f385216
yr:$00000484=	$3f396842	$3f3a7ca4	$3f3b8f3b	$3f3ca003
yr:$00000488=	$3f3daef9	$3f3ebc1b	$3f3fc767	$3f40d0da
yr:$0000048c=	$3f41d870	$3f42de29	$3f43e200	$3f44e3f5
yr:$00000490=	$3f45e403	$3f46e22a	$3f47de65	$3f48d8b3
yr:$00000494=	$3f49d112	$3f4ac77f	$3f4bbbf8	$3f4cae79
yr:$00000498=	$3f4d9f02	$3f4e8d90	$3f4f7a1f	$3f5064af
yr:$0000049c=	$3f514d3d	$3f5233c6	$3f531849	$3f53fac3
yr:$000004a0=	$3f54db31	$3f55b993	$3f5695e5	$3f577026
yr:$000004a4=	$3f584853	$3f591e6a	$3f59f26a	$3f5ac450
yr:$000004a8=	$3f5b941a	$3f5c61c7	$3f5d2d53	$3f5df6be
yr:$000004ac=	$3f5ebe05	$3f5f8327	$3f604621	$3f6106f2
yr:$000004b0=	$3f61c598	$3f628210	$3f633c5a	$3f63f473
yr:$000004b4=	$3f64aa59	$3f655e0b	$3f660f88	$3f66becc
yr:$000004b8=	$3f676bd8	$3f6816a8	$3f68bf3c	$3f696591
yr:$000004bc=	$3f6a09a7	$3f6aab7b	$3f6b4b0c	$3f6be858
yr:$000004c0=	$3f6c835e	$3f6d1c1d	$3f6db293	$3f6e46be
yr:$000004c4=	$3f6ed89e	$3f6f6830	$3f6ff573	$3f708066
yr:$000004c8=	$3f710908	$3f718f57	$3f721352	$3f7294f8
yr:$000004cc=	$3f731447	$3f73913f	$3f740bdd	$3f748422
yr:$000004d0=	$3f74fa0b	$3f756d97	$3f75dec6	$3f764d97
yr:$000004d4=	$3f76ba07	$3f772417	$3f778bc5	$3f77f110
yr:$000004d8=	$3f7853f8	$3f78b47b	$3f791298	$3f796e4e
yr:$000004dc=	$3f79c79d	$3f7a1e84	$3f7a7302	$3f7ac516
yr:$000004e0=	$3f7b14be	$3f7b61fc	$3f7baccd	$3f7bf531
yr:$000004e4=	$3f7c3b28	$3f7c7eb0	$3f7cbfc9	$3f7cfe73
yr:$000004e8=	$3f7d3aac	$3f7d7474	$3f7dabcc	$3f7de0b1
yr:$000004ec=	$3f7e1324	$3f7e4323	$3f7e70b0	$3f7e9bc9
yr:$000004f0=	$3f7ec46d	$3f7eea9d	$3f7f0e58	$3f7f2f9d
yr:$000004f4=	$3f7f4e6d	$3f7f6ac7	$3f7f84ab	$3f7f9c18
yr:$000004f8=	$3f7fb10f	$3f7fc38f	$3f7fd397	$3f7fe129
yr:$000004fc=	$3f7fec43	$3f7ff4e6	$3f7ffb11	$3f7ffec4
yr:$00000500=	$3f800000	$3f7ffec4	$3f7ffb11	$3f7ff4e6
yr:$00000504=	$3f7fec43	$3f7fe129	$3f7fd397	$3f7fc38f
yr:$00000508=	$3f7fb10f	$3f7f9c18	$3f7f84ab	$3f7f6ac7

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$0000050c=	$3f7f4e6d	$3f7f2f9d	$3f7f0e58	$3f7eea9d
yr:$00000510=	$3f7ec46d	$3f7e9bc9	$3f7e70b0	$3f7e4323
yr:$00000514=	$3f7e1324	$3f7de0b1	$3f7dabcc	$3f7d7474
yr:$00000518=	$3f7d3aac	$3f7cfe73	$3f7cbfc9	$3f7c7eb0
yr:$0000051c=	$3f7c3b28	$3f7bf531	$3f7baccd	$3f7b61fc
yr:$00000520=	$3f7b14be	$3f7ac516	$3f7a7302	$3f7a1e84
yr:$00000524=	$3f79c79d	$3f796e4e	$3f791298	$3f78b47b
yr:$00000528=	$3f7853f8	$3f77f110	$3f778bc5	$3f772417
yr:$0000052c=	$3f76ba07	$3f764d97	$3f75dec6	$3f756d97
yr:$00000530=	$3f74fa0b	$3f748422	$3f740bdd	$3f73913f
yr:$00000534=	$3f731447	$3f7294f8	$3f721352	$3f718f57
yr:$00000538=	$3f710908	$3f708066	$3f6ff573	$3f6f6830
yr:$0000053c=	$3f6ed89e	$3f6e46be	$3f6db293	$3f6d1c1d
yr:$00000540=	$3f6c835e	$3f6be858	$3f6b4b0c	$3f6aab7b
yr:$00000544=	$3f6a09a7	$3f696591	$3f68bf3c	$3f6816a8
yr:$00000548=	$3f676bd8	$3f66becc	$3f660f88	$3f655e0b
yr:$0000054c=	$3f64aa59	$3f63f473	$3f633c5a	$3f628210
yr:$00000550=	$3f61c598	$3f6106f2	$3f604621	$3f5f8327
yr:$00000554=	$3f5ebe05	$3f5df6be	$3f5d2d53	$3f5c61c7
yr:$00000558=	$3f5b941a	$3f5ac450	$3f59f26a	$3f591e6a
yr:$0000055c=	$3f584853	$3f577026	$3f5695e5	$3f55b993
yr:$00000560=	$3f54db31	$3f53fac3	$3f531849	$3f5233c6
yr:$00000564=	$3f514d3d	$3f5064af	$3f4f7a1f	$3f4e8d90
yr:$00000568=	$3f4d9f02	$3f4cae79	$3f4bbbf8	$3f4ac77f
yr:$0000056c=	$3f49d112	$3f48d8b3	$3f47de65	$3f46e22a
yr:$00000570=	$3f45e403	$3f44e3f5	$3f43e200	$3f42de29
yr:$00000574=	$3f41d870	$3f40d0da	$3f3fc767	$3f3ebc1b
yr:$00000578=	$3f3daef9	$3f3ca003	$3f3b8f3b	$3f3a7ca4
yr:$0000057c=	$3f396842	$3f385216	$3f373a23	$3f36206c
yr:$00000580=	$3f3504f3	$3f33e7bc	$3f32c8c9	$3f31a81d
yr:$00000584=	$3f3085bb	$3f2f61a5	$3f2e3bde	$3f2d1469
yr:$00000588=	$3f2beb4a	$3f2ac082	$3f299415	$3f286605
yr:$0000058c=	$3f273656	$3f26050a	$3f24d225	$3f239da9
yr:$00000590=	$3f226799	$3f212ff9	$3f1ff6cb	$3f1ebc12
yr:$00000594=	$3f1d7fd1	$3f1c420c	$3f1b02c6	$3f19c200
yr:$00000598=	$3f187fc0	$3f173c07	$3f15f6d9	$3f14b039
yr:$0000059c=	$3f13682a	$3f121eb0	$3f10d3cd	$3f0f8784

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$000005a0=	$3f0e39da	$3f0cead0	$3f0b9a6b	$3f0a48ad
yr:$000005a4=	$3f08f59b	$3f07a136	$3f064b82	$3f04f484
yr:$000005a8=	$3f039c3d	$3f0242b1	$3f00e7e4	$3eff17b2
yr:$000005ac=	$3efc5d27	$3ef9a02d	$3ef6e0cb	$3ef41f07
yr:$000005b0=	$3ef15aea	$3eee9479	$3eebcbbb	$3ee900b7
yr:$000005b4=	$3ee63375	$3ee363fa	$3ee0924f	$3eddbe79
yr:$000005b8=	$3edae880	$3ed8106b	$3ed53641	$3ed25a09
yr:$000005bc=	$3ecf7bca	$3ecc9b8b	$3ec9b953	$3ec6d529
yr:$000005c0=	$3ec3ef15	$3ec1071e	$3ebe1d4a	$3ebb31a0
yr:$000005c4=	$3eb8442a	$3eb554ec	$3eb263ef	$3eaf713a
yr:$000005c8=	$3eac7cd4	$3ea986c4	$3ea68f12	$3ea395c5
yr:$000005cc=	$3ea09ae5	$3e9d9e78	$3e9aa086	$3e97a117
yr:$000005d0=	$3e94a031	$3e919ddd	$3e8e9a22	$3e8b9507
yr:$000005d4=	$3e888e93	$3e8586ce	$3e827dc0	$3e7ee6e1
yr:$000005d8=	$3e78cfcc	$3e72b651	$3e6c9a7f	$3e667c66
yr:$000005dc=	$3e605c13	$3e5a3997	$3e541501	$3e4dee60
yr:$000005e0=	$3e47c5c2	$3e419b37	$3e3b6ecf	$3e354098
yr:$000005e4=	$3e2f10a2	$3e28defc	$3e22abb6	$3e1c76de
yr:$000005e8=	$3e164083	$3e1008b7	$3e09cf86	$3e039502
yr:$000005ec=	$3dfab273	$3dee3876	$3de1bc2e	$3dd53db9
yr:$000005f0=	$3dc8bd36	$3dbc3ac3	$3dafb680	$3da3308c
yr:$000005f4=	$3d96a905	$3d8a200a	$3d7b2b74	$3d621469
yr:$000005f8=	$3d48fb30	$3d2fe007	$3d16c32c	$3cfb49ba
yr:$000005fc=	$3cc90ab0	$3c96c9b6	$3c490e90	$3bc90f88
yr:$00000600=	$80000000	$bbc90f88	$bc490e90	$bc96c9b6
yr:$00000604=	$bcc90ab0	$bcfb49ba	$bd16c32c	$bd2fe007
yr:$00000608=	$bd48fb30	$bd621469	$bd7b2b74	$bd8a200a
yr:$0000060c=	$bd96a905	$bda3308c	$bdafb680	$bdbc3ac3
yr:$00000610=	$bdc8bd36	$bdd53db9	$bde1bc2e	$bdee3876
yr:$00000614=	$bdfab273	$be039502	$be09cf86	$be1008b7
yr:$00000618=	$be164083	$be1c76de	$be22abb6	$be28defc
yr:$0000061c=	$be2f10a2	$be354098	$be3b6ecf	$be419b37
yr:$00000620=	$be47c5c2	$be4dee60	$be541501	$be5a3997
yr:$00000624=	$be605c13	$be667c66	$be6c9a7f	$be72b651
yr:$00000628=	$be78cfcc	$be7ee6e1	$be827dc0	$be8586ce
yr:$0000062c=	$be888e93	$be8b9507	$be8e9a22	$be919ddd
yr:$00000630=	$be94a031	$be97a117	$be9aa086	$be9d9e78

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$00000634=	$bea09ae5	$bea395c5	$bea68f12	$bea986c4
yr:$00000638=	$beac7cd4	$beaf713a	$beb263ef	$beb554ec
yr:$0000063c=	$beb8442a	$bebb31a0	$bebe1d4a	$bec1071e
yr:$00000640=	$bec3ef15	$bec6d529	$bec9b953	$becc9b8b
yr:$00000644=	$becf7bca	$bed25a09	$bed53641	$bed8106b
yr:$00000648=	$bedae880	$beddbe79	$bee0924f	$bee363fa
yr:$0000064c=	$bee63375	$bee900b7	$beebcbbb	$beee9479
yr:$00000650=	$bef15aea	$bef41f07	$bef6e0cb	$bef9a02d
yr:$00000654=	$befc5d27	$beff17b2	$bf00e7e4	$bf0242b1
yr:$00000658=	$bf039c3d	$bf04f484	$bf064b82	$bf07a136
yr:$0000065c=	$bf08f59b	$bf0a48ad	$bf0b9a6b	$bf0cead0
yr:$00000660=	$bf0e39da	$bf0f8784	$bf10d3cd	$bf121eb0
yr:$00000664=	$bf13682a	$bf14b039	$bf15f6d9	$bf173c07
yr:$00000668=	$bf187fc0	$bf19c200	$bf1b02c6	$bf1c420c
yr:$0000066c=	$bf1d7fd1	$bf1ebc12	$bf1ff6cb	$bf212ff9
yr:$00000670=	$bf226799	$bf239da9	$bf24d225	$bf26050a
yr:$00000674=	$bf273656	$bf286605	$bf299415	$bf2ac082
yr:$00000678=	$bf2beb4a	$bf2d1469	$bf2e3bde	$bf2f61a5
yr:$0000067c=	$bf3085bb	$bf31a81d	$bf32c8c9	$bf33e7bc
yr:$00000680=	$bf3504f3	$bf36206c	$bf373a23	$bf385216
yr:$00000684=	$bf396842	$bf3a7ca4	$bf3b8f3b	$bf3ca003
yr:$00000688=	$bf3daef9	$bf3ebc1b	$bf3fc767	$bf40d0da
yr:$0000068c=	$bf41d870	$bf42de29	$bf43e200	$bf44e3f5
yr:$00000690=	$bf45e403	$bf46e22a	$bf47de65	$bf48d8b3
yr:$00000694=	$bf49d112	$bf4ac77f	$bf4bbbf8	$bf4cae79
yr:$00000698=	$bf4d9f02	$bf4e8d90	$bf4f7a1f	$bf5064af
yr:$0000069c=	$bf514d3d	$bf5233c6	$bf531849	$bf53fac3
yr:$000006a0=	$bf54db31	$bf55b993	$bf5695e5	$bf577026
yr:$000006a4=	$bf584853	$bf591e6a	$bf59f26a	$bf5ac450
yr:$000006a8=	$bf5b941a	$bf5c61c7	$bf5d2d53	$bf5df6be
yr:$000006ac=	$bf5ebe05	$bf5f8327	$bf604621	$bf6106f2
yr:$000006b0=	$bf61c598	$bf628210	$bf633c5a	$bf63f473
yr:$000006b4=	$bf64aa59	$bf655e0b	$bf660f88	$bf66becc
yr:$000006b8=	$bf676bd8	$bf6816a8	$bf68bf3c	$bf696591
yr:$000006bc=	$bf6a09a7	$bf6aab7b	$bf6b4b0c	$bf6be858
yr:$000006c0=	$bf6c835e	$bf6d1c1d	$bf6db293	$bf6e46be
yr:$000006c4=	$bf6ed89e	$bf6f6830	$bf6ff573	$bf708066

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$000006c8=	$bf710908	$bf718f57	$bf721352	$bf7294f8
yr:$000006cc=	$bf731447	$bf73913f	$bf740bdd	$bf748422
yr:$000006d0=	$bf74fa0b	$bf756d97	$bf75dec6	$bf764d97
yr:$000006d4=	$bf76ba07	$bf772417	$bf778bc5	$bf77f110
yr:$000006d8=	$bf7853f8	$bf78b47b	$bf791298	$bf796e4e
yr:$000006dc=	$bf79c79d	$bf7a1e84	$bf7a7302	$bf7ac516
yr:$000006e0=	$bf7b14be	$bf7b61fc	$bf7baccd	$bf7bf531
yr:$000006e4=	$bf7c3b28	$bf7c7eb0	$bf7cbfc9	$bf7cfe73
yr:$000006e8=	$bf7d3aac	$bf7d7474	$bf7dabcc	$bf7de0b1
yr:$000006ec=	$bf7e1324	$bf7e4323	$bf7e70b0	$bf7e9bc9
yr:$000006f0=	$bf7ec46d	$bf7eea9d	$bf7f0e58	$bf7f2f9d
yr:$000006f4=	$bf7f4e6d	$bf7f6ac7	$bf7f84ab	$bf7f9c18
yr:$000006f8=	$bf7fb10f	$bf7fc38f	$bf7fd397	$bf7fe129
yr:$000006fc=	$bf7fec43	$bf7ff4e6	$bf7ffb11	$bf7ffec4
yr:$00000700=	$bf800000	$bf7ffec4	$bf7ffb11	$bf7ff4e6
yr:$00000704=	$bf7fec43	$bf7fe129	$bf7fd397	$bf7fc38f
yr:$00000708=	$bf7fb10f	$bf7f9c18	$bf7f84ab	$bf7f6ac7
yr:$0000070c=	$bf7f4e6d	$bf7f2f9d	$bf7f0e58	$bf7eea9d
yr:$00000710=	$bf7ec46d	$bf7e9bc9	$bf7e70b0	$bf7e4323
yr:$00000714=	$bf7e1324	$bf7de0b1	$bf7dabcc	$bf7d7474
yr:$00000718=	$bf7d3aac	$bf7cfe73	$bf7cbfc9	$bf7c7eb0
yr:$0000071c=	$bf7c3b28	$bf7bf531	$bf7baccd	$bf7b61fc
yr:$00000720=	$bf7b14be	$bf7ac516	$bf7a7302	$bf7a1e84
yr:$00000724=	$bf79c79d	$bf796e4e	$bf791298	$bf78b47b
yr:$00000728=	$bf7853f8	$bf77f110	$bf778bc5	$bf772417
yr:$0000072c=	$bf76ba07	$bf764d97	$bf75dec6	$bf756d97
yr:$00000730=	$bf74fa0b	$bf748422	$bf740bdd	$bf73913f
yr:$00000734=	$bf731447	$bf7294f8	$bf721352	$bf718f57
yr:$00000738=	$bf710908	$bf708066	$bf6ff573	$bf6f6830
yr:$0000073c=	$bf6ed89e	$bf6e46be	$bf6db293	$bf6d1c1d
yr:$00000740=	$bf6c835e	$bf6be858	$bf6b4b0c	$bf6aab7b
yr:$00000744=	$bf6a09a7	$bf696591	$bf68bf3c	$bf6816a8
yr:$00000748=	$bf676bd8	$bf66becc	$bf660f88	$bf655e0b
yr:$0000074c=	$bf64aa59	$bf63f473	$bf633c5a	$bf628210
yr:$00000750=	$bf61c598	$bf6106f2	$bf604621	$bf5f8327
yr:$00000754=	$bf5ebe05	$bf5df6be	$bf5d2d53	$bf5c61c7
yr:$00000758=	$bf5b941a	$bf5ac450	$bf59f26a	$bf591e6a

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$0000075c=	$bf584853	$bf577026	$bf5695e5	$bf55b993
yr:$00000760=	$bf54db31	$bf53fac3	$bf531849	$bf5233c6
yr:$00000764=	$bf514d3d	$bf5064af	$bf4f7a1f	$bf4e8d90
yr:$00000768=	$bf4d9f02	$bf4cae79	$bf4bbbf8	$bf4ac77f
yr:$0000076c=	$bf49d112	$bf48d8b3	$bf47de65	$bf46e22a
yr:$00000770=	$bf45e403	$bf44e3f5	$bf43e200	$bf42de29
yr:$00000774=	$bf41d870	$bf40d0da	$bf3fc767	$bf3ebc1b
yr:$00000778=	$bf3daef9	$bf3ca003	$bf3b8f3b	$bf3a7ca4
yr:$0000077c=	$bf396842	$bf385216	$bf373a23	$bf36206c
yr:$00000780=	$bf3504f3	$bf33e7bc	$bf32c8c9	$bf31a81d
yr:$00000784=	$bf3085bb	$bf2f61a5	$bf2e3bde	$bf2d1469
yr:$00000788=	$bf2beb4a	$bf2ac082	$bf299415	$bf286605
yr:$0000078c=	$bf273656	$bf26050a	$bf24d225	$bf239da9
yr:$00000790=	$bf226799	$bf212ff9	$bf1ff6cb	$bf1ebc12
yr:$00000794=	$bf1d7fd1	$bf1c420c	$bf1b02c6	$bf19c200
yr:$00000798=	$bf187fc0	$bf173c07	$bf15f6d9	$bf14b039
yr:$0000079c=	$bf13682a	$bf121eb0	$bf10d3cd	$bf0f8784
yr:$000007a0=	$bf0e39da	$bf0cead0	$bf0b9a6b	$bf0a48ad
yr:$000007a4=	$bf08f59b	$bf07a136	$bf064b82	$bf04f484
yr:$000007a8=	$bf039c3d	$bf0242b1	$bf00e7e4	$beff17b2
yr:$000007ac=	$befc5d27	$bef9a02d	$bef6e0cb	$bef41f07
yr:$000007b0=	$bef15aea	$beee9479	$beebcbbb	$bee900b7
yr:$000007b4=	$bee63375	$bee363fa	$bee0924f	$beddbe79
yr:$000007b8=	$bedae880	$bed8106b	$bed53641	$bed25a09
yr:$000007bc=	$becf7bca	$becc9b8b	$bec9b953	$bec6d529
yr:$000007c0=	$bec3ef15	$bec1071e	$bebe1d4a	$bebb31a0
yr:$000007c4=	$beb8442a	$beb554ec	$beb263ef	$beaf713a
yr:$000007c8=	$beac7cd4	$bea986c4	$bea68f12	$bea395c5
yr:$000007cc=	$bea09ae5	$be9d9e78	$be9aa086	$be97a117
yr:$000007d0=	$be94a031	$be919ddd	$be8e9a22	$be8b9507
yr:$000007d4=	$be888e93	$be8586ce	$be827dc0	$be7ee6e1
yr:$000007d8=	$be78cfcc	$be72b651	$be6c9a7f	$be667c66
yr:$000007dc=	$be605c13	$be5a3997	$be541501	$be4dee60
yr:$000007e0=	$be47c5c2	$be419b37	$be3b6ecf	$be354098
yr:$000007e4=	$be2f10a2	$be28defc	$be22abb6	$be1c76de
yr:$000007e8=	$be164083	$be1008b7	$be09cf86	$be039502
yr:$000007ec=	$bdfab273	$bdee3876	$bde1bc2e	$bdd53db9

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Table B-2 Y Memory ROM Contents (full cycle of sine values) (Continued)

yr:$000007f0=	$bdc8bd36	$bdbc3ac3	$bdafb680	$bda3308c
yr:$000007f4=	$bd96a905	$bd8a200a	$bd7b2b74	$bd621469
yr:$000007f8=	$bd48fb30	$bd2fe007	$bd16c32c	$bcfb49ba
yr:$000007fc=	$bcc90ab0	$bc96c9b6	$bc490e90	$bbc90f88

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