

Field-Programmable Gate Arrays

Pierre Marchal

Field-programmable gate arrays (FPGAs) are integrated circuits, which constitute the "new kid in town" where digital hardware technology is concerned. An FPGA is an array of logic blocks (cells) placed in an infrastructure of interconnections, which can be programmed at three distinct levels (see Figure 1): (1) the function of the logic cells, (2) the interconnections between cells, and (3) the inputs and outputs. All three levels are configured via a string of bits that is loaded from an external source, either once or several times. In the latter case the FPGA is considered *reconfigurable*. FPGAs are highly versatile devices that offer the designer a wide range of design choices and options. However, this potential power necessitates a suite of tools in order to design a system. Essentially, these tools generate the configuration bit string, given such inputs as a logic diagram or a high-level functional description. Our focus here is on the hardware aspect of digital FPGAs; we shall not treat such issues as programming tools and analog FPGAs [4, 5].

FPGAs enable engineers to mitigate the effects entailed by the well-known tradeoff in computing between cost and performance. When one sets about implementing a certain computational task, obtaining the highest performance (speed) is inarguably achieved by constructing a specialized machine, that is, hardware. This possibility exists, for example, in the form of application-specific integrated circuits (ASICs); however, the price per application as well as the turnaround time (from design to actual operation) are both quite prohibitive. On the whole, the computing industry has opted for general-purpose computing, which trades maximum speed for much lower design and implementation costs. A general-purpose processor can be easily and quickly instructed to change its task, say, from word processing to number crunching. This ability is made possible since such a processor is *programmable*; nonetheless, programming (and reprogramming) does not change the processor's hardware. An FPGA is *programmable at*

the hardware level, thus combining the advantages of both general-purpose processors and specialized circuits.

Types of FPGAs

As shown in Figure 2, there are four classes of FPGAs, based on the way they are configured. *Configurable* circuits can only be configured once (by the user), after which no further changes are effected (for this reason they are also known as one-time programmable). *Reconfigurable* circuits can be configured several times, and are divided into two sub-classes: static and dynamic [2]. With static circuits the configuration string is loaded once at the outset, after which the task in question is executed with no further hardware changes taking place. With *dynamic* reconfigurable circuits the underlying hardware may change at any point dur-

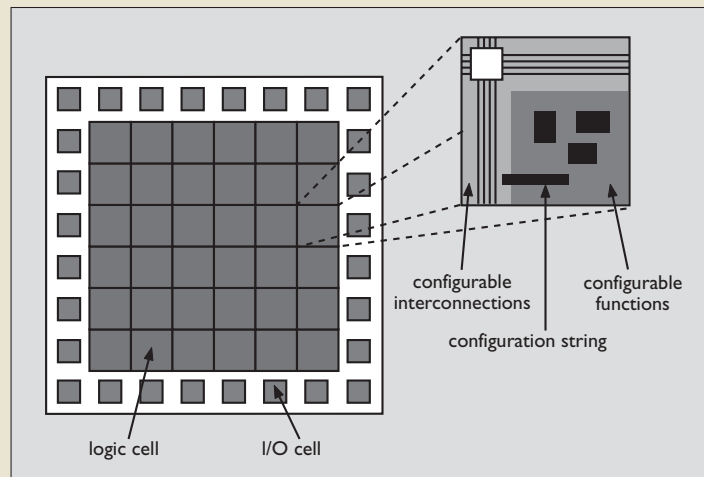


Figure 1. A schematic diagram of a field-programmable gate array (FPGA). An FPGA is an array of logic cells placed in an infrastructure of interconnections, which can be programmed at three distinct levels.

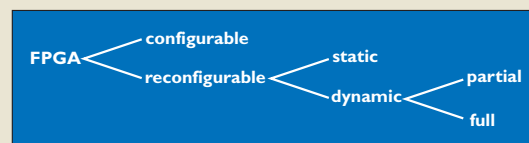


Figure 2. A classification of FPGAs, based on the way configuration is performed.

Company	Family	Granularity	Configuration Mode	Cell Count
Actel	MX	fine-grained	configurable	295–2,438
Altera	FLEX10KE	coarse-grained	static	6,656–12,160
Atmel	AT40K	fine-grained	partially reconfigurable	256–2,304
Dynachip	DL6000	coarse-grained	partially reconfigurable	265–3,136
Gatefield	GF260F	fine-grained	static	5,400–6,200
Lucent	ORCA 2C/2T	coarse-grained	static	100–900
QuickLogic	pASIC2	fine-grained	configurable	192–672
Xilinx	XC4000XLA/XV	coarse-grained	static	576–8,464

Table 1. Major FPGA manufacturers, along with characteristics of their product lines (note that for each family of products, there are circuits with different cell counts; the table lists the minimal and maximal values).

Parameter	1985	1998	Ratio
Transistor width	3 microns	0.25 micron	12
Die size	25mm ²	400mm ²	16
Clock frequency	20MHz	350MHz	17
Pins per package	48	630	13
Number of cells	64	1,368	21
Size of configuration string (in bits)	11,360	5,433,888	478
Power supply	5 volts	2.5 volts	2

Table 2.
Evolution
of FPGA
technology.

ing the task's execution. Dynamic circuits are further divided into *fully reconfigurable* devices, in which the whole circuit is reconfigured, and *partially reconfigurable* devices, in which only part of the circuit is reconfigured. A further distinction in the domain of FPGAs is between *fine-grained* circuits, in which the basic cell is simple (OR, AND, and NOT), and *coarse-grained* circuits, in which the basic cell is more complex (multiplexers, lookup tables, and arithmetic and logic units). Table 1 lists the major FPGA manufacturers, along with characteristics of their product lines.

The first family of FPGAs was introduced by Xilinx in 1985 and, as shown in Table 2, the technology has evolved considerably since then. With the era of deep submicron technology now upon us, a huge number of transistors can be placed on a single chip.¹ Managing such high-complexity circuits is quite complicated where ASICs are concerned, while FPGAs, with their regular structure, are easier

to handle (for example, automatic synthesis software tools are more easily used with FPGAs as compared to ASICs).

What We Can Expect from Future FPGAs

In order to solve a number of problems with extant architectures (low resource utilization, routing congestion, high interconnect delays, and insufficient I/O connections) researchers are looking into the possibility of stacking two-dimensional FPGA circuits so as to obtain three-dimensional structures. Another important issue is that of dynamic (run time) reconfiguration, which is currently resource-intensive. For example, as shown in Table 2, the most advanced FPGA circuits to date require a configuration string containing millions of bits; if one wishes to maintain dozens (or even hundreds) of

¹Submicron technology refers to circuits with transistor widths between 0.5–1 micron, while deep submicron technology involves transistor widths below 0.25 micron.

different configuration strings simultaneously, and switch between them dynamically, a huge memory is required—which is currently beyond our technological capabilities. Future FPGAs will need to overcome this obstacle.

Another development that can be expected to occur is the combination of general-purpose technology with reconfigurable technology, giving rise to two types of architectures: standard, general-purpose processor chips, equipped with a reconfigurable surface, and FPGA-like devices, in which the basic cell is a general-purpose processor (for example, the field-programmable processors arrays—FPFAs—described in [1]). Finally, while extant FPGAs use cells executing basic logic operations (AND and OR), an important research avenue is that of cells that execute mathematical operations [3] (adders, multipliers, dividers, and square rooters). These latter circuits require fewer resources, while facilitating the programming of complex operations (as an example, consider the division of two numbers, which might take up the entire surface of a logic-based FPGA chip; with these novel, mathematical-based chips, only a small portion of the FPGA would be used up).

The field of FPGAs is continually sprouting new offshoots, and the future shall probably see a plethora of exciting new developments and applications—not the least of which are in the field of evolvable hardware. **C**

REFERENCES

1. Girau, B., Marchal, P., Nussbaum, P., Tisserand, A., and Restrepo, F. Evolvable platform for array processing: a one-chip approach. In *Proceedings of MicroNeuro'99, 7th International Conference on Microelectronics for Neural, Fuzzy, and Bio-inspired Systems*. (Granada, Spain), 1999.
2. Sanchez, E., Sipper, M., Haenni, J.-O., Beuchat, J.-L., Stauffer, A. and Pérez-Urbe, A. Static and dynamic configurable systems. *IEEE Transactions on Computers*. To appear.
3. Tisserand, A., Marchal, P., and Piguet, C. An on-line arithmetic based FPGA for low-power custom computing. In *Proceedings of FCCM'99, 7th Annual IEEE Symposium on Field Programmable Custom Computing Machines* (Napa, CA), 1999.
4. Trimberger, S.M. *Field-Programmable Gate Array Technology*. Kluwer Academic Publishers, Boston, 1994.
5. Villasenor, J., and Mangione-Smith, W.H. Configurable computing. *Scientific American* 207, 6 (1997), 54–59.

PIERRE MARCHAL (pierre.marchal@csem.ch) is a staff scientist with the Centre Suisse d'Electronique et de Microtechnique SA in Switzerland; www.csem.ch

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