

Designing a Radiation Hardened 8051-like Micro-controller

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Abstract

This paper presents a prototype of a hardened version of the 8051 micro-controller, able to assure reliable operation in the presence of bit flips caused by radiation. Aiming at avoiding such faults in the 8051 micro-controller, Hamming code protection was used in its SRAM memory and registers. This paper shows implementation details of this technique in the micro-controller VHDL description and the impact on the area device.

1. Introduction

The constant improvement achieved in microelectronics technology, in the last 20 years, allows the manufacturing of very complex circuits performing the operation of boards or even computers of the past. Processor-like circuits, on a direct consequence of the integration technology availability, have made a dramatic impact in the way systems are designed. The concept of an application specific system including microprocessors covers a wide range of applications, from portable systems to dedicated embedded control devices or computers.

Military, avionics and aerospace applications utilize advanced electronic systems with microprocessors in order to meet spacecraft requirements such as physical volume, weight, power and cost. Fault-tolerance has always been an essential attribute of these systems, to keep them operational in such hostile environment.

Digital circuits operating in space are subject to different kinds of radiation, which effects can be permanent or transient [1]. The space radiation environment consists of various particles that may interact with digital microelectronic devices causing undesirable effects. Particles of concern are electrons, protons, photons, alpha particles and heavier ions. Permanent effects result of particles trapped at the silicon/oxide interfaces, and they happen only after a certain period of

exposure to radiation. On the other hand, transient effects may be provoked by the impact of a single charged particle (Single Event Effects, SEE) in sensitive circuit zones. According to the impact location, two kind of SEEs are distinguished: SEUs (Single Event Upsets) and SELs (Single Event Latchups). SEUs are responsible for transient changes in bits of information stored within an integrated circuit. SEUs are a major concern in space environment, and have also been observed on the earth atmosphere as the result of interactions of neutrons [2]. SELs result from the triggering of parasitic transistors presented in CMOS technology, and they provoke short circuits, capable to damage the component by thermal effect if the circuit is not powered-off at time.

The consequences of SEUs depend on the nature of the perturbed information, ranging from erroneous results to system crashes. For complex circuits like DSP processors, co-processors, or micro-controllers, the sensitivity to SEUs correlates strongly with the amount of internal memory (registers, memory bits, flip-flops, etc).

Fault tolerance techniques attempt to improve reliability by reducing the occurrence of faults. Radiation hardening using specific process technology is an expensive process and, when used for a low-volume production, will lead to very costly parts. The need for low-cost, state-of-the-art high performance computing systems in these areas has been pushing researchers to investigate new fault-tolerance technique applications.

This paper presents a radiation hardened version of the 8051 micro-controller designed with a VHDL description. The choice of this micro-controller was based on the fact that it is widely used in space applications, and consequently, large amount of data about its behavior under radiation is available. Besides, its hardening makes possible the reuse and protection of all systems that are already running based on it. The area of the microprocessor sensitive to SEU transient errors has been protected using the Hamming code technique [8]. This

technique is mainly based on the inclusion of error detecting and correcting capabilities.

A board implementation has been done with the robust 8051. The hardened description was prototyped into three programmable logic devices customizable by EEPROM technology. This board is being verified using a dedicated tester to analyze the capabilities of this technique.

Field Programmable Gate Arrays (FPGAs) based on SRAM technology are largely used to prototype digital systems due to their high-density, performance and fast turnaround time. However, SRAM elements are strongly sensitive to SEU. Aiming at avoiding the radiation effects in the 8051 prototype, such as bit flips in the chip customization, programmable logic devices (PLDs) customizable by EEPROM were used (these memories are known to be insensitive to radiation).

The paper is organized as follows: in section 2 the architecture of the 8051 is presented. In section 3, the implementation of the Hamming Code fault tolerance technique is described. The prototype of the fault tolerant 8051 is shown in section 4 with the experimental results concerning area overhead. This section also explains the radiation tester procedure using THESIC. Concluding remarks and future work are given in section 5.

2 The 8051 VHDL Description

The MSC8051 [3] VHDL description presented in [4, 5] was re-used to insert SEU radiation fault tolerant structures. The original code is entirely compatible with the INTEL 8051 microprocessor in terms of instruction timing. It contains 24 instructions that are executed in 12 or 24 clock periods. Although the insertion of new instructions is quite easy, only the instructions required by the target application are being used in this description.

The microprocessor description is divided into six main blocks, illustrated in figure 1. These units are finite state machine, control unit, validation unit, datapath and RAM and ROM memories. The Finite State Machine (FSM) block generates the states and number of cycles for each instruction to guide the circuit operation. It has a very simple combinational logic and a set of flip-flops. The control unit generates some control signals for the datapath, and it is basically composed of multiplexors. The validation unit generates the microcode word for each instruction, and it is also basically composed of multiplexors. The datapath includes an Arithmetic Logic Unit (ALU) and 12 registers (accumulator, PC, bus-like register, PC_2, RAM address, output, ALU register, Stack Pointer, alu_2 register, instruction register, ROM address and ALU output).

The original version of the 8051 developed in VHDL includes both RAM and ROM memories. This version can be implemented in FPGAs with embedded memory blocks.

However, the RAM and ROM memories can be defined as external to the microprocessor too.

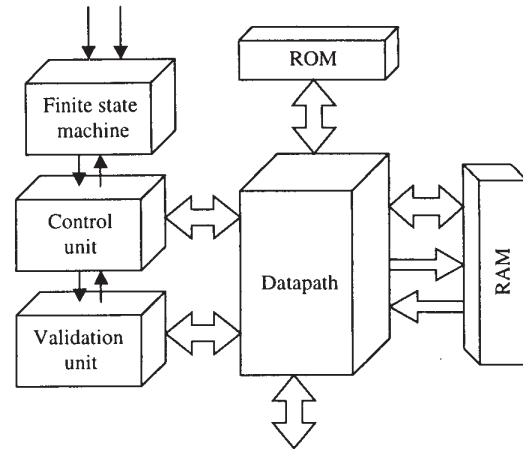


Figure 1 - General Scheme of the available 8051

A previous study [6] presented an at-speed self-testable version of this micro-controller in terms of permanent faults by inserting, in each 8051 unit, a specific built-in self-test structure. A study of the radiation effects in the 8051 architecture has been also done in [7], to detect the most vulnerable micro-controller units. Experimental results based on fault injection confirmed that transient faults (SEU) affect mainly the internal RAM memory. According to these results, the 8051 VHDL description was modified and fault tolerance technique based on Hamming code protection was included in the internal memory and also in internal registers from datapath and control unit. All these improvements are addressed in the next section.

3 Fault Tolerance Technique Implementation

Micro-controllers operating in the space environment can be affected by SEU. Thus, the memory cells and registers included in microprocessors must be protected to avoid potential transient errors. The technique used in this work to detect and correct faults in the 8051 memory cells (registers or RAM cells) consists on codifying each memory element by Hamming code [8], and to perform the verification of the stored word every time this memory point is accessed.

Hamming code is an error-detecting and error-correcting binary code that can detect all single and double-bit errors and correct all single-bit errors on an n -bit word. A Hamming code satisfies the relation $2^m \geq n + 1$, where n is the total number of bits in the data, k is the number of information bits in the data, and m is the number of check bits in the data, where $m = n - k$. The use of Error Detection and Correction (EDAC) schemes such as Hamming code is already common among current solid-

state recorders flying in space. This coding method is recommended for systems with low probabilities of multiple errors in a single data structure (e.g., only a single bit error in a byte of data).

In order to implement the Hamming code, two combinational components were described in VHDL and

used as a package in the 8051 VHDL description. The first component receives an 8-bit data and returns a 12-bit coded word. The second component receives a 12-bit word and returns an 8-bit decoded and corrected data. This structure is presented in figure 2.

```

FUNCTION hamming_code (data_in:word)
RETURN codedbyte IS
VARIABLE coded: codedbyte ;
BEGIN
coded(9) := data_in(7);
coded(7) := data_in(6);
coded(6) := data_in(5);
coded(5) := data_in(4);
coded(3) := data_in(3);
coded(2) := data_in(2);
coded(1) := data_in(1);
coded(0) := data_in(0);
coded(11) := data_in(7) XOR data_in(6) XOR data_in(4) XOR
data_in(3) XOR data_in(1);
coded(10) := data_in(7) XOR data_in(5) XOR data_in(4) XOR
data_in(2) XOR data_in(1);
coded(8) := data_in(6) XOR data_in(5) XOR data_in(4) XOR
data_in(0);
coded(4) := data_in(3) XOR data_in(2) XOR data_in(1) XOR
data_in(0);
return coded;
END;

FUNCTION hamming_decode(data_in:codedbyte)
RETURN palavra IS
VARIABLE coded, mask : codedbyte ;
VARIABLE decoded_out : palavra;
VARIABLE codigo : codeword;
BEGIN
codigo(0):=data_in(11) XOR data_in(9) XOR data_in(7) XOR
data_in(5) XOR data_in(3) XOR data_in(1);
codigo(1):=data_in(10) XOR data_in(9) XOR data_in(6) XOR
data_in(5) XOR data_in(2) XOR data_in(1);

codigo(2) := data_in(8) XOR data_in(7) XOR data_in(6) XOR
data_in(5) XOR data_in(0);
codigo(3) := data_in(4) XOR data_in(3) XOR data_in(2) XOR
data_in(1) XOR data_in(0);

CASE codigo IS
WHEN B"0001" => mask := B"100000000000";
WHEN B"0010" => mask := B"010000000000";
WHEN B"0011" => mask := B"001000000000";
WHEN B"0100" => mask := B"000100000000";
WHEN B"0101" => mask := B"000010000000";
WHEN B"0110" => mask := B"000001000000";
WHEN B"0111" => mask := B"000000100000";
WHEN B"1000" => mask := B"000000010000";
WHEN B"1001" => mask := B"000000001000";
WHEN B"1010" => mask := B"000000000100";
WHEN B"1011" => mask := B"000000000010";
WHEN B"1100" => mask := B"000000000001";
WHEN OTHERS => mask := B"000000000000";
END CASE;

coded := data_in XOR mask;
decoded_out(7) := coded(9);
decoded_out(6) := coded(7);
decoded_out(5) := coded(6);
decoded_out(4) := coded(5);
decoded_out(3) := coded(3);
decoded_out(2) := coded(2);
decoded_out(1) := coded(1);
decoded_out(0) := coded(0);
RETURN decoded_out;
END;

```

Figure 2 - Hamming Functions implemented in VHDL

Four structures in the 8051 VHDL description have been protected by Hamming Code: the Finite State Machine, the RAM memory, the Control unit and the Datapath. These blocks contain memory cells that can be affected by SEU radiation effects. The Validation unit is a completely combinational structure and in principle it is not subject to bit flips, making no necessary protection schemes for it. The ROM block is also immune to these faults, since its content can not be modified. Figure 3 shows the new 8051 scheme. The blocks in bold include the Hamming code protection. VHDL simulations have been used to check the correct Hamming code implementation.

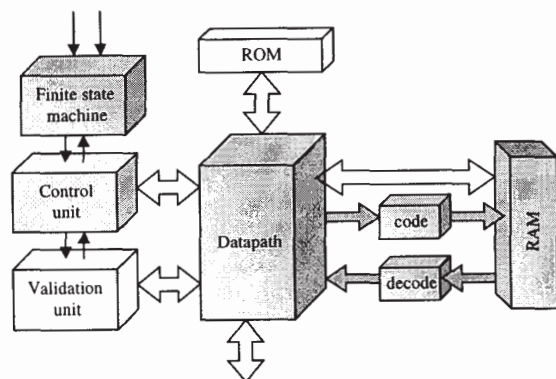


Figure 3 - 8051 with RAM tolerant to transient faults

3.1 Transient Fault Detection and Correction in SRAM memory

Instances of code and decode functions presented in Figure 2 were used to detect and correct transient faults in the SRAM 8051 memory. In the memory access protection, all data words are coded before being stored in the RAM memory, and all memory words are decoded (and possibly corrected) before being used in an operation.

3.2 Transient Fault Detection and Correction in Finite State Machine

The finite state machine (FSM) of 8051 has 24 states, which have been represented by a 5-bit register to form the next state of the machine. This register must be protected by Hamming code to avoid errors under radiation. This technique uses two packages functions, one called coded with 5 bits input and 9 bits output, and other called decoded with 9 bits inputs and 5 bits outputs. Its structure is similar to the packages previously described. This new structure is shown in figure 4.

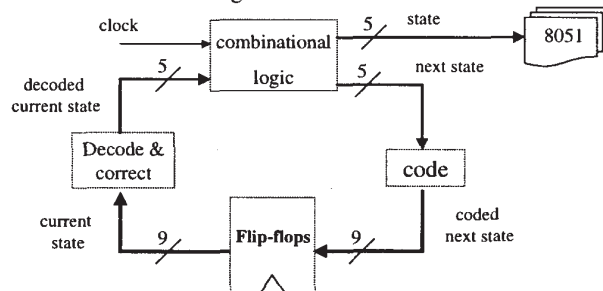


Figure 4 – Fault Tolerant Finite State Machine Scheme

In the new FSM, the next state is coded before being stored, and decoded before being used in the control unit. In case of occurrence of a transient fault, the error is corrected. Since coding and decoding operations are completely combinational, there is no difference in terms of machine cycles needed for an operation. Although the register sensitive area is much smaller than the internal RAM memory, the effects of a bit flip in this register can be very hazardous for the system.

3.3 Transient Fault Detection and Correction in Datapath and Control Registers

The same component models for coding and decoding used in the memory were also used to protect the registers in the datapath and in the control unit. Two registers have been protected in the Datapath, the accumulator and the program counter. The other registers: bus-like register, PC_2, RAM address, output register, ALU register, Stack Pointer, alu_2 register, instruction register, ROM address

and ALU output were replaced by combinational signals in the internal chip bus. In the control unit the instruction register and the interruption latches were protected.

4 Prototyping the Fault Tolerant 8051-like Micro-controller

The use of presently available high-density programmable circuits such as Field Programmable Gate Arrays (FPGAs) and Programmable Logic Devices (PLDs) is an attractive approach to fast prototyping and reducing cost. There are several ways to customize these chips: using SRAM, antifuse or EEPROM technology.

FPGAs based on SRAM are the most popular programmable devices, and they offer very high-density and performance. However, the SRAM cells are strongly sensitive to SEU and SEU mitigate solutions must be used to avoid transient errors under radiation. In other words, to implement a version of a transient errors protected micro-controller in a FPGA based on SRAM, it is necessary not only to design a robust microprocessor, but even to use some SEU mitigate solutions such as TMR (Triple Modular Redundancy) inside the programming bits of the chip.

PLDs customizable by EEPROM have been chosen to implement the first prototype of the fault tolerant 8051 micro-controller, since EPROM elements are not so radiation sensitive as SRAM programmable memories cells used in FPGAs. In such way, device customization has less chance to be affected by the radiation environment and the fault tolerant 8051 implementation can be tested by itself.

The fault tolerant 8051 was implemented in an Altera PLD [9], family MAX 9000. This version of the 8051 uses three chips, one EPM9560 with 208 pins and two EPM9400 with 84 pins. The EPM9400 has 580 flip-flops and 25 Logic Array Blocks (LABs) composed of 400 macrocells in total. The EPM9560 has 560 logic cells. The macrocell consists of three functional blocks: the product terms, the products select matrix and the programmable register. The macrocell can be individually configured for both sequential and combinational operation. The combinational logic is implemented in the local array, which provides five product terms per macrocell.

Table 1 shows the results of the robust 8051 prototyped into the PLD MAX9000 family and into the FPGA FLEX10K family from Altera.

The family FLEX10K has higher density comparing to MAX9000, however it is strongly sensitive to SEU effects due to their SRAM based customization. For this reason the FLEX 10K was not used to implement the 8051 prototype.

Table 1 – Results of robust 8051-like Micro-Controller implemented Programmable Logic Devices from Altera

Micro-controller Unit	# inputs	# output	MAX9000 family			FLEX10K family	# flip-flops
			# LABs	# expanders	# prd-terms	# LCs	
Code package (8 bits)	8	12	14	6	38	14	0
Decode package (12 bits)	12	8	18	8	60	24	0
Code package (5 bits)	5	9	9	1	17	9	0
Decoded package (9 bits)	9	5	15	13	61	12	0
State_g (1)	3	5	10	3	30	75	5
State_g (2)	3	5	106	67	405	111	18
Valida (1)	14	30	103	51	363	305	0
Control (1)	15	14	23	11	81	74	11
Control (2)	15	14	56	27	205	113	17
Datapath (2)	44	27	299	153	1160	437	16
Datapath (2)	46	29	493	265	1819	543	24
8051 (1)(3)	3	3				911	32
8051 (2)(3)	3	3				1065	59

(1) Original 8051 description (2) Hamming code protected 8051 description (3) memory described inside the chip

A board composed of the PLDs, the RAM and ROM memories and a logic interface was built. It is presented in figure 5. This board is going to be tested in the THESIC tester environment [10] under radiation ground test. The first tested in The French Aeronautics and Space Research Center (ONERA).

The radiation ground test consists in exposing the SEU hardened 8051 board, while it carries out a given activity, to an appropriate particle beam. Such on-line testing needs: a particle beam, a test methodology, defining the activity of the device under test (DUT) and an electronic test equipment for controlling and observing the behavior of the DUT during its exposition to radiation that is THESIC. The particle beam can be obtained by Radiation Facilities such as particle accelerators: cyclotron, linear accelerators and synchrotron equipment based on fission decay sources such as Cf^{252} .

The THESIC [10] system (Testbed for Harsh Environment Studies on Integrated Circuits) developed at TIMA is a flexible and general circuit qualification platform that takes into account the random nature of SEUs occurrence, both in time and affected memory cell. The capabilities of THESIC tester were widely proved during lastly performed test campaigns, which aimed at the evaluation of the operation under radiation of various microprocessors. During the radiation ground test, the THESIC motherboard is fixed to a moving stage support allowing performing the alignment DUT-beam. It

communicates to an external PC through a serial link connection. During a radiation test, target DUTs (Design Under Test) included on a daughter board are successively aligned with the beam. The DUT is the hardened 8051 board.

The main targets for upset errors of 8051 processor are: the 128 bytes internal RAM, the Special Function Registers, the Program Counter, Instruction registers, and in general, all the memory element (datapath registers, control part flip-flops,...).

5 Conclusion and future works

This paper has presented the prototype of a fault tolerant 8051-like micro-controller for space applications. A particular consequence of radiation environment, the Single Event Upsets phenomenon, was tackled by the insertion of error correcting codes in an existing VHDL design of this microprocessor, which is widely used in space projects. This robust processor was implemented in a programmable logic device customizable by EEPROM technology.

The effectiveness of the proposed strategy will be evaluated under radiation ground test and also by software fault injection experiments, performed by means of a dedicated system developed at TIMA laboratory.

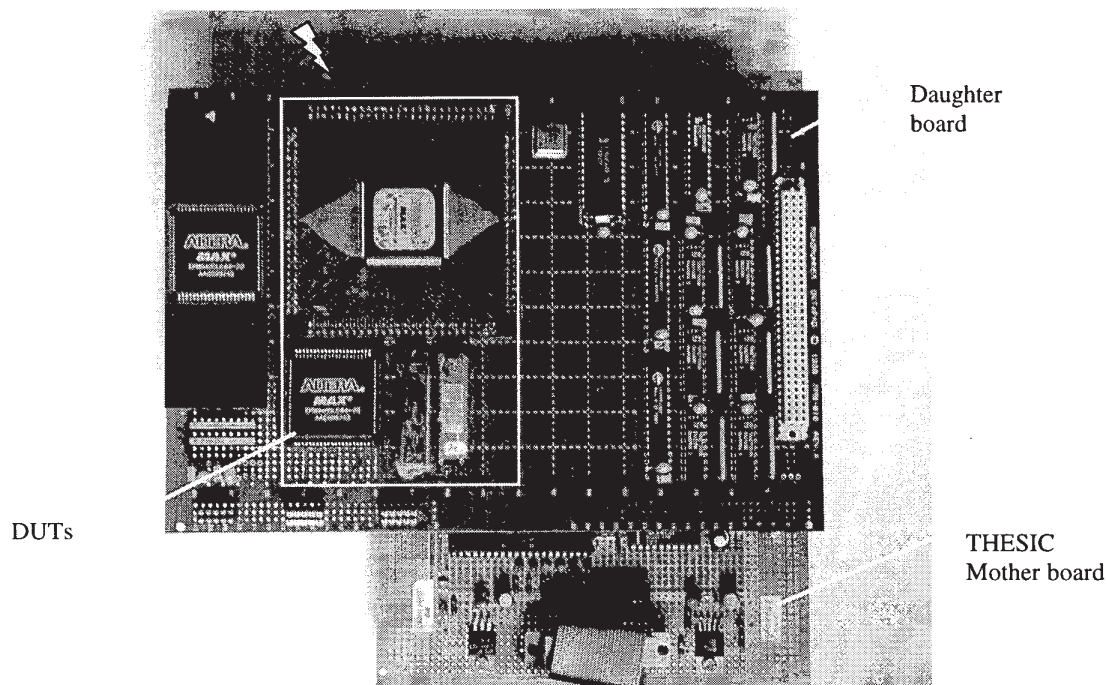


Figure 5 – SEU Hardened 8051 board and Thesic mother board

This tester, called THESIC, is a compact and flexible well suited tool for performing most of qualification tests (radiation, temperature, EMC) for complex integrated circuits.

Testing the SEU hardened version of the 8051 in the THESIC fault injection capabilities allows us analyze the behavior, with respect to transient bit flips, of architecture built around the micro-controller. Thousand of bit flips are going to be injected in parallel of the execution of a test program.

Preliminary results allow to predict that an 8051 robust version based on the hardening of internal RAM, datapath and finite machine registers by an error detection and correction strategy, will tolerate in 100% of the cases the effects of transient bit flips. The first results in area shows that the SEU immune processor is at least twice bigger if a PLD is used for the implementation.

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