

32-bit Radiation-Hardened Computers for Space

Captains Joseph Nedeau and Dan King
Phillips Laboratory/VTME
3550 Aberdeen Ave, SE
Kirtland AFB NM 87117
(505) 846-5810 and (505) 846-6067
nedeauj@plk.af.mil and kingd@plk.af.mil

Ken Hunt
Phillips Laboratory/VTMI
3550 Aberdeen Ave, SE
Kirtland AFB NM 87117
(505) 846-9143
huntk@plk.af.mil

Denise Lanza
Maxwell Technologies
2501 Yale Blvd SE, Suite 300
Albuquerque, NM 87106
(505) 846-2791
lanzad@plk.af.mil

Lester Byington
The Aerospace Corporation
Box 9045
Albuquerque NM 87119
(505) 846-5107
byington@kafb.aero.org

Abstract—Over the past 11 years, the Air Force Research Laboratory (AFRL), Phillips Research Center (formerly Phillips Laboratory) has championed the development of microprocessors and computers for United States Air Force (USAF) space and strategic missile application. The latest of these programs, the Advanced Technology Insertion Module (ATIM), is currently scheduled for completion at the end of 1997. ATIM is developing two single-board computers based on 32-bit reduced instruction set computer (RISC) processors. ATIM technology is baselined in the majority of today's Department of Defense (DoD), NASA, including Mars Pathfinder, and commercial satellite systems. The Improved Space Computer Program (ISCP) is envisioned as the next-generation space computer: merging advanced technologies and architectures to meet the high-performance, on-board processing needs for 21st century DoD, NASA, and commercial satellites. ISCP is a three pronged effort to evaluate evolving mission requirements, develop a commercial-heritage architecture, and integrate emerging technologies for space applications. These three areas are: the Phase I

Concept/Architecture Studies, the Improved Space Architecture Concept (ISAC), and the technology development efforts. ISAC lays out a sequential approach aimed at developing and demonstrating the potential for on-board, satellite processing. The combined serial and parallel development activities will prove that commercial-heritage architectures and technologies can reduce the development time and costs associated with building the next-generation spacecraft.

TABLE OF CONTENTS

1. INTRODUCTION
2. 16-BIT PROCESSORS FOR SPACE
3. 32-BIT PROCESSORS FOR SPACE
4. ISCP OVERVIEW
5. CONCEPT/ARCHITECTURE STUDY
6. IMPROVED SPACE ARCHITECTURE CONCEPT
7. TECHNOLOGY DEVELOPMENT
8. SUMMARY AND CONCLUSIONS

1. INTRODUCTION

Recent Air Force strategic planning reviews and on-going Technology Planning Integrated Product Teams (TPIPTs) have identified the

requirement for increased performance, lower mass, processing capabilities for future Air Force and other government space programs. Commercial advances in space also continue to demand increased processing capabilities. Air Force Research Laboratory's response to this need is the Improved Space Computer Program (ISCP).

The Space Electronics and Protection Branch of the AFRL Space Vehicles Directorate is focused on developing microelectronics for space. Several government sponsored programs include the Advanced Spaceborne Computer Module (ASCM) Control Processor Module (CPM), a 16-bit computer successfully deployed on several space platforms, including the recent Cassini mission, and the ASCM Advanced Technology Insertion Module (ATIM), a 32-bit RISC computer that will be available for space deployment by December 1997. This branch is also responsible for a number of smaller programs developing specific space electronic components, fostering fabrication process improvements, and exploring advanced packaging techniques. The Space Electronics and Protection Branch has initiated ISCP to develop the next generation space computer and to focus on the development of required underlying component technology.

This paper will provide an overview of the 16-bit and 32-bit space processors and discuss ISCP, including program objectives, our definition and use of architecture, the overall approach. Then, it will describe in more detail the Concept/Architecture Study segment, including some key results, and the Improved Space Architecture Concept (ISAC) segment focused on developing a space qualifiable flight experiment. The final section of this paper will introduce the technology

development efforts Air Force Research Laboratory is beginning this fiscal year.

2. 16-BIT PROCESSORS FOR SPACE^[1]

Generic Very High Speed Integrated Circuits (VHSIC) Spaceborne Computer (GVSC)

The GVSC, started in 1985, was the first development of fully-hardened complex logic devices in VHSIC I technology (1.0-1.2 μ m design rules). By contrast with the later CPM and ATIM programs (discussed later), this was only a chip set development, including only hardware and software for breadboard demonstration. By the end of the program in 1989, both contractors (Honeywell Space Systems and IBM Federal Systems, now Lockheed Martin Federal Systems) had fabricated GVSC microprocessors conforming to the MIL-STD-1750A instruction set and hardened to space and strategic radiation environments. Today, Honeywell is transferring the five-chip GVSC design into a single-chip package significantly reducing size, weight, and power.

The GVSC program was the first demonstration that a VHSIC-level bulk CMOS fabrication process could be hardened to military space levels, particularly in the areas of prompt dose and single-event upset. Both contractors met or exceeded the program goals of 10^6 rad(Si) total dose, 10^9 rad(Si) prompt dose, and 10^{-10} errors/bit-day single event upset (SEU). The throughput for the chip sets (embedded in a demonstration breadboard) was measured at 3 million instructions per second (MIPS) or better for both contractors. This was a substantial improvement over the 0.2-1.0 MIPS of previous space processors.

Control Processor Module (CPM)

Following the completion of the GVSC microprocessor program, Phillips Laboratory

began the Control Processor Module (CPM) program to build complete computer systems using the GVSC microprocessor technology as the core. The CPM was the first phase of the Advanced Spaceborne Computer Module (ASCM) contract awarded in 1989 to Honeywell Space Systems and IBM Federal Systems (now Lockheed Martin Federal Systems).

CPM had two principal goals: implementing and refining the Qualified Manufacturers List (QML) concept, and producing fully supported space-qualifiable 16-bit computers. The fabrication of these computers involved the development of complete processor, memory, input/output (I/O), and power converter capabilities. CPM, like the GVSC program, placed significant emphasis on producibility for the support and memory chips (1 micron CMOS interface chips and 256Kbit static RAM chips) as well as for assembly and packaging processes.

CPM was a pathfinder for the QML concept, a qualification method focusing on the manufacturing processes and the development of those processes, rather than end-of-line screening. QML is now a standard military electronics qualification method (MIL-M-38535) using statistical process control (SPC), and carefully designed and documented processes, to produce known-high-quality parts. Implementing SPC means identifying key parameter for all fabrication processes involved which impact the quality of the end product. By continually working to keep the process centered and to reduce variability, SPC has become a tremendously effective method to maintain the fabrication of high-quality products.

With respect to semiconductor manufacturing, QML and SPC means having a controlled process for the design-to-physical layout

transition to ensure the chip implements the intended design. The CPM program was the first application of QML to a radiation-hardened (and hence low-volume) fabrication line involving a considerable amount of independent verification testing and work on identifying die yield inhibitors.

Technology Insertions

GVSC chip sets were delivered for use on MILSTAR and at least one other DoD program, but the chip sets have primarily been incorporated in CPM-derived board-level products. Use of those products has been substantial in both military and civilian space, as discussed below.

CPM technology has been baselined in many of today's Air Force and DoD satellite systems. Additionally, technology from these programs has been transferred to civil and commercial satellite developers. A general summary of these insertions is shown in Figure 1 on page 4. Several of these systems have already been successfully launched. These include:

- TAOS (Technology for Autonomous Satellites)—increased processor performance enabled satellite autonomy demonstrations
- Clementine—standard components, such as CPM, enabled deployment of the satellite vehicle in less than two years.
- Cassini—GVSC microprocessor controlling all telemetry between the spacecraft and ground controllers back on Earth.

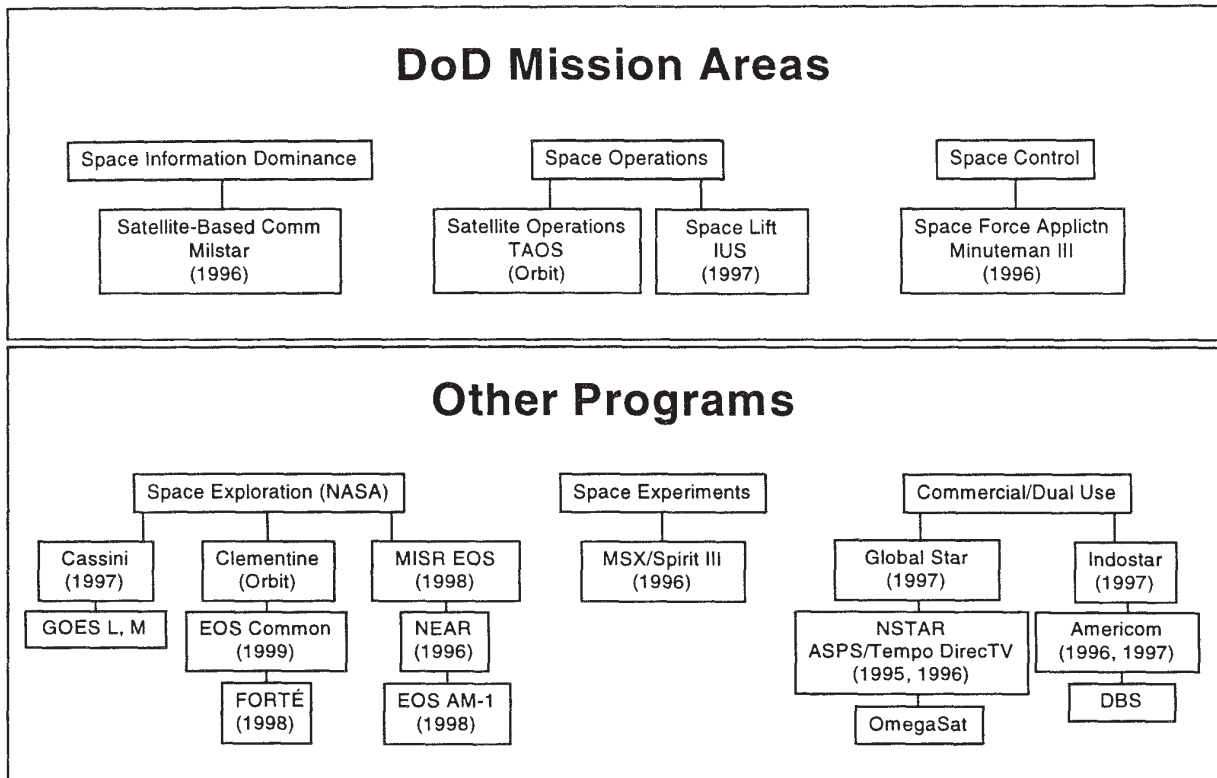


Figure 1. Programs that have flown or baselined CPM technology

3. 32-BIT PROCESSORS FOR SPACE^[1]

Advanced Technology Insertion Module (ATIM)

The 32-bit single board computer (SBC) systems under the Advanced Technology Insertion Module (ATIM) program are nearing completion. These SBCs incorporate the full complement of computer functions (processor, memory, and I/O) on a single 6" x 9" circuit card, while maintaining interoperability with the CPM subassemblies. ATIM extends the performance of previous space computers into the 32-bit arena by transferring and adapting commercial 32-bit RISC processor technology. The processors for the radiation-hardened SBCs is derived from the Honeywell Space Systems RH32 processor (developed by Rome Laboratory) and the IBM RISC/6000 (radiation hardened at Lockheed Martin

Federal Systems). The radiation-hardened 32-bit processors are fabricated sub-micron CMOS technologies supported by interface chips exceeding 100,000 equivalent gates. Both contractors employed the QML concepts pioneered under CPM to develop the ATIM SBCs.

Memory capabilities are also increased using 1 Mbit static RAM chips packaged in multi-chip modules (MCMs) for greatly increased density. I/O capabilities have been correspondingly increased. The ATIM computers will also come complete with advanced operating systems and sophisticated, user-friendly applications development environments. Software development has been greatly simplified by the adaptation of commercial operating systems and development environments that run on the

commercial parent processors from which the ATIM processors were derived.

ATIM has demonstrated SBCs in the 20-40 MIPS throughput range. Not only did processor performance improve through ATIM, but also increased support and memory chip densities were accomplished through the utilization of higher levels of integrated circuit integration and advanced MCM packaging (now available for technology transfer).

Technology Insertions

ATIM and its technologies are being used by civil and commercial customers for space qualified processing needs. The first launch of ATIM technology occurred in November 1996 with the Mars Pathfinder. Following that insertion are planned insertions in several

NASA space and planetary exploration missions, including the New Millennium ventures, and at least four commercial systems. Additional ATIM insertions are outlined on the chart in Figure 2.

4. IMPROVED SPACE COMPUTER PROGRAM (ISCP)

Overview

The ISCP program has been divided into three segments. The first segment was the Concept/Architecture Studies awarded to Maxwell Technologies and Mission Research Corporation in July and August 1996. During the studies, the contractors examined emerging requirements in order to derive the optimum space computer processor architecture. The second segment, the Improved Space Architecture Concept (ISAC)

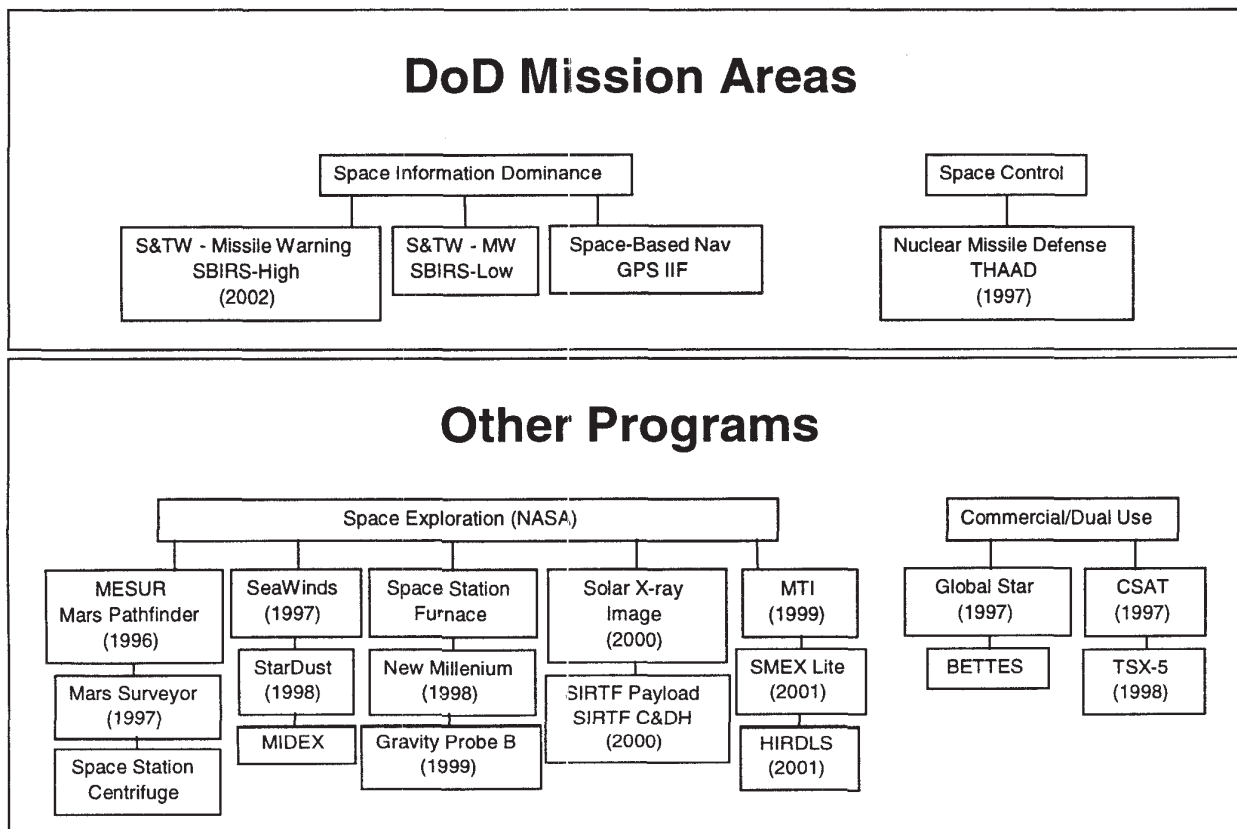


Figure 2. Programs that have flown or baselined ATIM technology

is a new project to design and develop an open, flexible, scalable architecture for space systems. The final segment is the associated advanced technology development to be integrated into ISAC and other government programs.

Architecture

Architecture has multiple meanings in the space community. A processor designer may define architecture in terms of the central processing unit, the I/O unit, the memory, and the data links used to connect these components. On the other hand, a satellite program may define architecture in terms of the constellation of satellites and their connectivity to ground and space networks. This section will discuss these various meanings and define what ISCP means by architecture.

Architectural Hierarchy

Borky, Singaraju, and Stevens^[2] define three levels of system architecture for advanced spacecraft: (1) force structure, (2) space system, and (3) satellite. During the course of defining ISCP, the program team examined these system level architectures presented and determined the spacecraft architectural hierarchy could be extended to six levels. Levels four through six are: boxes or subsystems, boards or subassemblies, and components^[3]. ISCP must consider all levels of the architectural hierarchy in order to ensure a complete and consistent solution for future spacecraft processing needs. However, ISCP focuses on levels four and below, while addressing issues of integration into systems at higher levels. A detailed description for each level as well as the implications on ISCP can be found in the 1997 IEEE Aerospace Conference Proceeding.

Objectives

ISCPs primary objective is to merge technologies and architectures to meet the next-generation of on-board, high-performance space computing needs. The most straightforward approach to accomplishing this objective is to make the architecture open. This will be done by using commercially developed and adopted standards wherever possible. Additionally, the architecture selected must be flexible. That is, the architecture must be designed not only to accommodate a variety of satellite systems but also allow for the portability of algorithms between platforms. Because ISCP is trying to satisfy the needs of multiple system platforms, the architecture must also address scalability. Each system has varying types and degrees of processing involved from the low-end communication tasks to the high-end image processing domain. Processing performance must scale well with the number of processors, and the architecture must be able to accommodate several different types of processors. In order to meet the intense processing requirements of advanced imaging systems as well as the flexibility and scalability requirements, ISCP must specify required enabling technologies such as component and subassembly developments.

The open, flexible, scalable architecture will enable on-board image processing. This advanced, and much-needed, capability will reduce the amount of bandwidth required to downlink the enormous images associated with emerging sensor developments. On-board processing allows a complete image to be downlinked directly to the battlefield commander, providing the operational forces with real-time imagery. This would reduce the dependence on the numerous ground stations.

An additional benefit of the high-performance space computer is the capacity to provide the user with autonomous mission operation, going beyond spacecraft control to increasingly independent information gathering, multispectral and hyperspectral data analysis, and data dissemination. ISCP will develop affordable, highly reliable, standardized functional modules and data interfaces to meet the next generation of space data and signal processing requirements. The program will demonstrate through the use of affordable electronics (an open, flexible architecture, standardized modules, and commercial heritage designs and standards, a reduction in development, test, and deployment time and costs. The increased satellite autonomy and processing capability will dramatically improve satellite system performance and decrease the support infrastructure while providing needed information directly to end users.

The system must meet the radiation-hardness requirements of the severest space environment. With the open system implementation, users with lower radiation-hardness requirements may substitute less-hard components within the same architecture.

5. CONCEPT/ARCHITECTURE STUDY

In 1996, two contractor teams were established to cooperatively determine the advanced processing requirements for ISCP and then independently derive detailed engineering requirements, evaluate several architecture candidates, and ultimately recommend an architecture for ISCP. The teams are:

Lead: Mission Research Corporation (MRC)

Members:

- BDM Federal, Inc.
- Boeing Defense and Space Group

- Harris Government Aerospace Systems Division
- Honeywell, Inc.
- Hughes Aircraft Company
- Lockheed Martin Advanced Technology Laboratories
- TRW

Lead: Maxwell Technologies, Inc.

Members:

- CPU Technology, Inc.
- Jaycor, Inc.
- Lockheed Martin Federal Systems
- Sanders with Lockheed Martin Space and Missile Systems and Lockheed Martin Astronautics
- Boeing (formerly Rockwell Autonetics and Missile Systems Division)

Tasking

Each contractor team received identical tasking. Both contractor teams were tasked to conduct a study in order to evaluate the payload processing requirements of the next generation of DoD sensor satellites, define a scalable processing architecture capable of meeting those requirements, and analyze the advanced technologies which enable the necessary processing speed. The contractor teams had to constrain themselves by the size, weight, and power consumption budgets of these satellites. Each contractor team will:

- (1) Conduct a survey of government agencies and industry prime contractors to determine the on-board processing needs of next-generation satellites.
- (2) Define and analyze key performance parameters and potential mission applications for advanced on-board processing capabilities.
- (3) Conduct engineering trades to define a system concept for an improved space

computer subsystem. In accordance with the prioritized performance parameters, the contractor teams will each identify, evaluate, and recommend an open, flexible, scalable architecture based on a comparison of existing commercial-heritage architectures.

(4) Define and analyze the opportunity to increase the functionality of the subsystem. The contractor teams will address the impact of incorporating analog electronics, discretes, radio frequency components, photonics, and/or electro-optic technologies. The contractor teams will also evaluate the opportunity to incorporate micro-electromechanical systems such as miniature sensors and/or inertial navigation instruments.

(5) Conduct a survey of the technology base for an improved space computer subsystem. The contractor teams will identify promising advanced technologies which will enable on-board payload processing objectives. They will assess the impact of the incorporation of individual technologies into the subsystem architecture, evaluate producibility and other cost implications of utilizing a technology and provide a prioritized, time-phased list of technologies recommended for further investigation.

Study Results

Both teams found the requirements analysis to be widespread, ranging from dozens of MIPS to over a TERAFLP (trillion floating point operations per second). With respect to the TERAFLP requirement, there was no processing flow described to justify the requirement, so it was impossible for the team to determine the validity of this particular requirement. It was also very interesting to observe that industry, when surveyed, was very conservative in their processing estimates. For the most part, industry respondents determined that any near-term

processing needs could be satisfied using available technology. This survey also reinforced the belief that the government does not have a good understanding of future requirements. When trying to derive the Engineering, Manufacturing, and Development (EMD) requirements for Space Based Infra-Red Systems (SBIRS)-Low, the teams had to rely on their industry partners who are working with the Program Office to understand what needs to be done on-board the satellite. From this description, the teams were able to derive and estimate the performance numbers.

SBIRS-Low was one of the common threads between the two teams when evaluating the architectures against "real-world" examples. Both teams also examined the Space Based Radar (SBR) system. However, the Maxwell Technologies team looked at a military satellite communication (MILSATCOM) task because they believed the processing flow and requirements, although not extremely intensive, stress the architecture in different ways (such as communication crosslinks and , data rate exchanges). The MRC Team looked at a Hyperspectral Imaging (HSI) application. All of the potential applications stress the architecture. By far, however, the HSI and SBR applications require intensive on-board processing in the dozens of GigaFLOPS. Current discussions with the SBR research and development personnel at AFRL have yielded some interesting processing requirement predictions. The near-term SBR application will require approximately 50 GFLOPS and the 2003-2005 application for SBR requires five times that processing capability on-board. These numbers, given the short span between applications, appear to be rather ambitious. During the next segment of ISCP, the government and industry will continue to examine these numbers.

The scalability and flexibility requirements drive the architecture interconnect selection to only a few choices: crossbar, mesh, and bus protocols. Simulation analysis determined that the crossbar interconnect was best suited for ISCP applications. Using a synthetic aperture radar (SAR) application, one of the most stressing, input frame periods for several nodes were modeled. Each of the interconnect types identified above were simulated with varying input frame lengths, ranging from 5 seconds down to 3.2. The bus type architecture began experiencing bottleneck problems at input frame lengths of 4 seconds. However, the crossbar and mesh architectures easily handled frame lengths of 3.2 and 3.4 seconds before bottlenecks occurred and data latency crept in. By eliminating the corner turns (reduce the large number of instructions between the multiply and inverse Fast Fourier Transform (FFT)), the crossbar and mesh architectures perform, without significant degradation, down to frame lengths of 3.2 seconds.

With ISCP's heterogeneous processing requirements, the architecture must support Multiple Instruction Multiple Data (MIMD). Coupling the crossbar interconnect with the MIMD architecture and distributed memory, enables the use of an unlimited number of computing nodes. Additionally, flexibility and scalability force the use of a message passing interface (MPI) layer to allow isolation between the application software and the underlying hardware. The MPI layer also has two other notable benefits: enhances the portability of algorithms between platforms and allows the architecture to be open and grow over time.

For standard system bus control and low-speed data rate transfers one of the current standards, 1553 or 1773, will be used. When high-speed data rate transfers are necessary, an

expansion module can be added which supports a high-speed interconnect, four point-to-point, full-duplexed interconnects at rates up to 320 Megabytes (MB) per second.

Finally, one would be remiss not to address software development. The development of a new operating system (OS) or development environment would be asinine. Therefore, a commercial-heritage OS would be modified not only for the space environment but also to handle the distributed and massively parallel processing architecture. With respect to the development environment, Maxwell Technologies, with strong support from Boeing and BDM Federal Inc., proposes a systems solution for software development. The proposed environment would entail a standard input and output format for each major activity associated with software development. For example, there would be an input "specification" for Hardware/Software partitioning and an output format leading to the hardware and software design document activities. Therefore, with the standard formatting the transition between vendor tools would be seamless because the output from the different tools would be similar. This approach maintains the industrial base and promotes competition while simplifying the software development process. Additional details for this development environment can be found in a paper titled "A Common Space Processing Development Environment," by Anderson, Bains, Borky, and Harold presented in Session 2, during the 1998 IEEE Aerospace Conference.

6. IMPROVED SPACE ARCHITECTURE CONCEPT (ISAC)

ISAC, segment two of ISCP, will provide, through modeling and simulation, hardware testbed, commercial computer equivalent demonstration, and space qualifiable demonstration, affordable, open-systems

mission payload architectures with the flexibility to meet a wide range of satellite missions. Affordability is defined as satellite life cycle cost (LCC), including launch costs, and must be computed on a mission by mission basis. Candidate architectures should be scalable to meet a variety of processing, memory, and application requirements. The next generation space mission payload architecture must be technically feasible (i.e. the first instantiation must be accomplished by FY01. The ISAC architecture should easily accommodate evolving technologies. The ISAC architecture will emphasize high performance processing at low power and low weight (500 MIPS/Watt, 200 MFLOPS/Watt, and MIPS/pound – numbers will be finalized during the first six months of ISAC. Finally, the ISAC architecture should enhance a system's ability to meet satellite mean mission duration and space electronics reliability requirements while reducing development cycle time and cost. ISAC is divided into three efforts.

Architecture Testbed Initiative (ARTI)

This is the basic effort, lasting 18 months, will develop a software simulation testbed (SSTB) and a hardware testbed (HWTB). The SSTB will be used to model several future, advanced space missions against one or more candidate open, flexible, scalable architectures. By using virtual prototyping (VP), several advanced processors will be modeled to demonstrate the adaptability of the architecture to accept emerging technologies easily and rapidly. Additionally, these same VP models can demonstrate the impact of higher-performance processors on the system. If models of current, or in-development, processors exist, they can also be evaluated on the SSTB. In particular, plans are being made to evaluate the Wafer Scale Signal Processor (WSSP) developed by Rome Laboratory. Air

Force Research Laboratory will use the hardware testbed to demonstrate emerging technologies and evaluate their potential integration into the space qualifiable flight experiment.

The SSTB will include at least one remote access site at AFRL, Kirtland AFB NM. The SSTB will be equipped with a Graphical User Interface (GUI) to promote the modification and development of alternate models for simulation and analysis. A series of Wizards will be developed during the course of ARTI to assist the non-experts in modeling and simulation. These Wizards will allow for the easy modification of the already developed models into an assortment of configurations. Multiple sites can be connected should other 3rd party organizations desire an interface to this testbed.

AFRL has begun the coordination process to integrate the modeling and simulation activities developed by Photon Research Associates (PRA) into the overall SSTB. By combining their payload and command and control (C²) models with our detailed on-board payload processor, we hope to demonstrate the benefits of on-board processing, both for reduced C² activities and for image processing and transmission directly to the battlefield. Both the SSTB and the HWTB will be delivered to AFRL. A Special Studies Option can be exercised to look at other applications, advanced technology, etc. The limitation is these Special Studies cannot be used for usable products (i.e. we could not use them to develop advanced technology).

Space Architecture Demonstration and Integration (SADI)

SADI is Option 1 to the ISAC contract, lasts 15 months, and culminates in the fabrication and performance evaluation of a commercial-heritage demonstration model (DM).

Radiation-hardened parts will not be used during this phase of the program; however, all commercial-heritage components selected must have, or be on, a clear, space qualifiable path (i.e. must have a path to radiation-hardening). The DM will be used to evaluate both low and high end processing applications. The low-end application would be similar to either a MILSATCOM or SBIRS-Low task where the processing is measured in hundreds of MIPS. The high-end application is currently a HSI task with a data rate of 5.4 megasamples per second. The image size is 2,000 by 2,000 with 210 wavebands at 12-bits per pixel with 50 images being collected daily. The Statement of Work (SOW) requires the contractor to demonstrate a representative subset of the high-end application. However, the contract scope includes potentially higher performance missions, such as Space Based Radar (SBR).

Flight Electronics Experiment (FELEX)

FELEX is Option 2 to the ISAC contract, lasts 21 months, including a six month overlap with SADI, and consists of the fabrication and test (performance, shock, vibration, ...) of a space qualifiable flight experiment. The contractor will work closely with the government and other space technology development programs to assure that the required radiation-hardened elements are available for integration into FELEX.

Using Oral Proposals in Science and Technology Acquisitions

The ISAC contract was awarded to Sanders, A Lockheed Martin Company, in October 1997, only 35 days after receipt of proposals from industry. This was the first use of Oral Proposals at AFRL, Kirtland AFB, for a large technical effort. Many members of the evaluation team had reservations and concerns about this "radical" process; however, at the

end of the week, the team unanimously agreed that Oral Proposals is an expedient yet thorough process.

One proposal was briefed and evaluated daily. The technical team had real-time discussions concerning one particular offeror as opposed to several evaluators reading different proposals. At the end of each day, that offeror's strengths and weaknesses had been documented and it was time to move on to the next offeror. At the end of the week, the four offerors on ISAC had been evaluated. With all of the strengths and weaknesses captured, it took only two weeks to prepare the complete technical evaluation, quantitative analysis, source selection decision memorandum, and source selection decision briefing.

The Oral Proposals forced the offerors to have a better understanding of the work to be performed. The structured time limit, in this case two hours, forced the offeror to clearly present his approach. Upon discussing the lessons learned, the technical team agreed a longer presentation would not have helped either the evaluation team or the offerors. However, the time limit should be considered on a program basis, with some programs opting for a shorter technical briefing. The ISAC program team has compiled our lessons learned and helped create in-house training for other programs.

Integrated Product and Process Development (IPPD)

ISCP was selected by the Science and Technology (S&T) Program Executive Officer (PEO) as one of the nine original Affordability Demonstration Pilot Programs. These programs were tasked with employing varying levels of IPPD tools during program execution. During ISAC, the House of Quality (HOQ) will be used as the primary requirements capture tool, and design

worksheets will capture all of the key aspects of the architecture. These worksheets will allow the ISAC team to evaluate several architecture concepts and components. Information from the HOQ and the design worksheets is transferred to a Value Scorecard, which captures all of the performance distributions. This allows an apples-to-oranges comparison between attributes because only probabilities are captured, and these probabilities can be summed across the table. The benefit of this tool is that a decision maker has all of the information concisely displayed on one sheet of paper.

Recently, Wright Laboratory has sponsored the development of a pilot program website. This website has a series of existing and in development IPPD and cost estimation tools. This website is being used by ISAC to link the various geographically distant sites. One of the key aspects to this website, is the inclusion a group decision tools which allow for "real-time" written communication. Group communication tools provide everyone the anonymous opportunity to participate. These tools also capture exactly what is said as opposed to paraphrasing discussion in telephone conferences. With all of the discussion captured and archived, team members who were unable to participate in the on-line discussions have the opportunity to review the discussion and provide comment directly to the other team members.

7. TECHNOLOGY DEVELOPMENT

The technology development activities, segment three of ISCP, serve as the foundation and are by far the most wide-spread activities. All of the efforts pursued under this portion of the program will not only support ISAC but also will support other DoD, government, and commercial programs. From the Concept/Architecture Studies, the government

understands that an advanced data processor that can operate in a parallel environment is required. Either a radiation-hardened version of the commercial PowerPC or an enhanced RH32 are likely candidates for the data processor.

The studies also identified the requirement for an advanced digital signal processor (DSP) such as a radiation-hardened version of the Analog Devices 21060 is needed. The 21060 provides over 100 MFLOPS of computing power for image processing applications. Unfortunately, the radiation-hardened version of the 21060 is too large to fit in a single-chip package primarily due to the fabrication processes at the radiation-hardened foundries. Also, the radiation-hardened version of the 21060 may not be developed in time to support ISAC. Therefore, the government with the help of industry may have to derive an alternate, near-term solution. For example, a 21020 currently being radiation-hardened by LMFS, could be optimized to perform in an MCM achieving 60 - 80% of the 21060's performance.

Other technology development activities will be identified during the course of ARTI with oversight coming from the Technology Development Integrated Product Team (IPT). This IPT consists of members from the government, the ISAC contractor, the technology development contractors, and any others who wish to participate. Technologies to be examined include sub 3.3 volt power converters, low-power, high density memory modules, and advanced packaging techniques to reduce size, weight, and power.

8. SUMMARY AND CONCLUSIONS

The Air Force Research Laboratory Space Vehicles Directorate has long history of successful technology developments and technology insertions. The Improved Space

Computer Program (ISCP) has been logically organized to provide a low-risk, low-cost demonstration of on-board processing. User participation and interest should grow as we move from one portion of ISAC to another. At any time, should interest wane, the contract has been logically processed to provide clear decision points eliminating termination costs. The Concept/Architecture Studies have recognized the need for on-board processing and demonstrates that on-board processing is possible within the next five years given a certain level of advanced technology investment. With the award of ISAC, AFRL is ready to continue the cooperation with other high-performance computing programs such as the Remote Exploration and Experimentation (REE) program from the NASA Jet Propulsion Laboratory and the Advanced Common Processor (ACP) program. Together these three programs can successfully demonstrate the advantages of high-performance computing to the DoD and NASA. The current 32-bit space processor is on Mars, and the future 32-bit space processor could be on its way to Europa.

REFERENCES

- [1] Gordon, King, et. al., "Technology Transfer of Military Space Microprocessor Development," 34th Space Congress Proceedings, May 1997.
- [2] Borky, John M., B.K. Singaraju, and Kurt B. Stevens, "An Advanced Spacecraft Avionics Architecture," 1996 Aerospace Applications Conference Proceedings, Vol. 1, pp. 227-242, Feb 1996.
- [3] Nedeau, King, et. al., "Improved Space Computer Program (ISCP): Very High Throughput Processing for 21st Century Satellites." 1997 IEEE Aerospace Conference Proceedings, Vol. Pp. 263-273, Feb 1997.

Captain Joe Nedeau is the Program Manager for the ISCP. He has BAs in Mathematics and

History from Assumption College and an MS in Systems Management from the Air Force Institute of Technology. Captain Nedeau has over seven years experience in project management, including a Department of Defense Level III Acquisition Professional Development Program Certification in Program Management. Prior to his assignment at Phillips Laboratory, Captain Nedeau managed the acquisition of F-16 Training Systems at Wright Patterson AFB OH.

Captain Dan King is the leader of the On-Board Processing Group and Program Manager for the Advanced Technology Insertion Module Program at the Air Force Phillips Laboratory. He has a masters degree in electrical engineering and a masters degree in computer engineering from the Air Force Institute of Technology. He has two years of experience in space systems and nine years of experience in program management.

Denise Lanza of Maxwell Technologies, Inc. provides onsite technical support to the ISCP Program Office. She has a BSEE from Virginia Tech and thirteen years of experience as a test engineer and in project management.