

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Kenneth Blemel
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DECLARATION OF DR. STAN SHANFIELD

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I, Dr. Stanley Shanfield, declare that:

1. I have been retained by Xilinx, Inc. as an independent technical expert in this proceeding before the United States Patent Trial and Appeal Board. I understand that Xilinx Inc. (“Xilinx” or “Petitioner”) is requesting that the PTAB institute an *inter partes* review proceeding of a set of claims in U.S. Patent No. 6,938,177 (“the ’177 patent”) (EX1001). Specifically, I have been asked to provide my technical review and analysis of ’177 claims 1-5, 10-15, and 17-20, which I will call the “challenged claims.”

2. I am being compensated at my ordinary and customary consultant rate for my work. My compensation is in no way contingent on the outcome of this proceeding or any other proceeding. I have no other interest in this proceeding or any other proceeding relating to the ’177 patent.

3. I set forth my opinions and the bases for my opinions below.

I. QUALIFICATIONS AND BACKGROUND INFORMATION

4. I have four decades of professional experience as a practicing engineer in the field of semiconductor fabrication, circuit design, and electronic module design and fabrication. My professional qualifications, experience, publications, presentations, the patents on which I am a named inventor, and a list of previous cases in which I have provided expert testimony are set forth in my *curriculum vitae*, attached as Appendix A.

5. I received my Bachelor of Science degree in Physics from the University of California, Irvine, in 1977. I received my Ph.D. from the Massachusetts Institute of

Technology (“MIT”) in 1981, with a dissertation on high field superconductors. During my doctoral program at MIT, I received a four-year scholarship from the Energy Research and Development Administration (now part of the Department of Energy).

6. After earning my Ph.D. in 1981, I began work as a Staff Scientist, then later as a Senior Staff Scientist, at Spire Corporation in Bedford, Massachusetts. At Spire Corporation, I developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. I also built, operated, and characterized an ion-assisted deposition system for making coating for semiconductors.

7. In 1985, I joined Raytheon Corporation, located in Lexington/Andover, Massachusetts, as a Section Manager in Semiconductors & Integrated Circuits. My work focused on developing processes for fabrication high power, high frequency multi-function integrated circuits. In 1992, I was promoted to Research Laboratory Manager, where I led a 90-person team, in high performance semiconductor devices and circuits, including measurement, assembly, and wafer fabrication. My work then focused on the design, fabrication, and measurement of state-of-the-art complementary metal-oxide semiconductor (“CMOS”) devices of the time, primarily for digital and mixed signal applications.

8. In 1996, I was promoted to Manager of Semiconductor Operations. In this capacity, I was involved in all aspects of CMOS-based IC fabrication. I was also responsible for a custom silicon application-specific integrated circuit (“ASIC”) design

and development group and the associated layout and simulation facilities. I was directly involved in the design of certain commercial products produced in the facility, including flip-chip modules for an AT&T wireless base station, and the transmit/receive modules for Iridium satellite handsets using chip-on-board (COB).

9. After 14 years at Raytheon, I became part of the founding team for AXSUN Technologies, located in Bedford/Billerica, Massachusetts, as a Vice President of Operations in 1999. In this capacity, I designed a complete facility for semiconductor processing, including establishing a fabrication facility in Belfast, North Ireland for producing thick oxide silicon-on-insulator material.

10. In 2003, I joined Draper Laboratory at MIT ("Draper"), located in Cambridge, Massachusetts, where I am still employed. Currently, I am the Division Leader of Advanced Hardware Development and am a Distinguished Member of Technical Staff and Technical Director. In my time at Draper, I have been responsible for in-house module and electronic system designs and have been involved in CMOS foundry implementation for multiple ASIC designs.

11. From 2003 through 2010, I was the division leader responsible for much of the design, layout, fabrication, and testing of Draper Lab's multi-chip module products, and participated directly in multiple MCM development programs. The MCM products were used as controllers for space and commercial satellites, sensor data collection, instrument controllers for terrestrial navigation, tracking and communication devices,

and specialized government applications. MCMs typically incorporated FPGAs, separate MCUs and additional DRAM and non-volatile memory chips, and were designed to emphasize minimum size, weight, and power. For example, in the early '00s I led teams in the design and in-house fabrication of a series of battery powered MCM instrument controllers which utilized an FPGA, GPS receiver chips, stacked flash memory and integrated patch antennas. These MCMs used several strategies for minimizing power use, including reduced clock rate and deep sleep and externally triggered wake up modes.

12. I have been a member of many professional societies and electrical engineering industry groups over the years, such as the Institute of Electrical and Electronics Engineers (IEEE) and the American Physical Society (APS).

13. I have received a number of academic awards and honors over the years, including awards and honors for the best Draper patent and most successful Draper development project.

14. I have also authored or co-authored over 25 technical papers covering various aspects of semiconductor devices and advanced semiconductor manufacturing.

15. I am a named inventor or co-inventor on more than nine (9) patents covering aspects of semiconductor devices, system and circuit design, and semiconductor manufacturing.

16. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '177 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time. Based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the early 2000s and specifically during the time of the alleged invention of the '177 patent.

II. MY UNDERSTANDING OF CERTAIN LEGAL PRINCIPLES

17. I am not a lawyer, but I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter. These include:

- a. A patent claim may be invalid as “anticipated” if every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference.
- b. In addition, a patent claim may be invalid as “obvious” to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”; see ¶¶24-26 below), based on a single reference (in view of background knowledge) or on a combination of multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art

references, there must be a reason that would have prompted a POSITA to modify the teachings of a single prior art reference, or to combine the teachings of two or more references, in a manner that provides the elements of the claimed invention.

- c. This reason to combine teachings of multiple references may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. Further, for a combination of prior art to render a claim obvious, the POSITA would have needed a reasonable expectation of success in making that combination.
- d. When evaluating whether an invention would have been obvious, the question is whether the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to POSITA at the time the purported invention was made. In other words, the question is not whether a single element “would have been obvious” but whether the claim as a whole would have been obvious given what was known in the prior art.
- e. An obviousness analysis should (1) identify the particular references that, singly or in combination, make the patent obvious; (2) identify which

elements of the patent claim appear in each of the asserted references; and

(3) explain a motivation, teaching, need or market pressure that would have inspired a POSITA to combine prior art references to solve a problem.

f. I understand that certain objective factors should be considered, if available, regarding whether a patent claim would have been obvious or nonobvious.

(I understand these are also called “secondary considerations” of non-obviousness). Such indicia include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention as compared to the closest prior art; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and if the patentee proceeded contrary to the accepted wisdom of the prior art. I am not aware of any such indicia of non-obviousness that would be pertinent to the '177 patent claims.

g. I am informed that the Supreme Court has ruled that if a technique has been used to improve one device, and a person of ordinary skill in the art would have recognized that it would improve similar devices in the same way, using the technique is obvious unless its actual application

is beyond that person's skill.

- h. I am informed that the general knowledge of a person with ordinary skill in the art at the time of the alleged invention can be used to (1) supply missing claim limitations that were generally known in the art prior to the invention; (2) support a motivation to combine particular disclosures; or (3) demonstrate the knowledge of the ordinarily-skilled artisan at the time of the invention for any other purpose related to patentability.
- i. I am also informed that it is improper to rely on hindsight in making the obviousness determination; I have not relied on such hindsight in forming and offering my opinions below. Instead, I have considered what was known to the POSITA prior to the alleged invention, e.g., as reflected in the prior art.

A. Critical Date

18. The application that led to the '177 patent (U.S. Appl. No. 10/028,556) was filed on December 19, 2001. EX1001 at cover page. For purposes of my analysis here, I have applied a date of December 19, 2001 (what I will call the "Critical Date") as the date of the alleged invention in my obviousness analysis, but my analysis would hold true even if the date of the alleged invention occurred earlier than December 19, 2001.

19. In particular, each of the teachings of Dehkordi, Frantz, Faura, Krasner, Christian, and Steele references that I describe below were publicly disclosed no later

than 1997 and mostly years earlier. The “newest” primary reference that I cite below is the Lyke reference (U.S. Patent No. 6,148,399), which is applicant admitted prior art to the ’177 patent. EX1001 at 1:20-21 (“Description of the Prior Art[. Lyke,] U.S. Pat. No. 6,148,399 is directed toward an Advanced Instrument Controller (AIC)”), 2:43-44 (“prior art MCM controllers, such as the AIC in [Lyke,] U.S. Pat. No. 6,148,399”). In fact, the AIC claimed in Lyke had been publicly disclosed no later than 1997, when other persons published at least one paper describing the AIC with some of the same text and images that later appear in the Lyke patent filed on October 26, 1998. *Compare, e.g.,* EX1015 (Avery) at 5-8 & Fig. 6 with EX1003 (Lyke) & Fig. 12. Avery is not cited by Lyke, and does not share any of the same inventors as Lyke. Therefore, my analysis of what would have been obvious to the POSITA, and my other opinions (including as to claim construction) would remain the same if the Critical Date was as early as October 26, 1998 (and potentially earlier, as Avery was published in 1997).

B. Claim Construction

20. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA at the time of the purported invention date.

21. I understand that the claims themselves, the patent itself including the specification and images, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. I have followed this approach in my analysis. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the Critical Date (not today).

22. I understand that the '177 patent was the subject of an unrelated proceeding in the District of Delaware in which the court addressed several terms of the '177 patent. In particular, the terms “oscillator(s)”, “processor configured to automatically activate from totally deactivated (unpowered) state”, “a plurality of gates arranged in a field programmable gate array”, “configured to run independent processes”, and “two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations,” were each said to have their “plain and ordinary meaning” with no additional construction. EX1012, 1-2. I note that the court ruled that the term “‘embedded’ shall have its plain and ordinary meaning, specifically, ‘embedded within the component that is required in that part of the claim’” and that “‘power converter’ shall have its plain and ordinary meaning, specifically, a power converter converts power.” *Id.*, 2. I use these constructions in my opinions below, but my opinion on the prior art does not change even if specific phrasings for plain and ordinary meaning were not offered by that court. The court also ruled that the claim’s preambles

that recite “an instrument controller” is not limiting and did not need construction. *Id.*,
2.

23. I further understand that there is a pending parallel district court action in which Xilinx and the Patent Owner may raise claim construction disputes. While in this IPR I have used the plain and ordinary meaning of terms, and the constructions as determined by the court in the unrelated proceedings noted in the paragraph above, I reserve the right to revisit my opinions if it becomes apparent that the parties have a dispute about the meaning of claim terms. In particular, my opinions in the IPR are made prior to receiving any proposed constructions by Sentient. I further reserve the right to address any situation where Sentient purports to use the plain and ordinary meaning of a term, but does not do so. As I discuss further herein, the prior art references describe these elements according to the plain and ordinary meanings of terms including as laid out above.

III. PERSON OF ORDINARY SKILL IN THE ART

24. For purposes of assessing this level of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior solutions to those problems, e.g., as found in prior art references, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field.

25. As previously described, I have reviewed and understand the '177 patent, and I understand these factors. I have considered the educational level of active workers in the field, including as known to me including through personal experience working with MCMs in the late 1990s and early 2000s as detailed above. I have considered the types of problems encountered in the art, the prior solutions to those problems, e.g., as found in the prior art references that I describe below and others with which I am familiar. I have also considered—again through my expertise and experience, as well as a review of the prior art—the speed at which innovations are made in this field and the level of the sophistication of the technology in forming my opinion as to the proper definition of the POSITA.

26. Based on these factors and my review of the '177 patent and its file history, I believe that a POSITA would have had a Bachelor's degree in electrical engineering, computer engineering, or a related field, and at least 2 years of experience related to the design or development of multi-chip modules operating as instrument controllers. Additional education could substitute for some experience, and substantial experience could substitute for some of the educational background. Based on my above-described experiences (including as I refer to in ¶¶3-16 above), I am familiar with and know of the capabilities of a POSITA at the time of and prior to the Critical Date defined in ¶18 above.

IV. MATERIALS CONSIDERED

27. As part of my independent analysis for this declaration, I have considered the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the alleged invention date for the '177 patent. In addition, I have read and considered the publications and materials including the following:

- U.S. Patent No. 6,938,177 (“’177 patent”) (EX1001)
- U.S. Patent No. 6,148,399 to James C. Lyke (“Lyke”) (EX1003)
- P. Dehkordi, T. Powell and D. Bouldin, *Development of a DSP/MCM subsystem assessing low-volume, low-cost MCM prototyping for universities*, Proceedings 1996 IEEE Multi-Chip Module Conference (Cat. No. 96CH35893), 1996, pp. 89-94 (“Dehkordi”) (EX1004)
- G. A. Frantz, K. Lin, J. B. Reimer and J. Bradley, “The Texas Instruments TMS320C25 Digital Signal Microcomputer,” in IEEE Micro, vol. 6, no. 6, pp. 10-28, Dec. 1986 (“Frantz”) (EX1005)
- J. Faura, C. Horton, P. van Duong, J. Madrenas, M. A. Aguirre and J. M. Inerser, *A novel mixed signal programmable device with on-chip microprocessor*, Proceedings of CICC 97 - Custom Integrated Circuits Conference, 1997, pp. 103-106 (“Faura”) (EX1006)
- U.S. Patent No. 5,663,734 to Norman F. Krasner (“Krasner”) (EX1007)
- U.S. Patent No. 4,279,020 to Ronald W. Christian et al (“Christian”) (EX1008)
- U.S. Patent No. 5,675,824 to Randy C. Steele (“Steele”) (EX1009)
- File Wrapper of the ’177 Patent (EX1010)
- Claim Construction Order in *Sentient Sensors v. Cypress Corp.*, 19-1868 (MN), (Jan. 28, 2021, D. Delaware) (D.I. 89) (EX1012)
- Data Sheet for Motorola 96002 Digital Signal Processor (EX1013)
- Data Sheet for Xilinx XC4000E and XC4000X Series (including Xilinx XC4010) (EX1014)

- K. Avery and D. Alexander, *Recent progress in space-based micro-controller design*, 16th DASC. AIAA/IEEE Digital Avionics Systems Conference. Reflections to the Future. Proceedings, 1997, pp. 2.1-7 (“Avery”) (EX1015)
- T. Goforth, S. Cannon, J. Lyke, *Space Testing of the Advanced Instrument Controller*, Proceedings of the 13th AIAA/USU Conference on Small Satellites, Aug. 23–26, 1999, Logan UT, SSC99-XI-3 pp. 1-11 (“Goforth”) (EX1016)
- L. Muller, M. H. Hecht, L. M. Miller, H. K. Rockstad and J. C. Lyke, *Packaging and qualification of MEMS-based space systems*, Proceedings of Ninth International Workshop on Micro Electromechanical Systems, 1996, pp. 503-508 (“Muller”) (EX1017)
- Blemel, Kenneth G., *Reactive Prognostic Management of Corrosion With Autonomous Sensors*. Paper presented at the CORROSION 2000, Orlando, Florida, March 2000 (EX1018)
- Hauck, Scott, *The Roles of FPGAs in Reprogrammable Systems*, Proceedings of the IEEE, Vol. 86, No. 4, pp. 615-638, April 1998 (EX1019)
- U.S. Patent No. 5,867,535 to William C. Phillips (“Phillips”) (EX1023)
- U.S. Patent No. 6,178,494 to Steve M. Casselman (“Casselman”) (EX1024)
- U.S. Patent No. 5,574,930 to Richard P. Halverson, Jr. (“Halverson”) (EX1025)
- U.S. Patent No. 5,872,960 to Oved Oz (“Oz”) (EX1026)
- T. Nishitani, I. Kuroda, Y. Kawakami, H. Tanaka and T. Nukiyama, *Advanced single-chip signal processor*, ICASSP ‘86. IEEE International Conference on Acoustics, Speech, and Signal Processing, 1986, pp. 409-412 (“Nishitani”) (EX1027)
- P. R. Christensen, et al. (2001), *Mars Global Surveyor Thermal Emission Spectrometer experiment: Investigation description and surface science results*, J. Geophys. Res., 106(E10), 23823– 23871 (“Christensen”) (EX1028)
- U.S. Patent No. 5,936,562 to Todd L. Brooks (“Brooks”) (EX1029)
- U.S. Patent No. 5,861,831 to Franklin M. Murden (“Murden”) (EX1030)
- U.S. Patent No. 5,638,092 to Tommy K. Eng (“Eng”) (EX1031)
- J. Faura, J.M. Moreno, M.A. Aguirre, P. van Duong, J.M. Insenser, *Multicontext dynamic reconfiguration and real-time probing on a novel mixed signal programmable device with on-chip microprocessor*. In: Luk, W.,

- Cheung, P.Y.K., Glesner, M. (eds) Field-Programmable Logic and Applications. FPL 1997. Lecture Notes in Computer Science, vol 1304. Springer (1997) (“FauraMoreno”) (EX1032)
- Y. Tian, J. Ying, X. Ye, W. Gu, *DDGIPS: a general image processing system in robot vision*; Proc. SPIE 4212, Reconfigurable Technology: FPGAs for Computing and Applications II, Oct. 6, 2000 (“Tian”) (EX1033)
 - U.S. Patent No. 5,874,834 to Bernard J. New (“New”) (EX1034)
 - Marchal, Pierre, *Field-programmable gate arrays*, Communications of the ACM, Vol. 42, No. 4 (1999), p. 57-59 (“Marchal”) (EX1035)
 - I. Kostarnov, S. Morley, J. Osmany, C. Solomon, *A reconfigurable approach to low cost media processing*. In: Luk, W., Cheung, P.Y.K., Glesner, M. (eds) Field-Programmable Logic and Applications. FPL 1997. Lecture Notes in Computer Science, vol 1304. Springer, Berlin, Heidelberg (“Kostarnov”) (EX1036).
 - U.S. Patent No. 5,757,690 to Scott H. R. McMahon (“McMahon”) (EX1037)
 - Analog Devices, ADuC824, MicroConverter, Dual-Channel 16-/24-Bit ADCs with Embedded FLASH MCU, 2001 (EX1038)
 - Analog Devices, ADuC824 FAQ, January 2001 (EX1039)
 - U.S. Patent No 5,892,962 to Jocelyn Cloutier (“Cloutier”) (EX1040)
 - U.S. Patent Publication No. to 2002/0129191 to Behram DaCosta (“DaCosta”) (EX1041)
 - de Lima, F.G., *Designing A Radiation Hardened 8051-like Micro-Controller*, Proceedings 13th Symposium on Integrated Circuits and Systems Design (Cat. No.PR00843), 18-24 September 2000 (“de Lima”) (EX1042)
 - J. J. Wang et al., *SRAM based re-programmable FPGA for space applications*, in IEEE Transactions on Nuclear Science, vol. 46, no. 6, pp. 1728-1735, Dec. 1999 (EX1043)
 - U.S. Patent No. 5,936,971 to Ellyahou Harari (“Harari”) (EX1044)
 - U.S. Patent No. 5,261,109 to Sudarshan B. Cadambi (“Cadambi”) (EX1045)
 - T. Griffin, *Multichip Modules Including Processing: A Literature Survey*, Army Research Laboratory publication ARL-MR-257, August 1995 (EX1046)

- J. Nedeau, D. King, D. Lanza, K. Hunt and L. Byington, *32-bit radiation-hardened computers for space*, 1998 IEEE Aerospace Conference Proceedings (Cat. No.98TH8339), 1998, pp. 241-253 vol.2 (EX1047)

V. BACKGROUND KNOWLEDGE OF THE '177 PATENT

A. '177 Patent Subject Matter Overview

28. The '177 patent describes “a multi-chip module instrument controller having various interface and operational capabilities.” EX1001, Abstract. Figure 1 of the '177 patent is “a functional schematic block diagram of a preferred embodiment of the MCM Controller of the present invention.” EX1001, 3:28-30.

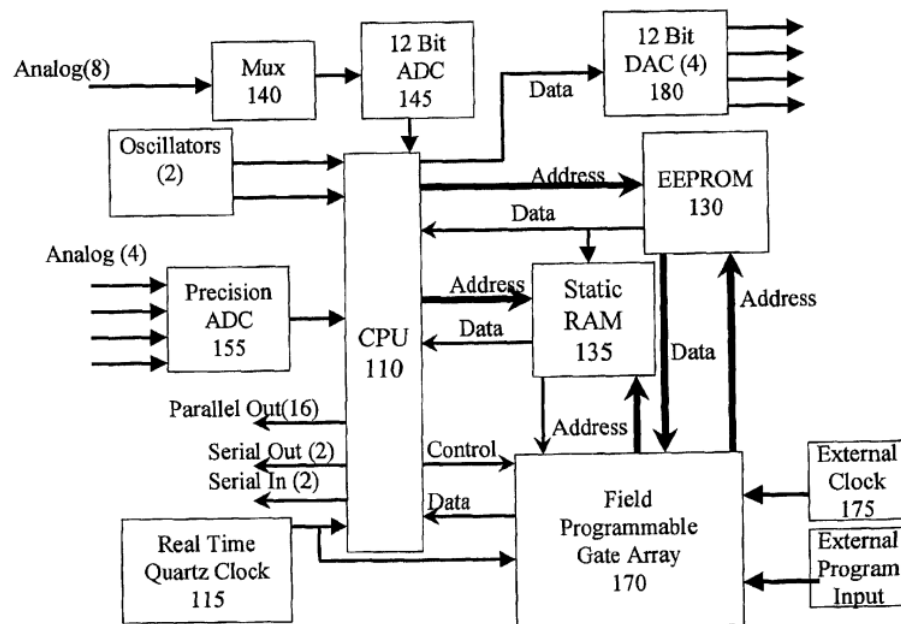


Fig. 1

EX1001, '177 patent, FIG. 1. The '177 patent purports that the “core elements of the present invention include a microprocessor, static random access memory (single or multi-ported), non-volatile memory (e.g., flash or EEPROM), a dynamically

reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion.” *Id.*, 2:66-3:5

29. I note that the ’177 patent is very similar to the Lyke prior art reference discussed in more detail below. Sections of the ’177 patent are identical or nearly identical to sections of the Lyke reference. *Compare* EX1001 with EX1003:

’177 Patent (EX1001)	Lyke Prior Art (EX1003)
“[T]he present invention includes an internal embedded power conversion module which greatly extends robustness of the design, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog control, this capability allows the present invention to not only maintain its internally correct operating power supply under external variation, but this capability permits the present invention to maintain interface integrity. ” 8:46-58.	“The internal embedded power conversion greatly extends AIC robustness, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog, this capability allows the AIC to not only maintain its internally correct operating power supply under external variation, but this capability permits the AIC to maintain interface integrity. ” 6:10-19.
“The present invention uniquely combines inherent core and I/O feature[s], design methodology, and operating principles to create an electronics building block having numerous monitoring/controlling applications. Along with its increased functionality and unique circuit design, the primary characteristics of the present invention are its compact size, light weight, low power consumption, and compatibility with robust application regimes. ” 2:59-65.	“The AIC uniquely combines inherent core and I/O features, design methodology, and operating principles to create an electronics building block with numerous monitoring/controlling applications. The AIC’s primary characteristics are small size, weight and power, versatile functionality, and compatibility with robust application regimes. ” 1:66-2:5.

“Each channel preferably has a fixed window for operation corresponding to zero and full scale digital readings, with the inputs defaulting to one of the fixed window values. Accordingly, such a typical default window might be 0–4.096 V for input range where a channel receiving a -2V signal would be represented as 0V at the input and a 10V signal would be represented as 4.096V.” 5:39-48	“Typical analog-to-digital and digital-to-analog convertors (ADCs and DACs) have a fixed window for operation corresponding to zero and full scale digital readings (ADCs) or settings for voltage control (DACs). A typical AIC possesses a default window of 0-4.096V for input range and 0-4.096V for output range. With a fixed window for this example, a -2V signal would be represent[ed] as 0V, and a 10V signal would be represented as 4.096V.” 5:17-25.
“In most applications, it is important for a controller to have a large number of serial interfaces. Most conventional controllers have few, if any, serial interfaces and it is often necessary to add additional hardware to allow for more serial interfaces. In a preferred embodiment of the current invention, a large number of serial interface are preferably readily accommodated without the need for additional hardware. Accordingly, in a preferred embodiment the present invention includes a number of both a synchronous serial ports (e.g., RS-232/RS422) as well as synchronous (e.g., clocked) serial ports. Preferably, the voltage levels of the serial ports default to CMOS-compatible levels; however, the present invention includes an adaptive I/O module which allows these voltage levels to be adjusted. For example, the RS-232 ports could be adjusted to +/-4V instead of (0,3.3V) levels.” 5:49-64.	“In cases where AICs are used in networks, it is important to have a large number of serial interfaces. In current designs, it is necessary to add additional hardware to address more interfaces, whereas in the AIC a larger number are readily accommodated. These interfaces need to be flexible as well. AIC contains a number of both asynchronous serial ports (e.g., RS-232/RS-422) as well as synchronous (e.g., clocked) serial ports. The voltage levels of the serial ports default to CMOS-compatible levels by default. Using the adaptive I/O, those voltage levels can be adjusted. For example, the RS-232 ports could be adjusted to +/-4V instead of (0,3.3V) levels.” 3:33-45.
“In a preferred embodiment, the invention has more than 10 externally available discrete signal channels. These channels	“The full-up version of the AIC typically has more than 30 externally available discrete signal channels 2. These are

are bi-directional lines having pull-up or pull-down characteristics that can be externally set. When used as outputs, these channels are set to CMOS level; however, a subset of the lines can be passed through an adaptive I/O function to adjust the levels to any two other desired voltage levels.” 6:65-6:5.	bi-directional lines with pull-up or pull-down characteristics that can be externally set. When used as outputs, the I/O are CMOS level, but a subset of the lines can be passed through the adaptive I/O function to adjust the levels to two other voltage levels.” 3:55-61.
“The present invention further includes a combination of large volatile and non-volatile memory storage components . These memory storage components are preferably customized and tightly coupled within the MCM for maximum performance. ” 6:7-11.	“The AIC combines a central processing unit, an analog application-specific integrated circuit (ASIC), a resistor ASIC, and volatile and non-volatile memory storage systems on a single tightly coupled MCM to achieve its stand-alone capabilities. ” 3:4-8.
“In a preferred embodiment the non-volatile memory storage components include at least two non-volatile memory units each with a minimum of 256K bytes of non-volatile memory space, preferably FLASH or EEPROM based. . . . The non-volatile memory is used for both program storage and data storage, which can be changed repetitively, limited only by the fatigue mechanism associated with the non-volatile device. ” 6:12-21.	“A typical AIC contains a minimum of 128K bytes of non-volatile memory , usually EEPROM based. The non-volatile memory is used for both program storage and data storage, which can be changed repetitively, limited only by the fatigue mechanism associated with the non-volatile device. ” 4:11-17.
“ The ability to exploit non-volatile data storage allows the present invention to preserve the context of key operations by periodically storing state information and intermediate results from algorithms executed by the microprocessor and/or the FPGA. The existence of this state information is tested upon reset especially after power is interrupted, to determine where the last left operation (a simple form of rollback). The non-volatile storage also allows serialization, for specific	“ The ability to exploit non-volatile data storage allows the AIC to preserve the context of key operations by periodically storing state information. The existence of this state information is tested upon reset, especially after power is interrupted, to determine where the AIC last left operation (a simple form of rollback). The non-volatile data storage allows for AIC serialization, for AIC-specific calibration parameter storage

calibration parameter storage (e.g., monitor the non-linearity of its own analog inputs and store the necessary corrective coefficients in memory), and for history depending operations such as data logging. It is possible to also store particular design specifications, usage/maintenance history for recall during diagnosis, maintenance, and repair of the present invention. The non-volatile memory of the present invention may also be used to program reconfigurable logic (e.g. the FPGA) and interconnect devices.” 6:47-64.	(e.g., monitor the non-linearity of its own analog inputs and store the necessary corrective coefficients in memory), and for history-depending operations such as data logging. It is possible to also store AIC specifications, usage/maintenance history for recall during diagnosis, maintenance, and repair. The non-volatile memory of the AIC would also be used to program reconfigurable logic and interconnect devices within the AIC.” 4:18-34.
“The distinction between the high-frequency and low-frequency oscillators is important as it is necessary for power preservation to maintain an independent oscillator that operates at a lower frequency. The third oscillator generates a clock signal which is used for the individually programmable FPGA. In order to offer accurate speed and performance at high-G applications or applications where both extreme cold and discontinuous operation are present, the present invention preferably utilizes non-crystal based oscillators for effective operation. Alternatively, crystal oscillators may be used. The present invention also permits external oscillators for cases where synchronization or more precise timing is important. In all cases, the low frequency clock signal is independently generated to minimize power consumption in divider networks and fast-switching drivers.” 7:7-25	“The distinction of ‘two’ oscillators is important, as it is necessary for power preservation to maintain an independent oscillator that operates at a lower frequency. In high-G applications or applications where both extreme cold and discontinuous operation are present, the AIC requires non-crystal based oscillators for effective operation. Otherwise, crystal oscillators may be used. The AIC also permits external oscillators for cases where synchronization or more precise timing is important. In all cases, the low frequency oscillator is independently generated to minimize power consumption in divider networks and fast-switching drivers.” 4:42-57.
“As described earlier, a preferred embodiment of the present invention	“The internal embedded power conversion greatly extends AIC

includes an internal embedded power conversion module which greatly extends robustness of the design, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog control, this capability allows the present invention to not only maintain its internally correct operating power supply under external variation, but this capability permits the present invention to maintain interface integrity.” 8:4-54.	robustness, particularly when a number of adjustable internal voltage references are provided. When combined with agile analog, this capability allows the AIC to not only maintain its internally correct operating power supply under external variation, but this capability permits the AIC to maintain interface integrity.” 6:10-16.
“As shown in FIG. 3, a first stage in the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG). A number of second stages convert from the fixed VREG to several power voltages consumed internal to the module. These second stage voltages provide for the supply of internal digital power, internal analog power, and a series of reference voltages. Many topologies known in the art of power convertor design may be applied, whether switching based, linear based, or a combination of the two.” 8:64-9:6.	“The first stage power converts an unregulated supply voltage to a fixed, regulated voltage (VREG). A number of second stage convertors convert from the fixed VREG to several power voltages consumed internal to the AIC. These second stage voltages provide for the supply of internal digital power, internal analog power, and a series of reference voltages. These reference voltages make possible the stable interface of AIC to other systems even in the presence of power fluctuations, through agile approaches, such as shown in FIG. 4. Many topologies known in the art of power convertor design may be applied, whether switching based, linear based, or a combination of the two.” 5:60-6:4.
“Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management security systems, miniature weapons computers, space probe central control	“Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management, security systems, miniature weapons computers, space probe central control

processor, beacon processor, and jet engine control. The invention may also be used on the manufacturing floor for smart, discontinuous low-level sensing test equipment probes, embedded credit card processors, wearable computers, or remote data logging.” 9:8-17.	processor, beacon processor, and jet engine control. AICs could also be used on the manufacturing floor for smart, discontinuous low-level sensing, test equipment probes, embedded credit card processors, wearable computers, or remote data logging.” 9:1-11.
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B. File History of the '177 Patent

30. I have reviewed the file history of the '177 patent (EX1010) as part of my analysis for this declaration. I understand that the '177 patent issued on August 30, 2005 from U.S. Patent Application No. 10/028,556 (“the '556 application”), which was filed on December 19, 2001. *See* EX1001. The '177 patent issued with 20 claims, of which claims 1, 6, 10, 13, 15, and 20 are independent. *Id.*

31. An initial non-final Office Action was issued December 8, 2004. In this initial Office Action, the Examiner concluded that many of the claim elements were described by Lyke, and identified two additional prior art references as obvious to combine with Lyke to disclose the elements of most of the then-pending claims. EX1010, 56-62. The Examiner identified four dependent claims as allowable if re-written into independent form, noting purported reasons for allowability: “the prior art fails to disclose or suggest ‘first portion of the gates configured to perform signal processing; and second portion of the gates configured to operate as a signal distribution matrix,’” “the prior art fails to disclose or suggest ‘resettable digital real-time quartz

controlled clock for accurate data and time stamping of date and time stamping of data before it is stored in the non-volatile memory,”” and “the prior art fails to disclose or suggest ‘a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter.’” EX1010, 60.

32. In response, the applicant did not argue against the Examiner’s conclusions that Lyke described many of the claim elements, and did not argue against the proposed combination of Lyke with the two additional prior art references. The applicant re-wrote the allowable claims into independent form, and added new claims having various features identified by the Examiner as allowable. EX1010, 32-46. A notice of allowance was issued on March 14, 2005.

33. Based on my review of the record, more pertinent references were not analyzed in any office action by the examiner during prosecution. Only three references are listed on the face of the ’177 patent as considered during prosecution—Lyke, Cloutier (U.S. Patent No. 5,892,962) (EX1040), and DaCosta (U.S. Patent Application Publication No. 2002/0129191) (EX1041).

34. Based upon my analysis of the publications cited in this declaration, I do not agree that the challenged claims of the ’177 patent are patentable over the prior art. For example, the combination of teachings from Dehkordi, Frantz, Faura, Krasner, Christian, and Steele references describe the elements of claims 1-5, 10-15, and 17-20, as I describe below. In particular, these references demonstrate that those of skill in the

art were aware of the features identified by the Examiner as the reasons for allowance relevant to those challenged claims.

C. A POSITA was familiar with MCM instrument controllers having features recited by the claims prior to the '177 patent

35. The '177 patent includes claims directed to configurations of hardware in a multi-chip module (MCM) instrument controller. *See, e.g.*, EX1001, Abstract, FIGS. 1-3. MCMs like those described by the '177 patent were well-known to POSITAs prior to the '177 patent, and were used in commercial applications going back to at least the early 1990s. *See, e.g.*, EX1046. I note that Lyke, which is mentioned in the '177 patent, describes a variety of applications for MCMs:

Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management, security systems, miniature weapons computers, space probe central control processor, beacon processor, and jet engine control. AICs could also be used on the manufacturing floor for smart, discontinuous low-level sensing, test equipment probes, embedded credit card processors, wearable computers, or remote data logging.

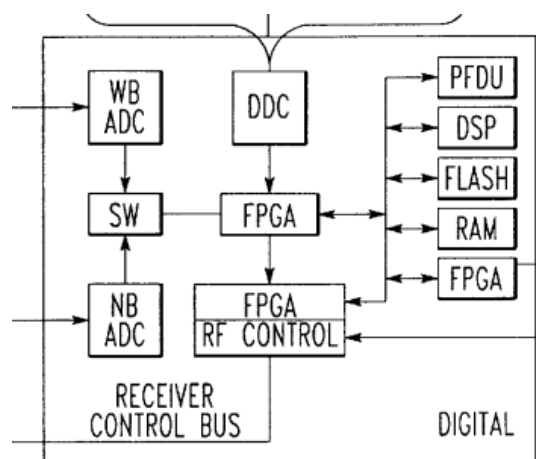
EX1003, 9:1-11. As another example confirming known structures and applications of MCMs, Avery described MCMs containing the types of processors, FPGAs, analog to digital converters, routing and power circuitry, and other elements recited in the claims of the '177. EX1015, 1.

36. More specifically, use of FPGAs in MCM modules was well known to POSITAs. As one example, an article authored by Kenneth Blemel (the sole listed

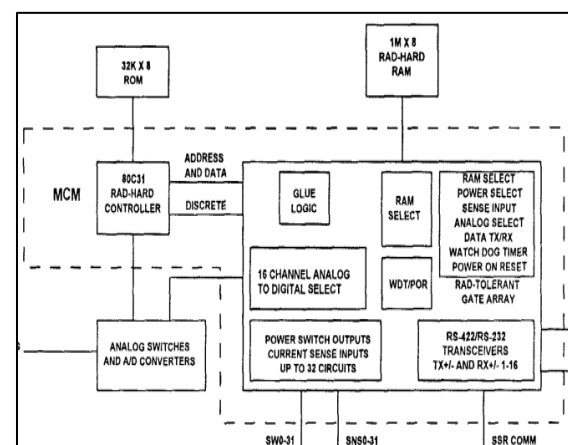
inventor of the '177 patent), and published more than a year before the '177 patent, described “an advanced instrument controller (AIC)” that was “made up of a microprocessor, a Field Programmable Gate Array (FPGA), a Fuzzy Logic Circuit and other electronics” for signal processing. EX1018, 6 (“In November 1999, the units will be installed on two navy H60 helicopters.”). As another example, a 1998 article in *Proceedings of the IEEE* describes such features in FPGA-based reprogrammable systems. EX1019, 16 (“Another system uses FPGA’s optimized for interchip communication on a multichip-module (MCM) substrate [Dobbelaere92], since MCM’s will be used to fabricate the system to achieve higher density circuits.”).

37. Example prior art diagrams showing MCM instrument controller components, or that would be recognized as applicable to same, are illustrated below, and others were certainly known beyond these examples:

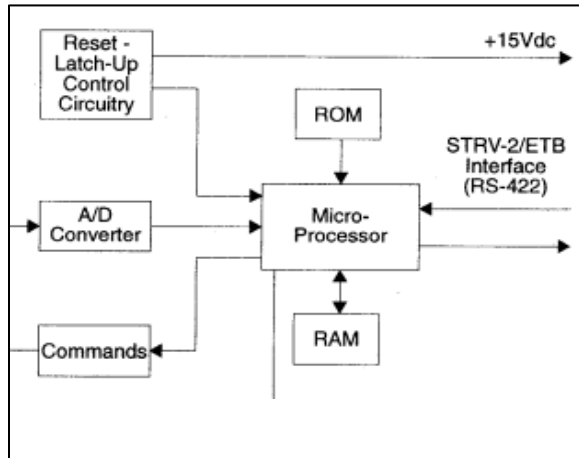
Phillips (EX1023), FIG. 2B (partial)



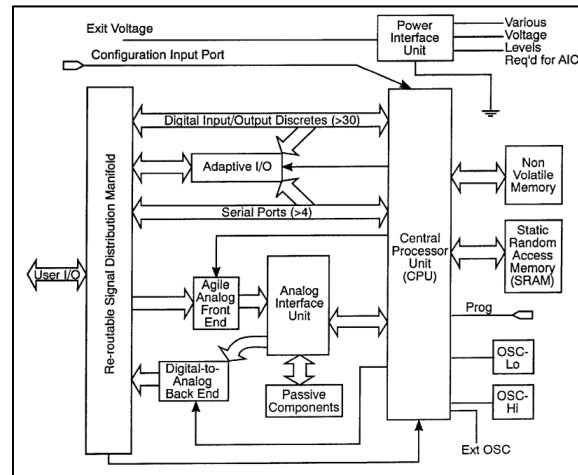
Muller (EX1017), FIG. 8



Avery (EX1015), FIG. 8



Lyke, (EX1003), FIG. 1



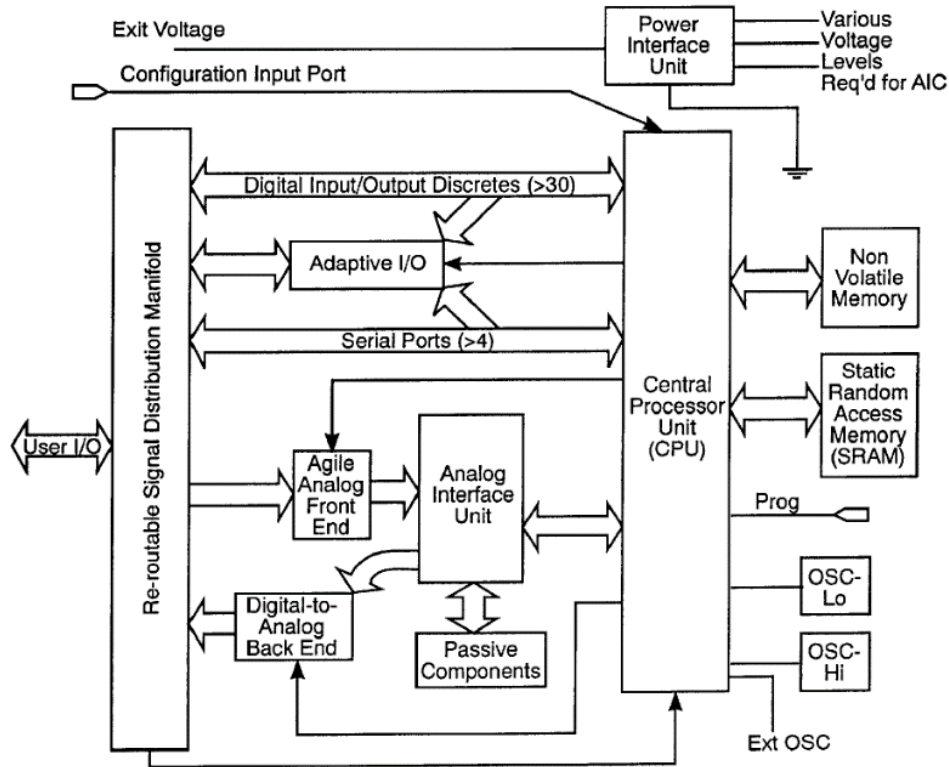
38. As early as 1997, the use of “embedded programmable logic arrays (i.e., field programmable gate arrays), and a programmable internal switch matrix for signal re-routing,” were described in prior art publications, such as Avery. *See, e.g.*, EX1015, 8. As I discuss in the detailed analysis of the claims below, publications prior to the ’177 patent also described configuring a portion of an FPGA to act as an internal power converter. *See, e.g.*, EX1009; EX1015, 6. I note these combined features were identified by the Examiner as reasons for allowing the claims, but these combined features were known to a POSITA. EX1010, 60. Furthermore, the “embedded memory for storing an initialization program...” element described a standard way that a processor in an MCM would have been configured. *See, e.g.*, EX1005, 2 (“[f]our-k

words of on-chip program ROM”), 17 (“large on-chip RAM of 544 words and on-chip ROM of 4K words allow it to execute a 256-tap adaptive filter (32-ms echo cancellation) without external data or program memory.”); EX1037, 1:10-23 (“microprocessor [with] an embedded ROM”), 10:64-11:4 (“[a] microprocessor with an embedded read-only instruction memory, the microprocessor comprising: a central processing unit (CPU) core for executing instructions; an embedded memory for storing read-only instructions, the embedded memory having row lines connected to read-only-memory ROM cells storing an instruction for execution by the CPU core.”).

VI. ANALYSIS OF THE CITED REFERENCES

A. Overview of Lyke (EX1003)

39. Lyke was filed on October 26, 1998 and issued on November 14, 2000. Lyke (EX1003) describes an “advanced instrument controller (AIC).” The AIC is a “MCM design [that] incorporates a CPU, volatile and non-volatile memories, an analog ASIC,” and “an embedded smart power convertor,” among other components. EX1003, Abstract. These components are shown in FIG. 1 of Lyke, which provides a block diagram schematic of the AIC:

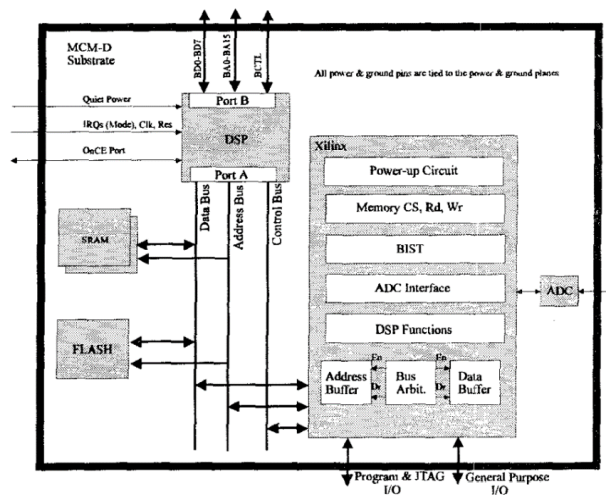


Lyke, EX1003, FIG. 1. Lyke also describes that “[t]he AIC contains internal oscillators 8, at least two, one for high-frequency operation and one for low-frequency operation.” *Id.*, 4:42-46. Lyke states that the “distinction of ‘two’ oscillators is important, as it is necessary for power preservation to maintain an independent oscillator that operates at a lower frequency.” *Id.* Lyke describes “analog to digital and digital-to-analog converters (ADCs and DACs).” *Id.*, 4:59-5:25. Lyke describes “variations” of the MCM design. For example, Lyke describes a “RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU and access of the non-volatile memory might also be included [in the MCM].” *Id.*, 8:55-59. (As an aside, it was well known to the POSITA that “SRAM” is “static random access memory” and is a type of volatile

memory, meaning that the memory maintains its data only when powered. Similarly, “FLASH” memory was a well known type of non-volatile memory, i.e., a memory that holds data even when not powered. *See, e.g.,* EX1003, Fig. 1 & 2:5-34.)

B. Overview of Dehkordi (EX1004)

40. Dehkordi describes a “typical application of a MCM [multi chip module] including a processor, memory, and gate-array.” EX1004, 1. Figure 1 of Dehkordi shows a block diagram of the system, which includes a “DSP [digital signal processor] processor along with 256 K-byte of SRAM [volatile memory], 128 K-byte of FLASH [non-volatile] memory, 10K-gate FPGA [field programmable gate array], and a 6-channel 12-bit ADC [analog-to-digital converter].” *Id.*



EX1004, FIG. 1.

41. Dehkordi indicates the MCM was “designed to exploit the multi-processing capability of the [processor]” and that the “FPGA is primarily a hardware pre-processor of incoming data but also provides other generic logic functions required for

implementation of the entire subsystem.” EX1004, 1. Dehkordi also describes that “[a] portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the [MCM],” and that the “FPGA can easily be reconfigured to route these lines to the module pins.” *Id.*, 3. The particular DSP used in the system described by Dehkordi is the Motorola 96002 digital signal processor, and the particular FPGA is the Xilinx 4010 FPGA. The Motorola 96002 digital signal processor and the Xilinx 4010 FPGA are described in more detail in the Motorola 96002 Manual (EX1013) and the Xilinx 4010 FPGA Manual (EX1014), respectively.

C. Overview of Frantz (EX1005)

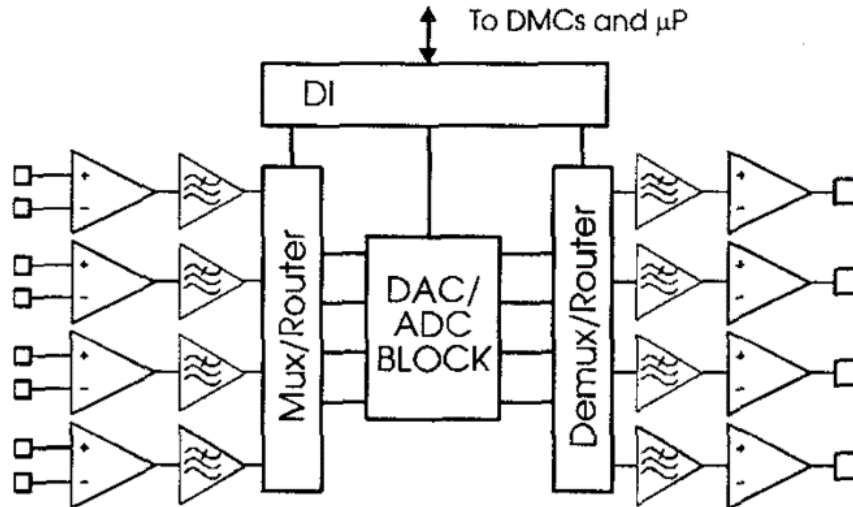
42. Frantz describes the “TMS320C25 digital signal processor” which has “[f]our-k words of on-chip program ROM” for storing programs run by the processor. EX1005, 2; *id.* (“4K 16-bit words of on-chip masked ROM”); *id.* at Fig. 1; *id.* at 4 (“Memory allocation. As mentioned above, the TMS320C25 provides 4K 16-bit words of on-chip program ROM.”); *id.* at 13 (“programs can be stored in ROM or downloaded via the system bus into program RAM.”). “Large programs can execute at full speed from this memory space.” *Id.* at 2. TMS320C25 processor can be “a stand-alone system (that is, as a single processor using 4K words of on-chip ROM and 544 words of on-chip RAM),” and optionally be a system to which “an external data RAM and a PROM/EPROM have been added.” *Id.* at 13. Frantz describes that “[t]he program bus can supply data from internal or external memory (RAM or ROM) and still maintain

single cycle operation.” *Id.* at 6. “The TMS320C25 is designed for real-time DSP and other computation-intensive tasks in telecommunications, graphics, image processing, high-speed control, speech processing, instrumentation, and numeric processing.” *Id.* at 15. For example, operating as a stand-alone system, the processor’s “large on-chip RAM of 544 words and on-chip ROM of 4K words allow it to execute a 256-tap adaptive filter (32-ms echo cancellation) without external data or program memory.” *Id.* at 17. Furthermore, “[p]rograms can also be downloaded from slow external memory to on-chip RAM for full-speed operation.” *Id.* at 2-3.

D. Overview of Faura (EX1006)

43. Faura is a paper titled “A Novel Mixed Signal Programmable Device with On-Chip Microprocessor,” and describes a “field programmable mixed signal integrated device consisting of a Field Programmable Gate Array (FPGA), a set of programmable and interconnectable analog cells, and a microprocessor core.” EX1006, 1. Faura describes “configurable analog hardware” that includes digital-to-analog converters and analog-to-digital converters. For example, Faura describes a “DAC/ADC block” that “is especially flexible and actually quite suitable for analog programmable hardware, in that it can be configured as a 10 bit block, two 9 bits blocks or four 8 bits blocks. Each block can be independently configured as [a] DAC or ADC.” EX1006, 2. The output of these blocks are provided to both the programmable logic (denoted DMC) as well as to a

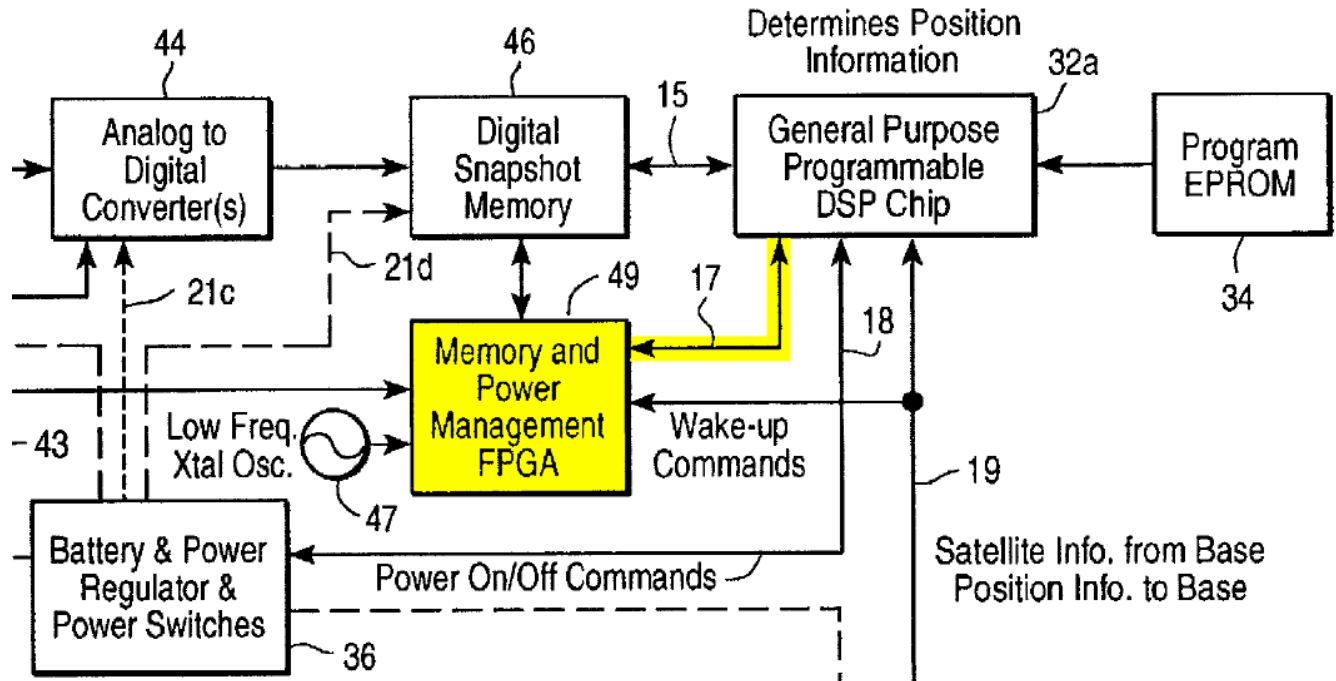
microprocessor (denoted μP). Figure 3 of Faura illustrates an example of this arrangement:



EX1006, FIG. 3.

E. Overview of Krasner (EX1007)

44. Krasner describes a system that includes a “DSP” processor, an FPGA, a volatile memory (“snapshot memory”), a non-volatile memory (“EPROM”), and analog to digital converters. These components are shown in the schematic block diagram of FIG. 1B.



EX1007, FIG. 1B (partial, annotated).

45. Krasner describes that a portion of the “memory and power management FPGA” is configured to activate other parts of the system by waking up the DSP. For example, Krasner indicates that “the FPGA 49, a low power device, serves to wake-up the DSP 32a chip.... The DSP 32a selectively powers on or reduces power to different components, according to a power management method.” EX. 1007, 8:26-42. Krasner also describes the “power management FPGA” signaling components to go into a deactivated state. *Id.*, 9:9-9-12 (“the power consumed by a component may be reduced by signaling to the component (as in the case of DSP 32a via interconnect 17 in FIG. 1B) to reduce power or wake up to full power”). I note that Krasner also describes other functions of the FPGA, including a portion of the FPGA that is responsible for “memory control and management.” EX1007, 9:17-23. “The memory and power management

FPGA 49 provides memory control and management, including addressing operations when data is being stored into the memory 46 from the [analog to digital] converters 44 or when the DSP component 32a is reading data from the memory 46.” *Id.* “The FPGA 49 may also be controlling other memory functions such as memory refresh if necessary.” *Id.*

F. Overview of Christian (EX1008)

46. Christian is titled “Power supply circuit for a data processor” and describes a system with a processor, memory, and power management circuitry. EX1008, Title, Abstract, FIGS. 1-3. Christian indicates that “when the processor is not in operation, the power supply applies no power to the processor.” *Id.*, 1:44-46. The system includes circuitry that “powers up and applies power to the processor in response to any input to the processor that calls for operation of the processor.” *Id.*, 1:46-48.

G. Overview of Steele (EX1009)

47. Steele is titled “Programmable logic having selectable output voltages” and describes an FPGA in a system that is configured to accept an input voltage and output a variety of voltages. EX1009, 4:6-65. A “user can select a particular voltage level for setting certain output signals” and the output voltages are “derived from that signal’s input power supply.” *Id.*, 2:29-65. An “object of the present invention is to provide a user with the capability of selecting a voltage level for an output signal, irregardless of the input voltage level,” and “to provide an output signal voltage level which is derived

from that signal's input power supply. These and other objects of the present invention are implemented in a programmable logic device wherein a user can select a particular voltage level for setting certain output signals." *Id.*, 2:37-47.

48. Steele describes that the "FPGA is comprised of eight configurable function blocks (CFBs)" and that, in one example, the FPGA receives an input voltage level of "5 volts." EX1009, 4:6-16; 4:28-49; *see also* 4:50-5:9; FIGS. 1-7. Each CFB is used to convert the input voltage to a desired output voltage to be used by other components. *Id.* The "user has the ability to choose the voltage level for signals output from the CFBs. This holds true, irregardless of what voltage levels are for the input signals. Thereby, the [FPGA] can act as an interface between external devices having different operating voltages." *Id.* EX1009, 4:50-58; 4:29-49 ("In this manner, a user can specify a plurality of different voltage levels for output signals."). Steele describes an example in which the FPGA outputs have operating and reference voltages of 5 volts and 3 volts. "[O]utput signals from CFB0 are at a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference," and "output signals generated by CFB1 are at a 3 volt level. These 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference." EX1009, 4:37-59. A POSITA would have readily recognized from Steele's description that other output voltage levels can be used as appropriate for other system components. For example, Steele indicates that "a plurality of different voltages can be supplied to the V_{cc0} pins of different functional

blocks, resulting in a plurality of different voltages, as desired, for output signals.” *Id.*, 2:62-65.

VII. GROUND 1: CLAIMS 1 AND 4 ARE OBVIOUS IN VIEW OF LYKE, DEHKORDI, FRANTZ, AND FAURA

49. For the reasons explained in detail below, and based on my review of the ’177 patent, the prosecution file history of the ’177 patent, and the prior art references cited here, it is clear that a POSITA would have readily understood that the teachings of Lyke, Dehkordi, Frantz, and Faura render obvious claims 1 and 4.

A. Combination of Lyke, Dehkordi, Frantz, and Faura

i. Lyke and Dehkordi

50. A POSITA would have been prompted to utilize the teachings of Dehkordi, including an FPGA for digital signal multi-processing, when implementing an MCM system in accordance with the teachings of Lyke, so as to achieve known benefits, and have had a reasonable expectation of success in doing so, including for the reasons I discuss below.

51. As I discussed above, Lyke describes an MCM design for signal processing tasks, and describes numerous example signal processing applications:

Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management, security systems, miniature weapons computers, space probe central control processor, beacon processor, and jet engine control. AICs could also be used on the manufacturing floor for smart, discontinuous low-level sensing, test

equipment probes, embedded credit card processors, wearable computers, or remote data logging.

EX1003, 8:66-9:11. Each of those systems involves signal processing (e.g., “cryocooler refrigerator controllers, distributed health and status monitoring systems”; “smart, discontinuous low-level sensing, test equipment probes”, etc.). Notably, Lyke also describes:

A RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU and access of the non-volatile memory might also be included [in the MCM].

EX1003, 8:55-59. Dehkordi provides additional details that a POSITA would have been prompted to look to for implementing such a system, and explained how such a system could be built. For example, Dehkordi specifies specific parts and shows how those parts interact and communicate with each other, EX1004, 1-3. Indeed, based on Lyke and Dehkordi’s teachings, a POSITA would have reasonably expected success in making the combination, especially in view of Dehkordi’s description of details of physical hardware in a system similar to that described by Lyke. *Id.* Multiple reasons confirm this analysis, as I describe in more detail below.

52. As a first reason, a POSITA would have been motivated to combine Lyke and Dehkordi based on Lyke’s explicit description of FPGAs. Lyke describes integrating an FPGA into the MCM in brief, and a POSITA would have thus been prompted, based on Lyke’s description of FPGAs, to look to known implementation

details from other sources, such as described by Dehkordi. I note that a POSITA would have been particularly prompted by Dehkordi because of the known benefits of FPGAs in such applications. For example, a POSITA would have been motivated to utilize an FPGA to facilitate near real-time operation and reduce latency. Reducing latency would have been recognized as particularly beneficial in applications in which the instrument controller is part of a control loop. A POSITA would have been motivated to impart an MCM in accordance with Lyke with such benefits.

53. As a second reason, a POSITA would have been led to combine Lyke and Dehkordi to achieve known benefits for such applications as signal processing systems suitable for use in outer space (e.g., as part of a space probe). I note that Lyke specifically describes use of an MCM in the “Deep Space II” system. EX1003, 5:6-16; 8:27-40 (“A specific experimental implementation of the AIC is on JPL’s Deep Space II (DS2) mission.”). A POSITA would have recognized the benefits of “field programmable” capabilities of an FPGA, especially in space applications in which the system is not readily accessible by human operators; for example see EX1015, 8 (noting advantage of “embedded programmable logic arrays (i.e., field programmable gate arrays), and even a programmable internal switch matrix for signal re-routing”). Such capabilities would facilitate updates to digital signal processing algorithms, as new experiments were carried out, etc. EX1043, 1 (“[T]here has been a tremendous interest in re-programmable FPGAs for the potential realization of a ‘re-programmable

satellite.”). A POSITA would have additionally been aware of further advantages of performing parallel signal processing using a FPGA (e.g., instead of simply using a general purpose processor), which was well-known prior to the '177 patent. Indeed, doing so would have facilitated reduced energy usage (and reduced temperature rise), and weak signal integration would have been performed directly on received and down converted storage (e.g., without energy associated with storing the data). Relatedly, use of an FPGA in this manner would have facilitated reduced physical volume because direct processing on incoming data would reduce the need for memory to store such data.

54. As a third reason, a POSITA would have been prompted to combine Lyke and Dehkordi in view of other known benefits of FPGAs in MCM systems, as discussed in other prior art publications. As one example, Avery (EX1015) discussed MCMs, including the physical module described in Lyke and other similar MCMs, and described that “embedded programmable logic arrays (i.e., field programmable gate arrays), and even a programmable internal switch matrix for signal re-routing” were an “intriguing possibility” for space-targeted MCM designs. EX1015, 8 (“Other intriguing possibilities for future controllers includes improved support for ‘plug and play’, embedded programmable logic arrays (i.e., field programmable gate arrays), and even a programmable internal switch matrix for signal re-routing.”). For these reasons, a POSITA would have sought out Dehkordi’s teachings to improve Lyke’s MCM in

accordance with the known benefits of integrating such capabilities into the MCM system using FPGAs, including Dehkordi's teaching that "portion of the FPGA is configured for multi-processing bus arbitration" and of the "easily... reconfigured... rout[ing]" of "data and address" lines. EX1004, 3. Here again, I note that a POSITA would have reasonably expected success in the combination given the similarities of the systems and discussion of use of FPGAs in similar prior art designs. *See, e.g., id; see also* EX1024, Abstract; 3:7-16 ("As shown, hybrid processor 101 comprises microprocessor (MP) 113 situated on a first level and pluggable into a second level, field programmable gate array (FPGA) 115 coupled to microprocessor 113, and controller unit 117 coupled to both, microprocessor 113 and FPGA 115. As a hybrid of a microprocessor and FPGA, processor 101 integrates FPGA and microprocessor technology to enhance algorithm execution performance.").

55. As a fourth reason, a POSITA would have been prompted to implement an MCM described by Lyke in accordance with Dehkordi's teachings because doing so would have been a common application of a known technique for utilizing an FPGA for digital signal multi-processing when implementing a known MCM system ready for improvement to yield predictable results. Indeed, a POSITA would have been aware of prior art references demonstrating that "the concept of parallel processing and the use of field programmable gate arrays is not new." EX1025, 2:27-31. I note that a POSITA would have recognized that this implementation (applying Dehkordi's suggestions to

Lyke's system) would not have significantly altered or hindered the functions performed by Lyke's system, and it would have been a relatively straightforward and ordinary task for a POSITA given the similarity of the system architecture in Lyke and Dehkordi.

ii. Lyke, Dehkordi, and Frantz

56. A POSITA would have been motivated to combine Frantz's teachings, including to use an embedded memory in a processor for executing instructions without loading instructions from a separate memory chip, e.g., a non-volatile memory, with the Lyke-Dehkordi combination, and had a reasonable expectation of success in doing so, including for the multiple reasons that I describe in more detail below.

As a first reason, a POSITA would have been prompted to combine Lyke, Dehkordi, and Frantz to have embedded memory in a processor for executing instructions in order to avail Lyke-Dehkordi of the physical space and weight reduction benefits: A POSITA would have recognized from Frantz's description of the embedded memory the space-saving benefits of such a configuration, as compared to a separate memory with an added footprint, for example. Lyke explicitly mentions "dimensionally constrained and/or remote locations" as target applications for its system. EX1003, 8:66-9:11. An embedded memory in accordance with Frantz reduced the need for extra physical chip, advancing Lyke's stated objective by providing yet further space savings. This was a recognized advantage for satellites and other devices intended for outer space, and where every dimension of the electronics was scrutinized for size and weight

concerns, because of limited payload and the effect on fuel. EX1047, 2 (“Today, Honeywell is transferring the five-chip [spaceborne module] design into a single-chip package significantly reducing size, weight, and power.”). Notably, the TMS320C25 processor described by Frantz was used in the Mars Global Surveyor Thermal Emission Spectrometer to provide DSP functionality. EX1028, 34 (“The digital signal processing electronics utilize a space-qualified Texas Instruments TMS320C25 digital signal processor clocked at 7256 kHz.”).

57. As a second reason, a POSITA would have been prompted to combine Lyke, Dehkordi, and Frantz to have embedded memory in a processor for executing instructions in order to provide reliability advantages. A POSITA would have readily recognized the importance of reducing failure rate for systems deployed to a “remote location,” as described by Lyke, and would have recognized that such benefits would have been achieved with embedded memory in the processor in accordance with Frantz. Separate memories in rough environments often called for “hardened” chips, such as “radiation hardened chips,” to reduce errors caused by ionizing radiation and such parts were difficult to source and expensive. EX1042, 1 (“Radiation hardening using specific process technology is an expensive process and, when used for a low-volume production, will lead to very costly parts.”). Combining Frantz’s teachings with the Lyke-Dehkordi combination would have been recognized as beneficially reducing the number of expensive parts by effectively combining two parts into one. Cf. EX1047, 2

(discussing advantages of combining multiple “fully-hardened” failure-tolerant chips into a single chip design).

58. As a third reason, a POSITA would have recognized the reduced energy usage, which is particularly relevant in space. Implementing the system in accordance with Frantz would facilitate less energy because the instructions would be available in the embedded memory (e.g. rather than called up from a separate non-volatile memory). The POSITA would have recognized this as a goal in space systems. *See e.g.*, EX1047, 2 (“Today, Honeywell is transferring the five-chip [spaceborne computer] design into a single-chip package significantly reducing ... power.”).

59. Additionally, reduced power usage by the combination would have additional benefits, including reduced temperature fluctuation and reduced peak operating temperature. A POSITA would have recognized the significance of temperature rise in modeling system performance, and the benefits of MCM instrument controllers with reduced temperature rise.

60. Relatedly, a POSITA would have been prompted to avail the combined system of embedded memory in the processor in accordance with Frantz in order to reduce return-to-sensing latency. For example, because a program is available in the embedded memory and not off-chip, the latency of program access is reduced. This was recognized as a concern in space systems (EX1016 (discussing “the latency of the

MOVX (move using external memory)” command) and an embedded memory would avoid extra delay.

61. As a fourth reason, a POSITA would have been prompted to combine Lyke, Dehkordi, and Frantz to have embedded memory in a processor for executing instructions because doing so would have been a common application of a known technique to a known MCM system ready for improvement to yield predictable results. As one example, McMahon describes a known design that provided a “microprocessor with an embedded read-only instruction memory.” EX1037, 10:64-65. Though the embedded instruction ROM was a commonly understood idea, Frantz explicitly teaches the use of such a ROM for storing an initialization program that enables the processor to start up processing, which would have been recognized as especially beneficial where a module had a specialized purpose (such as a controller) such that a ROM would provide a program for execution by the processor without loading the program from an external memory. Indeed, a processor with an embedded ROM for storing initialization program was a well-understood processor design approach, as corroborated by other pieces of prior art that would have been known to the POSITA; as one example, Nishitani’s digital signal processor also has an embedded “instruction ROM” containing an initialization program. EX1027, 2 (“The processor includes two 32-bit 512-word data RAMs (RAM0, RAM1), a 32-bit 1024-word data ROM (DATA ROM) and a **32-bit 2048-word instruction ROM (INST. ROM).**”); *id.* at 4 (“An 512-point complex FFT can be

computed in 4.6 msec using only on-chip memories.”).

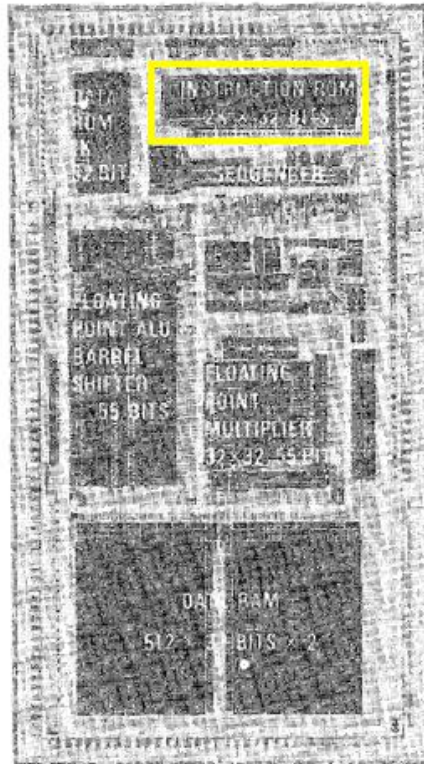


Fig. 5 PHOTOMICROGRAPH

EX1027, FIG. 5 (annotated to highlight instruction ROM embedded in the processor).

iii. Lyke, Dehkordi, Frantz, and Faura

62. A POSITA would have been motivated to combine Faura’s teachings, including to use a flexible analog-to-digital-converter (ADC) and digital-to-analog converter (DAC) with variable bit depths, with Lyke-Dehkordi-Frantz, and had a reasonable expectation of success in doing so, including for the multiple reasons that I describe in more detail below.

63. As a first reason, a POSITA would have been prompted to utilize a flexible analog-to-digital-converter (ADC) and digital-to-analog converter (DAC) with variable bit depths, in accordance with Faura, to facilitate flexibility and support a variety of design applications. EX1006, 2. I note that Lyke itself describes that its system was applicable in a variety of applications, each with different sensor requirements. EX1003, 8:66-9:11 (listing security systems, weapons computers, discontinuous low-level sensing, jet engine control, as example applications). For instance, for a weapons computer where precision is critically important, high resolution ADC or DAC would be desired. On the other hand, a discontinuous low-level sensing on the manufacturing floor may require comparatively low resolution ADC. Even in the same application, it was well known that multiple ADCs or DACs operating at different bit depths was desirable. *See, e.g.*, EX1039 (another contemporaneous example, ADuC824), 5:

Because the two ADCs are separate simultaneous ADC conversions can be done on both the primary and auxiliary ADCs. This means that for example the temperature can be measured at the same time as another signal and the ADC conversion does not have to be waited for. The resolution of the auxiliary ADC is only 16 bits to keep the power consumed by this ADC to a minimum.

Thus, a POSITA would have recognized that Lyke's objectives would have been furthered, and the flexibility of its system enhanced, especially based on Faura's description of an "especially flexible" DAC/ADC block capable of providing variable bit depth converters. EX1006, 2 ("In particular, the DAC/ADC block is especially flexible and actually quite suitable for analog programmable hardware, in that it can be

configured as a 10 bit block, two 9 bits blocks or four 8 bits blocks. Each block can be independently configured as DAC or ADC.”).

64. As a second reason, a POSITA would have been prompted to combine Faura’s teachings with Lyke-Dehkordi-Frantz for applications such as MCMs with programmable instrumentation to efficiently develop MCM systems and reduce the need for costly development of multiple versions of “hardened” hardware. For example, a POSITA would have recognized, from the descriptions of Lyke, Dehkordi, Frantz, and Faura, the benefits of flexible DAC/ADC block so that the block could be reprogrammed for the appropriate experiment. This would have been recognized as particularly beneficial for applications where the digital signal processing experiments might change over time and/or physical accessibility may be limited or difficult, such as a space probe with the ability to run different types of experiences. *See, e.g.*, EX1003, 5:6-16; 8:27-40; EX1043, 1 (discussing the “re-programmable satellite”). For example, a POSITA would have recognized the ability to reduce digitation noise by reverting to a lower bit depth in measurements where high accuracy was not needed.

65. As a third reason, a POSITA would have been prompted to combine Lyke, Dehkordi, Frantz, and Faura to have a flexible analog-to-digital-converter (ADC) and digital-to-analog converter (DAC) with variable bit depths because doing so would have reduced power consumption by the ADC, as some sensor signals need not be monitored with high accuracy/precision (e.g. thermistor temperature measurements of spacecraft or

engine temperature). Having the ability to use a lower bit depth converter when feasible saves power. See EX1039, 6 (explaining that relative to the primary ADC with 24-bit resolution, “[t]he resolution of the auxiliary ADC is only 16 bits to keep the power consumed by this ADC to a minimum.”). And saving power was a recognized desired issue in low-power systems such as those operating in space. EX1015, 1 (“it is obvious that space systems benefit from low-power electronics for processing”); *id.* at 2 (“reduction of size, weight, and power is paramount in many space applications.”). Relatedly, a reduced battery size would be facilitated because peak power requirement of the battery could be reduced.

66. As a fourth reason, a POSITA would have been prompted to combine Lyke, Dehkordi, Frantz, and Faura to have a flexible analog-to-digital-converter (ADC) and digital-to-analog converter (DAC) with variable bit depths because doing so would have been a common application of a known technique to a known MCM system ready for improvement to yield predictable results. Commercial products that utilized multiple converters with multiple possible bit depths were known to the POSITA. As one contemporaneous example, the Analog Devices ADuC824 was a device with a processor, two ADCs operating at different bit depths (16- and 24-bit depths), and

program and data memory. *See* EX1038¹; *see also* EX1039, 6 (“Because the two ADCs are separate simultaneous ADC conversions can be done on both the primary and auxiliary ADCs. This means that for example the temperature can be measured at the same time as another signal and the ADC conversion does not have to be waited for. The resolution of the auxiliary ADC is only 16 bits to keep the power consumed by this ADC to a minimum.”). In short, use of ADCs and DACs with a processor and memory was known and readily implemented with MCM systems suggested by Lyke-Dehkordi-Frantz-Faura to yield predictable benefits (as I discussed above). Indeed, the POSITA would have had a reasonable expectation of success, especially because of examples of prior art with systems that used such variable converters. Here again, like the Lyke-Dehkordi-Frantz combination, Faura describes a device with an FPGA and processor, further confirming the POSITA’s reasonable expectation of success in making the combination. *See* EX1006, 1-4.

¹ Though a physical system and not itself prior art used in this IPR, the ADuC824 from 2001 (see data sheet EX1038 dated 2001, and FAQ EX1039 dated January 2001) supports my understanding of the contemporaneous knowledge of a POSITA and their reasonable expectation of success at the timeframe of the ’177 patent.

B. Analysis of Lyke, Dehkordi, Frantz, and Faura with respect to claims 1 and 4.

67. Based on my review of Lyke, Dehkordi, Frantz, and Faura, and my knowledge and experience in the field, a POSITA would have understood that the teachings of Lyke, when predictably combined with Dehkordi, Frantz, and Faura for the reasons described above, provide all elements of claims 1 and 4.

Element [1.pre] An instrument controller comprising:

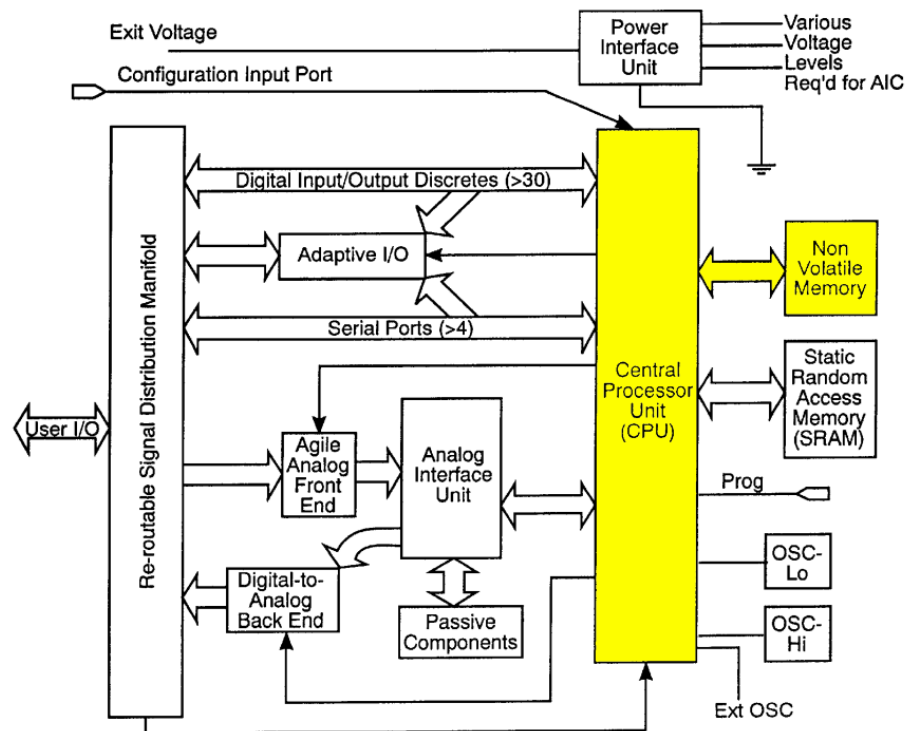
68. As I note above, ¶22, a judge in an earlier proceeding found that this patent claim preamble does not limit the scope of the patent. However, if the judges in this IPR proceeding were to disagree and find this preamble to be limiting, the Lyke-Dehkordi-Frantz-Faura combination provides “an instrument controller.” Lyke describes “a tightly coupled multi-chip Module (MCM),” which is used as an “Advanced Instrument Controller (AIC).” EX1003, 1:58-62. “The Advanced Instrument Controller (AIC) is a stand-alone low-to-medium performance microcontroller with versatile interface and operating options. A tightly coupled MCM design incorporates a CPU, volatile and non-volatile memories, an analog ASIC, a resistor ASIC, internal oscillator, an agile analog capability to implement a gain, offset, impedance, and filter control on all input channels, and an embedded smart power convertor.” *Id.*, Abstract.

69. I note that, similar to Lyke, Dehkordi describes “a multichip module” with “general purpose I/O,” which would have further led a POSITA to predictable combination to achieve an instrument controller as I discussed above, ¶¶35-38

(describing many uses for such controllers). EX1004, 1-3; *see also* EX1018 (describing a similar MCM where that comprises “an advanced instrument controller (AIC) [and] microsensors for temperature and humidity”).

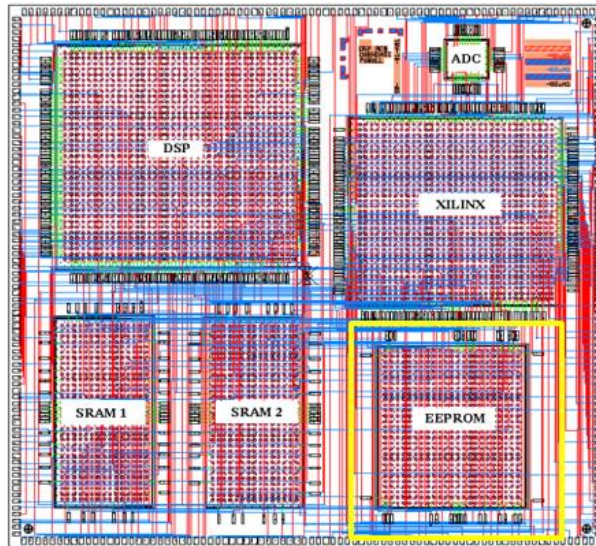
Element [1.1] a non-volatile memory storage component for program and data storage;

70. The Lyke-Dehkordi-Frantz-Faura combination provides a non-volatile memory storage component for program and data storage. Lyke describes a “non-volatile memory” used for “both program storage and data storage.” EX1003 4:14-15; *see also* 3:15-19 (“There is a large non-volatile program and data storage component 5.”).



EX1003, FIG. 1 (partial, annotated).

71. I note that, like Lyke, Dehkordi also describes a non-volatile memory component provided by its FLASH EEPROM. EX1004, Fig. 3. The FLASH EEPROM is shown below.



EX1004, FIG. 3 (annotated). Based on my knowledge and experience in the field, a POSITA would have recognized from Dehkordi's straightforward description that Dehkordi's non-volatile memory storage component is used for program and data storage including because this was a typical usage scenario with a Xilinx device; for example, Dehkordi uses an XC4000 FPGA; that data sheet (EX1014) describes use of an "industry standard" non-volatile memory EPROM for FPGA configuration storage, which includes both program and data. EX1014, 58; *id.*, 38.² Indeed, Dehkordi

² EPROM and FLASH were well-known examples to the POSITA back in 2001 of non-volatile memory that do not lose their memory contents when power is removed. See,

illustrates connection between the “FLASH” non-volatile memory and the “DSP” processor via the “Address Bus” and the “Data Bus.” EX1004, FIG. 1. Moreover, even if Lyke did not explicitly describe use of “non-volatile memory” used for “both program storage and data storage,” a POSITA would have been prompted to implement such memory in the MCM system to achieve widely known benefits of such a configuration, in accordance with Dehkordi. *See, e.g.*, EX1044, 1:30-40 (“EEProm’s ... are non-volatile, and retain their memory even after power is shut down”).

Element [1.2] a large volatile memory storage component for additional program and data storage;

72. The Lyke-Dehkordi-Frantz-Faura combination provides a large volatile memory storage component for additional program and data storage. For example, Lyke describes an “instrument controller” that has “a large volatile memory storage system with storage components comparable to or larger than the address space that the CPU operates upon.” EX1003, 9:15-22; *see also id.*, 4:35-41 (“The AIC contains a volatile static random access memory (SRAM) 6 with storage contents comparable to or larger than the address space that the CPU operates upon.”). Lyke’s large volatile memory storage system provides for additional program and data storage. Indeed, like the non-

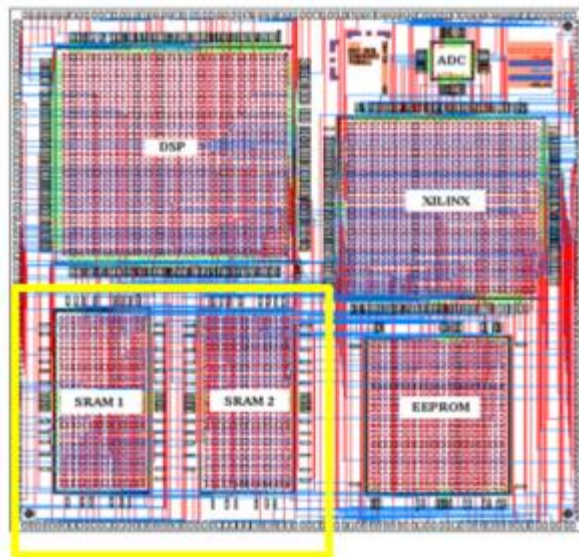
e.g., EX1044, 1:24-32 (describing background of a 1997 patent invention). In contrast, RAM memory devices like SRAMs or DRAMS “require constant power to maintain their memory (volatile)” and lose their contents if power is removed. *Id.*

volatile memory, Lyke indicates the “static random access memory” is connected with the CPU. *Id.*, FIG. 1; 4:35-41 (“The SRAM is always powered and contains a shadow copy of AIC program memory.”).

73. Lyke provides a “large” volatile memory storage component, as recited by the ’177 patent: The ’177 patent does not explicitly provide a lexicographic definition of “large,” but the ’177 specification describes an embodiment with “storage contents comparable to or larger than the address space that the CPU operates on.” EX1001, 6:45-46, 6:34-35. Lyke provides that same description verbatim, as quoted above, thereby providing a “large” volatile memory storage component consistent with the ’177 patent. *Compare* EX1003, 4:35-37 with EX1001, 6:34-35; *see also* EX1001, 6:43-46 (“the volatile memory can all be used to store programs and large amounts of data (greater than 2 megabits)”).

74. Even beyond the teachings of Lyke, Dehkordi describes “256 K-byte of SRAM” in the MCM, thereby likewise describing a large volatile memory storage component. EX1004, 1. Based on my knowledge and experience in the field, a POSITA would have known that Dehkordi’s volatile memory storage provides storage space for additional program and data storage, especially based on the connection between the “SRAM” volatile memory where program and data was typically stored, and the “DSP” processor via the “Address Bus” and the “Data Bus.” Moreover, I note that Dehkordi describes 256 K-bytes, or 2.048 megabits of volatile memory, thus

describing a specific example memory capacity recited by the '177 patent. EX1004, 89; EX1001, 6:43-46. A POSITA would have been prompted to utilize a large volatile memory storage, in accordance with Dehkordi, to achieve the predictable benefits of such memory, including additional storage space and reliability (e.g., as I discussed above), and with a reasonable expectation of success given the similarity in configuration and application.



EX1004, FIG. 3 (annotated).

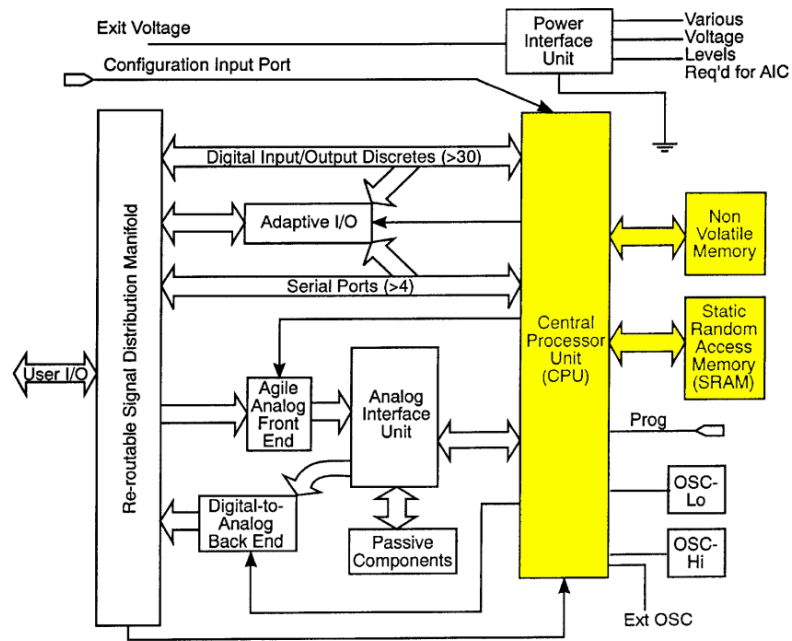
Element [1.3] a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory,

i. “a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components,”

75. The Lyke-Dehkordi-Frantz-Faura combination provides Element [1.3.i].

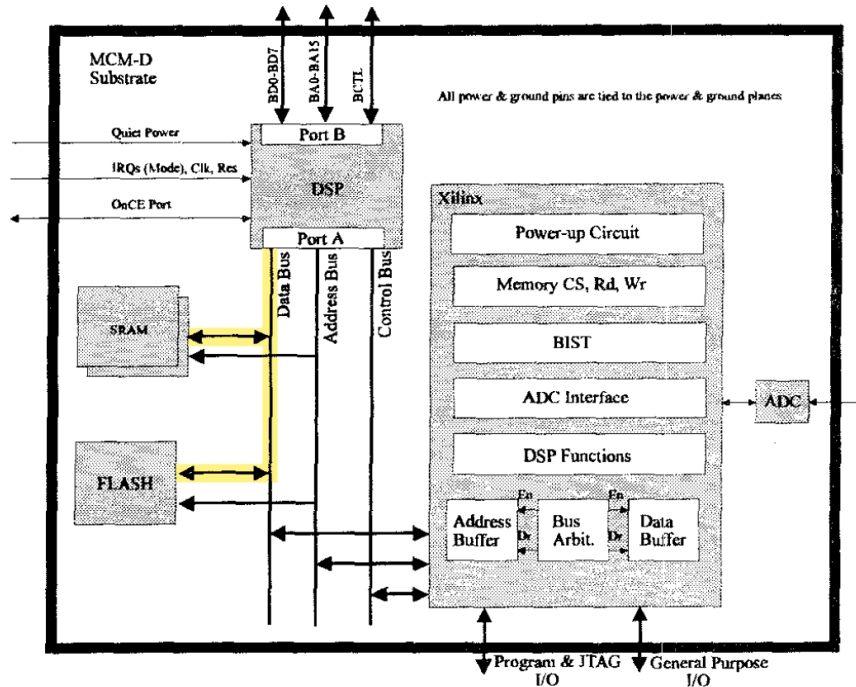
For example, Lyke describes a “tightly coupled MCM design” with a processor coupled

to the “non-volatile memory” and the “volatile static random access memory.” See EX1003, 3:66-4:41. FIG. 1 of Lyke illustrates the processor is coupled to both the non-volatile and large volatile memory storage components.



Lyke, EX1003, Fig. 1 (annotated)

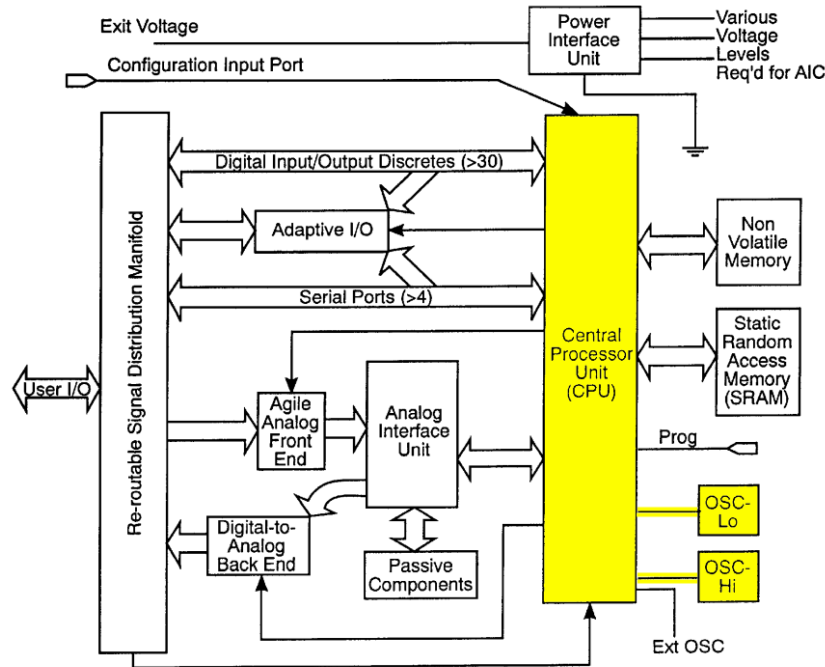
76. Even beyond Lyke’s teachings, Dehkordi describes a processor coupled to the “SRAM” (the large volatile memory storage component) and the “FLASH” (the non-volatile memory storage component), via a “Data Bus” and “Address Bus.” EX1004, Fig. 1. These connections are illustrated in FIG. 1 of Dehkordi. Such a configuration, and known benefits (e.g., as discussed above), were widely known to POSITA and readily implemented with a reasonable expectation of success, especially given the similar configuration and application described by Lyke.



Dehkordi, EX1004, Fig. 1 (annotated).

ii. “... the processor capable of high-frequency and low-frequency operations”

77. The Lyke-Dehkordi-Frantz-Faura combination provides Element [1.3.ii]. For example, Lyke describes an “AIC contain[ing] at least two [internal oscillators], one for high-frequency operation and one for low-frequency operation.” EX1003, 4:42-44. In one example, Lyke describes “an 11 MHz oscillator and 200 Hz oscillator for the high and low frequency internal reference, respectively” to drive the processor. *Id.*, 4:55-57. The two oscillators are directly coupled to the processor. *Id.* at Fig. 1.



EX1003, FIG. 1 (annotated). Lyke's description and connection between processor and oscillators that provide a "high and low frequency internal reference" indicate that the processor is capable of high-frequency and low-frequency operations. Indeed, such a configuration was well-known. As another example demonstrating this configuration in the background art, Oz (EX1026) describes high-frequency and low-frequency oscillators as "means for switching the CPU clock signal from the first clock source to the second clock source." EX1026, 98:59-61; *see also id.*, 14:16-17 ("Two crystal clock oscillators, 24a and 24b provide the basic frequencies needed. The high-speed oscillator 24a is designed to operate with an 40.96 MHz crystal. The low-speed oscillator 24b is designed to operate with a ceramic resonator at a frequency of 455 KHz.").

iii. "... and [the processor] having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory,"

78. The Lyke-Dehkordi-Frantz-Faura combination provides Element [1.3.iii].

For example, Frantz describes the “TMS320C25 digital signal processor” which has

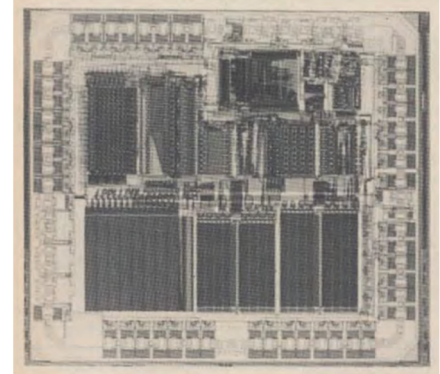
“[f]our-k words of on-chip program ROM” for storing

programs run by the processor. EX1005, 2. The

program ROM (read-only memory) is an embedded

memory located within the TMS320C25 processor

(i.e., the memory is embedded within the processor).



Frantz, EX1005, 1.

EX1005, 2 (“Some of the major features of the

TMS320C25 are... 4k 16-bit words of on-chip masked ROM”). Furthermore, the use of

embedded ROM permits the DSP to begin processing immediately on boot without

needing to retrieve a program from a separate non-volatile storage each time power is

interrupted. Frantz describes that the processor’s “large on-chip RAM of 544 words and

on-chip ROM of 4K words allow it to **execute a 256-tap adaptive filter (32-ms echo**

cancellation) without external data or program memory.” EX1005, 17. In other

words, in this digital signal processing embodiment, Frantz’s on-chip program ROM

(embedded memory) stores initialization program that allows the DSP to start processing

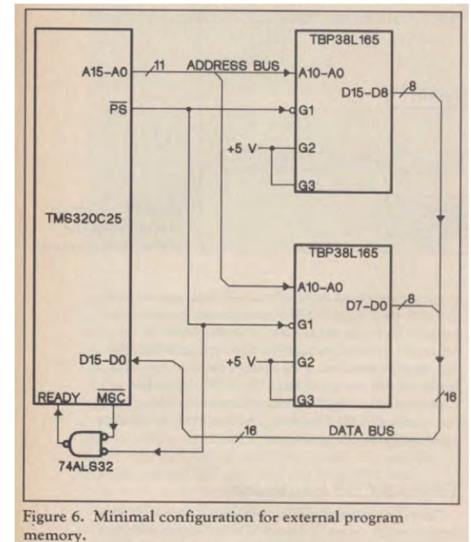
without first retrieving a program from the non-volatile memory.

Frantz also describes in Figure 6 a different configuration that includes external

program memory. EX1005, 13 (“In Figure 6, an external data RAM and a

PROM/EPROM have been added.”). When configured with external program memory,

“[p]rograms can also be downloaded from slow external memory to on-chip RAM for full-speed operation.” EX1005, 2-3; *see also id.* at 13 (“Direct memory access. The TMS320C25 supports direct memory access to its external program/data memory and I/O space through its HOLD and HOLDA signals. Direct memory access can be used for multiprocessing:



Frantz, EX1005, Fig. 6.

Execution on one or more processors can be temporarily halted to allow another processor to read from or write to the halted processor's local off-chip memory By asserting RS in conjunction with HOLD, the master processor can load the slave's local program memory with the necessary initialization code on reset or power-up. . . . programs can be stored in ROM or downloaded via the system bus into program RAM.”).

Therefore, a POSITA would have recognized Frantz’s teaching of starting up processing with the ROM-stored initialization program without first retrieving a program from the non-volatile memory, especially as Frantz contrasts that use with the alternate scenario of needing to first download a program from a “slow external memory,” e.g., an off-chip non-volatile RAM. EX1005, 4. This is especially so because a processor with an embedded ROM storing an initialization program was a well-understood microprocessor design approach. EX1027, 2 (“The processor includes two 32-bit 512-

word data RAMs (RAM0, RAM1), a 32-bit 1024-word data ROM (DATA ROM) and a 32-bit 2048-word instruction ROM (INST. ROM).”); *id.* at 4 (“An 512-point complex FFT can be computed in 4.6 msec using only on-chip memories.”); EX1037, 1:10-23 (“microprocessor [with] an embedded ROM”), 10:64-11:4; EX1039, 2 (describing the “‘power-on configuration routine’ that runs every time you apply power to the chip or reset it” in an on-chip ROM).

Element [1.4] at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

79. The Lyke-Dehkordi-Frantz-Faura combination provides this element. As I discussed previously (*see*, Analysis of Element 1.3 at ¶77 [1.3.ii]), Lyke describes an AIC having at least two internal oscillators, one for high-frequency operation and one for low-frequency operation, which are illustrated as coupled to the processor. EX1003, 4:42-44 (“The AIC contains internal oscillators 8, at least two, one for high-frequency operation and one for low-frequency operation.”); FIGS. 1 & 2; *see also* EX1026, 98:59-61; 14:16-17. Lyke teaches that oscillators are used for “precise timing” and that “[a] typical AIC has an 11 MHz oscillator and 200 Hz oscillator for the high and low frequency internal reference,” i.e., the clocking signals. EX1003, 4:42-57. While taught in Lyke, this limitation would also be known to the POSITA based on background knowledge in the art that two oscillators running at different frequencies were commonly used to provide high and low frequency clock signals; *see, e.g.*, Oz, EX1026, which describes high-frequency and low-frequency oscillators as “means for switching the

CPU clock signal from the first clock source to the second clock source.” EX1026, 98:59-61; *see also id.*, 14:16-17 (“Two crystal clock oscillators, 24a and 24b provide the basic frequencies needed. The high-speed oscillator 24a is designed to operate with an 40.96 MHz crystal. The low-speed oscillator 24b is designed to operate with a ceramic resonator at a frequency of 455 KHz.”).

Element [1.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and

i. “a plurality of gates arranged in a field programmable gate array, ...”

80. The Lyke-Dehkordi-Frantz-Faura combination provides Element [1.5.i].

Lyke describes an MCM that includes one or more “**field programmable gate array(s)** interfaced internally within the AIC,” thereby providing a plurality of gates arranged in a field programmable gate array. EX1003, 8:55-69. An FPGA is a plurality of gates. *See, e.g.*, EX1014, 45 (showing the gates counts in the XC4000 FPGA family); EX1014, 1 (“Over 180,000 usable gates”).

81. Even beyond Lyke’s teachings, Dehkordi also describes this element.

Dehkordi describes “an MCM” that includes a “field programmable gate array.”

EX1004, 1. In particular, Dehkordi describes an FPGA provided by the Xilinx 4010 FPGA. I note that a POSITA would have readily recognized that an FPGA includes a plurality of gates, and the Xilinx 4010 manual explicitly indicates this fact. *See, e.g.*, EX1014, 1 (describing the FPGA includes “[o]ver 180,000 Usable Gates”).

ii. *“...the gate array coupled to the processor and configured to run independent processes in parallel with the processor; and”*

82. The Lyke-Dehkordi-Frantz-Faura combination provides Element [1.5.ii].

For example, Lyke describes “a RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU and access of the non-volatile memory might also be included [in the module].” EX1003, 8:55-59. Lyke’s description that the “RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU” provides that “the gate array [is] coupled to the processor,” which is how the FPGA can be configured. EX1003, 8:55-58. (The “program” running on the FPGA is more accurately described in the parlance as the “configuration” of the FPGA. *See, e.g.*, EX1014 (Xilinx XC4000 data sheet) at 3:

The devices are customized by loading **configuration** data into internal memory cells. The FPGA can either actively read its **configuration data** from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

EX1014, 3. I note that the configuration of a gate array (e.g., FPGA) coupled to a processor was well known in such applications prior to the ’177 patent. As one example of a POSITA’s knowledge, Halverson describes an FPGA “coupled to” the CPU.

EX1025, 2:50-52; 27:11-14 (“said field programmable gate array circuitry coupled to

said central processing unit so as to receive configuration data for configuring data for configuring said field programmable gate array.”).

83. A POSITA would have additionally recognized (e.g., from Lyke’s description that the FPGA is “configured [from] the non-volatile memory”) that Lyke provides that the FPGA is configured with a program (known as the “configuration” for the FPGA (*see* EX1025, 2:50-56 (“[FPGA] configuration data defines... what computation functions the field programmable gate array circuitry will perform.”); EX1014, 3)) that would run independently in parallel with whatever program code that was separately running in the processor, especially as Lyke is describing how FPGAs were typically deployed with processors prior to the time of the ’177 patent. EX1036 (“Kostarnov”), 4 (“The CPU and FPGA execute as two independent execution units.”); EX1025 (“Halverson”), 2:27-31 (“[T]he concept of parallel processing and the use of field programmable gate arrays is not new.”). Halverson further describes “parallel” as “[p]ertaining to a process in which multiple events or computations occur within the same interval of time, each handled by a separate but similar functional unit,” further confirming the common practice of an FPGA configured to run independent processes in parallel with the processor that would have been recognized from Lyke. *Id.*, 2:1-3. A POSITA would have readily recognized and been prompted to pursue the known benefits of using an FPGA to run independent processes in parallel with the processor

(e.g., as discussed above), and would have had a reasonable expectation of success in doing so.

84. Here again, Dehkordi confirms a POSITA's understanding based on Lyke. Dehkordi describes a gate array coupled to the processor that is configured to run independent processes in parallel with the processor. As I noted previously, Dehkordi depicts a Xilinx FPGA coupled to a Motorola digital signal processor. Such a configuration is described at page 1, and illustrated in FIGS. 1 and 3, of Dehkordi. The FPGA runs independent processes in parallel with the digital signal processor. For example, Dehkordi illustrates a "DSP functions" block of the FPGA, indicating a portion of the Dehkordi FPGA is configured for digital signal processing as part of its reconfigurable logic. EX1004, FIG. 1. Dehkordi additionally indicates the FPGA is a "pre-processor of incoming data." *Id.*, 1.

As another example of independent processes in parallel with the processor, Dehkordi describes that "a portion of the FPGA is configured for **multi-processing bus arbitration.**" EX1004, 3; FIG. 1. Dehkordi's description is that the FPGA is serving as what was recognized in the art as a "traffic cop" for routing data as the data is processed by either the FPGA or the DSP. *Id.*; *see also* EX1045, 1:49-68 (describing bus arbitration as a "traffic cop" role). Dehkordi's FIG. 1 illustrates this process with a "Bus Arbit." box in the FPGA. Indeed, Dehkordi explains that the FPGA "module was designed to exploit the multi-processing capability of the [DSP]." EX1004, 1. It makes

good technical sense to designate a part of the customizable FPGA as the full-time communication arbiter, since a portion of the gates can be dedicated to this arbitration task, rather than put this task on the general DSP, or other bus arbitration hardware.

As yet another example, Dehkordi describe the FPGA “also provides other generic logic functions required for implementation of the entire subsystem.” EX1004, 1. Dehkordi additionally describes a “RAM-based configuration where the configuration may come from outside the module.” *Id.*, 3. Dehkordi’s description that a “configuration [originates from] outside the module” provides that Dehkordi’s FPGA was running a separate configuration (i.e., programming) aside from what was running on the processor and would run independent processes in parallel with the processor. EX1004, 2:27-31. Again, FPGAs were typically deployed with processors in this independent manner. EX1036, 4 (“The CPU and FPGA execute as two independent execution units.”). And indeed, a POSITA would have been prompted to implement such a configuration to avail the system of the known benefits of a parallel configuration described above.

Element [1.6] a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

i. “a plurality of analog-to-digital converters for receiving a plurality of analog inputs,...”

85. The Lyke-Dehkordi-Frantz-Faura combination provides this element. As an initial matter, I note that during original examination of the application that led to the

'177 patent, the Examiner concluded that Lyke discloses “a plurality of analog-to-digital converts for receiving a plurality of analog inputs, digitizing said analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing said digital inputs to [the] processor.” EX1010, 57. The Examiner particularly referenced Lyke’s description at 3:28-33 and Fig. 1. *Id.* The Applicant of the '177 patent did not argue against the Examiner’s analysis and conclusion that Lyke provided the entirety of Element [1.6].

86. I agree that Lyke describes Element [1.6]. Indeed, I note that Lyke explicitly described that its system included a collection of analog function blocks that included multiplexed or non-multiplexed analog to digital convertors.” EX1003, 7:30-33 (describing “collection of analog function blocks; the d+e terminals represent multiplexed or non-multiplexed analog to digital convertors; and the f +g terminals represent digital to analog convertors.”). Lyke describes that its “AIC extends the useable range of ADCs and DACs by providing an agile analog capability 9. Agile analog implements a global gain and offset on all input channels, as well as channel specific values for gain and offset.” EX1003, 5:29-33. Lyke further describes “the bandwidth characteristics of the ADCs and DACs can be affected with a second-order programmable filter. All of these features are selectable for each channel.” *Id.* It was well known to the POSITA that an ADC block generates a digital output, which a digital processor can use as an input. *See* EX1029, Abstract (describing that an ADC “receives

the analog output as an input and provides a [] digital output” and a “digital processor ... receives the [] digital outputs.”); EX1030, 3:9-29 (“Each ADC digitizes a sample”).

87. In addition to Lyke’s teachings, Faura describes a similar system that includes a plurality of analog-to-digital converters that receive a plurality of analog inputs. For example, Faura describes a “DAC/ADC block” component and that multiple of these components exist on a chip. EX1006, 1-2 (“[e]ach FIPSOC family members [sic] will have a different number of these blocks.”). Faura describes that each DAC/ADC block “can be independently configured as [a] DAC or ADC.” EX1006, 2. “The DAC/ADC block is especially flexible [and] can be configured as a 10 bit block, two 9 bit blocks or four 8 bit blocks.” *Id.* For example, “two 9 bit blocks or four 8 bit blocks” are a plurality of analog-to-digital converters for receiving a plurality of analog inputs. *Id.* It was known to the POSITA that a multi-channel ADC was able to receive a plurality of analog inputs. *See, e.g.,* EX1030, 6:27-29 (“a dual-channel ADC can process two signals”); EX1031, 10:5-12 (“ADC is a conventional four channel ADC ... Left-right receiver coil is coupled to a first channel ... and up-down receiver coil is coupled to a second channel”).

88. Faura’s system provides a plurality of analog digital converters for receiving a plurality of analog inputs. EX1006, 1-2. My understanding is further confirmed by the FauraMoreno reference (EX1032), which is another prior art reference describing the same Faura system and including additional detail about Faura’s

DAC/ADC block. FauraMoreno indicates that the “ADC/DAC block is especially suitable for reconfigurable applications: it can be configured as ... two 9-bit DAC/ADCs, four 8-bit DAC/ADCs, or even one 9-bit DAC/ADC and two 8-bit DAC/ADCs at the same time.” EX1032, 3.

ii. “...*digitizing the analog inputs at one of at least two possible bit depths, ...*”

89. The Lyke-Dehkordi-Frantz-Faura combination provides this element. As I discussed above, the Examiner found Lyke to provide digitizing the analog inputs at one of at least two possible bit depths, as recited by Element [1.6]. EX1010, 57. Indeed, Lyke describes digitizing “a large number of analog inputs at high resolution (equal to or greater than 10 bits).” EX1003, 28:33. A POSITA would have readily recognized from Lyke’s description that “[e]qual to” 10 bits and “greater than 10 bits” are two possible bit depths. Moreover, Lyke describes the ASIC includes “thirty-two external analog inputs with 12-bit resolution” and also describes additional “channels with 10-bit resolution fed back to some of the internal A/D channels.” EX1003, 4:58-5:5. A “12-bit resolution” and “10-bit resolution,” as described by Lyke, would have been recognized by a POSITA as two additional examples of at least two possible bit depths, as recited by Element [1.6].

90. Even beyond Lyke’s teachings, Faura also provides digitizing the analog inputs at one of at least two possible bit depths. As I discussed previously, Faura

describes examples of digitizing the analog inputs at one of at least two possible bit depths, including 9-bit and 8-bit ADCs at the same time.

iii. “... *thereby generating digital inputs and providing the digital inputs to the processor;*”

91. The Lyke-Dehkordi-Frantz-Faura combination provides this element. A POSITA would have readily recognized from Lyke’s description that the combined system includes digital signals output by the analog to digital converters that are provided to the processor. For example, FIGS. 1 and 2 of Lyke illustrate the “analog interface unit” connected to “central processor unit (CPU).” EX1003, FIGS. 1-2. I note that an objective of the ADC was to allow processing on the “digital inputs,” e.g., by the processor, which is carried out by the processor receiving these inputs (e.g., as depicted in FIG. 12, below).³

³ The purpose of the ADC is to generate digital signals from an analog signal, so that the digital signals are “digital inputs” to something else. See EX1029, Abstract (describing an ADC “receives the analog output as an input and provides a [] digital output” and a “digital processor ... receives the [] digital outputs.”); EX1030, 3:9-29 (“Each ADC digitizes a sample”). These digital signals become the “digital inputs” to the next component in the system.

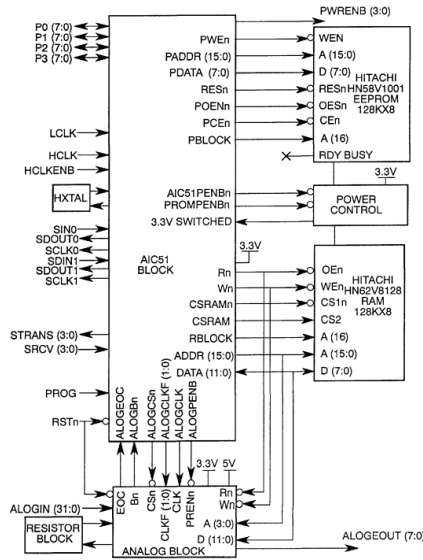
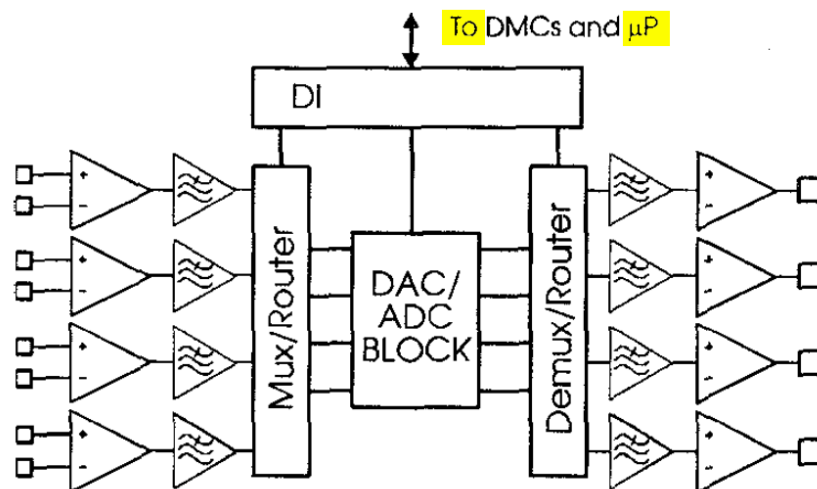


Fig. 12

EX1003, FIG. 12.

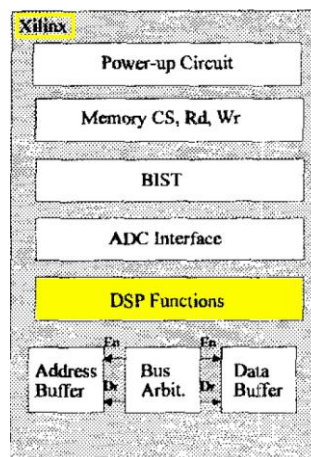
92. Even if Lyke didn't describe this element, Faura describes generating digital inputs and providing the digital inputs to the processor as recited by Element [1.6]. Faura illustrates connection of the output of DAC/ADC block to the microprocessor (denoted μP), providing digital inputs to the processor.



EX1006, Fig. 6 (annotated)

Element [1.7] wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

93. The Lyke-Dehkordi-Frantz-Faura combination provides this element. For example, Dehkordi describes a signal processing MCM having a Motorola 96002 DSP processor and an FPGA that is “a hardware pre-processor of incoming data.” Dehkordi indicates that the FPGA provides “DSP Functions,” i.e., [D]igital [S]ignal [P]rocessing functions. See EX1004, 1; FIG. 1. Dehkordi’s “DSP Functions” are being configured on a portion of the gates of the FPGA. Indeed, Dehkordi illustrates such a configuration in FIG. 1 as part of the “Xilinx” FPGA chip:



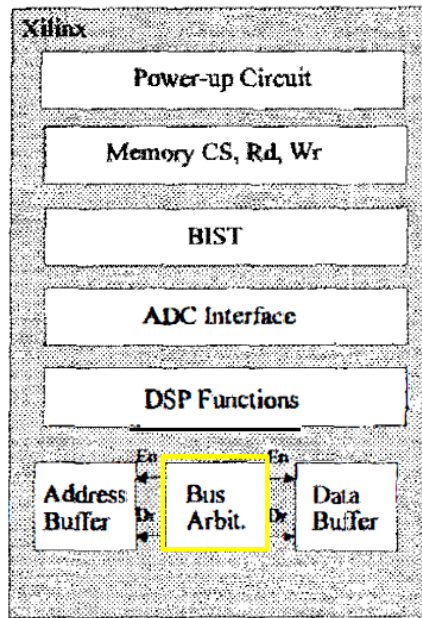
Dehkordi, EX1004, Fig. 1 (partial, highlighted).

Element [1.8] wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the instrument controller.

94. The Lyke-Dehkordi-Frantz-Faura combination provides this element. For example, Dehkordi describes that “[a] portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the

module,” and that the “FPGA can easily be reconfigured to route these lines to the module pins for possible probing and debugging during tests,” thereby describing a signal distribution matrix for rerouting signals within the instrument controller. First, as I noted above, Dehkordi’s description is that the FPGA is serving as what was recognized in the art as a “traffic cop” for routing data as the data is processed by either the FPGA or the DSP. *Id.*; *see also* EX1045, 1:49-68 (describing bus arbitration as a “traffic cop” role).

The Xilinx chip used in Dehkordi, part of the Xilinx 4000 series, was also known for having a “general routing structure that permits arbitrary point-to-point communication” due to the FPGA’s “switch matrix... routing structure.” EX1019, 3 & FIG. 6)); EX1004, 3; *see also* EX1015, 8 (describing “programmable internal switch matrix for signal re-routing”). In accordance with Dehkordi’s description, the Lyke-Dehkordi-Frantz-Faura thus includes a first portion of the FPGA for signal processing and a second portion of the FPGA for operating as a signal distribution matrix for routing data to the module pins (e.g., rerouting signals within the instrument controller), providing Element [1.8].



EX1004, FIG. 1 (partial) (depicting “Bus Arbit.”).

95. I note that configuring portions of FPGAs for different operations, and in particular use of FPGAs having a second portion of the gates in the field programmable gate array configured to operate as a signal distribution matrix for rerouting signals within the instrument controller, was a known and understood application of FPGAs. Such configurations provided the known benefit of a flexible signal routing, for example, and a POSITA would have been motivated to avail the combined system of such a feature, where the Xilinx FPGA reconfigurable fabric allows very flexible routing scenarios. EX1019, 3; FIG. 6 (“The Xilinx array is an ‘Island-style’ FPGA with logic cells embedded in a general routing structure ... The switch matrix allows this signal to travel vertically and/or horizontally from the switch matrix”). I also note that this was recognized as an application that would be desirable; for example, the Avery reference,

EX1015, describes a system with “embedded programmable logic arrays (i.e., field programmable gate arrays), and even a programmable internal switch matrix for signal re-routing.”

Claim [4] The instrument controller of claim 1, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.

i. *“a plurality of analog outputs, each output being controlled by an independent digital-to-analog converter, ...”*

96. The Lyke-Dehkordi-Frantz-Faura combination provides this element. As an initial matter, I note that during original examination of the application leading to the '177 patent, the Examiner concluded that Lyke described the features of Claim [4]. The Examiner indicated that Lyke discloses “a plurality of analog outputs, each being controlled by an independent digital-to-analog converter, each of said independent digital-to-analog converters being configured to convert from one of at least two possible depths to analog.” EX1010, 58. The Examiner specifically cited Lyke’s description at column 3, lines 63-65. Lyke additionally describes a “collection of analog function blocks [including] digital to analog convertors” (EX1003, 7:28-33), and, Lyke further describes that its “AIC extends the useable range of ADCs and DACs by providing an agile analog capability 9... Additionally, the AIC can implement gross impedance control on inputs and outputs by offering several switch-activated settings.” EX1003, 5:29-36. Lyke further describes “the bandwidth characteristics of the ADCs

and DACs can be affected with a second-order programmable filter. All of these features are selectable for each channel.” *Id.* The POSITA would know that a DAC (i.e., “digital to analog converter”) block generates an analog output. *See* EX1029, 1:51-53 (“DAC1 receives the digital code from ADC1 and converts this digital code back into an analog signal.”). I also note that, here again, the Applicant did not argue against the Examiner’s analysis and conclusion that Lyke describes these features.

97. Further beyond the examiner’s finding, Faura also describes these features. As I discussed previously (refer to Element [1.6]), Faura describes a similar system that includes a plurality of analog-to-digital converters that receive a plurality of analog inputs. For example, Faura describes a “DAC/ADC block” component and that multiple of these components exist on a chip. EX1006, 1-2 (“[e]ach FIPSOC family members [sic] will have a different number of these blocks.”). Faura describes that each DAC/ADC block “can be independently configured as [a] DAC or ADC.” EX1006, 2. “The DAC/ADC block is especially flexible [and] can be configured as a 10 bit block, two 9 bit blocks or four 8 bit blocks.” *Id.* For example, “two 9 bit blocks or four 8 bit blocks” are a plurality of analog-to-digital converters for receiving a plurality of analog inputs. *Id.* A multi-channel DAC had a plurality of analog outputs each being controlled by an independent digital-to-analog converter. *See, e.g.*, EX1003, 4:61-63 (“eight independently programmable digital-to-analog convertor (DAC) channels with 10-bit resolution.”); EX1006, 4 (“two 8-bit DACs, and then using these two DACs to

provide the [analog signals]”). Further, Faura’s system provides a plurality of plurality of analog outputs, each output being controlled by an independent digital-to-analog converter. EX1006, 1-2, 4. My understanding is further confirmed by the FauraMoreno reference (EX1032), which is another prior art reference describing the same Faura system and including additional detail about Faura’s DAC/ADC block. FauraMoreno indicates that the “ADC/DAC block is especially suitable for reconfigurable applications: it can be configured as ... two 9-bit DAC/ADCs, four 8-bit DAC/ADCs, or even one 9-bit DAC/ADC and two 8-bit DAC/ADCs at the same time.” EX1032, 3.

ii. *“...each of the independent digital-to-analog converters being configured to convert from one of at least two possible bit depths to analog.”*

98. The Lyke-Dehkordi-Frantz-Faura combination provides this element. As I discussed previously, the examiner found that Lyke described this feature. *See* Analysis of Element [1.6] and Claim [4.i]; EX1010, 58. I note that Lyke specifically describes the “AIC has analog voltage signals that can be individually set; an independent digital-to-analog convertor 4 controls each,” and describes “eight independently programmable digital-to-analog convertor (DAC) channels with 10-bit resolution.” EX1003, 4:58-5:5. The “bandwidth characteristics of the ... DACs can be affected with a second-order programmable filter.” *Id.*, 5:26-48. A POSITA would have readily recognized the use of multiple bit depths to achieve known benefits (as I discussed above regarding the Lyke-Dehkordi-Frantz-Faura combination). *Id.*; *see also, id.* 5:29-36 (“AIC extends the useable range of ADCs and DACs by providing an agile analog capability 9...

Additionally, the AIC can implement gross impedance control on inputs and outputs by offering several switch-activated settings,” and “the bandwidth characteristics of the ADCs and DACs can be affected with a second-order programmable filter. All of these features are selectable for each channel.”).

99. Second, even beyond Lyke , the combined system would have included this feature in accordance with Faura’s teachings. As I discussed above (refer to the analysis of Element [4.i], Faura describes multiple examples of digital to analog converters operating at one of at least two possible bit depths, including 9-bit and 8-bit DACs operating at the same time.

VIII. GROUND 2: CLAIM 2 IS OBVIOUS IN VIEW OF LYKE, DEHKORDI, FRANTZ, FAURA, AND KRASNER

100. For the reasons articulated in detail below, and based on my review of the ’177 patent, the prosecution file history of the ’177 patent, and the prior art references cited here, it is clear that a POSITA would have readily understood that the teachings of Lyke, Dehkordi, Frantz, Faura, and Krasner renders obvious claim 2.

A. Combination of Lyke, Dehkordi, Frantz, Faura, and Krasner

101. A POSITA would have been motivated to utilize Krasner’s suggestions of FPGA-controller power management to reduce power consumption in the Lyke-Dehkordi-Frantz-Faura MCM system, and have had reasonable expectations of success, including for the reasons I describe in the below paragraphs. Lyke itself referenced power consumption challenges, as did other relevant references of the time period.

EX1003, 4:3-17; 4:42-57 (describing objective to “minimize power consumption” in the MCM); EX1007, 9:9-15 (describing advantages to “signaling to the [DSP] component ... to wake up to reduce power or wake up to full power”); EX1016 (describing that “if power consumption can be made dramatically low ... then it is possible to consider large networks of controllers in satellites for fine grain health and status monitoring”). A POSITA would have been motivated to conserve battery power in the MCM system by utilizing FPGA-controller power management in accordance with Krasner, and would have recognized that enhanced power efficiency would facilitate new applications for the MCM system. In the combined system, a portion of the gates of the FPGA would have been configured for power management (e.g., to “wake up” the CPU of the combined system), in accordance with Krasner.

102. Multiple additional reasons would have prompted a POSITA to implement the Lyke-Dehkordi-Frantz-Faura MCM instrument controller utilizing FPGA-controller power management in accordance with Krasner, as I explain next.

103. As a first reason, a POSITA would have been motivated to combine Lyke, Dehkordi, Frantz, Faura, and Krasner to further Lyke’s stated objectives of managing power consumption. For example, a POSITA would have recognized from Lyke’s description that “the AIC typically physically powers down the non-volatile device when power consumption needs to be minimized” that powering down components on the MCM would be advantageous. EX1003, 4:3-17. Based on Lyke’s description, a

POSITA would have been motivated to seek out techniques for reducing power consumption in this way, including Krasner's suggestion of being able to shut down other parts of the device using a power management FPGA. A POSITA would have readily recognized that doing so would facilitate the predictable benefit of enhanced power savings, consistent with Lyke.

104. As a second reason, a POSITA would have sought out Krasner's power management FPGA technique because the Lyke-Dehkordi-Frantz-Faura system already included an FPGA, and implementing power management in accordance with Krasner's teachings would have produced a more efficient use of the FPGA. Based on my knowledge and experience in the field, a POSITA readily understood an FPGA to facilitate "a user to incrementally stuff in logic if there is availability." EX1009, 8:3-24. In other words, the FPGA facilitates additional functionality "for free" simply by configuring additional gates. *Id.* Accordingly, a POSITA would have been motivated to utilize the already-present FPGA to impart the system with enhanced power management.

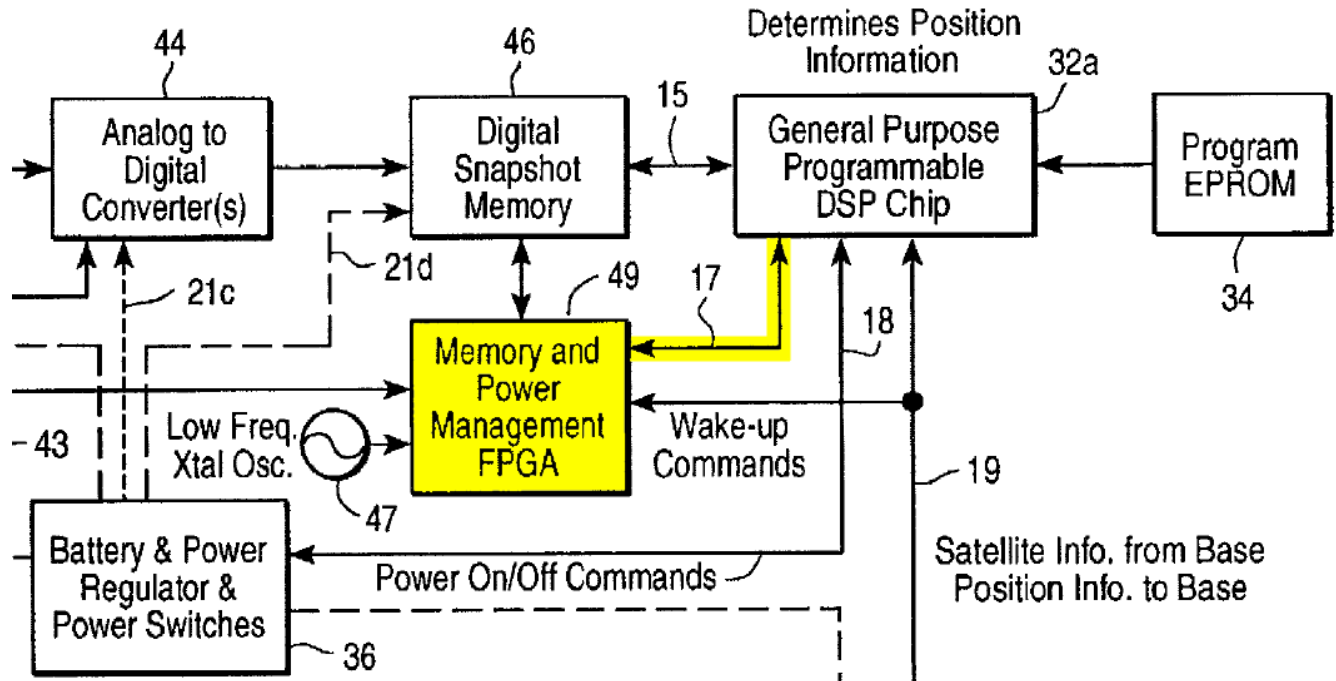
105. As a third reason, implementing the Lyke-Dehkordi-Frantz-Faura MCM instrument controller in accordance with Krasner's suggestions of FPGA-controller power management would have amounted to a common application of known techniques to enhance a known system. In particular, doing so would have been a routine use of unused gates in an existing FPGA of the Lyke-Dehkordi-Frantz-Faura

system. I note that a POSITA would have recognized that this implementation (applying Krasner's suggestions to the Lyke-Dehkordi-Frantz-Faura MCM instrument controller) would not have significantly altered or hindered the functions performed by the Lyke-Dehkordi-Frantz-Faura instrument controller. Moreover, doing so would have been a relatively straightforward and ordinary task for a POSITA given the similarity of the system architectures and the use of FPGAs in Lyke-Dehkordi-Frantz-Faura. Any additional implementation details were well within the ordinary skill and would have been carried out as a matter of routine implementation.

B. Analysis of Lyke, Dehkordi, Frantz, Faura, and Krasner with respect to claim 2.

Claim [2] The instrument controller according to claim 1, wherein a third portion of the gates in the field programmable gate array is configured to activate the instrument controller from a deactivated state, or to deactivate the instrument controller from an active state.

106. The Lyke-Dehkordi-Frantz-Faura-Krasner combination provides Claim [2]. As I discussed previously, the combined system includes a third portion of the gates configured to activate the instrument controller from a deactivated state, or to deactivate the instrument controller from an active state. Krasner describes a "Memory and Power Management FPGA" which "serves to wake up the DSP chip upon sensing activity." EX1007, 8:30-34.



EX1007, FIG. 1B (partial, annotated). “[T]he FPGA 49 sends a wake up signal to the DSP 32a through interconnect 17.” *Id.*, 8:60-64. “[T]he DSP 32a can then wake up other circuitry by providing power on/off commands to the Battery and Power Regulator and Power Switches circuit 36.” *Id.* In the combined system, a portion of the gates are configured for power management functions, including to provide “wake up” commands (such as to the processor), in accordance with Krasner.

Krasner also teaches that the “power management FPGA 49” can deactivate the system. “The power consumed by a component may be reduced by signaling to the component (as in the case of DSP 32a via interconnect 17 in FIG. 1B) to reduce power or wake up to full power.” EX1007, 9:8-13. The “reduce power” statement is juxtaposed to the “wake up” statement to indicate the “power management FPGA 49” can manage power by both deactivating or activating other components in the system.

I note that in Krasner's FPGA, and in the combined system, only a portion of the gates are used to perform power management. Krasner explicitly indicates that the FPGA performs other functions beyond the power management function, such as "memory control and management, including addressing operations when data is being stored into memory from the converters or when the DSP component is reading data from the memory." *Id.*, 9:19-25. Krasner's FPGA also "control[s] other memory functions such as memory refresh if necessary." *Id.*

A POSITA would have readily recognized from Krasner that the portion of the FPGA gates configured to provide "wake up" commands, such as to the processor (e.g., which in turn "wake[s] up other circuitry") activates the instrument controller from a deactivated state, as recited by the first "or" alternative of Claim 2, or deactivates from an active state, as recited by the second "or" alternative of Claim 2. EX1007, 8:62-63; 9:8-13. I note that Dehkordi and other references confirm the POSITA's understanding as to this partial use of a portion of gates to perform power management while the remainder of the FPGA could do other things. EX1004, 3 ("a portion of the FPGA is configured for multi-processing bus arbitration"); EX1034, 4:65-5:7 ("The CLE circuit can be programmed to implement any number of functions, either by itself, or in combination with other CLE circuits" and depicting a plurality of CLE circuits in a FPGA at FIG. 3); EX1035, 2 ("with these novel, mathematical-based chips, only a small portion of the FPGA would be used up").

IX. GROUND 3: CLAIM 3 IS OBVIOUS IN VIEW OF LYKE, DEHKORDI, FRANTZ, FAURA, AND CHRISTIAN

107. For the reasons articulated in detail below, and based on my review of the '177 patent, the prosecution file history of the '177 patent, and the prior art references cited here, it is clear that a POSITA would have readily understood that the teachings of Lyke, Dehkordi, Frantz, Faura, and Christian renders obvious claim 3.

A. Combination of Lyke, Dehkordi, Frantz, Faura, and Christian

108. APOSITA would have been motivated to utilize Christian's suggestions of an unpowered processor when not in use to reduce power consumption in the Lyke-Dehkordi-Frantz-Faura MCM system, and would have had a reasonable expectation of success, including for the reasons I describe below. I note, here again, that Lyke itself stated an objective of a "low-power electronics control system," and referenced power consumption challenges. EX1003, 4:3-17; 4:42-57 (describing objective to "minimize power consumption" in the MCM). Based on my knowledge and experience in the field and my review of the art, multiple additional reasons would have prompted a POSITA to implement the Lyke-Dehkordi-Frantz-Faura MCM instrument controller using configuration in which the processor is completely unpowered when not in use, as I explain next.

109. As a first reason, a POSITA would have been motivated to implement power management techniques in accordance with Christian to further Lyke's stated objective of reduced power consumption for applications in which power management is

critical. Lyke describes use of its MCM in outer space, an environment that a POSITA would have readily recognized as placing power at a premium due to the remote location of the system and harsh operating conditions. *Id.* As Lyke describes, the AIC designed for the Deep Space II mission is for example designed to function with discontinuous applied power due to the high probability that the extreme cold will temporarily render the battery non-functional periodically.” EX1003, 5:6-16. Indeed, Lyke repeatedly identified “greatly reduced ... power consumption,” and the benefits of “greatly reduced size, weight, and power consumption over discrete implementations.” *Id.*, 1:40-55; 5:6-16. A POSITA would have recognized this to especially be the case in such environments that rely on a “battery” source of power (e.g., and environments like outer space in which extreme cold will temporarily render the batter non-functional periodically). Based on Lyke’s description, for example, a POSITA would have been prompted to look to references like Christian that address the need for reduced power consumption. Indeed, Christian likewise describes an objective of extending battery life, and a solution that power not be applied to the processor when not operating. EX1008, Abstract; 1:18-22. “[I]n order to extend battery life when batteries are used ... it is highly desirable that power not be applied to the processor when it is not operating.” *Id.* A POSITA would have been prompted to include a processor that can transition back and forth from a totally unpowered state as needed, in accordance with Christian, in the Lyke-Dehkordi-Frantz-Faura combination to advance these low-power goals. For

example, see EX1003, 5:6-16. (describing need to address “discontinuous applied power”).

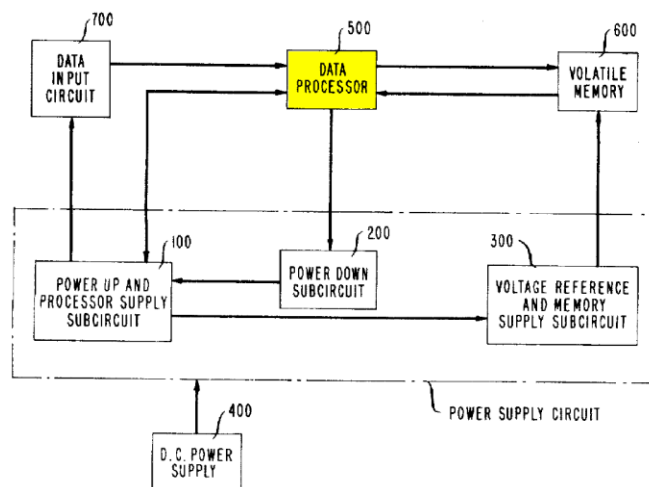
110. As a second reason, a POSITA would have been prompted to combine Christian with the Lyke-Dehkordi-Frantz-Faura system based on Lyke’s teachings. Lyke described the need for an MCM “to function with discontinuous applied power” (EX1003, 5:6-16), and Christian described a configuration in which “the processor is operated on an intermittent basis.” EX1008, 1:23-32. Accordingly, Christian describes a straightforward technique, readily implemented in the Lyke-Dehkordi-Frantz-Faura system, in which the processor operates with discontinuous applied power.

111. As a third reason, implementing the Lyke-Dehkordi-Frantz-Faura MCM instrument controller in accordance with Christian’s suggestions to selectively apply power to a processor for power savings would have amounted to a common application of known techniques to enhance a known system. A POSITA would have recognized that this implementation (applying Christian’s suggestions to the Lyke-Dehkordi-Frantz-Faura MCM instrument controller) would not have significantly altered or hindered the functions performed by the Lyke-Dehkordi-Frantz-Faura instrument controller. Moreover, doing so would have been a relatively straightforward and ordinary task for a POSITA given the similarity of the system architectures and the use of FPGAs in Lyke-Dehkordi-Frantz-Faura. Any additional implementation details were well within the ordinary skill and would have been carried out as a matter of routine implementation.

Claim [3] The instrument controller according to claim 1, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

- i. “wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, ...”

112. The Lyke-Dehkordi-Frantz-Faura-Christian combination provides Claim [3]. In the Lyke-Dehkordi-Frantz-Faura-Christian system, the processor is configured to automatically activate from a totally deactivated/unpowered state upon receiving an external activation signal, in accordance with Christian. *See, supra* Predictable Combination of Lyke-Dehkordi-Frantz-Faura-Christian. Christian describes that “when the processor is not in operation, the power supply applies no power to the processor.” *Id.*, 1:44-46. The power supply “powers up and applies power to the processor in response to any input to the processor that calls for operation of the processor.” *Id.*, 1:46-48.



EX1008, Fig. 1 (annotated). Likewise, in the combined system, when the processor is not in operation, no power is applied to the processor, and the power supply powers up and applies power to the processor in response to any input to the processor that calls for operation of the processor. *Id.*, 1:44-46. Accordingly, the combination includes a processor configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal.

- ii. *“perform proscribed operations, and automatically return to a totally deactivated state using no power.”*

113. In the Lyke-Dehkordi-Frantz-Faura-Christian system, the processor is configured to perform proscribed operations and automatically return to a totally deactivated state using no power. For example, Christian describes that “when the processor has completed its operation, it provides an output to the power supply circuit,” which “remov[es] power from the processor,” thereby describing the processor is both configured to perform proscribed operations and return to a completely deactivated state in which it uses no power. *Id.*, 1:57-60.

x. GROUND 4: CLAIMS 5, 10, 11, 13, 14 15, 17, 19, AND 20 ARE OBVIOUS IN VIEW OF LYKE, DEHKORDI, FRANTZ, FAURA, AND STEELE

114. For the reasons articulated in detail below, and based on my review of the '177 patent, the prosecution file history of the '177 patent, and the prior art references cited here, it is clear that a POSITA would have readily understood that the teachings of

Lyke, Dehkordi, Frantz, Faura, and Steele renders obvious claims 5, 10, 11, 13, 14 15, 17, 19, and 20.

A. Combination of Lyke, Dehkordi, Frantz, Faura, and Steele

115. A POSITA would have been motivated to utilize power conversion in the FPGA of Lyke-Dehkordi-Frantz-Faura system, in accordance with Steele, and had a reasonable expectation of success, including for the reasons I describe next. Power conversion in an MCM instrument controller module for various system components was known. For example, Lyke described “an internal embedded power convertor means capable of generating each operating and reference voltage needed within the instrument controller.” EX1003, 5:54-6:9. Based on my knowledge and experience in the field, other MCM systems known to a POSITA provided similar teachings. *See, e.g.*, EX1015 (“Like MAPLE-2, the ETB also had to provide ... direct power conversion support between spacecraft voltage level ... to sub experiment required voltage levels”). A POSITA would have been prompted (e.g., based on Lyke’s description) to seek out implementation details such as that of Steele to embed a power converter in the FPGA to achieve known benefits (similar to known benefits described above with respect to combination with Frantz, ¶¶56-61 and additional reasons described below).

116. As a first reason, a POSITA would have been motivated to implement the Lyke-Dehkordi-Frantz-Faura MCM instrument controller utilizing a portion of the FPGA for power conversion in accordance with Steele, to avail the system of space

saving benefits. For example, a POSITA would have recognized from Steele's description the space-saving benefits of such a configuration, as compared to a separate power converter with an added footprint, for example. Lyke explicitly mentions "dimensionally constrained and/or remote locations" as target applications for its system. EX1003, 8:66-9:11. Based on my knowledge and experience in the field, a POSITA would have recognized that utilizing a portion of the existing FPGA for power conversion, in accordance with Steele, would have advanced Lyke's stated objective by providing yet further space savings.

117. As a second reason, a POSITA would have been prompted to combine Lyke, Dehkordi, Frantz, Faura, and Steele to utilize a portion of the FPGA for power conversion in order to provide reliability advantages. A POSITA would have readily recognized the importance of reducing failure rate for systems deployed to a "remote location," as described by Lyke, and would have recognized that such benefits would have been achieved by using the FPGA for power conversion functions in accordance with Steele. Separate electronic components in rough environments often called for "hardened" chips, such as "radiation hardened chips," and that such parts were difficult to source and expensive. EX1042, 1 ("Radiation hardening using specific process technology is an expensive process and, when used for a low-volume production, will lead to very costly parts."); EX1047, 2 (discussing advantages of combining multiple "hardened" chips into just a single "hardened" chip). Combining Steele's teachings with

the Lyke-Dehkordi-Frantz-Faura system would have been recognized as beneficially reducing the number of expensive parts and the possibility of their separate failure by effectively utilizing the FPGA for additional power conversion functions (e.g., instead of an additional power converter component).

118. As a third reason, a POSITA would have been prompted to combine Lyke, Dehkordi, Frantz, Faura, and Steele to utilize a portion of the FPGA for power conversion because doing so would have been a common application of a known technique to a known MCM system ready for improvement to yield predictable results. Steele described that an FPGA allowed “a user to incrementally stuff in logic if there is availability,” and provided a known system that utilized an FPGA for power conversion. EX1009, 8:3-24. Based on my knowledge and experience in the field, a POSITA would have readily recognized that the FPGA facilitates additional functionality “for free” simply by configuring additional gates, and would have been motivated to utilize the already-present FPGA to impart the system with power conversion functionality via the FPGA. Moreover, I note that doing so would have been a relatively straightforward and ordinary task for a POSITA given the similarity of the system architectures and the use of FPGAs in Lyke-Dehkordi-Frantz-Faura. Any additional implementation details were well within the ordinary skill and would have been carried out as a matter of routine implementation.

Claim [5] The instrument controller according to claim 1, wherein a third portion of the gates in the field programmable gate array are configured to operate as an

internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

119. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides Claim [5]. In the Lyke-Dehkordi-Frantz-Faura-Steele system, the FPGA receives an input voltage level and generates output voltages needed by other system components. *See* EX1009, 2:35-39 (“capability of selecting a voltage level for an output signal, irregardless of the input voltage level”). For example, Steele describes a field programmable gate array that receives an input voltage level (a “5.0 voltage supply”). The system generates output voltages (e.g., operating/reference voltages), including “a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference” and “a 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference.” EX1009, 4:7-43. The FPGA is capable of receiving an input voltage level and generating each operating and reference voltage needed with the instrument controller. *See, e.g., id.*, 2:55-56 (“The purpose of the V_{cc0} pin is to supply the output signal voltage.”); 2:62-65 (describing “a plurality of different voltages can be supplied to the V_{cc0} pins of different functional blocks, resulting in a plurality of different voltages, as desired, for output signals.”); 4:34-35 (“a user can specify a plurality of different voltage levels for output signals.”).

120. Only a portion of the FPGA gates in Steele is used to implement the power conversion functionality: this is seen including by the fact that Steele describes the

FPGA programmable logic device would additionally be used for other purposes beyond a power conversion function. EX1009, 8:3-24 (“[A] user [can] incrementally stuff in logic” into unused gates of the programmable logic device.); *see also* 7:43-54 (“It is this software which also groups the logic functions requiring a particular output signal level to certain CFBs.”); 8:28-10:21. I additionally note that Steele describes an example system that only requires one configurable function block (CFB) per output voltage out of eight CFBs in the exemplary FPGA, further confirming that only a portion of the gates of the FPGA are configured for an internal embedded power converter logic. *Id.*, Fig. 2, 4:6-5:9.

Element [10.pre] An instrument controller comprising:

121. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides an instrument controller for the reasons I discussed above regarding Ground 1, Element [1.pre].

Element [10.1] a non-volatile memory storage component for program and data storage;

122. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a non-volatile memory storage component for program and data storage for the reasons I discussed above regarding Ground 1, Element [1.1].

Element [10.2] a large volatile memory storage component for additional program and data storage;

123. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a large volatile memory storage component for additional program and data storage for the reasons I discussed above regarding Ground 1, Element [1.2].

Element [10.3] a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing and initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory;

124. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing and initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory for the reasons I discussed above regarding Ground 1, Element [1.3].

Element [10.4] at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

125. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations for the reasons I discussed above regarding Ground 1, Element [1.4].

Element [10.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor;

126. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor for the reasons I discussed above regarding Ground 1, Element [1.5].

Element [10.6] a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor;

127. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing the digital inputs to the processor for the reasons I discussed above regarding Ground 1, Element [1.6].

Element [10.7] wherein a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed with the instrument controller.

128. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed with the instrument controller for the reasons I discussed above regarding Ground 4, Claim [5].

Claim [11] The instrument controller of claim 10, further comprising a plurality of analog outputs, each output being controlled by an independent digital-to-analog

converter, each of said independent digital-to-analog converter, being configured to convert from one of at least two possible depths to analog.

129. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides the features of Claim [11] for the reasons I discussed above regarding Ground 1, Claim [4].

Claim [13.pre] A method for conducting multiple parallel processing using a single instrument controller having a processor and a field programmable array, the method comprising:

130. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a method for conducting multiple parallel processing using a single instrument controller having a processor and a field programmable array. For example, as I discussed in the analysis of Ground 1, Elements [1.3] and [1.5], Dehkordi describes a “a single instrument controller having a processor and a field programmable array.” Dehkordi additionally describes the MCM with a “DSP processor as shown in Figure 1” and that the MCM is “designed to exploit the multi-processing capability of the [processor].” EX1004, 1.

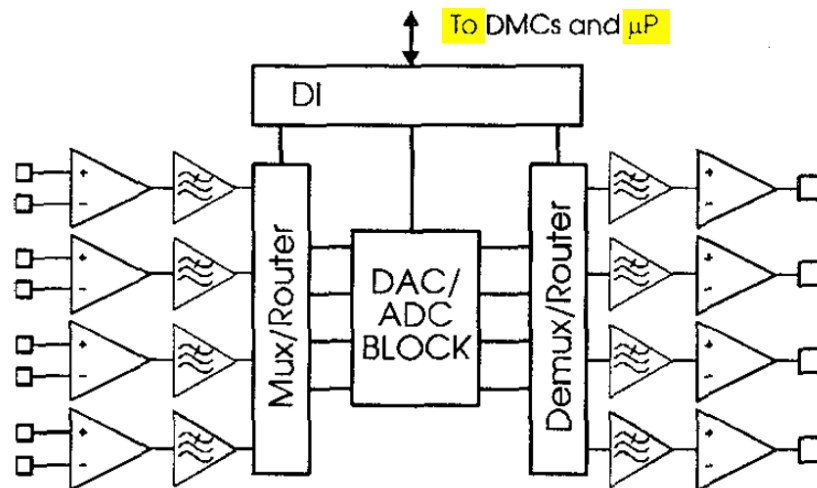
131. I note that Dehkordi describes multiple parallel processing, consistent with claim 13, as I discuss in more detail below regarding Element [13.5].

Element [13.1] receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths (thereby generating digital inputs);

132. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths (thereby generating digital inputs) for the reasons I discussed above regarding Ground 1, Element [1.6].

Element [13.2] providing a first portion of the digital inputs to the processor;

133. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides providing a first portion of the digital inputs to the processor for reasons similar to those discussed above with respect to Ground 1, Element [1.6.iii] and Claim [14] below (e.g., through Lyke's description). Alternatively, Faura describes "a device consisting of a Field Programmable Gate Array (FPGA), a set of programmable and interconnectable analog cells, and a microprocessor core." EX1006, 1.



Faura, EX1006, Fig. 3 (highlighted).

134. As I discussed above, Faura describes a collection of DAC/ADC blocks ("a number of these blocks") wherein the output of the DAC/ADC block is connected to the microprocessor ("μP") and the FPGA ("DMCs"), as needed. See EX1006, Fig. 3; see also, *id.*, 3 ("the ADCs can be directly read ... by the microprocessor in real time, [and] the ADCs can be connected to the ... the DMCs inputs."). Even beyond Faura's teachings, Dehkordi also shows a portion of the FPGA configured as an "ADC Interface," i.e., that would be used to provide a portion of the digital signals to the digital

signal processor. EX1004, Fig. 1 & 1 (“The module also includes 256 K-byte of SRAM, 128 K-byte of EEPROM, a 10 K -gate Xilinx 4010 FPGA and a 6-channel 12-bit ADC. The module was designed to exploit the multi-processing capability of the 96002 [DSP processor]”).

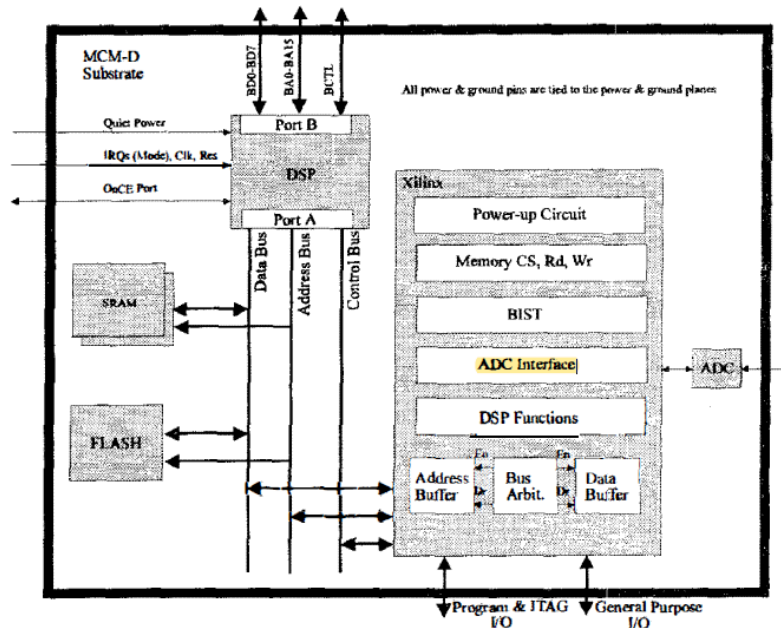


Figure 1. The Block Diagram of the DSP Sub-system.

Dehkordi, EX1004, Fig. 1 (highlighted).

Element [13.3] providing a remaining portion of the digital inputs to the field programmable gate array;

135. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides providing a remaining portion of the digital inputs to the field programmable gate array. For example, Faura describes a FPGA with “programmable digital cells (the FPGA)” referred to as “Digital Macro Cells” (DMCs).” EX1006, 1, 2. As I discussed previously (refer to analysis of Element [13.2]), Faura describes “a number of these blocks” and the

output of the DAC/ADC block is connected to the microprocessor (μ P) and the FPGA (DMCs), as needed. See EX1006, Fig. 3. Indeed, I note here again that Faura describes that “the ADCs can be directly read ... by the microprocessor in real time, [and] the ADCs can be connected to the ... the DMCs inputs.” EX1006, 3.

136. Moreover beyond Faura’s teachings, Dehkordi provides this element. As I discussed above, Dehkordi describes an FPGA with “DSP functions” (in addition to the separate DSP processor itself), EX1004, Fig. 1, and that the “FPGA is primarily a hardware pre-processor of incoming data.” EX1004, 1. A remaining portion of the digital signals (i.e., what [13.3] calls “digital inputs”) would thus be provided to the FPGA as part of the hardware pre-processing of “incoming data,” i.e., data coming from the ADC. *Id.* A POSITA would have been motivated to implement such features in the combination for the known benefits (e.g., as I discussed previously).

Element [13.4] performing digital signal processing on the first portion of the digital inputs utilizing the processor;

137. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides performing digital signal processing on the first portion of the digital inputs utilizing the processor. For example, in Dehkordi’s system the MCM is “designed to exploit the multi-processing capability of the [processor].” EX1004, 1. A first portion of the digital signals (i.e., what [13.2] calls “digital inputs”) would be provided to the “digital signal processor” so that the DSP could perform its intended function (digital signal processing) as part of the MCM’s “multi-processing.” *Id.* Frantz also describes

performing various types of digital signal processing on digital inputs through the TMS320C25 digital signal processor:

TMS320C25 applications

The TMS320C25 is designed for real-time DSP and other computation-intensive tasks in telecommunications, graphics, image processing, high-speed control, speech processing, instrumentation, and numeric processing. In these applications, the TMS320C25 provides an excellent means for **executing signal processing algorithms** such as fast Fourier transforms (FFTs), digital filters, frequency synthesizers, correlators, and convolution routines.

EX1005, 15. For instance, TMS320C25 DSP performs FIR filtering:

Digital filtering. Filters are often implemented in digital signal processing systems. Such filters fall into two categories: finite impulse response (FIR) filters and infinite impulse response (IIR) filters. 4.6 For both types of filter, the coefficients of the filter (weighting factors) may be fixed or adapted during the course of the signal processing. **The TMS320C25 reduces the execution time of all filters** by virtue of its 100-ns instruction cycle time and optimized instructions for filter operations.

EX1005, 15. TMS320C25 DSP also performs digital signal processing for telecommunications applications, such as echo cancellation:

Telecommunications applications. Digital signal processing will be more extensively used in telecommunications as it evolves toward all-digital networks. Below, we discuss several typical uses of the TMS320C25 in telecommunications applications.

Echo cancellation. In echo cancellation, an adaptive FIR filter performs the modeling routine and signal modifications needed to adaptively cancel the echo caused by impedance mismatches in telephone transmission lines. **The TMS320C25's large on-chip RAM of 544 words and on-chip ROM of 4K words allow it to execute a 256-tap adaptive filter (32-ms echo cancellation)** without external data or program memory.

EX1005, 17. TMS320C25 DSP further performs digital signal processing for control systems, including signal conditioning and filtering:

High-speed control applications. These applications use the TMS320C25's general-purpose features for bit-test and logical operations, timing synchronization, and fast data transfers (10 million 16-bit words per second). They use the **TMS320C25 in closed-loop systems for control signal conditioning, filtering, high-speed computing, and multichannel multiplexing**. The following examples demonstrate typical control applications.

EX1005, 17.

Element [13.5] receiving the remaining portion of the digital inputs at the field programmable gate array and configuring a first portion of the field programmable gate array to perform digital signal processing on the remaining portion of the digital inputs, thereby conducting multiple parallel processing using a single instrument controller; and

138. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides Element [13.5]. For example, Dehkordi describes an FPGA that receives digital inputs from the ADC. This configuration is illustrated in FIG. 1, which shows the ADC connected to the FPGA. EX1004, FIG. 1. Digital signal processing is performed on remaining portion of the digital inputs. In particular, a first portion of Dehkordi's FPGA is configured for digital signal processing as part of its reconfigurable logic, designated by the "DSP Functions" block in FIG. 1. *Id.*; see also *id.* at 1 (describing one role of the FPGA as a "pre-processor of incoming data"). The FPGA provides the "DSP functions" or Digital Signal Processing Functions. See, e.g., EX1004, FIG. 1 (illustrating the "DSP Functions" as a block of the FPGA). As I discussed previously regarding the analysis of

Elements [1.8] and [2], and further below in [15.1] and [15.2], I note that Dehkordi describes other processing in the second, third, and additional portions of the FPGA. EX1004, 1. Indeed, a portion of FPGA provides a “pre-processor of incoming data,” and “a portion of the FPGA is configured for multi-processing bus arbitration.” *Id.*, 1-3. In accordance with Dehkordi, the Lyke-Dehkordi-Frantz-Faura-Steele combination includes configuring a first portion of that FPGA to perform digital signal processing on the remaining portion of the digital inputs, thus conducting multiple parallel processing using a single instrument controller.

Element [13.6] configuring a second portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

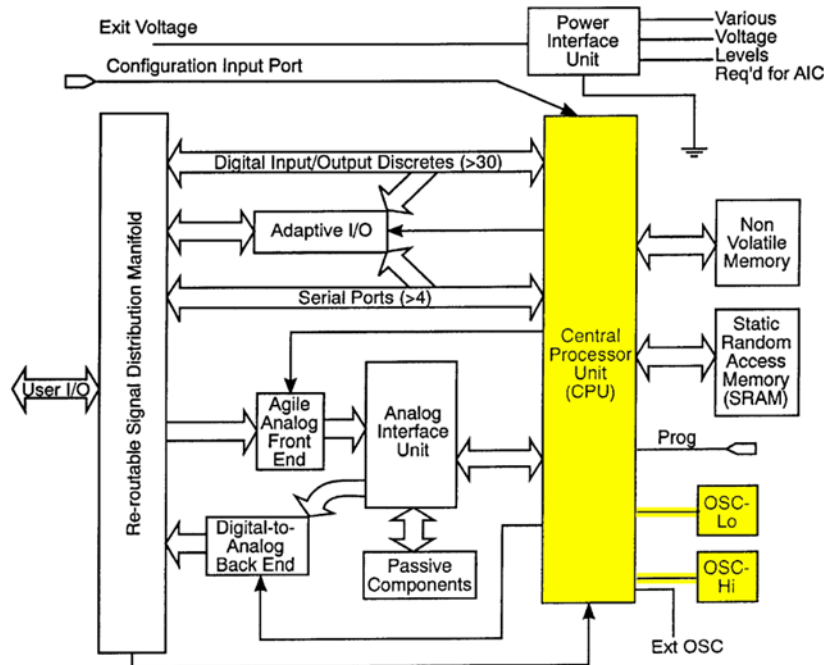
139. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides configuring a second portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller for the reasons I discussed above regarding Claim [5].

Claim [14] The method for conducting multiple parallel processing using a single instrument controller as in claim 13, further comprising the additional step of providing at least two internal oscillator signals to the processor for low-speed and high-speed digital signal processing operations.

140. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides Claim [14]. For example, Lyke describes an “AIC contain[ing] internal oscillators, at least two, one

for high-frequency operation and one for low-frequency operation.” EX1003, 4:42-44,

Figs. 1 & 2.



EX1003, FIG. 1 (annotated). As illustrated in FIG. 1, the at least two internal oscillators are coupled to the processor. I additionally note that the high and low oscillators are in contrast to the “external oscillator,” further confirming that the high and low oscillators are internal oscillators. *Id.*, 4:42-57 (“The AIC also permits external oscillators for cases where synchronization or more precise timing is important.”); 3:12-27 (“built-in bypassable oscillators [are] for high and low speed operation.”). Lyke’s description and connection between processor and oscillators provide a “high and low frequency internal reference,” indicating the processor is capable of high-frequency and low-frequency operations. *Id.* Indeed, such a configuration would have been recognized as describing well-known processor systems capable of both high-frequency and low-frequency

operations, as I describe next.

As one example of such a configuration well-known to a POSITA, Oz describes high-frequency and low-frequency oscillators as “means for switching the CPU clock signal from the first clock source to the second clock source.” EX1026, 98:59-61; *see also id.*, 14:16-17 (“Two crystal clock oscillators, 24a and 24b provide the basic frequencies needed. The high-speed oscillator 24a is designed to operate with an 40.96 MHz crystal. The low-speed oscillator 24b is designed to operate with a ceramic resonator at a frequency of 455 KHz.”). Additionally, a POSITA would have implemented the “high and low speed operation” to apply to any processing performed by the processor, including digital signal processing operations, in accordance with Lyke.

Element [15.pre] A stand-alone instrument controller comprising:

141. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a stand-alone instrument controller. As discussed above, the combined system provides an instrument controller. *See* Ground 1, Element [1.pre]. Moreover, the combined system provides a stand-alone instrument controller. Lyke explicitly describes an “Advanced Instrument Controller (AIC) [that] is a **stand-alone**, compact, low-power electronics instrument controller.” EX1003, 2:34-35. I note that Dehkordi likewise provides a MCM with I/O. EX1004, 1-3. Based on my knowledge and experience in the field, a

POSITA would have recognized Dehkordi as describing a stand-alone instrument controller.

Element [15.1] a plurality of gates arranged in a field programmable gate array having multiple portions of gates, the multiple portions of gates including: a first portion of the gates in the field programmable gate array is configured to perform Signal processing, a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, and a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter;

142. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides Element [15.1].

i. *“a plurality of gates arranged in a field programmable gate array having multiple portions of gates, the multiple portions of gates including:”*

143. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a plurality of gates arranged in a field programmable gate array having multiple portions of gates, for reasons similar to those discussed regarding Ground 1, Element [1.5.i]. I note Dehkordi describes that its FPGA has multiple portions of gates. *See, e.g.,* EX1004, 1; FIG. 1 (illustrating multiple different blocks within the FPGA); *see also* Ground 1, Element [1.7]-[1.8].

ii. *“a first portion of the gates in the field programmable gate array is configured to perform signal processing,”*

144. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a first portion of the gates in the field programmable gate array is configured to perform signal processing, for reasons similar to those discussed regarding Ground 1, Element [1.7].

iii. *“a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, and”*

145. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix, for reasons similar to those discussed regarding Ground 1, Element [1.8].

iv. *“a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter;”*

146. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter, for reasons similar to those discussed regarding Claim [5].

Element [15.2] a microprocessor coupled to the plurality of gates, and configured to operate independently or under the control of the plurality of gates;

147. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a microprocessor coupled to the plurality of gates, and configured to operate independently or under the control of the plurality of gates. *See, e.g.*, Analysis of Ground 1, Element [1.5]. For example, Lyke describes a microprocessor provided by the “AIC51 CPU.” EX1003, Fig. 11. Second, Lyke describes that “field programmable gate array(s) [are] interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU.” EX1003, 8:55-59; *see also id.* at 4:32-34 (“The non-volatile memory of the AIC would also be used to

program reconfigurable logic”). Lyke describes that the “gate array(s) [is] configured [with the module’s] CPU” thereby providing “a microprocessor coupled to the plurality of gates.” The configuration information—the programming of the FPGA and how it operates—comes from the “non-volatile memory.” *Id.* at 8:59. This is the customary way that an FPGA operates, including as shown by the contemporaneous Marchal reference, where the configuration bits are loaded from memory :

An FPGA is an array of logic blocks (cells) placed in an infrastructure of interconnections, which can be programmed at three distinct levels (see Figure 1): (1) the function of the logic cells, (2) the interconnections between cells, and (3) the inputs and outputs. All three levels are configured via a string of bits that is loaded from an external source, either once or several times.

EX1035, 1; *see also* EX1035, 2-3 (describing loading the FPGA configuration string from “memory”). The FPGA loads this configuration (the program) and then operates whatever program is contained in that memory.

148. Lyke’s description that the FPGA is “configured [from] the non-volatile memory” provides that the FPGA is configured with a program that would run independently in parallel with the processor (i.e., a separate program for the FPGA as opposed to the processor), and in fact this is how FPGAs were typically deployed with processors prior to the time of the ’177 patent. As examples, *see*: Halverson, EX1025, 2:22-31 (“Programs that would otherwise be performed by serial data processing are divided into steps to be performed by a standard or reduced instruction set CPU (central processing unit) and computations to be performed in parallel by the FPGAs. [T]he

concept of parallel processing and the use of field programmable gate arrays [in parallel with a processor] is not new.”). Halverson further describes “parallel” as “[p]ertaining to a process in which multiple events or computations occur within the same interval of time, each handled by a separate but similar functional unit,” further confirming the common practice of an FPGA configured to run independent processes in parallel with the processor that would have been recognized from Lyke. *Id.*, 2:1-3.

In addition, Lyke describes the microprocessor as running its own “operational software (program code)”, EX1003, 2:22-23, while Lyke’s FPGA runs a separate program “configured [from] the non-volatile memory.” *Id.* at 8:55-59. These separate programs running on Lyke’s CPU and FPGA thereby satisfy the requirement that the microprocessor is configured to operate independently of the plurality of gates. Moreover, a POSITA would have readily recognized and been prompted to pursue the known benefits of using an FPGA to run independent processes in parallel with the processor (e.g., as discussed above), and would have had a reasonable expectation of success in doing so.

149. Here again, Dehkordi confirms a POSITA’s understanding based on Lyke. Dehkordi describes a gate array coupled to the processor that is configured to run independent processes in parallel with the processor. As I noted previously Dehkordi depicts a Xilinx FPGA (“gate array”) coupled to a Motorola digital signal processor (“processor”). Such a configuration is described at page 1, and illustrated in FIGS. 1 and

3, of Dehkordi. Dehkordi teaches its particular DSP is a Motorola 96002 processor. EX1004, 1 (“[Multichip module] consists of a complete DSP subsystem based on the Motorola 96002 32-bit floating point DSP processor as shown in Figure 1.”). A POSITA would know that Motorola 96002 has its own built-in embedded “bootstrap ROM” and “program memory,” as shown in the 96002 data sheet, which control the operation of the DSP. EX1013, 1. The microprocessor thus runs the program in own program memory, separate from the FPGA.

This independent operation is further confirmed by Dehkordi itself. For example, Dehkordi illustrates a “DSP functions” block of the FPGA, indicating a portion of the Dehkordi FPGA is configured for digital signal processing as part of its reconfigurable logic. EX1004, FIG. 1. Dehkordi additionally indicates the FPGA is a “pre-processor of incoming data.” As another example of independent processes in parallel with the processor, Dehkordi describes that “a portion of the FPGA is configured for **multi-processing bus arbitration.**” EX1004, 3. Dehkordi’s FPGA is serving as a “traffic cop” for data as the data is processed by either the FPGA or the DSP. *See also* EX1045, 1:49-68 (describing bus arbitration as a “traffic cop” role). Dehkordi’s FIG. 1 illustrates this process with a “Bus Arbit.” box in the FPGA. Indeed, Dehkordi explains that the FPGA “module was designed to exploit the multi-processing capability of the [DSP].” EX1004, 1.

As yet another example, Dehkordi describe the FPGA “also provides other generic

logic functions required for implementation of the entire subsystem.” EX1004, 1.

Dehkordi additionally describes a “RAM-based configuration where the configuration may come from outside the module.” *Id.*, 3. Dehkordi’s “configuration [originating from] outside the module” is providing that Dehkordi’s FPGA were not constrained and would run independent processes in parallel with the processor. EX1004, 2:27-31.

Indeed, a POSITA would have been prompted to implement such a configuration to avail the system of the known benefits of a parallel configuration described above, where this was a routine configuration. EX1036, 4 (“The CPU and FPGA execute as two independent execution units.”). Further confirming the microprocessor’s independent operation is Dehkordi’s depiction that “[t]he DSP has a dual data and address port architecture,” which a POSITA would understand that the DSP can process data completely inaccessible to the FPGA, through “Port B” in the figure. EX1004, 3 & 1 (showing “Port B”).

150. The alternative language in the claim of a “microprocessor... configured to operate... under the control of the plurality of gates,” was also well known to the POSITA, and would have been seen as a way to program the MCM as taught by the Lyke-Dehkordi-Frantz-Faura-Steele combination. Based on my knowledge and experience in the field, this programming model of a microprocessor operating under the control of an FPGA would have been well within the general knowledge of the POSITA, as shown for example by the reference Tian, EX1033. Tian describes a system wherein

the processor (the same “TMS320 family” processor taught in Frantz) is “under the control” of the FPGA. EX1033, 4 (“We setup two processor modules in our system. They both work **under the control of the FPGA.**”); *id.* at 2 (“We try to construct a two-DSP-based FPGA-computational system with two TMS320C6201s.”). Tian teaches that “[a]s the core of the system, FPGA plays a very important role: it takes charge of DPS [sic: DSP] control, DSP communication, memory space access arbitration.” EX1033, 2. Tian further teaches that the FPGA can “dispatch processing instructions and subtasks” to the microprocessor, which “is the basic processing cell to perform the subtask.” EX1033, 4.

151. The POSITA would have known it to be straightforward to have the FPGA as taught in Lyke or Dehkordi control the code running on the processor. The processors in Lyke and Dehkordi are running a program that can be changed. Specifically, Lyke taught the ability for “in-situ reprogramming of the controller’s operational software (program code).” EX1003, 2:22-23. Similarly, Dehkordi taught a “programmable DSP processor.” EX1004, 1. In the appropriate system, the FPGA would provide that code (e.g., as in Tian’s “dispatch[ing] processing instructions and subtasks.”), where, as I described above in section §VII.A.i, the POSITA would have appreciated the need to change the program running on the processor at runtime. For instance, in the space-applications targeted in Lyke, the device would not be easily accessed, if at all, by humans once launched into space, but programs would need to be changed as new

experiments were run, for example. See §VII.A.i (citing EX1003, 5:6-16; 8:27-40 (discussing the Lyke MCM as part of “Deep Space II”)). Doing so would have been a routine way to program the processor (i.e., to perform the “in-situ reprogramming of the... program code” described by Lyke) and a simple engineering exercise, with a reasonable expectation of success, as demonstrated by Tian.

Element [15.3] a non-volatile memory storage system with non-volatile storage components for programs and data storage coupled to both the microprocessor and the plurality of gates;

152. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a non-volatile memory storage system with non-volatile storage components for programs and data storage coupled to both the microprocessor and the plurality of gates. For example, Lyke describes a “non-volatile memory [that] is used for both program storage and data storage.” EX1003 4:14-15; see also 3:15-19 (“There is a large non-volatile program and data storage component 5.”). The non-volatile memory storage system includes non-volatile storage components for programs and data storage coupled to both the microprocessor and the plurality of gates. See, *supra* Analysis of Elements [1.1], [1.3.i] and [15.2]. Here again, beyond Lyke’s teachings, Dehkordi similarly describes a non-volatile memory storage component (“FLASH”) coupled to both the processor and the FPGA through the Data Bus and Address Bus. EX1004, Fig. 1. Dehkordi’s “DSP” is a processor, and Dehkordi’s FPGA comprises a plurality of gates.

Element [15.4] a large volatile memory storage system coupled to the microprocessor with volatile storage components having a memory size that is comparable to, or larger than, an address space operated upon by the microprocessor;

153. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a large volatile memory storage system coupled to the microprocessor with volatile storage components having a memory size that is comparable to, or larger than, an address space operated upon by the microprocessor. For example, Lyke describes a “volatile static random access memory (SRAM) with storage contents comparable to or larger than the address space the CPU operates on.” EX1003, 4:35-37; *see also* 3:15-19; cl. 1, Fig. 1. The SRAM is coupled to the processor. *Id.*; *see also* Analysis of Element [15.2] (explaining that Lyke’s CPU is a microprocessor).

Element [15.5] a plurality of analog-to-digital converters for receiving a plurality of analog inputs and digitizing the analog inputs, thereby providing digital inputs for use in the instrument controller; and

154. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a plurality of analog-to-digital converters for receiving a plurality of analog inputs and digitizing the analog inputs, thereby providing digital inputs for use in the instrument controller, for reasons similar to those discussed regarding Element [1.6].

Element [15.6] a plurality of analog outputs where each analog output is controlled by an independent digital-to-analog converter, and each independent digital-to-analog converter is configured to convert from one of at least two possible depths to analog.

155. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a plurality of analog outputs where each analog output is controlled by an independent digital-to-analog converter, and each independent digital-to-analog converter is configured to

convert from one of at least two possible depths to analog, for reasons similar to those discussed regarding Claim [4].

Claim [17] The stand-alone instrument controller of claim 15, wherein the internal embedded power converter is configured to receive an input voltage level and to generate each operating and reference voltage needed within the instrument controller.

156. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides claim 17, for reasons similar to those discussed regarding claims [5], [10.7], [13.6], and [15.1].

Claim [19] The stand-alone instrument controller of claim 15, further comprising at least two internal oscillators coupled to the microprocessor for providing clock signals for low-frequency and high-frequency operations.

157. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides claim 19, for reasons similar to those discussed regarding claims [1.4], [10.4], and [14].

Element [20.pre] A method for conducting multiple parallel processing using a single instrument controller having a field programmable array, the method comprising:

158. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides a method for conducting multiple parallel processing using a single instrument controller having a field programmable array, for reasons similar to those discussed regarding Element [13.pre]. I note that Dehkordi teaches a type of multiple parallel processing, describing portions of the FPGA that are used for different functions. In particular, a first portion of Dehkordi's FPGA is configured for digital signal processing as part of its reconfigurable logic, designated by the "DSP Functions" block in FIG. 1. EX1004, FIG. 1; see also 1 ("pre-processor of incoming data"). As I discussed previously regarding the analysis of Elements [15.1] and [15.2], I note that Dehkordi describes other

processing in the second, third, and additional portions of the FPGA. EX1004, 1.

Indeed, a portion of FPGA provides a “pre-processor of incoming data,” and “a portion of the FPGA is configured for multi-processing bus arbitration.” *Id.*, 1-3.

Element [20.1] configuring a portion of the gates in the field programmable gate array to operate as an internal embedded power converter capable of receiving at least one input voltage level and generating each operating and reference voltage needed for activation, operation, and deactivation of the instrument controller.

159. The Lyke-Dehkordi-Frantz-Faura-Steele combination provides Element [20.1] for reasons similar to those discussed regarding Claim [5]. For example, Steele describes configuring part of an FPGA that receives an input voltage level and that outputs “a plurality of different voltages,” i.e., generation of any output voltage that is needed by the system. EX1009, 2:62-65; *see also id.*, 4:28-48. Steele describes a field programmable gate array that receives an input voltage level (a “5.0 voltage supply”), and generates output voltage, including “a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference” and “a 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference.” EX1009, 4:7-43:

The FPGA is comprised of eight configurable function blocks (CFBs) 200–207 coupled together by a global interconnect 208. ...

The PLD is powered by a 5.0 supply voltage on the V_{cc} pin. V_{ss} is ground. In addition, in the currently preferred embodiment of the present invention, there is a **separate V_{cco} pin associated with each of the CFB's 200-207** (i.e., eight V_{cco} pins). **The V_{cco} pins correspond to the output supply voltage.** By coupling the desired output voltage to a V_{cco} pin,

a user can select the voltage level of signals being output from a particular CFB. Once a user specifies a V_{cco} voltage for a particular CFB, that whole block outputs signals at the specified voltage level. In this manner, a user can specify a plurality of different voltage levels for output signals. For example, a user could couple the V_{cco} of CFB0 to a supply voltage of 5 volts while simultaneously coupling the V_{cco} of CFB1 to a supply voltage of 3 volts. **Hence, output signals from CFB0 are at a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference. Meanwhile, output signals generated by CFB1 are at a 3 volt level. These 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference.**

Steele also teaches that the output voltage V_{cco} can be set to ground by the “output buffer [portion of the circuit] used to select the voltage level for an output signal.”:

A low signal (i.e., 0 volts) on input line 606 switches the p-channel transistors 603 and 604 “ON” while a corresponding low signal on line 608 switches in-channel transistor 605 “OFF” **This results in the voltage on the V_{cco} pin being output** Conversely, a high signal (i.e., 5 volts) on input line 606 switches the p-channel transistors 603 and 604 “OFF” while a corresponding high signal 608 switches n-channel transistor 605 “ON.” **This results in effectively [the] grounding output line.**

EX1009, 7:13-22.

Furthermore, output buffer 601 is capable of being tristated. **In other words, its output is either V_{cco} , effectively grounded,** or floating (i.e., high impedance looking back into the drains of transistors 604 and 605).

EX1009, 7:23-26

The FPGA is “capable of receiving an input voltage level and generating each operating and reference voltage needed with the instrument controller.” Steele’s exemplary FPGA output voltages of “5 volts,” “3 volts,” and “ground” (0 volts) are exemplary operating and reference voltages needed for activation, operation, and deactivation of the controller. As it states above, Steele teaches that the “output signals from CFB0 are at a 5 volt level, which can be properly utilized by external devices operating on a 5 volt signal reference. Meanwhile, output signals generated by CFB1 are at a 3 volt level. These 3 volt output signals can then be used by those devices operating on signals at a 3 volt reference.” Finally, the “ground” signal would also be used in deactivation of the instrument controller in which no voltage is applied, where a “ground” signal (e.g., zero volts) is the reduced power level used to deactivate the components. See, e.g., EX1008, 4:10-15 (describing that when NPN transistors “Q1 and Q2 are turned off... no power is applied to the processor).

XI. GROUND 5: CLAIMS 12 AND 18 ARE OBVIOUS IN VIEW OF LYKE, DEHKORDI, FRANTZ, FAURA, CHRISTIAN AND STEELE

160. For the reasons articulated in detail below, and based on my review of the ’177 patent, the prosecution file history of the ’177 patent, and the prior art references cited here, it is clear that a POSITA would have readily understood that the teachings of Lyke, Dehkordi, Frantz, Faura, Christian, and Steele renders obvious claims 12 and 18.

A. Combination of Lyke, Dehkordi, Frantz, Faura, Christian, and Steele

161. As I discussed above, a POSITA would have been prompted to combine Christian's teachings with the Lyke-Dehkordi-Frantz-Faura combination to achieve known benefits. *See, supra*, Predictable Combination of Lyke, Dehkordi, Frantz, Faura, and Christian. Based on my knowledge and experience in the field and my review of the references herein, a POSITA would have been prompted to combine Christian with the Lyke-Dehkordi-Frantz-Faura-Steele combination.

Claim [12] The instrument controller according to claim 1, wherein the processor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

162. The Lyke-Dehkordi-Frantz-Faura-Christian-Steele combination provides claim 12, for reasons similar to those discussed regarding Ground 1, Claim [1] and Ground 3, Claim [3].

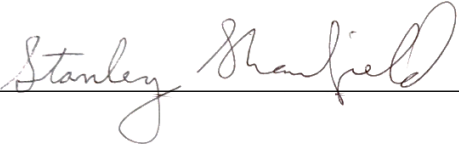
Claim [18] The stand-alone instrument controller of claim 15, wherein the microprocessor is configured to automatically activate from a totally deactivated (unpowered) state upon receiving an external activation signal, perform proscribed operations, and automatically return to a totally deactivated state using no power.

163. The Lyke-Dehkordi-Frantz-Faura-Christian-Steele combination provides claim 18, for reasons similar to those discussed regarding Ground 3, Claim [3] and Ground 4, Claim [15].

ADDITIONAL REMARKS/CONCLUSION

164. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

165. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: 2/1/23 By: 

APPENDIX A

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry

Semiconductor Fabrication: Silicon and III-V Materials

Semiconductor Device & Integrated Circuit Engineering

Semiconductor Equipment: Front & Back End

Semiconductor Packaging Design and Manufacturing

Passive Component Design and Manufacturing

RF Design and Fabrication

Digital Design & Fabrication

Semiconductor Manufacturing in Silicon and III-V Materials

MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices

Fiber Optic Device Design and Fabrication

Integrated Optics & Electro-Optical Devices

Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components

Six Sigma Semiconductor Manufacturing

Microwave Engineering

US Patent Law in Technology

Patent Application and Prosecution

Semiconductor Plasma Processing

Thin Film Physics and Technology

MEMS-based Gyroscopes and Accelerometers

Thermoelectric Materials & Technology

Phased Array Radar Engineering

Antennas and Electromagnetic Propagation

Solid State Optical Devices

Fiber Optic Communication System Operation

HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA

2003 – present

Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award. Recent work in ASIC process design and circuit design for ultra-high performance government and space systems.

Clarendon Photonics Newton, MA

2001 – 2003

Director, Packaging & Integration

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA

1999 – 2001

Vice President, Operations, Co-Founder 1999 – 2000

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology

2000 – 2001

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA

1985 - 1999

Manager, Semiconductor Operations

1996 – 1999

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

Research Laboratory Manager

1992 – 1996

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

Section Manager, Semiconductors & ICs

1985 – 1992

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA

1981 – 1984

**Staff Scientist
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al_{0.24}GaAs/In_{0.16}GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents**US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - Ion Beam Deposition Apparatus

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - Boron Nitride Films and Process of Making Same

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - Coating Method

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

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