

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Kenneth Blemel
U.S. Patent No.: 6,938,177 Attorney Docket No.: 42653-0048IP1
Issue Date: August 30, 2005
Appl. Serial No.: 10/028,556
Filing Date: December 19, 2001
Title: MULTI-CHIP MODULE SMART CONTROLLER

DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.
2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.
3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. The MARC record has been the standard format for computerized library records since the early 1970s. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability. In other words, an interested member of the public would have been able to access a reference at the library soon after its MARC record was created.

5. I am including five MARC records for each reference addressed in my declaration because in my experience MARC records are the most detailed

records of library ownership, cataloging and circulation. These details include fields describing title, author and publishers but also more technical, unique designations such as International Standard Book Numbers (ISBN), International Standard Serial Numbers (ISSN) or OCLC Control Numbers (OCN). These numerical codes are registered to creators and right holders to designate specific titles by specific authors. As such, matching the unique details of these MARC records to ISBN, ISSN and OCN records (i) provide a formal basis for comparison when examining multiple copies of the same material, (ii) provide a rough timeline for that material's availability, and (iii) indicate the publisher's intent to make the material broadly available.

6. I have reviewed Exhibit 1004, "Development of a DSPMCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities" by Peyman Dehkordi, Tim Powell and Donald Bouldin as published in *Proceedings: 1996 IEEE Multi-Chip Module Conference*.
7. Attached hereto as Appendix DEHKORDI01 is a true and correct copy of "Development of a DSPMCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities" as published in *Proceedings: 1996 IEEE*

Multi-Chip Module Conference. I secured this copy myself from the Northwestern University Library's digital holdings. In comparing Appendix DEHKORDI01 to Exhibit 1004, it is my determination that Exhibit 1004 is a true and correct copy of "Development of a DSPMCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities" by Peyman Dehkordi, Tim Powell and Donald Bouldin.

8. Attached hereto as Appendix DEHKORDI02 is a true and correct copy of the MARC record for *Proceedings: 1996 IEEE Multi-Chip Module Conference* as held by the Northwestern University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEHKORDI02 accurately describes the title, author, publisher, and ISBN number of *Proceedings: 1996 IEEE Multi-Chip Module Conference*.

9. Attached hereto as Appendix DEHKORDI03 is a true and correct copy of the MARC record for *Proceedings: 1996 IEEE Multi-Chip Module Conference* as held by the University of Wisconsin-Madison library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEHKORDI03 accurately describes the

title, author, publisher, and ISBN number of *Proceedings: 1996 IEEE Multi-Chip Module Conference*.

10. Attached hereto as Appendix DEHKORDI04 is a true and correct copy of the MARC record for *Proceedings: 1996 IEEE Multi-Chip Module Conference* as held by the University of Cincinnati library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEHKORDI04 accurately describes the title, author, publisher, and ISBN number of *Proceedings: 1996 IEEE Multi-Chip Module Conference*.

11. Attached hereto as Appendix DEHKORDI05 is a true and correct copy of the MARC record for *Proceedings: 1996 IEEE Multi-Chip Module Conference* as held by the Linda Hall library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEHKORDI05 accurately describes the title, author, publisher, and ISBN number of *Proceedings: 1996 IEEE Multi-Chip Module Conference*.

12. Attached hereto as Appendix DEHKORDI06 is a true and correct copy of the MARC record for *Proceedings: 1996 IEEE Multi-Chip Module*

Conference as held by the Queen's University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix DEHKORDI06 accurately describes the title, author, publisher, and ISBN number of *Proceedings: 1996 IEEE Multi-Chip Module Conference*.

13. The MARC records included within Appendices DEHKORDI02 - 06 all contain 008 fields that designate the date of record creation, indicating a range of public availability via these libraries and institutions. Appendices DEHKORDI02 & DEHKORDI06 have a 008 field of August 30, 2001.

Appendices DEHKORDI03 - 05 have a 008 field of April 5, 1996.

Considering this information, it is my determination that *Proceedings: 1996 IEEE Multi-Chip Module Conference* and therefore "Development of a DSPMCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities" was made available and accessible to the public by shortly after April 5, 1996 and certainly no later than August 30, 2001.

14. I note that Dehkordi was cited in other IEEE publications prior to 2001, further confirming public availability. For example, IEEE Explore lists other IEEE publications that have cited Dehkordi, including six other

publications with publication dates in the 1990s. *See* Appendix Dehkordi07 (<https://ieeexplore.ieee.org/document/510775/citations#citations>).

15. I have reviewed Exhibit 1006, “A Novel Mixed Signal Programmable Device with On-Chip Microprocessor” by Julio Faura, Chris Horton, Phuoc van Duong, Jordi Madrenas, Miguel Angel Aguirre and Josep Maria Insenser as published in *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*.

16. Attached hereto as Appendix FAURA01 is a true and correct copy of “A Novel Mixed Signal Programmable Device with On-Chip Microprocessor” as published in *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*. I secured this copy myself from the Northwestern University Library’s digital holdings. In comparing Appendix FAURA01 to Exhibit 1006, it is my determination that Exhibit 1006 is a true and correct copy of “A Novel Mixed Signal Programmable Device with On-Chip Microprocessor” by Julio Faura, Chris Horton, Phuoc van Duong, Jordi Madrenas, Miguel Angel Aguirre and Josep Maria Insenser.

17. Attached hereto as Appendix FAURA02 is a true and correct copy of the MARC record for *Proceedings of 1997 IEEE Custom Integrated Circuits*

Conference as held by the Northwestern University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FAURA02 accurately describes the title, author, publisher, and ISBN number of *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*.

18. Attached hereto as Appendix FAURA03 is a true and correct copy of the MARC record for *Proceedings of 1997 IEEE Custom Integrated Circuits Conference* as held by the Indiana University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FAURA03 accurately describes the title, author, publisher, and ISBN number of *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*.

19. Attached hereto as Appendix FAURA04 is a true and correct copy of the MARC record for *Proceedings of 1997 IEEE Custom Integrated Circuits Conference* as held by the Queen's University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FAURA04 accurately describes the title, author, publisher, and ISBN number of *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*.

20. Attached hereto as Appendix FAURA05 is a true and correct copy of the MARC record for *Proceedings of 1997 IEEE Custom Integrated Circuits Conference* as held by the Linda Hall library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FAURA05 accurately describes the title, author, publisher, and ISBN number of *Proceedings of 1997 IEEE Custom Integrated Circuits Conference*.

21. The MARC records included within Appendices FAURA02 - 05 all contain 008 fields that designate the date of record creation, indicating a range of public availability via these libraries and institutions. Appendix FAURA02 has a 008 field of August 30, 2001. Appendices FAURA03 & 05 have a 008 field of July 11, 1997. Appendix FAURA04 has a 008 field of February 10, 1998.

22. Considering this information, it is my determination that *Proceedings of 1997 IEEE Custom Integrated Circuits Conference* and therefore "A Novel Mixed Signal Programmable Device with On-Chip Microprocessor" was made available and accessible to the public by shortly after July 11, 1997 and certainly no later than February 10, 1998.

23. I note that Faura was cited in other IEEE publications prior to 2001, further confirming its public availability. For example, IEEE Explore lists other IEEE publications that have cited Faura, including four other references with publication dates in the 1990s. See Appendix Faura06 (<https://ieeexplore.ieee.org/document/606594/citations#citations>).

24. I have reviewed Exhibit 1005, “The Texas Instruments TMS320C25 Digital Signal Microcomputer” by Gene A. Frantz, Kun-Shan Lin, Jay B. Reimer and Jon Bradley as published in *IEEE Micro*, December 1986.

25. Attached hereto as Appendix FRANTZ01 is a true and correct copy of “The Texas Instruments TMS320C25 Digital Signal Microcomputer” as published in *IEEE Micro*. I secured this copy myself from the Carnegie Library of Pittsburgh’s holdings. In comparing Appendix FRANTZ01 to Exhibit 1005, it is my determination that Exhibit 1005 is a true and correct copy of “The Texas Instruments TMS320C25 Digital Signal Microcomputer” by Gene A. Frantz, Kun-Shan Lin, Jay B. Reimer and Jon Bradley as published in *IEEE Micro*, December 1986.

26. Attached hereto as Appendix FRANTZ02 is a true and correct copy of the MARC record for *IEEE Micro* as held by the Carnegie Library of Pittsburgh.

I secured this record myself from the library's public catalog. The MARC record contained within Appendix FRANTZ02 accurately describes the title, author, publisher, and ISSN number of *IEEE Micro*.

27. Attached hereto as Appendix FRANTZ03 is a true and correct copy of the MARC record for *IEEE Micro* as held by the Carnegie Mellon University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FRANTZ03 accurately describes the title, author, publisher, and ISSN number of *IEEE Micro*.

28. Attached hereto as Appendix FRANTZ04 is a true and correct copy of the MARC record for *IEEE Micro* as held by the Penn State University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FRANTZ04 accurately describes the title, author, publisher, and ISSN number of *IEEE Micro*.

29. Attached hereto as Appendix FRANTZ05 is a true and correct copy of the MARC record for *IEEE Micro* as held by the Ohio University library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FRANTZ05 accurately describes the title, author, publisher, and ISSN number of *IEEE Micro*.

30. Attached hereto as Appendix FRANTZ06 is a true and correct copy of the MARC record for *IEEE Micro* as held by the SUNY Buffalo library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix FRANTZ06 accurately describes the title, author, publisher, and ISSN number of *IEEE Micro*.

31. The MARC records included within Appendices FRANTZ02 - 06 all contain 008 fields that designate the date of record creation, indicating a range of public availability via these libraries and institutions. For periodicals such as *IEEE Micro*, this date also signifies the first date of subscription to that periodical as future issues of the same periodical will be appended to a singular record. Appendices FRANTZ02, FRANTZ03 & FRANTZ06 have 008 fields of October 6, 1980. Appendix FRANTZ04 has a 008 field of January 5, 1982. Appendix FRANTZ05 has a 008 field of January 30, 1985. Appendices FRANTZ02 – 06 each indicate that each library collected further issues of *IEEE Micro* in perpetuity after initial acquisition and each library's collection contains the December 1986 edition of *IEEE Micro* containing "The Texas Instruments TMS320C25 Digital Signal Microcomputer". Considering this information, it is my determination that *IEEE Micro* and therefore "The Texas Instruments TMS320C25 Digital

Signal Microcomputer” was made available and accessible to the public by shortly after initial publication in Winter 1986.

32.I note that Frantz was cited in other IEEE publications prior to 2000, further confirming its public availability. For example, IEEE Explore lists other publications that have cited Frantz, including eleven references with publication dates in the 1980s-1990s. *See* Appendix FRANTZ07 (<https://ieeexplore.ieee.org/document/4089742/citations#citations>).

33.I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of \$100.00 per hour plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

34.I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 2/2/2023

A handwritten signature in black ink, appearing to read "June Ann Munford". The signature is written in a cursive style with a large initial "J" and "M".

June Ann Munford

APPENDIX CV

J. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.
- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.
- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in

Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over \$400,000 and total assets of approximately \$1,300,000.

- Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.
- Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.
- Led the organization and digitization of the library's archival records.
- Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.
- Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013

Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

- Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.
- Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.
- Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013

Library Assistant, Hart Area Public Library
Hart, MI

- Responsible for verifying imported MARC records and original MARC

cataloging for the local-level collection as well as the Michigan Electronic Library.

- Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

- Treasurer, 2012

Library Of Michigan

- Level VII Certification, 2008
- Level II Certification, 2013

Michigan Library Association Annual Conference 2014

- New Directors Conference Panel Member

Southwest Michigan Library Cooperative

- Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008

Petoskey, MI

- Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011

Nashville, TN

- Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012

Fairbanks, AK

- Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 • Fish & Richardson

IPR Petitions of 865 Patent, Apple v. Qualcomm (IPR2018-001281 / 39521-00421IP & IPR2018-01282 / 39521-00421IP2)

2019 • Erise IP

Implicit, LLC v. Netscout Systems, Inc (Civil Action No. 2:18-cv-53-JRG)

2019 • Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Cases IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 • O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case 5:19-cv-00036-RWS)

2021 • Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case IPR2020-1449)

Limited Case History & Potential Conflicts

Alston & Bird

- Nokia (v. Neptune Subsea, Xtera)

Arnold & Porter

- Ivantis (v. Glaukos)

Erise I.P.

- Apple

v. Future Link Systems (IPRs 6317804, 6622108, 6807505, and 7917680)

v. INVT

v. Navblazer LLC (Case No. IPR2020-01253)

v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Quest Nettech Corp, Wynn Technologies (Case No. IPR2019-00XXX, RE. Patent Re38137)

- Fanduel (v CGT)
- Garmin (v. Phillips North America LLC, Case No. 2:19-cv-6301-AB-KS Central District of California)
- Netscout
 - v. Longhorn HD LLC)
 - v. Implicit, LLC (Civil Action No. 2:18-cv-53-JRG)
- Sony Interactive Entertainment LLC
 - v. Bot M8 LLC
 - v. Infernal Technology LLC
- Unified Patents (v GE Video Compression, Civil Action No. 2:19-cv-248)

Fish & Richardson

- Apple
 - v. LBS Innovations
 - v. Masimo (IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1)
 - v. Neonode
 - v. Qualcomm (IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)
- Dish Network
 - v. Realtime Adaptive Streaming, Case No 1:17-CV-02097-RBJ)

v. TQ Delta LLC

- Huawei (IPR 76933211)
- Kianxis
- LG Electronics (v. Bell Northern Research LLC, Case No. 3:18-cv-2864-CAB-BLM)
- Metaswitch
- MLC Intellectual Property (v. MicronTech, Case No. 3:14-cv-03657-SI)
- Realtek Semiconductor
- Quectel
- Samsung (v. Bell Northern Research, Civil Action No. 2:19-cv-00286-JRG)
- Texas Instruments

Irell & Manella

- Curium

O'Melveny & Myers

- Apple (v. Maxell, Case 5:19-cv-00036-RWS)

Perkins-Coie

- TCL Industries (v. Koninklijke Philips NV, PTAB Case Nos. IPR2021-00495, IPR2021-00496, and IPR2021-00497)

Pillsbury Winthrop Shaw Pittman

- Intel (v. FG SRC LLC, Case No. 6:20-cv-00315 W.D. Tex)

APPENDIX DEHKORDI01

Development of a DSP/MCM Subsystem

Assessing Low-volume, Low-cost MCM Prototyping for Universities

Peyman Dehkordi, Tim Powell, Donald Bouldin
University of Tennessee¹

Abstract

*This paper discusses the design and development of a general-purpose programmable DSP subsystem packaged in a multichip module. The subsystem contains a 32-bit floating-point programmable DSP processor along with 256 K-byte of SRAM, 128 K-byte of FLASH memory, 10 K-gate FPGA and a 6-channel 12-bit ADC. The complete subsystem is interconnected on a 37 mm by 37 mm MCM-D substrate and packaged in a 320-pin ceramic quad flat pack. The design has been submitted to the MIDAS brokerage service to be fabricated by Micro Module Systems. Our experience shows that low-volume MCM prototyping is **achievable** and **somewhat affordable** for universities. The design flow, electrical and thermal analyses, CAD tools, cost and lessons learned are discussed in this paper.*

Introduction

Multichip module packaging has been in use by IBM and others for high-volume and/or high-cost products for many years but only recently has a low-volume and low-cost service become available to the design community. A variety of other reasons have also impeded growth including the availability of known good die (KGD) and the expense of sophisticated CAD tools optimized for this purpose. Previous work such as [1] discusses various MCM design techniques in depth; however, real-world MCM design problems are not well documented for the first-time users [2]. There has been a tremendous push from Advanced Research Project Agency (ARPA) for wide-spread usage of this technology for the past few years through their Application Specific Electronic Module (ASEM) program. As a result, MIDAS is now offering MCM services for low-cost prototyping [3]. As a part of our ARPA project, we have exercised the availability of this technology for universities. We have performed this exercise by acquiring the appropriate CAD tools and designing a subsystem using bare dies that were procured in small quantities within the required time period. The final design has been submitted to MIDAS for fabrication.

Design Flow

We decided to implement a design representing a typical application of a MCM including a processor, memory and gate-array. It consists of a complete DSP subsystem based on the Motorola 96002 32-bit floating point DSP processor as shown in Figure 1. The module also includes 256 K-byte of SRAM, 128 K-byte of EEPROM, a 10 K-gate Xilinx 4010 FPGA and a 6-channel 12-bit ADC. The module was designed to exploit the multi-processing capability of the 96002. The FPGA is primarily a hardware pre-processor of incoming data but also provides other generic logic functions required for implementation of the entire subsystem.

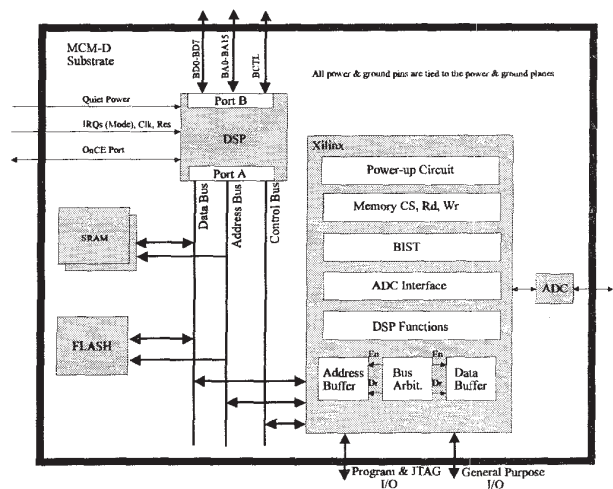


Figure 1. The Block Diagram of the DSP Sub-system.

The design flow is shown in Figure 2 along with the CAD tools used. We had to modify our original plans several times in order to be certain that all of the dies could be acquired within the desired time frame. We found out that it is a good practice to establish a good working relationship with the die supplier to reduce the design cycle as well as die cost and to take advantage of the availability of dies which have already been tooled by the supplier. We performed an early analysis on the candidate design to make

¹ This work was sponsored in part by ARPA under grant DAAH04-94-G-0004

sure the selected components would fit within the various available substrate sizes offered by MIDAS.

We were constrained to select one of a few choices of substrates and packages offered by MIDAS at the time. The substrate selected is a 37 mm x 37 mm 5-layer (1 pad, 2 power, and 2 routing layers, 62 μ pitch) MCM-D based on the MMS *Merged Via D500* process [4]. It utilizes copper/polymide for interconnect/dielectric and an aluminum substrate as a ground plane. The package is a cavity-down, 320-pin ceramic quad flat pack with preassigned power and ground pins and a lead pitch of 0.65 mm.

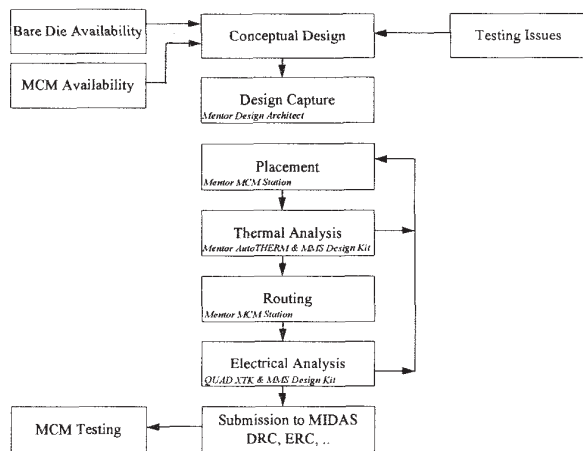


Figure 2. The Design Flow and CAD Tools.

Obtaining the bare dies was probably the most challenging part of this exercise. Traditionally, third party die suppliers have been providing bare dies for the MCM and hybrid markets. Due to increased MCM activities, some of the semiconductor manufacturers (i.e Intel, Motorola) have started selling some of their products in bare die form. For example, Intel offers some of its dies through its *Smart die* program. We have found that there is a long lead time (16 weeks) with these parts and it is necessary to execute a legal agreement between the supplier and the university. This step alone can delay a project by several months in our experience. Another issue was the minimum quantity which suppliers wanted us to buy was sometimes several hundred dies costing several thousand dollars, which exceeded our budget for this low-volume project.

We contacted three die suppliers; however, only Chip Supply was very helpful with our die needs. *Known Good Die* was another issue we faced [5]. A true KGD (fully tested at speed and burned-in) could be very expensive, especially considering that the NRE cost for tooling a new die may be \$15,000. We ended up purchasing bare dies which had been only wafer probed and visually inspected.

All other bare die were donated to us and had undergone similar testing which was acceptable since we will prototyping only five copies of our MCM.

Electrical Analysis

Once the design was finalized and all the components were selected, the MCM physical design was performed using the *Mentor Graphics MCM Station*. The foundry design kit for MMS was obtained via MIDAS and facilitated template generation for the components and their bond-pads on the substrate. This included all the connections to the power and ground layers as well as thermal via generation for each die. Once a good placement of the components was reached (conforming to the electrical and thermal constraints), the critical nets were manually routed and the autorouter was then invoked. Figure 3 shows the final routed layout.

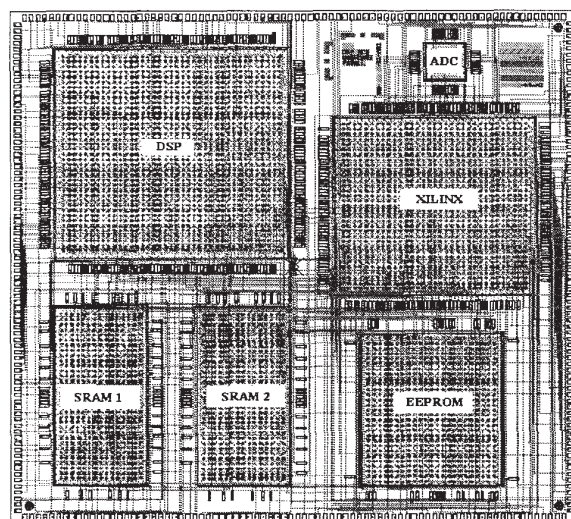


Figure 3. The Physical Layout of the MCM.

None of the components were speed-rated due to the procurement reasons described above. We assume a nominal frequency of operation of about 40 MHz since the DSP die has come from a 40 MHz lot. The entire design was simulated with QUAD's XNS tool which uses a time-domain finite element analysis technique to compute over/under shoot, simultaneous switching noise, rise/fall times, and coupling noises on circuit networks of arbitrary topology. A typical multi-drop net model and its electrical simulation are shown in Figure 4 and 5 respectively.

The maximum delay was found to exist between the DSP and the FPGA on an address line and computed to be 1.8 nS. Approximately 55% of the signals are under 1.0 nS delay and the longest total net length including all branches was

77.286 mm. The delay distribution on the module is shown in below:

	percent paths exceeding											
	0	10	20	30	40	50	60	70	80	90	100	
time(nS)	----- ----- ----- ----- ----- ----- ----- ----- ----- ----- ----- -----											
0.00	*****											
0.17	*****											
0.33	*****											
0.50	*****											
0.67	*****											
0.83	*****											
1.00	*****											
1.17	*****											
1.33	***											
1.50	**											
1.67	*											

The maximum crosstalk was also induced on an address line and was simulated to be 214 mV. The crosstalk was only calculated on the plane of the routed trace. The other routing plane which might couple intersecting traces was not considered. The reflections were simulated to be low since the source impedance of the driver added to the line resistance presenting a source-series termination [6]. The simulation data suggests that the limiting speed factor in this design (with the current models) would be the data bus. Almost all data lines exhibited noticeably more slewing than address lines. We were not able to get the I/O models from the die vendors. Various published I/O models from other vendors were used in the simulation. Although the results may not be very accurate (due to I/O buffer assumption), they can outline the trouble nets and general characteristics of the design. A detailed analysis is presented in [7].

Thermal Analysis

MCMs integrate several large VLSI dies consuming several watts within a small area. Thermal analysis of an MCM is very important to ensure a reliable operation. The objective of thermal analysis is to predict the junction temperature of the dies in determining long-term reliability of the components and the module. The thermal path from the die to the heat sink is comprised of the following three paths [4]:

$$\begin{aligned} \text{Path}_1 &= R_{\text{die}} + R_{\text{die epoxy}} + R_{\text{interconnect}} + R_{\text{interconnect epoxy}} \\ \text{Path}_2 &= R_{\text{interconnect epoxy}} \\ \text{Path}_3 &= R_{\text{thermal grease}} + R_{\text{heat sink}} \end{aligned}$$

Thermal vias were placed under all the dies to improve the thermal conductivity path from the dies to the backing plate. Thermal vias were created in such a fashion to allow two traces between them. This resulted in less routing penalty under the dies due to the thermal vias. The junction temperature distribution is shown in Figure 5 for an ambient

temperature of 25° C. The results were generated by the *Mentor Graphic AutoTHERM* using two-dimensional finite-element mesh analysis. The maximum junction temperature was simulated to be 50° C at the DSP which is well within the maximum rating of the dies. The module specification is shown in Table 1.

Cost & Testing Issues

The purpose of this section is to provide the reader with a *rather realistic* cost for this MCM. We have prototyped a total of 5 MCMs which each MCM costing about \$ 2,780. The total cost of the bare die was \$ 1,300, assuming retail prices for the donated die. The cost of the bare dies included the dies and wafer-probe and visual inspections for the *stocked* dies. The substrate cost of \$ 1,480 per MCM included the fabrication and test of the substrate, assembly of the dies onto the substrate and the CQFP package. The cost associated with the final system testing, design time, and the CAD tools have *not* been included in the \$2,780.

Due to their small feature sizes, MCMs cannot easily be probed or reworked [8]. Therefore, testing and fault isolation becomes a challenging area for MCM designs. Complete boundary scan testing was not feasible for this MCM since only the FPGA supported JTAG. The DSP supports a serial emulation port which was connected to the module pins along with the FPGA TAP port for testing purposes. The FPGA has a RAM-based configuration where the configuration may come from outside the module. A portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the module. The FPGA can easily be reconfigured to route these lines to the module pins for possible probing and debugging during testing. The DSP has a dual data and address port architecture in which the second port was also connected to the module pins for enhanced multi-processing and testing. Testing procedures are being constructed at the time of this publication.

Conclusion

Multichip modules are becoming a viable choice of packaging for high performance / miniaturized electronics. This technology is no longer considered to be an exotic technology and is being used in telecommunications, consumer electronics and workstations. Low-cost, low-volume prototyping capabilities are a "must" for university related programs as well as small/medium size companies who wish to utilize this technology. We have found out that accessing this technology is becoming a reality for university programs at *almost* low-cost. The MMS design-kit was *very* useful not only with the physical layout but also since it provided a variety of check points and design tips. Availability of the bare dies (and their I/O buffer models), testing and rework issues will continue to be challenging issues to be considered. We are looking forward to getting

the MCM back to confirm the functionality as well as validating the thermal/electrical analysis.

Substrate	37 mm by 37 mm MCM-D
Package	320 pin CQFP
Power consumption	10 W
Power Density	0.73 W/cm ²
Number of dies	6
Number of signal nets	284
Silicon Efficiency	51 %
Average net length	22 mm
Longest net length	77 mm
Total vias	510
Total wire-bonds	930
Module Cost	\$ 2,780 (MCM + dies)

Table I) Module Specification

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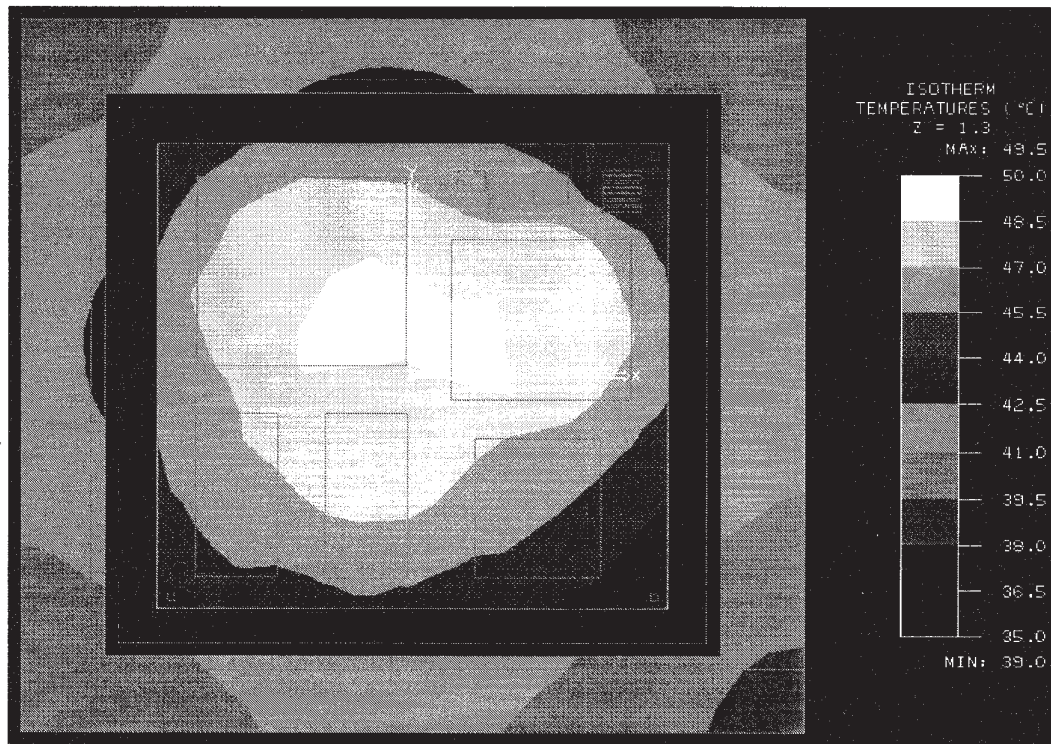
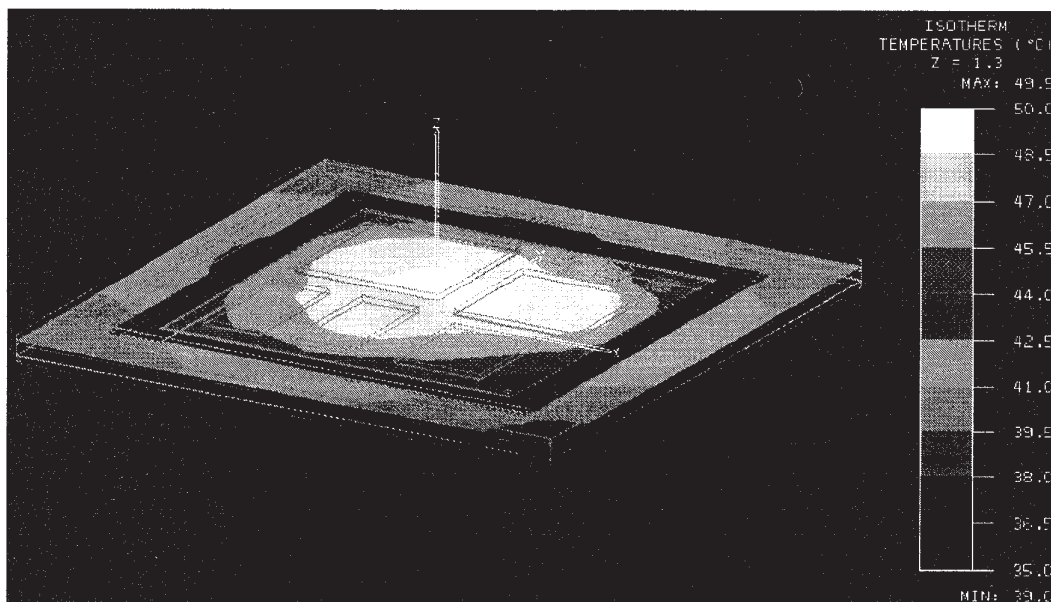


Figure 6. Thermal Analysis Simulation Results.

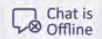
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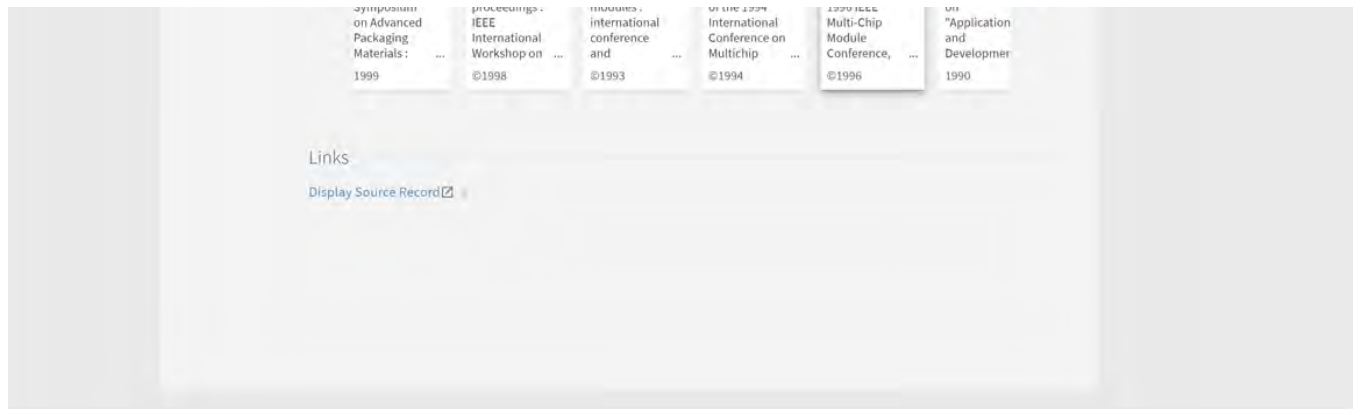
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- ☐ **Polymer optical couplers for applications in multi-chip modules**
- Tsang-Der Ni; D. Sturzebecher
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- R.A. Shick; B.L. Goodall; L.H. McIntosh; S. Jayaraman; P.A. Kohl; S.A. Bidstrup-Allen; N.R. Grove
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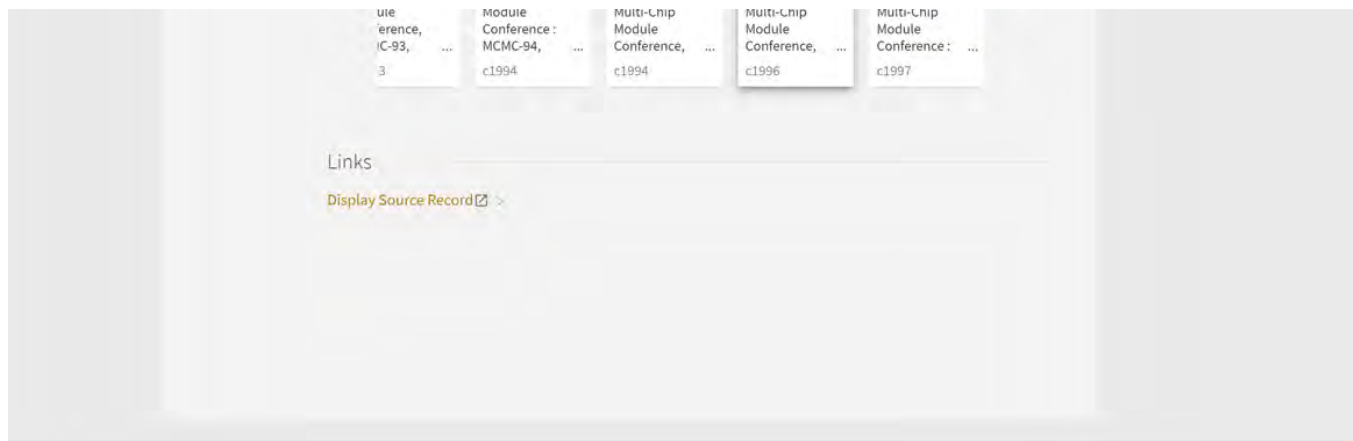
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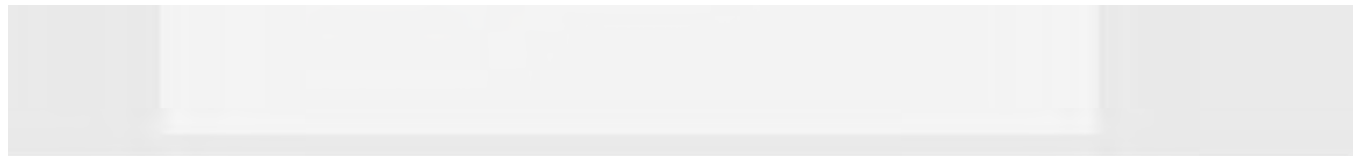
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APPENDIX FAURA01

A NOVEL MIXED SIGNAL PROGRAMMABLE DEVICE WITH ON-CHIP MICROPROCESSOR

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Abstract

In this paper we present a novel field programmable mixed-signal integrated device consisting of a Field Programmable Gate Array (FPGA), a set of programmable and interconnectable analog cells, and a microprocessor core. This processor can run general purpose user programs, handle the dynamic reconfiguration of the programmable blocks and probe in real time internal digital and analog signals. The device is especially suitable for development and fast prototyping of mixed signal integrated applications.

Introduction

As the complexity of electronic systems grows, it becomes more and more difficult to follow a traditional design methodology of working separately on different subsystems with different design and prototyping tools. System designers have been craving for flexible prototyping systems onto which they could map large designs to validate them before fabrication. Typically, these designs may include a digital part, an analog part and a software program running on a microprocessor or microcontroller. However, these three domains (digital, analog and software) have to be designed and prototyped separately, using different CAD tools and hardware parts for each one. Besides FPGAs, only recently analog arrays have been available (1) (2), which confirms the interest shown by the industry for field-programmable devices suitable for fast prototyping and small time to market applications.

Within this framework we introduce the FIPSOC (Field Programmable System On Chip) prototyping and integration system, consisting of a mixed-signal Field Programmable Device (FPD) with a standard microprocessor core (a 8051), a suitable set of CAD tools to easily program it, and a set of library macros and cells which support a number of typical applications to be easily mapped onto the FPD and migrated to an ASIC afterwards, if required.

The advantage of this approach relies upon the fully integrated design and prototyping methodology that the user can follow with such a system, because he can download his application onto the programmable hardware and then use the internal microcontroller to probe it in real time (both digital and analog). A powerful integrated set of user-friendly CAD tools is provided, with the final target of

letting the user specify, simulate, emulate (probe in real time) and map the complete design on to a single chip using one design environment. Also, a suitable library has been developed providing a very easy path for migration to ASIC after the prototyping phase.

The FIPSOC project is still under development, and will provide a complete family of devices comprising a number of different sizes and models. Only worst case simulation results from the first family member will be given.

This paper is mainly focused on the FIPSOC chip architecture and is organized as follows. The following section describes the circuit in its three parts (digital hardware, analog cells and microprocessor core and interface). Next, we explain how the multicontext dynamic reconfiguration works in this device and how it can be applied to hardware-software interaction. Then, we describe how this system can be used as a prototyping workbench with real time probing. Finally, we give some ideas about the CAD tools being developed to manage this chip.

System Description

Fig. 1 shows a block diagram of the FIPSOC device.

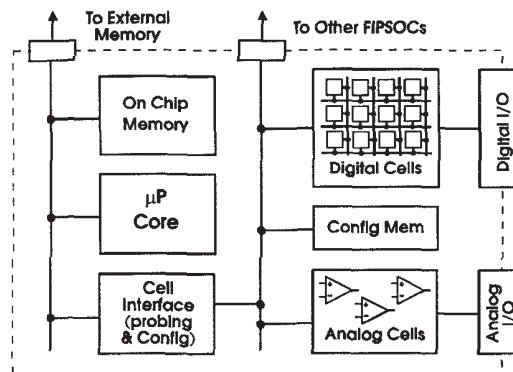


Fig.1: Block diagram of the FIPSOC chip

The chip is a mixed signal field programmable device with an on-chip microcontroller. It includes a Field Programmable Gate Array (FPGA), a set of fixed-functionality yet configurable analog cells, and a microprocessor core with RAM memory and some peripherals. The programmable digital and analog blocks are well defined and are separated from one another due to

noise immunity considerations. Nevertheless, the different interfaces between these blocks themselves and to the microprocessor provide a very powerful interaction between software, digital hardware and analog hardware.

The chip has been designed using a full custom methodology for the FPGA and the analog area, and a synthesized *soft core* for the microcontroller. A 0.5μm triple metal layer CMOS 3V process provided by ATMEL ES2 was chosen to implement the first generation of this device. In the next paragraphs we describe separately the programmable digital cells (the FPGA), the configurable analog blocks, and the microcontroller. Finally, we talk about the interfaces between these three blocks.

A. Programmable Digital Hardware

The FIPSOC chip includes a two-dimensional array of programmable DMCs (Digital Macro Cell). The DMC is a large granularity, Look Up Table (LUT) based, synthesis targeted 4-bit wide programmable cell. Fig. 2 shows a simplified block diagram of the DMC.

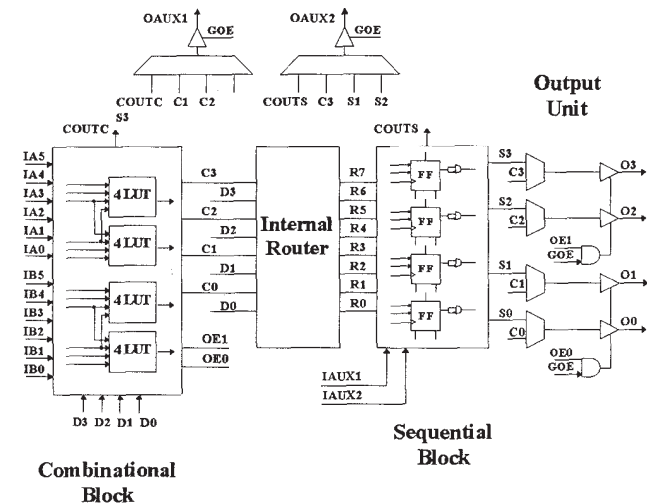


Fig.2: Simplified DMC block diagram

The DMC has two main blocks: a combinational part, composed of four 4-input LUTs, and a sequential block including four FFs. Between them there is an internal router which provides the necessary connectivity, and makes it possible to feed direct inputs into the FFs rather than using the combinational outputs. This makes it possible to use the combinational and the sequential blocks more or less independently. Each lookup table (LUT) can implement any Boolean function of 4 inputs. Every two 4-input LUTs share two inputs, and two LUTs can be combined to form a 5 input function or a 4 to 1 multiplexer (four inputs and two control bits). The four LUTs of a DMC can be combined to perform any 6 input Boolean function. The whole combinational part of the DMC can be configured as a 16x4 RAM memory (in fact, two independent 16x2 memories) or as a cascadable 4-bit adder or subtractor with carry-in and carry-out (also some other arithmetic functions are possible).

The sequential part of the DMC includes four two-input flip-flops (FF), each of which can be independently configured

as mux-type or enable-type, as latch or FF, and with synchronous and asynchronous set or reset. Again, the whole sequential part of the DMC can be configured as a cascadable shift register with load and enable or as a cascadable 4-bit up/down counter with load and enable.

These combinational and sequential macro functions are especially suitable to be used by synthesis programs (4). The routing architecture of this FPGA core has been designed according to this large granularity philosophy. Tracks spanning one, two and four DMCs (horizontally and vertically) are provided for general purpose interconnect. Long lines spanning the whole height or width of a column or a row and dedicated tracks for global reset and clock spine distribution are provided. Interconnection switches composed of MOS transistors are controlled with RAM memory cells writeable by the microprocessor.

Table 1 summarizes the preliminary worst case timing characteristics obtained from simulation in worst case conditions.

Parameter	Value (Worst)	Units
LUT delay	4.3	ns
FF propagation time	2.2	ns
FF setup time	2.4	ns
Routing track delay (spanning 1 DMC)	3.0	ns

Table 1: Preliminary Timing Characteristics (Worst Case Simulation)

B. Configurable Analog Hardware

The analog subsystem is composed of fixed functionality (yet programmable) blocks of coarse granularity. The basic building block is depicted in fig. 3. Each FIPSOC family members will have a different number of these blocks.

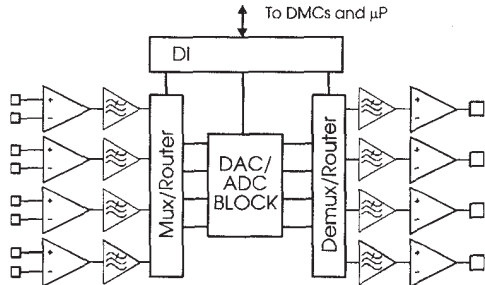


Fig.3: Analog block

The analog block is intended to support four input/output analog channels with amplification, filtering, comparison and digital conversion. The functionality of the analog cells is fixed, although the cells themselves are programmable. For instance, the amplifier cell can only work as an amplifier (not as a filter or as a comparator) but its gain can be selected from a given range. In particular, the DAC/ADC block is especially flexible and actually quite suitable for analog programmable hardware, in that it can be configured as a 10 bit block, two 9 bits blocks or four 8 bits blocks. Each block can be independently configured as DAC or ADC. As it can be seen, the user can select between accuracy and number of channels depending of the design tradeoffs.

A flexible interconnection architecture is provided to let the user build a custom application out of these blocks. In particular, nearly any internal point of the analog block can be routed to the ADC. Then, the microprocessor can use the ADC to probe in real time nearly any internal signal of the analog structure by dynamically reconfiguring these analog routing resources.

Finally, it is worth noting that having dedicated hardware for each analog function allows an easy path for migration to ASIC, as the same cells used in the prototype can be used in the final ASIC design should production volume subsequently justify it.

C. Microprocessor Core

As it has been said, the chip contains a standard 8051 microcontroller, which can be used either for general purpose user applications or for configuration tasks. Apart from FPGA-microprocessor interface issues (3), most of the efforts done for on-chip integration of a microprocessor and programmable hardware have been targeted to enhance the processing power of the microprocessor (8) (9), by providing reconfigurable coprocessors or customizable instruction sets, while we have focused a bit more on prototyping needs.

As the commercial device, the microcontroller contains not only a microprocessor core but a serial port (RS232), timers, parallel ports, etc. In particular the serial port is used to allow the chip to communicate to a PC, so the user can download the configuration and debug his applications using a simple monitor program running in the microprocessor and controlling it from the PC.

The microprocessor core is totally standard so all commercial tools (assemblers, compilers, debuggers, etc.) available for 8051 can be used for the FIPSOC device.

D. Interfaces between Subsystems

Most of the power of this chip when used as a prototyping benchmark is the fact that the internal signals of the programmable hardware can be read and even sometimes written by the microprocessor as long as they are mapped as memory locations in the address map. For the digital part, the outputs of any DMC can be read as a memory location, and the FFs can also be written to by the microprocessor in real time. For the analog blocks, the ADCs can be directly read and the DACs can be directly written by the microprocessor in real time, and the comparators can be read as memory locations as well. Finally, the microprocessor address bus can also be physically connected to the digital routing channels, which could be necessary for building microprocessor peripherals (for example communication ports, coprocessors, etc.). These communication points between the analog hardware and the digital world are also linked to the digital programmable hardware: The output of the comparators and the ADCs can be connected to the digital routing channels (and therefore to the DMCs inputs), and the inputs of the DACs can be driven by DMC outputs.

Multicontext Dynamic Reconfiguration

As it has been already mentioned, the chip configuration is managed by the internal microprocessor. To do so, the configuration memory is organized in words which are mapped onto the microprocessor address space. Furthermore, the configuration data is duplicated. It can be shown that such a duplication only needs a chip area overhead of below 12%. These two possible configurations are called *contexts*.

The microprocessor can then read and write these memory locations while in operation. This allows the user to reconfigure a context while the other one is still active, then change the active context to the new one. With this approach, the whole circuit can be reconfigured just by issuing a microprocessor command, and the reconfiguration time would be that of a microprocessor write cycle. In fact, a set of cells rather than the whole chip can be selected before applying the reconfiguration command. The main advantage of this technique is the possibility of loading the new context data *while* the active context is still in operation, thus not having to stop while the reconfiguration is taking place. Furthermore, the data inside the FFs is also duplicated, and can also be read and written by the microprocessor while the application is running. When the context is swapped, the status of the FFs can be maintained or stored with the rest of the context. This makes possible to initialize the FFs in the non-active context before setting it as active, and also to save the values of the circuit nodes when changing the context.

This technique has been christened as *hardware swap*, and it makes it possible to efficiently work with *virtual hardware*. Non-active contexts hold their configuration and data just like virtual memory is stored into a swap archive in a computer system. A hardware swap takes place when the virtual hardware is mapped back onto the actual hardware resources, just like the information inside the swap archive is restored onto the actual memory of a computer when required again. Moreover, an analogy can be established between virtual hardware and software procedures: global variables in software procedures can be likened to data in the FFs which is kept after hardware swap, and procedure parameters can be compared to data in the FFs which are saved and restored during the hardware swap. Finally, this tool is specially suitable to apply *hardware procedures* as described in (5).

Several experiences (7) have already been reported on the use of multicontexts for programmable devices, although our approach here is different: The static RAM memory we use to store the contexts can be used as program memory. Therefore, the user can choose between having different contexts (thus being able to immediately change the hardware function) or having more program memory (thus sacrificing reconfiguration speed but gaining memory space). In (6) an interesting study on dynamic reconfiguration and its applications can be found. It can be

seen how the improvements suggested there have been already implemented in this new system.

Hardware-Software Interaction

The FIPSOC chip is especially suitable for hardware-software co-design techniques due to the flexible interfaces between the programmable hardware areas and the microprocessor core. The interaction between hardware and software is enhanced mainly due to: a) Internal signals from the programmable hardware can be probed and read as memory locations from the microprocessor core (analog signals have to be converted with the ADC). b) The microprocessor can dynamically reprogram a piece of hardware by overwriting the configuration memory. A co-design CAD tool could then be targeted to this device, putting in hardware those critical processes needing too high a computational speed, and performing with software those tasks which would be prohibitively area-consuming.

The FIPSOC as an Integrated Prototyping Workbench with Internal Probing Capability

It is possible to emulate a whole laboratory benchmark using just a FIPSOC Chip and a PC. The communication between them is normally done through the on-chip RS232 serial port (an external driver is needed for RS232 voltage levels). It has already been explained how the outputs of the DMCs can be probed as memory locations, and how the internal ADC block can be dynamically rewired to probe nearly any internal point of the analog architecture. Even the internal DAC could also be used as a function generator, accepting data from the microprocessor core or from some DMCs configured as counters and memories.

The rest of the laboratory workbench is a matter of software: A digital oscilloscope could be emulated to present the acquired analog data (from the internal ADC) on the PC screen; a logic state analyzer could be provided printing out the digital data obtained from the DMC outputs in real time. The real advantage is the integrated approach that the user can follow to develop his system application: Everything is integrated, and the final hardware and software solution is exactly what the user is measuring when probing in real time. The proposed analog programmable hardware is especially suitable for this operation. In particular, the possibility of severing the DAC/ADC block into a 9-bit ADC and two 8-bit DACs, and then using these two DACs to provide the ADC references, greatly simplifies the emulated digital oscilloscope described: the "offset" and "amplification factor" knobs would directly apply over the reference DACs.

CAD Tools for FIPSOC

An integrated set of software CAD tools is being developed for design entry and optimization, technology mapping, placement and routing, device programming, mixed-signal simulation and real-time system probing from a WindowsTM-based PC station. A convenient set of library functions is also provided to support typical design needs,

both digital and analog hardware functions as well as software procedures for the microcontroller. An easy path for migration to ASIC is then provided, because the analog cells of the library are exactly the same as those included in the field-programmable device, which ensures the reliability of the measurements done in the prototype. The digital hardware would normally be resynthesized to the ASIC library for an optimum area utilization.

Conclusions

A new concept to mixed-signal system design and prototyping for the FIPSOC device has been described and is currently under development. The key point of this workbench is the integrated methodology that can be carried out due to the flexibility of the configurable analog and digital hardware, and the simple interface between the digital resources, the analog subsystem and the microprocessor. It is estimated that the design cycle can be cut down by 30-40% by the use of the configurable hardware and the integrated emulation and verification design flows, compared with the use of separate analog and digital off-the-shelf FPGAs with their corresponding design tools. The use of the FIPSOC chip entails immediate reduction of PCB space, device reusability, dynamic reconfigurability and small time-to-market, which altogether makes the chip more than suitable for prototyping, pre-series fabrication and microelectronics research.

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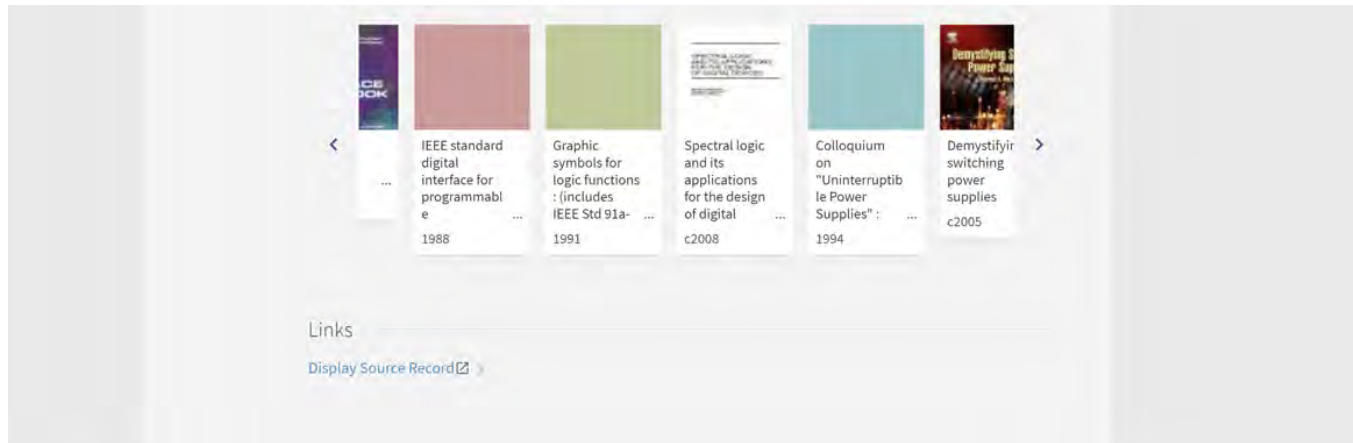
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ESD protection circuit by halo implant



P.V. Gilbert; P.G.Y. Tsui; Shih-Wei Sun; S. Jamison;
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- ☐ **A 0.25 /spl mu/m CMOS/SIMOX PLL clock generator embedded in a gate array LSI with 5 to 400 MHz lock range**



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- ☐ **A CMOS data and clock recovery macrocell for burst-mode/continuous-mode transmissions**



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- ☐ **Self-calibration of digital phase-locked loops**



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- ☐ **Fully integrated LVD clock generation/distribution IC**



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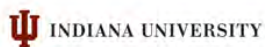
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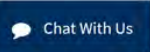
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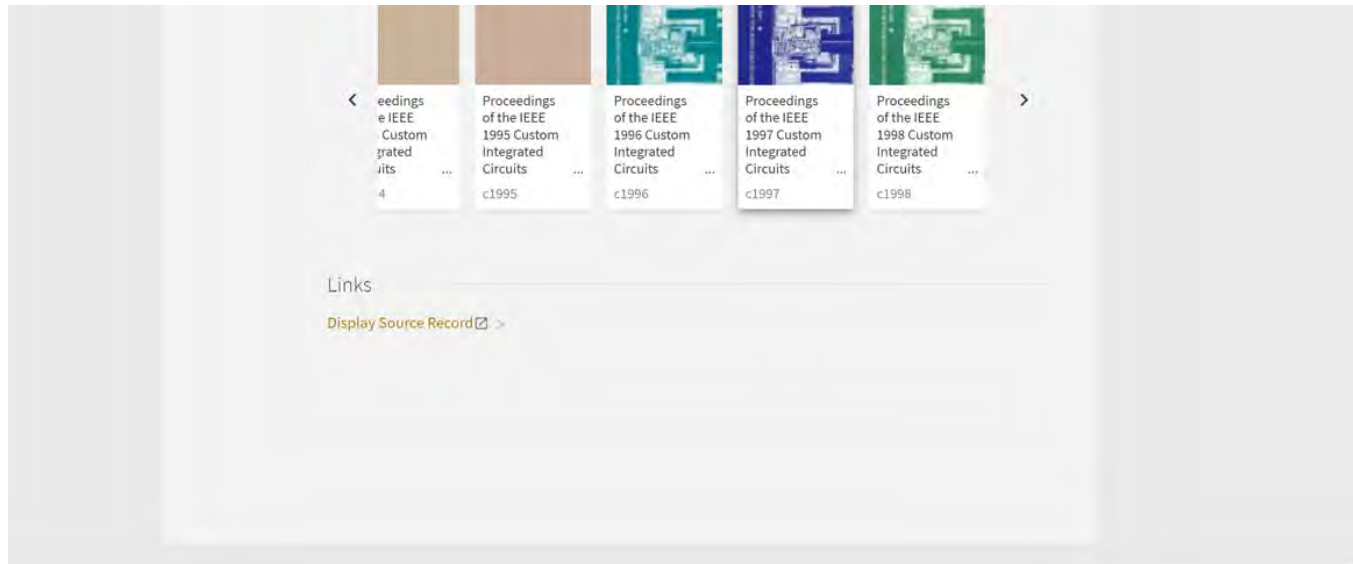
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In the next issue:

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See p. 88.

DEPARTMENTS

- 3 From the Editor-in-Chief
- 4 Letters to the Editor
- 74 MicroLaw
Software copyright developments
- 80 MicroStandards
Trial-use standards
- 81 MicroNews
- 84 MicroReview
Mirror; Ram-Resident Printmerge;
Referee
- 85 New Products
- 88 Advertiser/Product Index
- 88A Reader Service Card;
Reader Interest Card

FEATURE ARTICLES

DIGITAL SIGNAL PROCESSING

6

Guest Editor's Introduction

L. Robert Morris

10

The Texas Instruments TMS320C25 Digital Signal Microcomputer

Gene A. Frantz, Kun-Shan Lin, Jay B. Reimer, and Jon Bradley
Capable of 10 million operations per second, the newest member of the TMS320 family can serve as an inexpensive alternative to bit-slice processors or custom ICs in digital signal processing applications.

29

The Motorola DSP56000 Digital Signal Processor

Kevin L. Kloker

The DSP56000 brings 10.25-MIPS performance to digital signal processing and retains enough similarities to other Motorola microprocessors to make it easy to learn and program.

49

The ADSP-2100 DSP Microprocessor

John P. Roesgen

The 2100 accesses external memory efficiently and devotes its silicon area to providing greater functionality and processing throughput.

60

NEC's μ PD77230 Digital Signal Processor

Bill Eichen

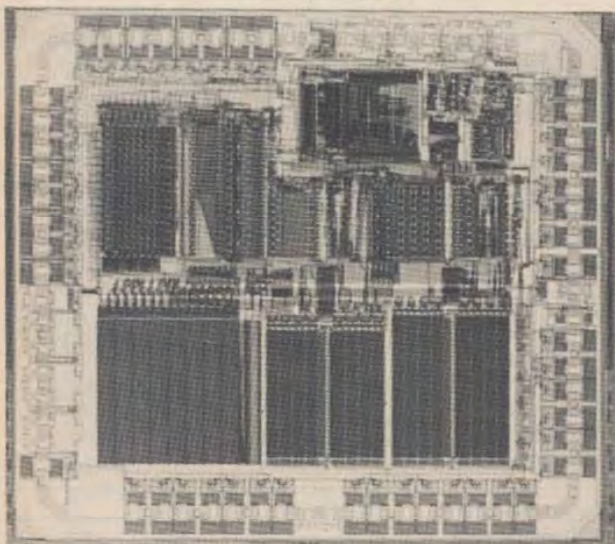
This 150-ns device performs full 32-bit floating-point arithmetic, incorporates on-chip instruction and data memory, and provides both serial and parallel I/O.

70

1986 Annual Index

The Texas Instruments TMS320C25 Digital Signal Microcomputer

Gene A. Frantz, Kun-Shan Lin,
Jay B. Reimer, and Jon Bradley
Texas Instruments Incorporated



Capable of 10 million operations per second, the newest member of the TMS320 family can serve as an inexpensive alternative to bit-slice processors or custom ICs in digital signal processing applications.

Digital signal processing encompasses a variety of applications, including digital filtering, speech vocoding, image processing, fast Fourier transforms, and digital audio.¹⁻⁵ All DSP applications have several characteristics in common. First, they employ algorithms that are mathematically intensive. An example is the finite-duration impulse response, or FIR, filter, which in the time domain takes the form

$$y(n) = \sum_{i=1}^N a(i) \cdot x(n-i), \quad (1)$$

where $y(n)$ is the output sample at time n , $a(i)$ is the i th coefficient or weighting factor, and $x(n-i)$ is the $(n-i)$ th input sample. From this equation, we can see that the FIR filter contains an abundance of multiplications and additions (that is, sums of products). This equation is the general form of an FIR filter⁶ as well as the convolution of two sequences of numbers $a(i)$ and $x(i)$.⁷ Both operations are fundamental to digital signal processing.

Second, DSP algorithms must be performed in real time; i.e., they must not produce a delay noticeable to the user. In a speech recognition system, for example, the algorithms must not produce a noticeable delay between a word being spoken and that word being recognized. In an image processing system, processing needs to be completed within a frame update period.

Third, all DSP applications involve the sampling of a signal. Referring to Equation 1, we can see that the output $y(n)$ is calculated to be the weighted sum of the previous N inputs. In other words, the input signal is sampled at periodic intervals, and the samples are multiplied by a weighting factor $a(i)$ and then added together to give the output result $y(n)$. In a typical DSP application, the processor must be able to perform arithmetic computations and effectively handle sampled data in large quantities.

Last, DSP systems must be flexible enough to incorporate improvements in the state of the art. Many DSP techniques are still developing, and therefore their algorithms tend to change. Speech recognition, for example, is presently an inexact technique still undergoing algorithmic modification. This implies that DSP systems need to be programmable so that they can easily accommodate revised algorithms.

Over the past several decades, digital signal processing machines have taken several forms in response to application need and available technology. Array processors have long been the accepted solution for the research laboratory and have been extended to end applications in some instances. However, as integrated circuit technology has matured, digital signal processing has migrated from the array processor to the bit-slice processor to the single-chip processor. This has brought the cost of DSP solutions down to a point that allows pervasive use of the technology.

The members of the TMS320 family of devices are examples of the single-chip digital signal processor. The first member of the family, the TMS32010, was introduced to the market in 1983.^{8,9} It can perform five million DSP

operations per second, including the add and multiply functions¹⁰ required in Equation 1. The newest member of the family, the TMS320C25, can perform 10 million DSP operations per second,¹¹ and it combines the multiply/accumulate functions into one single-cycle operation.

Basic TMS320 architecture

The fundamental attribute of a digital signal processor is fast arithmetic operations. The members of the TMS320 family,¹⁰⁻¹² like many other digital signal processors, achieve fast arithmetic operations by employing

- a Harvard architecture,
- a dedicated hardware multiplier,
- special DSP instructions, and
- extensive pipelining.

Use of these concepts allows a digital signal processor to handle a vast amount of data and execute most DSP operations in a one-cycle instruction.

The TMS320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture,^{13,14} the program memory and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The TMS320 family's modification of the Harvard architecture allows transfers between the program space and data space, thereby increasing the flexibility of the devices in the family. This architectural modification eliminates the need for a separate coefficient ROM and also maximizes processing power by maintaining two separate bus structures (program and data) for full-speed execution.

The TMS320 family's dedicated hardware multiplier employs a 16×16 -bit organization, which yields a 32-bit result and allows multiplication to take place in a single cycle. The special DSP instructions include DMOV (data move) and RPT (repeat), which speed up DSP operations. The extensive pipelining ensures maximum throughput for real-time applications.

The TMS320C25 architecture

The TMS320C25 digital signal processor is a microcomputer with a 32-bit internal Harvard architecture and a 16-bit external interface. It is a pin-compatible CMOS version of the TMS32020 microprocessor but has an instruction execution rate twice as fast and includes additional hardware and software features. The TMS320C25's instruction set is a superset of that of the TMS32010 and that of the TMS32020, and it maintains source-code compatibility with them. In addition, it is completely object-code-compatible with the TMS32020 so that TMS32020 programs can run unmodified on the TMS320C25. Some of the major features of the TMS320C25 are

- a 32-bit ALU and accumulator,
- an instruction cycle time of 100 ns,

- a single-cycle multiply/accumulate,
- use of low-power CMOS technology with a power-down mode,
- 4K 16-bit words of on-chip masked ROM,
- 544 words of on-chip data RAM,
- 128K words of data/program memory space,
- eight auxiliary registers with a dedicated arithmetic unit,
- an eight-level hardware stack,
- a fully static double-buffered serial port,
- concurrent DMA that uses an extended hold operation,
- bit-reversed addressing modes for fast Fourier transforms,
- extended-precision arithmetic and adaptive filtering support,
- full-speed operation of data move instructions from external memory,
- an accumulator carry bit and related instructions, and
- fabrication in 1.8- μ m CMOS and packaging in a 68-pin PLCC.

The 100-ns instruction cycle time provides a significant throughput advantage for many applications. Since most of the TMS320C25's instructions can execute in a single cycle, it can execute 10 million instructions per second. Most of the other features listed above also contribute to the TMS320C25's high throughput.

The TMS320C25 includes instructions to perform the data transfers between program space and memory space discussed earlier. Externally, the program and data memory spaces are multiplexed over the same bus so as to maximize the address range for both spaces and minimize the pin count of the device. Internally, the TMS320C25 architecture maximizes processing power by maintaining two separate bus structures, program and data, for full-speed execution.

Program execution in the device takes the form of a three-level instruction fetch-decode-execute pipeline. This pipeline is invisible to the user except in cases in which it must be broken, such as for branch instructions. In this case, the instruction timing takes into account the fact that the pipeline must be emptied and refilled.

Two large, on-chip data RAM blocks (a total of 544 words), one of which is configurable either as program or data memory, are provided. An off-chip, 64K-word, directly addressable data memory address space is included to facilitate implementations of DSP algorithms with large data memory requirements. Four-K words of on-chip program ROM and 64K words of off-chip program address space are available. Large programs can execute at full speed from this memory space. Programs can also be

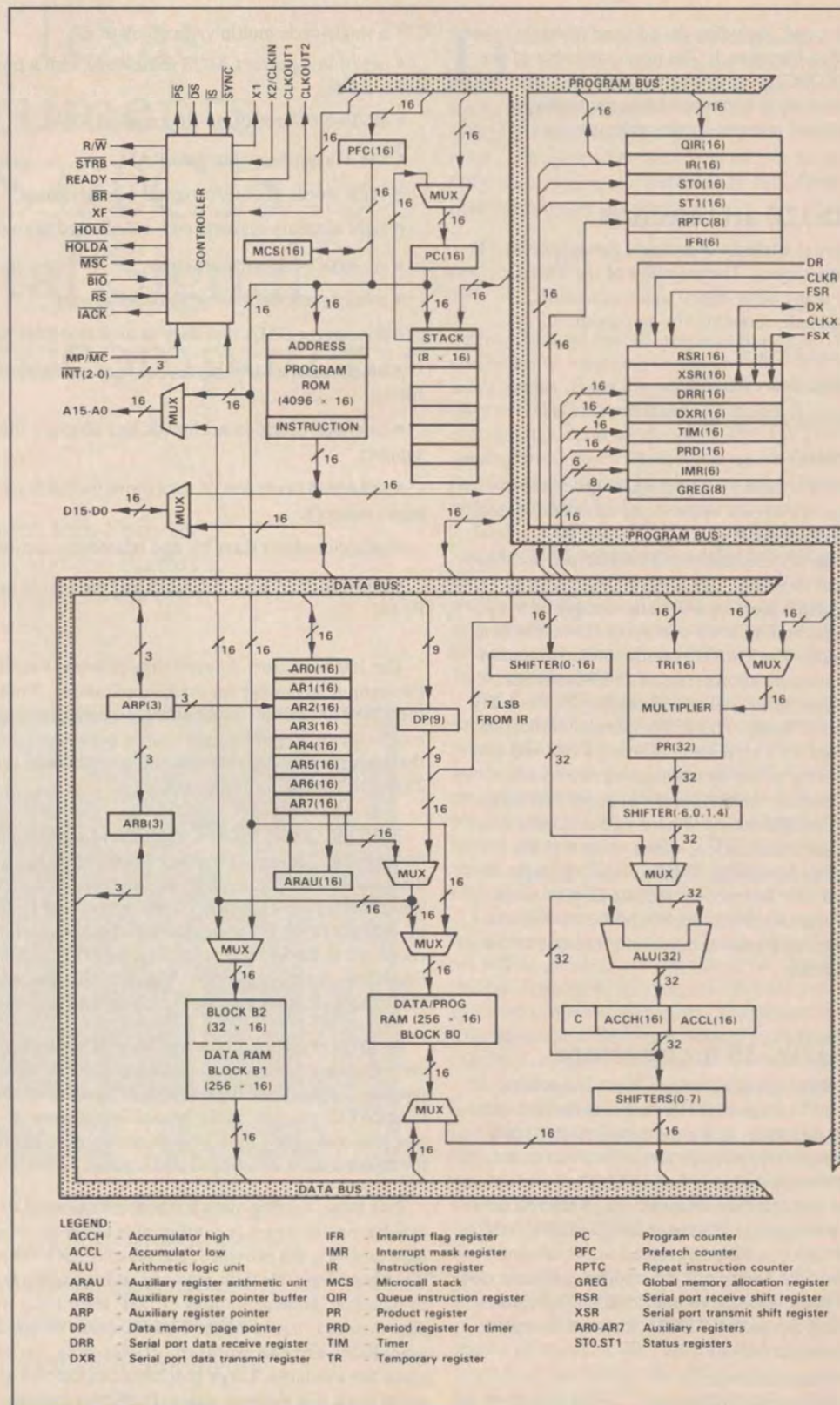


Figure 1.
TMS320C25
block diagram.

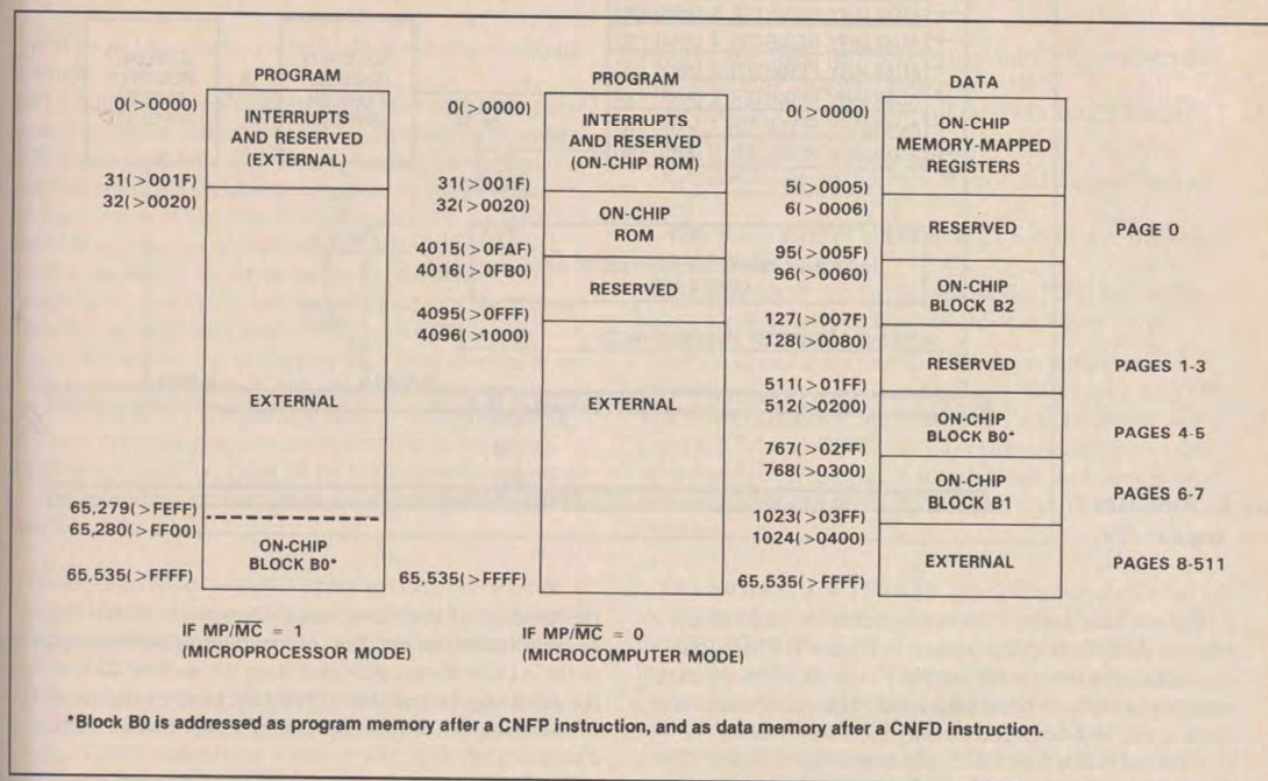


Figure 2. TMS320C25 memory maps.

downloaded from slow external memory to on-chip RAM for full-speed operation.

The TMS320C25 also incorporates a hardware timer and a block data transfer capability.

The diagram of the TMS320C25 in Figure 1 shows the principal blocks and data paths within the processor. It also shows all of the TMS320C25's interface pins.

The TMS320C25's architecture is built around the program and data buses. The program bus carries the instruction code and immediate operands from program memory. The data bus interconnects elements such as the central arithmetic logic unit (CALU) and the auxiliary register file to the data RAM. Together, the program and data buses can carry data from on-chip data RAM and internal or external program memory to the multiplier in a single cycle for multiply/accumulate operations.

A high degree of parallelism exists in the device—for example, while data are being operated on by the CALU, arithmetic operations can be implemented in the auxiliary register arithmetic unit (ARAU). Such parallelism results in a powerful set of arithmetic, logical, and bit-manipulation operations that can be performed in a single machine cycle.

Memory allocation. As mentioned above, the TMS320C25 provides 4K 16-bit words of on-chip program ROM and 544

16-bit words of on-chip data RAM. The RAM is divided into three blocks, B0, B1, and B2. Of the 544 words, 256 words (block B0) are configurable as either data memory or program memory; 288 words (blocks B1 and B2) are always data memory. A data memory size of 544 words allows the TMS320C25 to handle a data array of 512 words but still leaves 32 locations for intermediate storage.

The TMS320C25 maintains separate address spaces for program memory, data memory, and I/O. In addition to blocks B0, B1, and B2, the on-chip data memory map (see Figure 2) includes memory-mapped registers. Six peripheral registers, the serial-port registers (DRR and DXR), timer register (TIM), period register (PRD), interrupt mask register (IMR), and global memory allocation register (GREG), have been mapped into the data memory space so they can be easily modified.

The TMS320C25 has a register file containing eight auxiliary registers that can be used for indirect addressing of data memory or for temporary storage. These registers, AR0-AR7, can be either directly addressed by an instruction or indirectly addressed by a three-bit auxiliary register pointer (ARP). The auxiliary registers and the ARP can be loaded either from data memory or by an immediate operand defined in the instruction. The contents of the registers can also be stored in data memory.

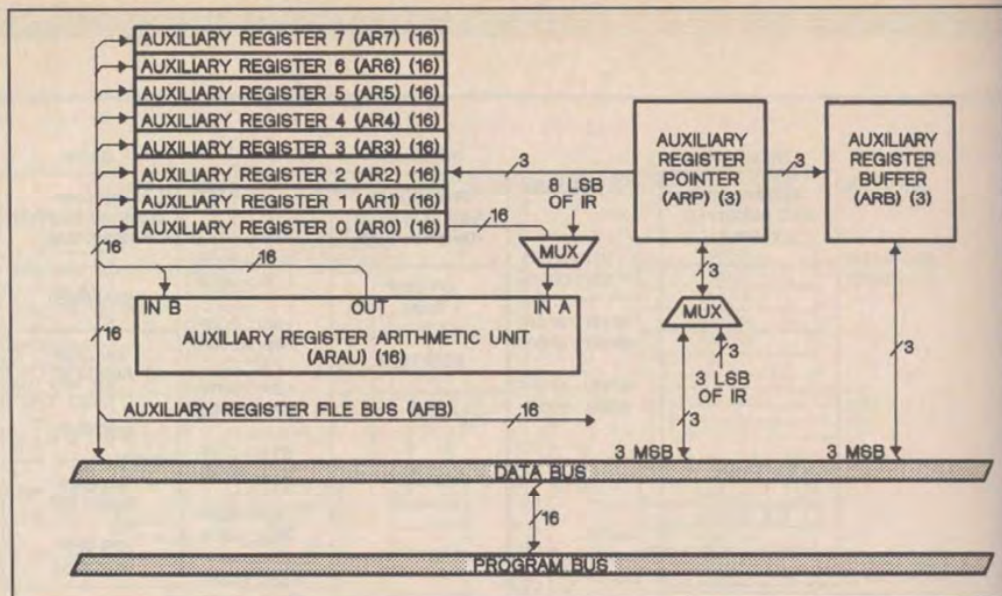


Figure 3. Auxiliary register file.

The auxiliary register file is connected to the auxiliary register arithmetic unit as shown in Figure 3. The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. The current auxiliary register can also be indexed either by $+1/-1$ or by the contents of AR0. As a result, the accessing of tables of information does not require the CALU for address manipulation, thereby freeing it for other operations.

Although the ARAU was designed to support address manipulation in parallel with other operations, it can also serve as an additional general-purpose arithmetic unit since the auxiliary register file can communicate directly with data memory. The ARAU implements 16-bit unsigned arithmetic, whereas the CALU implements 32-bit two's-complement arithmetic. The ARAU also provides branches dependent on the comparison of AR0 to the auxiliary register pointed to by the ARP.

Central arithmetic logic unit. The CALU contains a 16-bit scaling shifter, a 16×16 -bit parallel multiplier, a 32-bit ALU, and a 32-bit accumulator. The scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to the ALU. This shifter produces a left shift of 0 to 16 bits on the input data, as programmed in the instruction. The least significant bits of the output are filled with zeroes, and the most significant bits are either filled with zeroes or sign-extended, depending upon the state of the sign-extension mode bit of status register ST1. Additional shifters at the outputs of both the accumulator and the multiplier are suitable for numerical scaling, bit extraction, extended-precision arithmetic, and overflow prevention. Due to the pipelining in the TMS320C25, shifting is accomplished as part of an instruction and thus does not require additional cycles for execution.

The 32-bit ALU and accumulator perform a wide range of arithmetic and logical instructions. An overflow saturation mode permits the accumulator to be loaded with the most positive or negative number (the choice depending on

the direction of overflow), and it allows an overflow flag to be set whenever an overflow occurs. One of the two inputs to the ALU is always provided from the accumulator, and the other may be transferred from the product register (PR) of the multiplier or from the scaling shifter loaded from data memory.

The implementation of a typical ALU instruction requires these steps:

- data are fetched from the Rcarrrn the data bus;
- data are passed through the scaling shifter and through the ALU, where the arithmetic is performed; and
- the result is moved into the accumulator.

The 32-bit accumulator is split into two 16-bit segments for storage in data memory: ACCH (accumulator high) and ACCL (accumulator low). Shifters at the output of the accumulator provide a shift of 0 to 7 places to the left. This shift is performed while the data are being transferred to the data bus for storage. The contents of the accumulator remain unchanged. The accumulator also has an in-place one-bit shift to the left or right (SFL or SFR instruction) and a rotate through carry (ROL or ROR instruction) for shifting its contents.

A carry bit is provided to the accumulator, allowing more efficient extended-precision computation. ADDC (add with carry) and SUBB (subtract with borrow) are two instructions using the carry bit. Branch instructions that use the carry bit are also provided.

Hardware multiplier. The TMS320C25 uses a 16×16 -bit hardware multiplier that can compute a 32-bit product during every machine cycle. Two registers are associated with the multiplier: a 16-bit temporary register (TR) that holds one of the operands for the multiplier, and a 32-bit product register (PR) that holds the product.

The output of the product register can be left-shifted one or four bits. This is useful for implementing fractional arithmetic or justifying fractional products. The output of the PR can also be right-shifted six bits to enable the execu-

tion of up to 128 consecutive multiply/accumulates without overflow.

The multiplier performs both signed and unsigned operations. Two signed instructions, MAC (multiply/accumulate) and MACD (multiply/accumulate and data move), can process both operands simultaneously, thereby fully utilizing the computational bandwidth of the multiplier. For MAC and MACD, the two operands are transferred to the multiplier at each cycle via the program and data buses. This enables MAC and MACD to be performed in a single cycle when they are used with repeat (RPT or RPTK) instructions. The program bus can supply data from internal or external memory (RAM or ROM) and still maintain single-cycle operation. An unsigned multiply (MPYU) instruction facilitates extended-precision multiplication. It multiplies the unsigned contents of the TR by the unsigned contents of the addressed data memory location, and places the result in the PR.

Control operations. Control operations are provided on the TMS320C25 by an on-chip timer, a repeat counter, three external maskable user interrupts, and internal interrupts generated by serial-port operations or by the timer.

A memory-mapped 16-bit timer (TIM) register (a down counter) is continuously clocked by CLKOUT1. A timer interrupt (TINT) is generated whenever the timer decrements to zero. The timer is reloaded with the value contained in the period (PRD) register within the first cycle after it reaches zero so that interrupts may be programmed to occur at regular intervals of $(PRD + 1) \cdot CLKOUT1$ cycles. This feature is useful for control operations and for synchronous sampling of or writing to peripherals.

The repeat counter (RPTC) is loaded with either a data memory value (in the case of the RPT instruction) or an immediate value (in the case of the RPTK instruction). The repeat feature enables a single instruction to be executed up to 256 times. It can be used with instructions such as multiply/accumulates, block moves, I/O transfers, and table read/writes. Those instructions that are normally multicyle are pipelined when the repeat feature is used and effectively become single-cycle instructions. For example, the table read (TBLR) instruction ordinarily takes three or more cycles, but when it is repeated, it becomes a single-cycle instruction.

The three external maskable user interrupts, $\overline{INT}2$ to $\overline{INT}0$, enable external devices to interrupt the processor. Internal interrupts are generated by either the serial port, the timer, or the software interrupt instruction. Interrupts are prioritized, with reset having the highest priority and the serial-port transmit interrupt the lowest.

Serial port. An on-chip serial port provides direct communication with serial devices such as codecs and serial A/D and D/A converters. The serial port's interface requires a minimum of external hardware. The port has two memory-mapped registers—a data transmit register and a data receive register—which can be operated in either an eight-bit byte mode or a 16-bit word mode. The transmit

framing sync pulse can be generated internally or externally. The serial port's maximum speed is 5 MHz.

The primary enhancements of the TMS320C25's serial port are

- double buffering for both receive and transmit operations,
- the elimination of a minimum CLKR/CLKX frequency ($f_{min} = 0$ Hz), and
- the provision of a frame sync mode (FSM) bit, which allows continuous operation with no frame sync pulses.

The FSM is useful for communicating on pulse-code-modulated telephone system highways. As a result the TMS320C25 can communicate directly on PCM highways such as AT&T T-1 and CCITT G.711/712 by counting the transmitted and received bytes in software and performing the instructions needed to set (SFSM) and reset (RFSM) the FSM bit.

I/O interface. The TMS320C25's I/O space consists of 16 input and 16 output ports. These ports provide a full 16-bit parallel I/O interface via the processor's data bus. A single input (IN) or output (OUT) operation typically takes two cycles; however, when executed in the repeat mode, such an operation becomes single-cycle. The TMS320C25 supports a range of system interfacing requirements. As previously mentioned, three separate address spaces—program, data, and I/O—provide interfacing to memory and I/O, thereby maximizing system throughput. The TMS320C25 simplifies I/O design by treating I/O the same way it treats memory. It maps I/O devices into the I/O address space using its external address and data buses in the same way as it uses them for mapping memory devices into memory address space.

The local memory interface consists of a 16-bit parallel data bus (D15-D0), a 16-bit address bus (A15-A0), three pins for data memory, program memory, and I/O space select ($\overline{DS}$, $\overline{PS}$, and $\overline{IS}$, respectively), and various system control signals. The $\overline{R/W}$ signal controls the direction of a data transfer, and $\overline{STRB}$ provides a timing signal to control the transfer. When using on-chip program RAM, ROM, or high-speed external program memory, the TMS320C25 runs at full speed without wait states. By using the $\overline{READY}$ signal, it can generate wait states so it can communicate with slower off-chip memories.

The TMS320C25 supports direct memory access to external program and data memory. Another processor can take complete control of the TMS320C25's external memory by asserting $\overline{HOLD}$ low, causing the TMS320C25 to place its address, data, and control lines in the high-impedance state. Two modes are available on the device. In the first mode, execution is suspended during assertion of $\overline{HOLD}$. In the second mode—the “concurrent DMA mode”—the TMS320C25 continues to execute its program while operating from internal RAM or ROM, thereby greatly increasing throughput in data-intensive applications. Signaling between the external processor and the TMS320C25 can be performed through interrupts.

Table 1.
TMS320C25 instructions.

ACCUMULATOR MEMORY REFERENCE INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	OPERATION
ABS	Absolute value of accumulator	1	$ ACC \rightarrow ACC$
ADD	Add to accumulator with shift	1	$ACC + [(dma) \times 2^{shift}] \rightarrow ACC$
ADDC [†]	Add to accumulator with carry	1	$ACC + (dma) + (C) \rightarrow ACC$
ADDH	Add to high accumulator	1	$ACC + [(dma) \times 2^{16}] \rightarrow ACC$
ADDK [‡]	Add to accumulator short immediate	1	$ACC + 8\text{-bit constant} \rightarrow ACC$
ADDS	Add to low accumulator with sign extension suppressed	1	$ACC + (dma) \rightarrow ACC$
ADDT [†]	Add to accumulator with shift specified by T register	1	$ACC + [(dma) \times 2^{Treg}] \rightarrow ACC$
ADLK [†]	Add to accumulator long immediate with shift	2	$ACC + [16\text{-bit constant} \times 2^{shift}] \rightarrow ACC$
AND	AND with accumulator	1	$ACC(15:0).AND.(dma) \rightarrow ACC(15:0),$ $0 \rightarrow ACC(31:16)$
ANDK [†]	AND immediate with accumulator with shift	2	$ACC(30:0).AND.[16\text{-bit constant} \times 2^{shift}] \rightarrow$ $ACC(30:0), 0 \rightarrow ACC(30:0)$
CMPL [†]	Complement accumulator	1	$\overline{ACC} \rightarrow ACC$
LAC	Load accumulator with shift	1	$(dma) \times 2^{shift} \rightarrow ACC$
LACK	Load accumulator immediate short	1	8-bit constant $\rightarrow ACC$
LACT [†]	Load accumulator with shift specified by T register	1	$(dma) \times 2^{Treg} \rightarrow ACC$
LALK [†]	Load accumulator long immediate with shift	2	$(16\text{-bit constant}) \times 2^{16} \rightarrow ACC$
NEG [†]	Negate accumulator	1	$(ACC) \rightarrow ACC$
NORM [†]	Normalize contents of accumulator	1	
OR	OR with accumulator	1	$ACC(15:0).OR.(dma) \rightarrow ACC(15:0)$
ORK [†]	OR immediate with accumulator with shift	2	$ACC(30:0).OR.[16\text{-bit constant} \times 2^{shift}] \rightarrow$ $ACC(30:0)$
ROL [‡]	Rotate accumulator left	1	$ACC(30:0) \rightarrow ACC(31:1), (C) \rightarrow ACC(0),$ $ACC(31) \rightarrow C$
ROR [‡]	Rotate accumulator right	1	$ACC(31:1) \rightarrow ACC(30:0), (C) \rightarrow ACC(31),$ $ACC(0) \rightarrow C$
SACH	Store high accumulator with shift	1	$[(ACC) \times 2^{shift}] \rightarrow dma$
SACL	Store low accumulator with shift	1	$[(ACCL) \times 2^{shift}] \rightarrow dma$
SBLK [†]	Subtract from accumulator long immediate with shift	2	$ACC - [16\text{-bit constant} \times 2^{shift}] \rightarrow ACC$
SFL [†]	Shift accumulator left	1	$ACC(30:0) \rightarrow ACC(31:1), 0 \rightarrow ACC(0)$
SFR [†]	Shift accumulator right	1	$ACC(31:1) \rightarrow ACC(30:0), ACC(31) \rightarrow ACC(31)$
SUB	Subtract from accumulator with shift	1	$ACC - [(dma) \times 2^{shift}] \rightarrow ACC$
SUBB [‡]	Subtract from accumulator with borrow	1	$ACC - (dma) - (\overline{C}) \rightarrow ACC$
SUBC	Conditional subtract	1	
SUBH	Subtract from high accumulator	1	$ACC - [(dma) \times 2^{16}] \rightarrow ACC$
SUBK [‡]	Subtract from accumulator short immediate	1	$ACC - 8\text{-bit constant} \rightarrow ACC$
SUBS	Subtract from low accumulator with sign extension suppressed	1	$ACC - (dma) \rightarrow ACC$
SUBT [†]	Subtract from accumulator with shift specified by T register	1	$ACC - [(dma) \times 2^{Treg}] \rightarrow ACC$
XOR	Exclusive-OR with accumulator	1	$ACC(15:0).XOR.(dma) \rightarrow ACC(15:0)$
XORK [†]	Exclusive-OR immediate with accumulator with shift	2	$ACC(30:0).XOR.[16\text{-bit constant} \times 2^{shift}] \rightarrow$ $ACC(30:0)$
ZAC	Zero accumulator	1	$0 \rightarrow ACC$
ZALH	Zero low accumulator and load high accumulator	1	$(dma) \times 2^{16} \rightarrow ACC$
ZALR [‡]	Zero low accumulator and load high accumulator with rounding	1	$(dma) \times 2^{16} + >8000 \rightarrow ACC$
ZALS	Zero accumulator and load low accumulator with sign extension suppressed	1	$(dma) \rightarrow ACCL, 0 \rightarrow ACCH$

[†]These instructions are not included in the TMS32010 instruction set.

[‡]These instructions are not included in the TMS32020 instruction set.

AUXILIARY REGISTERS AND DATA PAGE POINTER INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. WORDS	OPERATION
ADRK [‡]	Add to auxiliary register short immediate	1	(ARn) + 8-bit constant → ARn
CMPR [†]	Compare auxiliary register with auxiliary register ARO	1	If ARn CM ARO, then 1 → TC; else 0 → TC
LAR	Load auxiliary register	1	(dma) → (ARn)
LARK	Load auxiliary register short immediate	1	8-bit constant → ARn
LARP	Load auxiliary register pointer	1	3-bit constant → ARP, (ARP) → ARB
LDP	Load data memory page pointer	1	(dma) → DP
LDPK	Load data memory page pointer immediate	1	9-bit constant → DP
LRLK [†]	Load auxiliary register long immediate	2	16-bit constant → ARn
MAR	Modify auxiliary register	1	
SAR	Store auxiliary register	1	(ARn) → dma
SBRK [‡]	Subtract from auxiliary register short immediate	1	(ARn) - 8-bit constant → ARn

T REGISTER, P REGISTER, AND MULTIPLY INSTRUCTIONS

MNEMONIC	DESCRIPTION	NO. WORDS	OPERATION
APAC	Add P register to accumulator	1	(ACC) + (shift Preg) → ACC
LPH [†]	Load high P register	1	(dma) → Preg (31-16)
LT	Load T register	1	(dma) → Treg
LTA	Load T register and accumulate previous product	1	(dma) → Treg, (ACC) + (shifted Preg) → ACC
LTD	Load T register, accumulate previous product, and move data	1	(dma) → Treg, (dma) → dma + 1, (ACC) + (shifted Preg) → ACC
LTP [†]	Load T register and store P register in accumulator	1	(dma) → Treg, (shifted Preg) → ACC
LTS [†]	Load T register and subtract previous product	1	(dma) → Treg, (ACC) - (shifted Preg) → ACC
MAC [†]	Multiply and accumulate	2	(ACC) + (shifted Preg) → ACC, (pma) × (dma) → Preg
MACD [†]	Multiply and accumulate with data move	2	(ACC) + (shifted Preg) → ACC, (pma) × (dma) → Preg, (dma) → dma + 1
MPY	Multiply (with T register, store product in P register)	1	(Treg) × (dma) → Preg
MPYA [‡]	Multiply and accumulate previous product	1	(ACC) + (shifted Preg) → ACC, (Treg) × (dma) → Preg
MPYK	Multiply immediate	1	(Treg) × 13-bit constant → Preg
MPYS [‡]	Multiply and subtract previous product	1	(ACC) - (shifted Preg) → ACC, (Treg) × (dma) → Preg
MPYU [‡]	Multiply unsigned	1	Usn (Treg) × Usn (dma) → Preg
PAC	Load accumulator with P register	1	(shifted Preg) → ACC
SPAC	Subtract P register from accumulator	1	(ACC) - (shifted Preg) → ACC
SPH [‡]	Store high P register	1	(shifted Preg (31-16)) → dma
SPL [‡]	Store low P register	1	(shifted Preg (15-0)) → dma
SPM [†]	Set P register output shift mode	1	2-bit constant → PM
SQRA [†]	Square and accumulate	1	(ACC) + (shifted Preg) → ACC, (dma) × (dma) → Preg
SQRS [†]	Square and subtract previous product	1	(ACC) - (shifted Preg) → ACC, (dma) × (dma) → Preg

SYMBOL	MEANING
ACC	Accumulator
ARB	Auxiliary register pointer buffer
ARn	Auxiliary Register n (AR0 through AR7 are predefined assembler symbols equal to 0 through 7, respectively)
ARP	Auxiliary register pointer
BIO	Branch control input
C	Carry bit
CM	2-bit field specifying compare mode
CNF	On-chip RAM configuration control bit
dma	Data memory address
DP	Data page pointer
FO	Format status bit
FSM	Frame synchronization mode bit
HM	Hold mode bit
INTM	Interrupt mode flag bit
>nn	Indicates nn is a hexadecimal number. (All others are assumed to be decimal values.)
OV	Overflow flag bit
OVN	Overflow mode bit
P	Product register

SYMBOL	MEANING
PA	Port address. (PA0 through PA15 are predefined assembler symbols equal to 0 through 15, respectively.)
PC	Program counter
PM	2-bit field specifying P register output shift code
pma	Program memory address
Preg	Product register
RPTC	Repeat counter
STn	Status Register n (ST0 or ST1)
SXM	Sign extension mode bit
T	Temporary register
TC	Test control bit
TOS	Top of stack
Treg	Temporary register
TXM	Transmit mode bit
Usn	Unsigned value
XF	XF pin status bit
→	Is assigned to
	An absolute value
[]	Optional items
()	Contents of

Table 1 cont'd

BRANCH/CALL INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	OPERATION
B	Branch unconditionally	2	$pma \rightarrow PC$
BACC [†]	Branch to address specified by accumulator	1	$(ACC(15-0)) \rightarrow PC$
BANZ	Branch on auxiliary register not zero	2	If $(AR(ARP)) \neq 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BBNZ [†]	Branch if TC bit $\neq 0$	2	If $(TC) = 1$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BBZ [†]	Branch if TC bit = 0	2	If $(TC) = 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BC [‡]	Branch on carry	2	If $(C) = 1$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BGEZ	Branch if accumulator ≥ 0	2	If $(ACC) \geq 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BGZ	Branch if accumulator > 0	2	If $(ACC) > 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BIOZ	Branch on I/O status = 0	2	If $(BIO) = 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BLEZ	Branch if accumulator ≤ 0	2	If $(ACC) \leq 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BLZ	Branch if accumulator < 0	2	If $(ACC) < 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BNC [‡]	Branch on no carry	2	If $(C) = 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BNV [†]	Branch if no overflow	2	If $(OV) \neq 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BNZ	Branch if accumulator $\neq 0$	2	If $(ACC) \neq 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BV	Branch on overflow	2	If $(OV) = 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
BZ	Branch if accumulator = 0	2	If $(ACC) = 0$, then $pma \rightarrow PC$; else $(PC) + 2 \rightarrow PC$
CALA	Call subroutine indirect	1	$(ACC(15-0)) \rightarrow PC$, $(PC) + 1 \rightarrow TOS$
CALL	Call subroutine	2	$(PC) + 2 \rightarrow TOS$, $pma \rightarrow PC$
RET	Return from subroutine	1	$(TOS) \rightarrow PC$
I/O AND DATA MEMORY OPERATIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	OPERATION
BLKD [†]	Block move from data memory to data memory	2	$(dma1, \text{addressed by } PC) \rightarrow dma2$
BLKP [†]	Block move from program memory to data memory	2	$(pma, \text{addressed by } PC) \rightarrow dma$
DMOV	Data move in data memory	1	$(dma) \rightarrow dma + 1$
FORT [†]	Format serial port registers	1	1-bit constant $\rightarrow FO$
IN	Input data from port	1	$(data \text{ bus, addressed by } PA) \rightarrow dma$
OUT	Output data to port	1	$(dma) \rightarrow data \text{ bus, addressed by } PA$
RFSM [‡]	Reset serial port frame synchronization mode	1	0 $\rightarrow FSM$
RTXM [†]	Reset serial port transmit mode	1	0 $\rightarrow TXM$
RXF [†]	Reset external flag	1	0 $\rightarrow XF$
SFSM [‡]	Set serial port frame synchronization mode	1	1 $\rightarrow FSM$
STXM [†]	Set serial port transmit mode	1	1 $\rightarrow TXM$
SXF [†]	Set external flag	1	1 $\rightarrow XF$
TBLR	Table read	1	$(pma, \text{addressed by } ACC(15-0)) \rightarrow dma$
TBLW	Table write	1	$(dma) \rightarrow pma, \text{addressed by } ACC(15-0)$
CONTROL INSTRUCTIONS			
MNEMONIC	DESCRIPTION	NO. WORDS	OPERATIONS
BIT [†]	Test bit	1	$(dma \text{ bit at } (15\text{-bit code})) \rightarrow TC$
BITT [†]	Test bit specified by T register	1	$(dma \text{ bit at } (15\text{-Treg})) \rightarrow TC$
CNFD [†]	Configure block as data memory	1	0 $\rightarrow CNF$
CNFP [†]	Configure block as program memory	1	1 $\rightarrow CNF$
DINT	Disable interrupt	1	1 $\rightarrow INTM$
EINT	Enable interrupt	1	0 $\rightarrow INTM$
IDLE [†]	Idle until interrupt	1	$(PC) + 1 \rightarrow PC$, powerdown
LST	Load status register ST0	1	$(dma) \rightarrow ST0$
LST1 [†]	Load status register ST1	1	$(dma) \rightarrow ST1$

[†]These instructions are not included in the TMS32010 instruction set.

[‡]These instructions are not included in the TMS32020 instruction set.

CONTROL INSTRUCTIONS cont'd

NOP	No operation	1	(PC) + 1 → PC
POP	Pop top of stack to low accumulator	1	(TOS) → ACC
POPD [†]	Pop top of stack to data memory	1	(TOS) → dma
PSHD [†]	Push data memory value onto stack	1	(dma) → TOS
PUSH	Push low accumulator onto stack	1	(ACCL) → TOS
RC [‡]	Reset carry bit	1	0 → C
RHM [‡]	Reset hold mode	1	0 → HM
ROVM	Reset overflow mode	1	0 → OVM
RPT [†]	Repeat instruction as specified by data memory value	1	(dma) → RPTC
RPTK [†]	Repeat instruction as specified by immediate value	1	8-bit constant → RPTC
RSXM [†]	Reset sign-extension mode	1	0 → SXM
RTC [‡]	Reset test/control flag	1	0 → TC
SC [‡]	Set carry bit	1	1 → C
SHM [‡]	Set hold mode	1	1 → HM
SOVM	Set overflow mode	1	1 → OVM
SST	Store status register ST0	1	ST0 → dma
SST1 [†]	Store status register ST1	1	ST1 → dma
SSXM [†]	Set sign-extension mode	1	1 → SXM
STC [‡]	Set test/control flag	1	1 → TC
TRAP [†]	Software interrupt	1	(PC) + 1 → TOS, 30 → PC

The TMS320C25's conditions and modes are stored in two status registers, ST0 and ST1. Instructions are provided to allow these registers to be stored in or loaded from data memory. This capability allows the current status of the device to be saved during interrupts and subroutine calls.

TMS320C25 software

Earlier, we characterized digital signal processing as the real-time processing of mathematically intensive algorithms. This characterization equates to a requirement for high-speed, multiply/accumulate capability in a processor. The performance of a signal processor is therefore measured in terms appropriate to this requirement—that is, it is measured in terms of the speed of execution of individual instructions, the power of the instruction set, and the I/O capabilities. The speed is given as the basic instruction cycle time and the number of cycles required to complete any instruction.

As we noted earlier, pipelining of instruction fetching, decoding, and execution provides an instruction cycle time of only 100 ns. The overwhelming majority of the TMS320C25's instructions (97 out of 133) are executed in a single instruction cycle. Of the 36 instructions requiring additional cycles for execution, 21 involve branches, calls, and returns that result in a reload of the program counter and a break in the execution pipeline. Another seven of

the instructions are two-word, long immediate instructions. The remaining eight—IN, OUT, BLKD, BLKP, TBLR, TBLW, MAC, and MACD—support I/O and transfers of data between memory spaces, or provide for additional parallel operation in the processor. Furthermore, these eight instructions become single-cycle when used in conjunction with the repeat counter. The instruction set of the TMS320C25 exploits the parallelism of the processor, allowing complex or numerically intensive computations to be implemented in relatively few instructions. Table 1 lists the TMS320C25's instructions.

Addressing modes. Most TMS320C25 instructions are coded in a single 16-bit word—the reason most can be executed in a single cycle. The 16-bit word comprises an eight-bit opcode and an eight-bit address. Three memory addressing modes are available: direct, indirect, and immediate (Table 2). Both direct and indirect addressing are used to access data memory. Immediate addressing uses the contents of the memory addressed by the program counter. Figure 4 illustrates operand addressing in the direct, indirect, and immediate modes.

In direct addressing, seven bits of the instruction word are concatenated with the nine-bit data memory page pointer (DP) to form the 16-bit data memory address. The DP register points to one of 512 possible data memory pages, each 128 word in length, to obtain a 64K total data memory space. The seven-bit address in the instruction

Table 2.
Addressing modes.

ADDRESSING MODE	OPERATION
OP A	Direct addressing
OP * (.NARP)	Indirect; no change to AR
OP *+ (.NARP)	Indirect; current AR is incremented.
OP *- (.NARP)	Indirect; current AR is decremented.
OP *O+ (.NARP)	Indirect; AR0 is added to current AR.
OP *O- (.NARP)	Indirect; AR0 is subtracted from current AR.
OP *BR0+ (.NARP)	Indirect; AR0 is added to current AR (with reverse carry propagation)
OP *BR0- (.NARP)	Indirect; AR0 is subtracted from current AR (with reverse carry propagation)

NOTE: The optional NARP field specifies a new value of the ARP.

points to the specific location within the data memory page.

Indirect addressing is provided by the eight auxiliary registers AR0-AR7. These registers can be used to indirectly address data memory, as loop counters, or for temporary data storage. Indirect auxiliary register addressing (Figure 5) allows placement of the data memory address of an instruction operand into one of the eight auxiliary registers. These registers are pointed to by a three-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7 designating AR0 through AR7, respectively. The auxiliary registers and the ARP may be loaded either from data memory or by an immediate operand defined in the instruction. Furthermore, the contents of the auxiliary registers may be stored in data memory.

There are seven types of indirect addressing (see Table 2 again):

- indexing with increment,
- indexing with decrement,
- indexing by adding the contents of AR0,
- indexing by subtracting the contents of AR0,
- indexing by adding the contents of AR0 with the carry propagation reversed (for bit-reversing an FFT),
- indexing by subtracting the contents of AR0 with the carry propagation reversed (also for bit-reversing an FFT), and
- no indexing.

All indexing operations are performed on the current auxiliary register in the same cycle as the original instruction, with loading of a new ARP value available as an option. The operations performed in the ARAU can even be performed during branch instruction execution, allowing efficient control with conditional looping.

Bit-reversed indexed addressing modes allow efficient I/O to be performed for the resequencing of data points in a radix-2 FFT program. The direction of carry propagation in the ARAU is reversed when this mode is selected, and AR0 is added to or subtracted from the current auxiliary register.

In immediate addressing, the instruction word contains the value of the immediate operand. Both single-word (8-bit and 13-bit constant) short immediate instructions and two-word (16-bit constant) long immediate instructions are included in the instruction set. In the case of long immediate

instructions, the word following the instruction opcode is used as the immediate operand. MPYK is an example of an immediate instruction; it multiplies the contents of the T register by a signed 13-bit constant. Seventeen immediate operand instructions are included in the instruction set (see Table 1 again).

Instruction set parallelism—an example. The MACD (multiply/accumulate and data move) instruction serves as an informative example of the parallelism designed into the TMS320C25 instruction set as well as into the TMS320C25 architecture. As shown in Equation 1, the requirement for parallelism exists in common DSP operations such as convolution and filtering.^{6,7}

Parallelism in the execution of instructions enables a complete multiply/accumulate/data move operation to be completed in a single 100-ns instruction cycle. The execution of the MACD involves the following steps:

- 1) The contents of the 32-bit P register are shifted (scaled) by an output shifter.
- 2) The 32-bit ALU accumulates the shifted result of the 32-bit P register with the current contents of the 32-bit accumulator.
- 3) The 16-bit contents of a data memory location (usually addressed indirectly via one of the auxiliary registers) are loaded into the T register.
- 4) The 16-bit contents of a program memory location (addressed via the prefetch counter PFC) are introduced to the multiplier and a 16×16 -bit multiply is executed, resulting in a new 32-bit product. The product is placed in the P register to be accumulated during the next cycle.
- 5) The 16-bit contents of the data memory location are copied to the next higher data memory address.
- 6) The carry and overflow status bits are set, as appropriate, in the status registers.
- 7) The 16-bit contents of the auxiliary register pointed to by the ARP are modified (typically decremented) in preparation for the use of the data memory address on the next cycle.
- 8) The 16-bit contents of the PFC are incremented in preparation for the use of the program memory address on the next cycle.
- 9) The repeat counter is decremented.

As can be seen from the above, one of the data values is taken from data memory while the other is taken from program memory. A single-cycle execution and data move is accomplished when the data memory being addressed is the on-chip data memory. The program memory location can be either on or off chip and, if on chip, can come from either ROM or the reconfigurable memory block B0.

Parallel operation of certain subsets of TMS320C25 functions is also available. These subsets include loading the T register in combination with addition (LTA), subtraction (LTS), or a move of the P register's contents to the accumulator (LTP). The accumulation can be supplemented by the data move function (LTD). Another combination (MPYA/MPYS) provides the accumulation of the previous

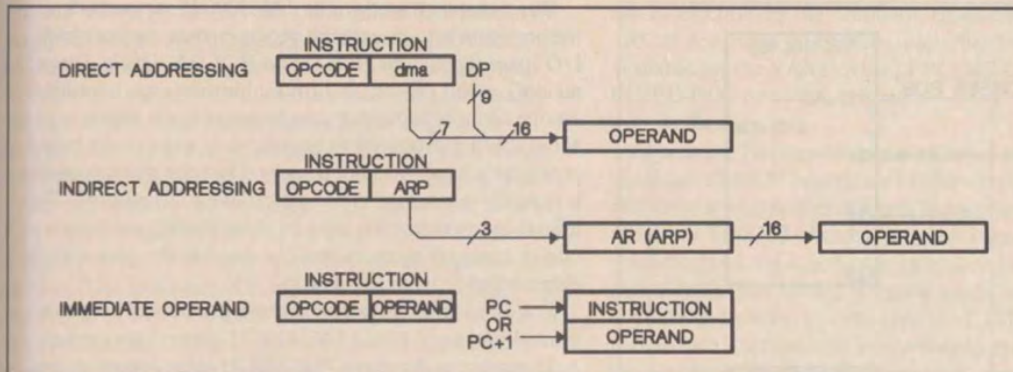


Figure 4. Methods of addressing the instruction operand.

product along with the execution of the multiplier to generate a new product. This combination is particularly useful in adaptive filtering techniques such as those embodied in the least-mean-square (LMS) algorithm.^{4,15} The implementation of an adaptive filter by means of these instructions will be described in detail in the section on applications.

Block moves. The TMS320C25 provides six instructions for data and program block moves and transfers of data via the I/O ports. When these instructions are pipelined by means of the repeat instruction, significantly higher throughput is achieved—the pipelining results in a transfer rate of 160 million bits per second.

The BLKD instruction moves a block within data memory, and the BLKP instruction moves a block from program memory to data memory. Block transfers between program and data memory spaces can also be implemented with the TBLR and TBLW (table read and table write) instructions. The advantages of TBLR and TBLW are that they allow the source address as well as the destination address to be determined during programming and that they permit the data to be transferred from data memory to program memory. The IN and OUT instructions permit data to be transferred between the I/O and data memory spaces. While the source address is determined by the prefetch counter, which is incremented on every cycle, the destination address is determined by an auxiliary register whose contents can be modified in any of the previously specified ways. This permits sequential and contiguous data placement (*+, *−), sequential but noncontiguous data placement (*0+, *0−), or scrambled data placement (*BR0+, *BR0−). The value of these address modifications during block data transfers becomes particularly apparent in the use of indexing with reverse-carry propagation to set up the data block in an FFT. The result is not only a savings in execution time but a savings in program memory space as well.

Floating-point support. The TMS320C25 supports floating-point operations for applications requiring a large dynamic range. The NORM (normalization) instruction normalizes fixed-point numbers contained in the accumulator

or by performing left shifts. The LACT (load accumulator with shift specified by the T register) instruction denormalizes a floating-point number by arithmetically left-shifting the mantissa through the input scaling shifter. The shift count, in this case, is the value of the exponent specified by the four low-order bits of the T register. ADDT and SUBT instructions (add to/subtract from accumulator with shift specified by the T register) have been provided to allow additional arithmetic operations.

TMS320C25 hardware

The most important task for a hardware designer is interfacing the DSP device to the rest of the system as inexpensively as possible. Here, we will discuss the TMS320C25's interfacing capabilities.

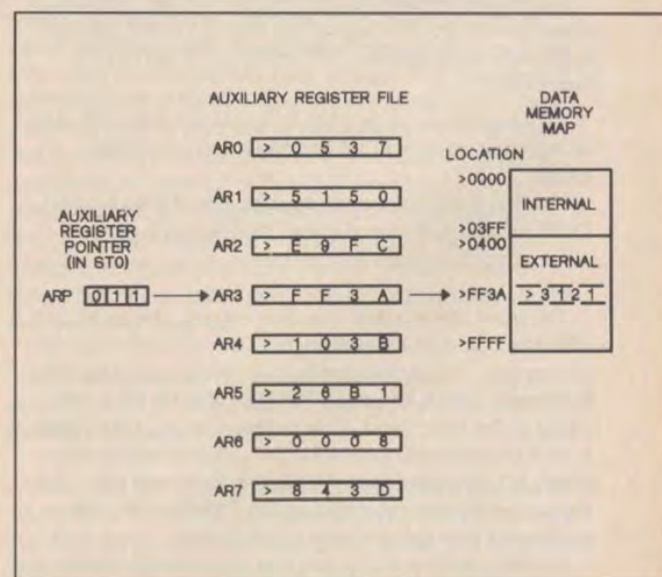


Figure 5. Example of indirect auxiliary register addressing.

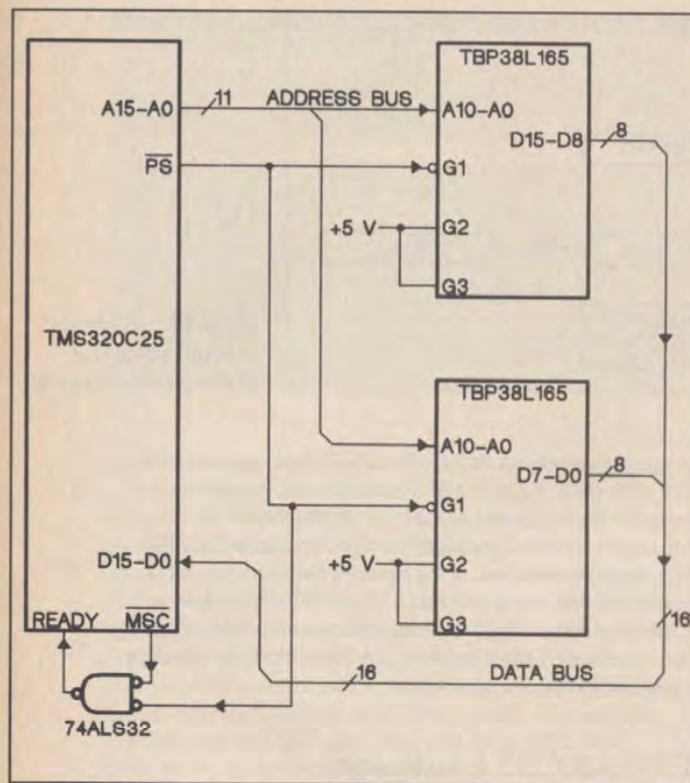


Figure 6. Minimal configuration for external program memory.

System configurations. The flexibility of the TMS320C25 allows systems configurations that satisfy a broad range of application requirements. The TMS320C25 can be configured as

- a stand-alone system (that is, as a single processor using 4K words of on-chip ROM and 544 words of on-chip RAM),
- part of a parallel multiprocessing system (two or more TMS320C25s) with shared global data memory, or
- a coprocessor for a host processor.

The stand-alone system interface consists of a 16-bit parallel data bus, a 16-bit address bus, three pins for memory space select, and various system control signals. In Figure 6, an external data RAM and a PROM/EPROM have been added to the basic stand-alone system. The READY signal is used for wait-state generation for communicating with slower off-chip memories. All the memories and I/O devices are directly controlled by the TMS320C25, thus minimizing external hardware requirements.

Parallel multiprocessing and host/coprocessor systems take advantage of the TMS320C25's direct memory access and global memory configuration capabilities.

Direct memory access. The TMS320C25 supports direct memory access to its external program/data memory and I/O space through its $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. Direct memory access can be used for multiprocessing: Execution on one or more processors can be temporarily halted to allow another processor to read from or write to the halted processor's local off-chip memory. Here the multiprocessing is typically performed in a master/slave configuration. The master can initialize the slave by downloading a program into its program memory space or provide the slave with the data needed to complete a task.

In a direct memory access scheme, the master may be a general-purpose CPU, a TMS320C25, or perhaps even an A/D converter. A master TMS320C25 takes complete control of the slave's external memory by asserting $\overline{\text{HOLD}}$ low through its external flag (XF). This causes the slave to place its address, data, and control lines in a high-impedance state. By asserting $\overline{\text{RS}}$ in conjunction with $\overline{\text{HOLD}}$, the master processor can load the slave's local program memory with the necessary initialization code on reset or power-up. The two processors can be synchronized through use of the $\overline{\text{SYNC}}$ pin to make the transfer over the memory bus faster and more efficient.

After control of the slave's buses is given to the master processor, the slave alerts the master by asserting $\overline{\text{HOLDA}}$. This signal can be tied to the master's $\overline{\text{BIO}}$ pin. The slave's XF pin can be used to indicate to the master when the slave has finished performing its task and needs to be reprogrammed or given additional data to continue processing. In a multiple-slave configuration, the priority of each slave's task can be determined by tying the slave's XF signals to the appropriate $\overline{\text{INT}}$ pin on the master.

A PC environment provides an example of a direct memory access scheme in which the system bus is used for data transfer. In this configuration, either the master CPU or a disk controller may place data on the system bus for downloading into the local memory of the TMS320C25. Here the TMS320C25 acts like a peripheral processor with multifunction capability. In a speech application, for example, the master can load the TMS320C25's program memory with algorithms to perform tasks such as speech analysis, synthesis, or recognition, and its data memory with the required speech templates. In a graphics application, the TMS320C25 can serve as a dedicated graphics engine. Programs can be stored in ROM or downloaded via the system bus into program RAM. Again, data can come from PC disk storage or be provided directly by the master CPU. In this configuration, decode and arbitration logic is used to control the direct memory access. When the address on the system bus resides in the local memory of the peripheral TMS320C25, this logic asserts the $\overline{\text{HOLD}}$ signal while sending the master a not-ready indication to allow wait states. After the TMS320C25 acknowledges the direct memory access by asserting $\overline{\text{HOLDA}}$, $\overline{\text{READY}}$ is asserted and the information is transferred.

Global memory. In some digital signal processing tasks, the algorithm being implemented can be divided into sections and a processor dedicated to each. In this case, the

first and second processors can share global data memory, as can the second and third, the third and fourth, and so on. Arbitration logic may be required to determine which section of the algorithm will execute and which processor will have access to the global memory. The dedication of each processor to a distinct section of the algorithm makes pipelined execution—and thus higher throughput—possible.

External memory can be divided into global and local sections. Special registers and pins on the TMS320C25 allow multiple processors to share up to 32K words of global data memory. This facilitates efficient "shared data" multiprocessing, in which data are transferred between two or more processors. Unlike a direct memory access scheme, reading or writing global memory does not require one of the processors to be halted.

TMS320C25 development tools and support

A digital signal processor is essentially an application-specific microprocessor or microcomputer. Like any microprocessor, it needs good development tools and technical support—no matter how impressive its performance or how easy its interfacing to other devices, it cannot be easily designed into systems without such tools and support. In developing an application, a designer encounters problems

can be executed by the simulator, emulator, or the TMS320C25 processor. The macro assembler/linker is currently available for the VAX/VMS, TI PC/MS-DOS, and IBM PC/PC-DOS operating systems.

Simulator. The simulator is a software program that simulates TMS320 operations to allow program verification. Its debug mode enables the user to monitor the state of the simulated TMS320 while his program is executing. The simulator uses the object code produced by the macro assembler/linker. During program execution, the internal registers and memory of the simulated TMS320 are modified as each instruction is interpreted by the host computer. Once program execution is suspended, the internal registers and the program and data memories can be inspected and modified. The simulator is currently available for the VAX/VMS, TI PC/MS-DOS, and IBM PC/PC-DOS operating systems.

Hardware tools. Tools are provided for in-circuit emulation and hardware program debugging such as breakpointing and tracing so that DSP algorithms can be developed and tested in a real-product environment.

Evaluation module. The evaluation module, or EVM, is a stand-alone board that contains all the hardware tools

No matter how impressive its performance or how easy its interfacing to other devices, a digital signal processor cannot be designed into systems without good development tools and vendor support.

and needs to ask questions. Often the tools and vendor support given him are the difference between the success and failure of his project.

The TMS320C25 is supported by many development tools.¹⁶ These tools range from inexpensive modules for application evaluation and benchmarking to an assembler/linker and software simulator to a full-capability hardware emulator.

Software tools. An assembler/linker and software simulator that enable users to develop and debug TMS320 DSP algorithms are available for the TI PC, IBM PC, and VAX.

Assembler/linker. The macro assembler translates assembly language source code into executable object code. It allows the programmer to work with mnemonics rather than hexadecimal machine instructions and to reference memory locations with symbolic addresses. It supports macro calls and definitions along with conditional assembly. The linker permits a program to be designed and implemented in separate modules that are later linked to form the complete program. The linker resolves external definitions and references for relocatable code, creating an object file that

needed to evaluate the TMS320C25 and that provides in-circuit emulation of it. The EVM's firmware package contains a debug monitor, an editor, an assembler, a reverse assembler, and software communication to two EIA ports. These ports allow the EVM to be connected to a terminal and to either a host computer or a line printer. The EVM accepts either source or object code downloaded from the host computer. Its resident assembler converts incoming source text into executable code in just one pass by automatically resolving labels after the first assembly pass is completed. When a session is finished, code is saved via the host computer interface.

Software development system. The SWDS is a plug-in card for the TI PC and IBM PC that provides the same functionality as the EVM.

Emulator. The XDS (Extended Development System) is an emulator providing full-speed in-circuit emulation with real-time hardware breakpointing and tracing and program execution capability from target memory. The XDS allows integration of hardware and software modules in the debug mode. By setting breakpoints based on internal conditions

or external events, the XDS user can suspend execution of the program and give control to the debug mode. In the debug mode, he can inspect and modify all registers and memory locations. Single-step execution is available. Full-trace capabilities at full speed and a reverse assembler that translates machine code back into assembly instructions also increase debugging productivity. The XDS system is designed to interface with either a terminal or a host computer. Object code generated by the assembler/linker can be downloaded to the XDS and then controlled through a terminal.

Analog interface board. The AIB is an analog-to-digital (A/D) and digital-to-analog (D/A) conversion board that can be used in conjunction with the EVM or XDS. It can also be used in an educational environment to help familiarize the user with real-world digital signal processing techniques. The AIB includes A/D and D/A converters with 12-bit resolution as well as antialiasing and smoothing filters that have a cut-off frequency programmable from 4.7 kHz to 20 kHz.

In addition to the above design tools, development support includes

- the Digital Filter Design Package, which runs on both TI and IBM PCs and which allows the user to design digital filters (low-pass, high-pass, band-pass, and band-stop types) using a menu-driven approach,
- TI Regional Technology Centers staffed with qualified engineers who provide technical support and design services,
- access to third parties with DSP expertise in various application areas,
- a series of DSP books covering DSP theory, algorithms, and applications and TMS320 implementations,^{4,5,7}
- documentation such as user's guides,¹⁰⁻¹² data sheets, a development support reference guide,¹⁶ and comprehensive application reports,⁴ and
- a technical support hotline and a bulletin board service.

TMS320C25 applications

The TMS320C25 is designed for real-time DSP and other computation-intensive tasks in telecommunications, graphics, image processing, high-speed control, speech processing, instrumentation, and numeric processing. In these applications, the TMS320C25 provides an excellent means for executing signal processing algorithms such as fast Fourier transforms (FFTs), digital filters, frequency synthesizers, correlators, and convolution routines. It can also execute general-purpose functions since it includes bit-manipulation instructions, block data move capabilities, large program and data memory address spaces, and flexible memory mapping.

Since digital filters are used in so many DSP applications, let us examine them as a prelude to our discussion of TMS320C25 applications.

Digital filtering. Filters are often implemented in digital signal processing systems. Such filters fall into two categories: finite impulse response (FIR) filters and infinite impulse response (IIR) filters.^{4,6} For both types of filter, the coefficients of the filter (weighting factors) may be fixed or adapted during the course of the signal processing. The TMS320C25 reduces the execution time of all filters by virtue of its 100-ns instruction cycle time and optimized instructions for filter operations.

As we stated earlier, the FIR filter is simply the sum of products in a sampled data system (see Equation 1 again). A simple implementation of the FIR filter uses the MACD instruction (multiply/accumulate and data move) for each filter tap and the RPT/RPTK instruction to repeat the MACD for each tap. Thus, a 256-tap FIR filter can be implemented as

```
RPTK 255
MACD *- ,COEFFP
```

Here, the coefficients can be stored anywhere in program memory (in the reconfigurable on-chip RAM, in the on-chip ROM, or in external memories). When the coefficients are stored in on-chip ROM or externally, the entire on-chip data RAM can be used to store the sample sequence. This allows filters of up to 512 taps to be implemented. Execution of the filter will be at full speed, or 100 ns per tap, as long as the memory (either on-chip RAM or high-speed external RAM) supports full-speed execution.

Up to this point, we have assumed that the filter coefficients are fixed from sample to sample. If the coefficients are adapted or updated with time, as they are in adaptive filters for echo cancellation,^{4,15} the DSP algorithm requires a greater computational capacity from the processor. To adapt or update the coefficients, usually with each sample, the TMS320C25 uses three instructions—multiply and add/subtract previous product to/from accumulator (MPYA/MPYS), zero-out low-order accumulator bits and load high-order accumulator bits with data (ZALR), and store high-order bits of accumulator to data memory (SACH). The method it uses to adapt the coefficients is the least-mean-square, or LMS, algorithm, which can be expressed as

$$b_k(i+1) = b_k(i) + 2B [e(i) \cdot x(i-k)], \quad (2)$$

where $b_k(i+1)$ is the weighting coefficient for the next sample period, $b_k(i)$ is the weighting coefficient for the present sample period, B is the gain factor or adaptation step size, $e(i)$ is the error function, and $x(i-k)$ is the input of the filter.

In an adaptive filter, the coefficients $b_k(i)$ must be updated to minimize the error function $e(i)$, which is the difference between the output of the filter and a reference signal. Quantization errors arising during coefficient updating can strongly affect the performance of the filter, but these errors can be minimized if the updated values are obtained by rounding rather than truncating. For each coefficient in the filter at a given point in time, the factor

$2*B*e(i)$ is a constant. This factor can be computed once and stored in the T register for each of the updates. This reduces the computational requirement to one multiply/accumulate plus rounding. Without the new instructions, the adaptation of each coefficient would take five instructions corresponding to five clock cycles, as the following instruction sequence shows:

```
LRLK AR2,COEFFD ; LOAD ADDRESS OF COEFFICIENTS.
LRLK AR3,LASTAP ; LOAD ADDRESS OF DATA SAMPLES.
LARP AR2
LT ERRF          ; errf = 2*B*e(i)
.
.
ZALH *,AR3      ; ACC = bk(i)*2**16
ADD ONE,15      ; ACC = bk(i)*2**16 + 2**15
MPY *,AR2
APAC            ; ACC = bk(i)*2**16
                  + errf*x(i-k) + 2**15
SACH *+        ; SAVE bk(i+1).
```

When the MPYA and ZALR instructions are used, the adaptation reduces to three instructions corresponding to three clock cycles, as shown below:

```
LRLK AR2,COEFFD ; LOAD ADDRESS OF COEFFICIENTS.
LRLK AR3,LASTAP ; LOAD ADDRESS OF DATA SAMPLES.
LARP AR2
LT ERRF          ; errf = 2*B*e(i)
.
.
ZALR *,AR3      ; ACC = bk(i)*2**16 + 2**15
MPYA *,AR2      ; ACC = bk(i)*2**16
                  + errf*x(i-k) + 2**15
                  ; PREG = errf*x(i-k+1)
SACH *+        ; SAVE bk(i+1).
```

Note that the processing order has been slightly changed to incorporate the use of the MPYA instruction. This is due to the fact that the accumulation performed by the MPYA is the accumulation of the previous product.

We have now seen the basic code for a FIR filter tap and a coefficient update. Figure 7 shows a routine to filter a signal and update the coefficients for a 256-tap adaptive FIR filter. Note that for each tap one instruction cycle is needed to perform the FIR filter (i.e., to execute a MACD), three instruction cycles are needed to update the filter coefficients, and 33 instruction cycles are needed for overhead. Therefore, the total number of execution cycles needed for the routine is $33 + 4n$, where n is the filter length. Also, note that data memory and program memory requirements are $5 + 2n$ and $30 + 3n$ words, respectively. For adaptive filters, the filter length is restricted by both execution time and memory. There is obviously more processing to be completed per sample due to the adaptation, and the adaptation

```
TITL 'ADAPTIVE FILTER'
DEF ADPFIR
DEF X,Y

*
* THIS 256-TAP ADAPTIVE FIR FILTER USES ON-CHIP MEMORY BLOCK
* BO FOR COEFFICIENTS AND BLOCK B1 FOR DATA SAMPLES. THE
* NEWEST INPUT SHOULD BE IN MEMORY LOCATION X WHEN CALLED.
* THE OUTPUT WILL BE IN MEMORY LOCATION Y WHEN RETURNED.
* ASSUME THAT THE DATA PAGE IS 0 WHEN THE ROUTINE IS CALLED.
*
COEFFP EQU >FF00      ; BO PROGRAM MEMORY ADDRESS
COEFFD EQU >0200      ; BO DATA MEMORY ADDRESS
*
ONE EQU >7A           ; CONSTANT ONE (DP=0)
BETA EQU >7B          ; ADAPTATION CONSTANT (DP=0)
ERR EQU >7C           ; SIGNAL ERROR (DP=0)
ERRF EQU >7D          ; ERROR FUNCTION (DP=0)
Y EQU >7E             ; FILTER OUTPUT (DP=0)
X EQU >7F             ; NEWEST DATA SAMPLE (DP=0)
FRSTAP EQU >0300      ; NEXT NEWEST DATA SAMPLE
LASTAP EQU >03FF      ; OLDEST DATA SAMPLE
*
* FINITE IMPULSE RESPONSE (FIR) FILTER.
*
ADPFIR CNFP           ; CONFIGURE BO AS PROGRAM:
MPYK 0                ; Clear the P register.
LAC ONE,14            ; Load output rounding bit.
LARP AR3
LRLK AR3,LASTAP      ; Point to the oldest sample.
FIR RPTK 255
MACD COEFFP,*-        ; 256-tap FIR filter.
CNFD                 ; CONFIGURE BO AS DATA:
APAC
SACH Y,1              ; Store the filter output.
NEG
ADD X,15              ; Add the newest input.
SACH ERR,1            ; err(i) = x(i) - y(i)
*
* LMS ADAPTATION OF FILTER COEFFICIENTS.
*
LT ERR
MPY BETA
PAC                  ; errf(i) = beta * err(i)
ADD ONE,14           ; ROUND THE RESULT.
SACH ERRF,1
*
MAR *+
LAC X                ; INCLUDE NEWEST SAMPLE.
SACL *
*
LRLK AR2,COEFFD      ; POINT TO THE COEFFICIENTS.
LRLK AR3,LASTAP      ; POINT TO THE DATA SAMPLES.
LT ERRF
MPY *,AR2            ; P = 2*beta*err(i)*x(i-255)
*
ADAPT ZALR *,AR3      ; LOAD ACCH WITH b255(i) & ROUND.
MPYA *,AR2            ; b255(i+1) = b255(i) + P
SACH *+              ; P = 2*beta*err(i)*x(i-254)
                      ; STORE b255(i+1).
*
ZALR *,AR3            ; LOAD ACCH WITH b254(i) & ROUND.
MPYA *,AR2            ; b254(i+1) = b254(i) + P
SACH *+              ; P = 2*beta*err(i)*x(i-253)
                      ; STORE b254(i+1).
*
ZALR *,AR3            ; LOAD ACCH WITH b253(i) & ROUND.
MPYA *,AR2            ; b253(i+1) = b253(i) + P
SACH *+              ; P = 2*beta*err(i)*x(i-252)
                      ; STORE b253(i+1).
.
.
.
*
ZALR *,AR3            ; LOAD ACCH WITH b1(i) & ROUND.
MPYA *,AR2            ; b1(i+1) = b1(i) + P
SACH *+              ; P = 2*beta*err(i)*x(i-0)
                      ; STORE b1(i+1).
*
ZALR *,AR3            ; LOAD ACCH WITH b0(i) & ROUND.
APAC *,AR2            ; b0(i+1) = b0(i) + P
SACH *+              ; STORE b0(i+1).
*
RET                  ; RETURN TO CALLING ROUTINE.
```

Figure 7. 256-tap adaptive FIR filter routine.

itself dictates that the coefficients be stored in the reconfigurable block of on-chip RAM. Thus, an adaptive filter with no external data memory is limited to 256 taps.

Telecommunications applications. Digital signal processing will be more extensively used in telecommunications as it evolves toward all-digital networks.¹⁷ Below, we discuss several typical uses of the TMS320C25 in telecommunications applications.

Echo cancellation. In echo cancellation, an adaptive FIR filter performs the modeling routine and signal modifications needed to adaptively cancel the echo caused by impedance mismatches in telephone transmission lines. The TMS320C25's large on-chip RAM of 544 words and on-chip ROM of 4K words allow it to execute a 256-tap adaptive filter (32-ms echo cancellation) without external data or program memory.

High-speed modems. For high-speed modems, the TMS320C25 can perform functions such as modulation and demodulation, adaptive equalization, and echo cancellation.^{18,19}

Voice coding. Voice-coding techniques such as full-duplex, 32,000-bit-per-second adaptive differential pulse-code modulation (CCITT G.721), CVSD, 16,000-bit-per-second subband coding, and linear predictive coding are frequently used in voice transmission and storage. The speed of the TMS320C25 in performing arithmetic and its normalization and bit-manipulation capabilities enable it to implement these functions, usually within itself (i.e., with no external devices).

Graphics and image processing applications. In these applications, a signal processor's ability to interface with a host processor is important. The TMS320C25 multiprocessor interface enables it to be used in a variety of host/coprocessor configurations. Graphics and image processing applications can use the TMS320C25's large directly addressable external data space and global memory capability to allow graphical images in memory to be shared with a host processor, thus minimizing data transfers. The TMS320C25's indexed indirect addressing modes allow matrices to be processed row by row when matrix multiplication is performed for 3-D image rotation, translation, and scaling.

High-speed control applications. These applications use the TMS320C25's general-purpose features for bit-test and logical operations, timing synchronization, and fast data transfers (10 million 16-bit words per second). They use the TMS320C25 in closed-loop systems for control signal conditioning, filtering, high-speed computing, and multichannel multiplexing. The following examples demonstrate typical control applications.

Disk control. In disk drives, a closed-loop actuation mechanism positions the read/write heads over the disk surface. Accurate positioning requires various signal conditioning tasks to be performed. The TMS320C25 can replace costly bit-slice, custom, and analog solutions in performing such tasks as compensation, filtering, and fine/coarse tuning.

Robotics. The TMS320C25's digital signal processing and bit-manipulation power, coupled with its host interface, allow it to be useful in robotics control. The TMS320C25 can replace both the digital controllers and the analog signal processing hardware a robot needs to communicate to a central host processor, and it can perform the numerically intensive control functions typical of robotic applications.

Instrumentation. Instruments such as spectrum analyzers often require a large data memory space and a processor capable of performing long-length FFTs and generating high-precision functions with minimal external hardware. The TMS320C25 fulfills these requirements.

Numeric processing applications. Numeric and array processing applications benefit from the TMS320C25's performance. The device's high throughput and its multiprocessing and data memory expansion capabilities make it a low-cost, easy-to-use replacement for a typical bit-slice array processor.

Benchmarks. The TMS320C25 has demonstrated impressive performance of benchmarks representing common DSP routines and applications. Table 3 shows this performance.

The TMS320C25 digital signal processor is the newest member of the TMS320 family. It is a pin-compatible, CMOS version of the TMS32020 but offers several enhancements of that device—a 100-ns instruction cycle time, 4K words of on-chip masked ROM, eight auxiliary registers, an eight-level hardware stack, and a double-buffered serial port. It also enhances the TMS32020 instruction set to support adaptive filtering, extended-precision arithmetic, bit-reversed addressing, and faster I/O.

The TMS320C25's multiprocessor capability, large memory spaces, and general-purpose features allow it to be used in a variety of systems, including ones currently employing costly bit-slice processors or custom ICs.

Table 3.
TMS320C25 benchmarks.

DSP ROUTINES/APPLICATIONS	PERFORMANCE
FIR filter tap	100 ns per tap
256-tap FIR filter sample rate	37 kHz
LMS adaptive FIR filter tap	400 ns per tap
256-tap adaptive FIR filter sample rate	9.5 kHz
Biquad filter element	1 μ s
Echo canceller	32 ms per single chip (with internal memory)
32,000-bit/s CCITT ADPCM	1 channel full-duplex, single-chip (with internal memory)
16,000-bit/s subband coding	2 channels full-duplex, single-chip (with 0.5K external data memory)
2400-bit/s LPC-10 coding	2 channels full-duplex, single-chip (with 2K external data memory)

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Gene A. Frantz has been Texas Instruments' applications manager for digital signal processing products since 1984. He is also a senior member of the Technical Staff at TI. He joined TI in 1974 as a system design engineer and worked on calculators in TI's Consumer Products Division. In 1976 he was assigned to the Li'l Professor design team. He was next assigned to the Speak & Spell project, where he served as program manager. Since then, he has been involved with every speech-related consumer product developed at TI.

Frantz received a BSEE from the University of Central Florida in 1971, an MSEE from Southern Methodist University, and an MBA from Texas Tech University.



Kun-Shan Lin has been involved in digital signal processing applications in the TI Semiconductor Group since 1984. He is a senior member of the TI Technical Staff. He joined Texas Instruments in 1979 and was assigned to the Consumer Products Division, where he developed speech techniques for learning aids. Prior to joining TI, he was an assistant professor of electrical engineering at Tennessee State University and an adjunct assistant professor of EE at the University of New Mexico. Lin received his PhD from the University of New Mexico in 1976.



Jay Reimer, a member of the TI Technical Staff, handles DSP applications engineering for the TMS320 family of products. He joined TI in 1979 to work with speech products in the company's Consumer Products Division. In 1984, he transferred to the Semiconductor Group to work with digital signal processors. His responsibilities include software development for the TMS320 family and applications assistance for customers using the processors. Reimer received a BS in physics from Fort Hays State University, Kansas, in 1975 and an MS in physics from the University of Kansas in 1977.



Jon Bradley is an applications engineer for the TMS320 family. He joined Texas Instruments in 1976 and has been an applications engineer for most of TI's microprocessor and peripheral products, starting with the TMS9900 family. His responsibilities have included microprocessor system design, digital and analog circuit design, integrated circuit design, test engineering, and programming. Bradley received a BSEE from Worcester Polytechnic Institute, Massachusetts, in 1976.

Questions about the products discussed in this article can be directed to Texas Instruments, Digital Signal Processing Dept.—Mail Station 6400, PO Box 1443, Houston, TX 77001; (713) 879-2320.

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