

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRO DEVICES, INC.,
and ATI TECHNOLOGIES ULC

Petitioner,

v.

SENTIENT SENSORS LLC

Patent Owner.

Case IPR2023-00195
U.S. Patent No. 6,938,177

PATENT OWNER'S PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit No.	Description
2001	USAF Cooperative Research and Development Agreement between Air Force Research Laboratory, Space Vehicles Directorate and MSI November 24, 1998 Confidential
2002	JTAG Article FPGA4fun (1) https://www.fpga4fun.com/JTAG1.html
2003	TAP Article FPGA4fun (2) https://www.fpga4fun.com/JTAG2.html
2004	Xilinx JTAG Programmer Guide 1991-1999
2005	XLINX XC4000 TAP Application Note November 16, 1999
2006	USPTO Office Action Dated December 8, 2004
2007	Examiner Stoynov 1st Prior Art Search 11/19/04 (5 pages)
2008	Examiner Stoynov 2nd Prior Art Search 11/22/04 (7 pages)
2009	Examiner Stoynov 3rd Prior Art Search 11/22/04 (5 pages)

2010	Examiner Stoynov 4th Prior Art Search 11/23/04 (8 pages)
2011	Examiner Stoynov 5th Prior Art Search 11/23/04 (10 pages)
2012	Examiner Stoynov 6th Prior Art Search 11/24/04 (5 pages)
2013	Examiner Stoynov 7th Prior Art Search 11/29/04 (14 pages)
2014	Examiner Stoynov 8th Prior Art Search 3/09/05 (3 pages)
2015	Proof of Service on Registered Delaware Agent
2016	MSI/Sentient Ownership Interest Confidential
2017	Letter from James Lyke in support of Management Sciences, Inc. dated Apr. 29, 1997 Confidential
2018	Bus Arbitration In Computer Organization Article https://www.geeksforgeeks.org/bus-arbitration-in-computer-organization/

STATEMENT OF MATERIAL FACTS IN DISPUTE

Petitioners XILINX, INC., ADVANCED MICRO DEVICES, INC., and ATI TECHNOLOGIES ULC (collectively, “Petitioners” or “Xilinx Inc. *et al.*”) did not submit a specific articulated statement of material facts in their Petition. Accordingly, no response is required under 37 C.F.R. § 42.23(a), and no facts are admitted.

Pursuant to the Notice of Filing Date Accorded to Petition of March 24, 2023,¹ Sentient Sensors, LLC (“Sentient” or “Patent Owner”) hereby timely submits its Preliminary Response to the Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 6,938,177 (“’177”) filed by Xilinx Inc. *et. al.* (“Xilinx” or “Petitioners”).

I. INTRODUCTION

The Board should deny institution of the Xilinx IPR challenging claims 1-5, 10-15, and 17-20 of ’177 Patent. Petitioners’ challenges are merely duplicative of past prior art rejections to the claims of the ’177 Patent encountered during its prosecution that were fully considered by the United States Patent & Trademark Office (“USPTO”) and overcome during examination. Petitioners merely repackage and/or recycle similar arguments made during prosecution through use of the same or cumulative prior art in an attempt to alter the intrinsic record that found the same or similar positions unavailing.

The points of technical improvement (novelty) relied on by Patent Owner as a basis for filing the ’177 Patent represent the functional shortcomings of the prior art and are founded on actual work with U.S. Patent No. 6,148,399 to James Lyke (the “’399 Patent” or “*Lyke*”)—Petitioners’ primary reference—and its described Advanced Instrument Controller (“AIC”) that was cited and extensively considered

¹ See Paper 3.

during prosecution. The U.S. Government also found the shortcomings in the '399 Patent and AIC as compelling reasons to sponsor Mr. Kenneth Blemel's efforts to improve the AIC, which resulted in the inventions of the '177 Patent. Products covered by the '177 Patent have been sold by Patent Owner to many branches of the U.S. military, including the Office of the Secretary of Defense and the U.S. Missile Defense Agency, and incorporated into numerous aerospace platforms.

Sentient Sensors

Sentient is a small family-owned business that was founded by inventor and entrepreneur Kenneth Blemel and his wife of 63 years, Marlene ("Kay") Blemel.² For over 50 years, Mr. Blemel, a life-long engineer, and sole inventor of the '177 Patent, has operated his small business in New Mexico providing high-tech specialty solutions for military and aerospace applications and successfully guiding multiple research and development programs for, among others, the U.S. Air Force and other branches of the U.S. military, including the R&D program culminating in the issuance of the challenged '177 Patent.

The inventions described and claimed in the '177 Patent have been used to provide instrumentation for monitoring and control of systems and components of instruments, aircraft, ships, homes, and machinery. A few examples include:

² See, e.g., Sentient's website at <http://www.mgtsciences.com/>

- Monitoring signals on UH-60 helicopters;
- Instrumentation for prognostic health monitoring of aircraft propulsion systems;
- Instrumentation interface to paired flight data recorders;
- Instrumentation monitoring health signatures of aircraft propulsion systems;
- Instrumentation for monitoring and control of diesel generator sets;
- Instrumentation for monitoring health of ballistic missiles;
- Instrumentation of hybrid micro-grids; and
- Edge node flight data collection and analysis for B-52 and other military aircraft.

The teachings of the '177 Patent enable the rapid prototyping and deployment of complex hardware and software platforms thus providing enhanced flexibility for various real-world applications. As just one example, the '177 Patent describes and claims an instrument controller including a microprocessor for controlling inputs and outputs, logic gates arranged in a manner consistent with a field programmable gate array ("FPGA") that can be used as a freely reconfigurable parallel *and independent* processor, and a real-time clock for time-stamping of data before it is stored in non-volatile memory, all of which contribute to the creation of a customizable development platform that allows for a wide range of hardware controller solutions.

As of its filing date in December 2001, the technology described and claimed in the '177 Patent provided for novel and innovative in-field control and monitoring system with time-stamped selectable collection and digitizing of analog and digital

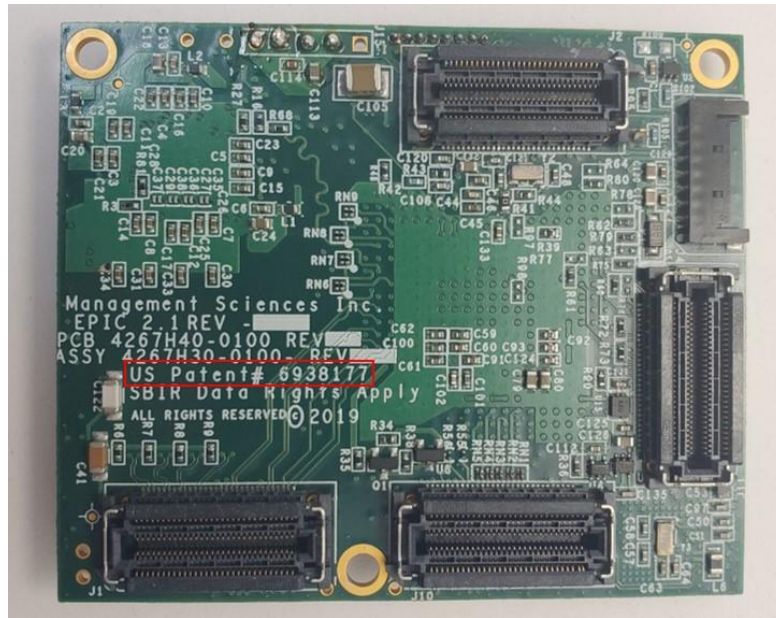
data streams, and enabled, *inter alia*, real-time concurrent data processing to measure and control stresses on components and to generate alerts for anomalous conditions. The use of such programmable logic-based “system on a chip” and “network on a chip” instrument controllers are now widespread with diverse applications, including general computer-based system control, machinery control, field programmable automation of process lines, telecommunications, and diagnostic and prognostic health monitoring of equipment.

The research and development program that led to the innovations described and claimed in the ’177 Patent was funded by the U.S. Air Force and conducted at Kirtland Air Force base in Albuquerque, New Mexico. *See* EX. 1001 at 1:5-10. These advancements were initially directed toward use in the Strategic Defense Initiative program initiated in the 1980s, colloquially known at the time as “Star Wars.” As a result, the U.S. government, via the Space Vehicles Directorate of the U.S. Air Force, entered into a Collaborative Research and Development Agreement (the “Space Directorate CRADA” (EX. 2001)) with Sentient and secured a license to practice the inventions of the ’177 Patent. *Id.*

Products covered by the ’177 Patent have been sold by Patent Owner to many branches of the U.S. military, including the Office of the Secretary of Defense and the U.S. Missile Defense Agency, among others, and incorporated into numerous aerospace platforms. Pictures of marked versions of Sentient’s Embodied

Programmable Instrumentation Controller “EPIC” products covered by the ’177

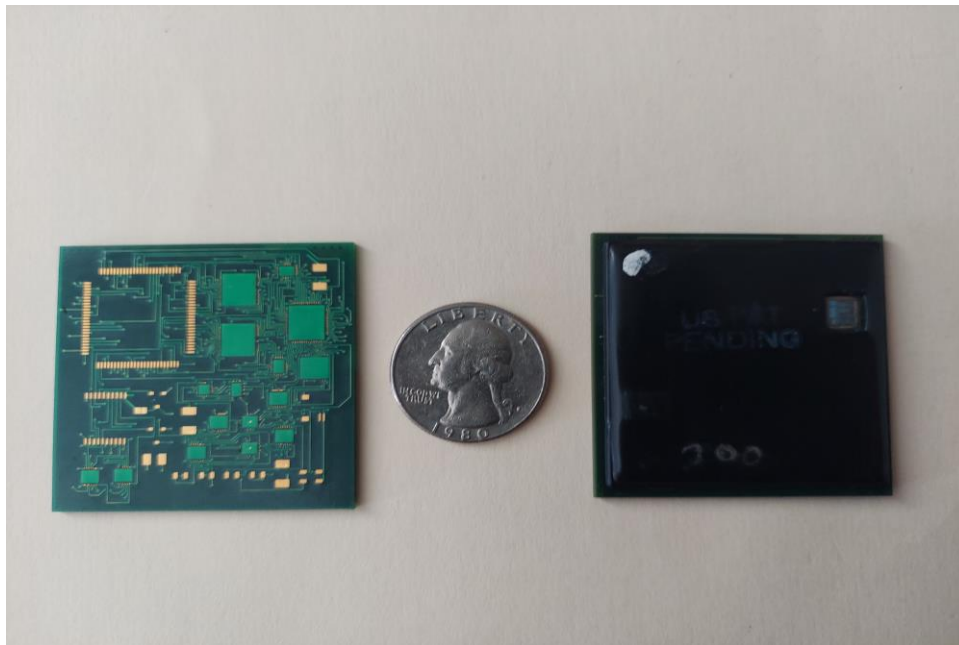
Patent are shown below^{3;4;5}.



³ <https://www.mgtsciences.com/products/>

⁴ https://www.mgtsciences.com/wpcontent/uploads/2016/09/EPIC2_Brochure_Breif_May_31_2016.pdf

⁵ https://www.mgtsciences.com/wpcontent/uploads/2016/09/Sentient_Guardian_Brochure_Aug_2016.pdf



Hardware purveyors such as Xilinx and the licensees of the '177 Patent have employed the inventions of the '177 Patent for their own commercial exploitation (*e.g.*, as automotive and industrial control devices) and used them for controllers of a wide array of electro-mechanical systems.

Prosecution of the '177 Patent in the USPTO In View Of Lyke

The '399 Patent to *Lyke*, and the AIC described therein, was considered in great detail during prosecution of the '177 Patent and its functional shortcomings were the basis for the inventions described in therein. Indeed, the purpose of Space Directorate CRADA dated November 24, 1998, between Management Sciences, Inc. (“MSI”)⁶ and the Air Force Research Laboratory, Space Vehicles Directorate, was to improve the existing AIC technology to develop novel AIC-based systems. In fact, James Lyke was aware that the Air Force sought to improve upon the technology disclosed in his '399 Patent by engaging Mr. Blemel, who was highly regarded by Mr. Lyke. See EX. 2001 and p.14 including section 2.0; see also EX. 2017 (Apr. 29, 1997 Letter from J. Lyke recommending that Management Sciences, Inc.’s “Phase II SBIR proposal,” which would eventually lead to the inventions in the '177 Patent, be funded).

Various technical goals were enumerated in the Space Directorate CRADA including, for example, producing “AIC technologies for the commercial market for use in sensing monitoring and controlling diverse applications across a broad spectrum of applications including, but not limited to *process control, aerospace,*” *etc.* (EX. 2001 at p.14, section 2.0); and is intended to create “smarter systems” with

⁶ MSI is the managing member of Sentient. See paper 4; see also EX. 2016.

the ability to “embed intelligence” and improve the capability and responsiveness of the war fighter (*id.* at p.15, section 5.2.3). *See also* Section 8 pages 16-17.

During the development period that began in November 1998, numerous technical limitations were noted with regard to the systems of the '399 Patent. For example, in the DESCRIPTION OF THE PRIOR ART section, the '177 Patent explains with particularity the function of the '399 Patent technology and its limitations. *See* '177 Patent at 1:21-2:8.

The '177 Patent explains that the '399 Patent suffers from numerous deficiencies, such as its *inability to run parallel and independent processes*. *See* '177 Patent at 2:9-2:31. Thus, according to the '177 Patent, there was a need for a circuit design capable of executing multiple parallel processes in an independent fashion. EX. 1001 Patent 2:9-18.

- However, there are several limitations to the design in
- ¹⁰ U.S. Pat. No. 6,148,399. First the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel
- ¹⁵ processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

This theme is repeated numerous times throughout the '177 specification. *See* EX. 1001 at, *e.g.*, 2:48-55, 8:18-22. This feature is also specified in, *e.g.*, independent claims 1, 6, 10, and 15. *See, e.g.*, 10:4-7 and 12:14-19.

During examination, the USPTO studied the '399 Patent. By granting the '177 Patent, the USPTO came to the same conclusion as Mr. Blemel. Namely that *Lyke* does not teach or suggest a field programmable gate array coupled to the processor for parallel independent processing. EX. 2006 USPTO Office Action p. 4-5:

Lyke fails to disclose an embedded memory for storing an initialization program
and a field programmable gate array coupled to the processor for parallel processing.

Accordingly, all available intrinsic evidence is consistent in that the '399 Patent *does not* teach or suggest a field programmable gate array that runs *independent parallel processes*.

Extensive Prior Art Searching by the USPTO

The USPTO conducted extensive prior art searching while examining the '177 Patent. As can be seen from EXs. 2007-2014, Examiner Stoynov—an experienced Examiner in the integrated circuit art unit 2116 that handles the U.S. classification 713 (Electrical computers and digital processing systems: support) under which both the '399 and '177 Patents were prosecuted (*see* EX. 1003, front page, line 52; EX. 1001, front page, line 52)—conducted no less than *eight different comprehensive prior art searches*. The first seven searches were conducted over a period of 10 days before the first Office Action (EXs. 2007-2013) and include an impressive *56 pages of search terms and strategy* covering interwoven and overlapping search strings relating to the claimed features—including an FPGA and

independent parallel processes—yielding dozens of U.S. Patent documents. Petitioners now rely on some of those documents found by Examiner Stoynov as supposedly “new” or that Petitioners assume the USPTO found unhelpful. *See, e.g.*, EX. 2014 (showing that Examiner Stoynov found U.S. Patent 5,574,930 to *Halverson* (EX. 1025) and used it as a key term in additional searches). EX. 2014.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

L12	25	("5574930").URPN.	USPAT	OR	OFF	2005/03/09 11:15

The eighth search was conducted before issuance to yet again confirm patentability.

After his extensive searching, Examiner Stoynov found that the *Cloutier* (EX. 1040), *Lyke* (EX. 1003) and *DaCosta* (EX. 1041) references listed on the face of the '177 Patent were the most relevant and used them to reject the pending claims. The fact that Petitioners Xilinx—the world’s largest and oldest FPGA manufacturer—and AMD—one of the world’s most valuable semiconductor companies—with their combined vast resources and institutional knowledge, failed to produce non-duplicative or non-cumulative references confirms Examiner Stoynov’s diligence and the quality of his searches.

Dehkordi (EX. 1004)

Dehkordi describes an MCM-based DSP subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA. As shown in the annotated figure from *Dehkordi* below, the DSP processor and FPGA are connected through

numerous buses, the most notable of which is the *control bus* (highlighted in yellow).

A POSA would understand that the control bus allows the processor to control the FPGA with operational instructions, including providing a clock signal. Accordingly, the FPGA is *dependent* on the processor in a configuration that is necessarily a master/slave.

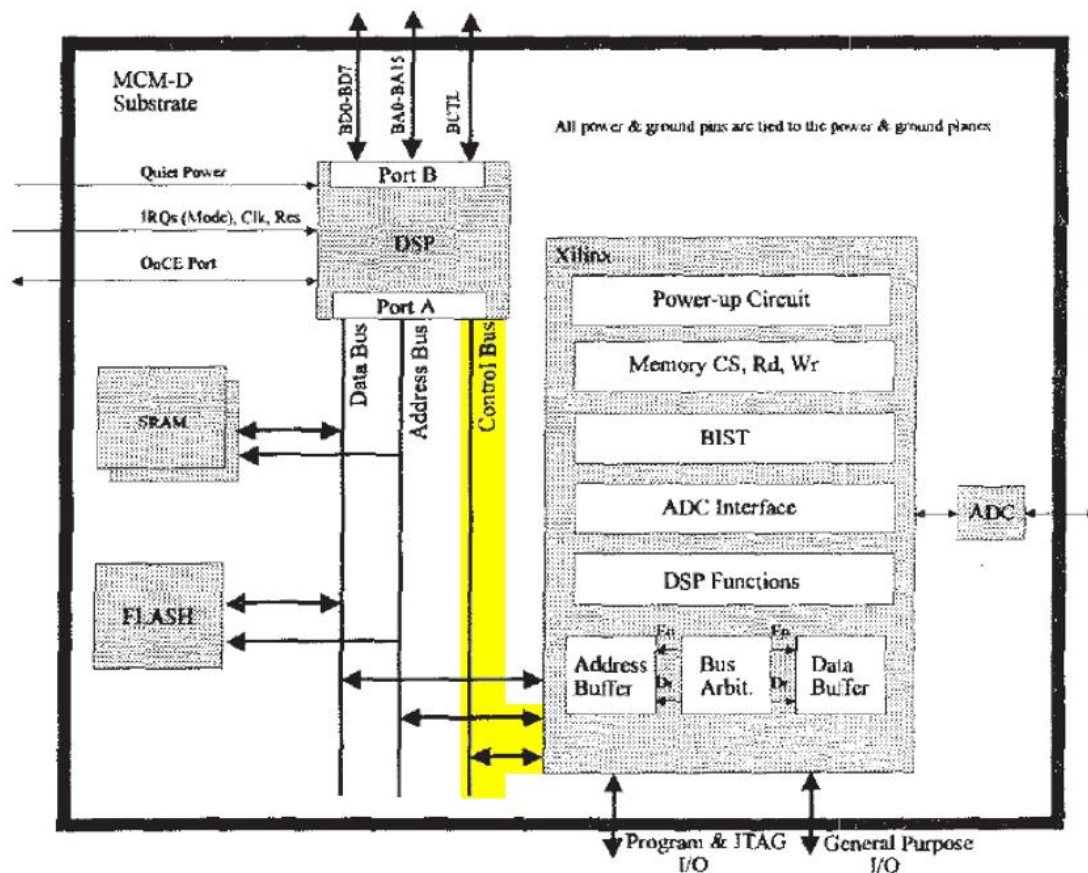


Figure 1. The Block Diagram of the DSP Sub-system.

This is confirmed by Xilinx's own documentation. In fact, the Xilinx 4010 datasheet (EX. 1014) explains that the most common configuration of the 4010 FPGA is the Slave Serial configuration, such as that shown in *Dehkordi*, which

means the DSP processor is in control of the FPGA. EX. 1014 at 6-45. This is consistent with *Dehkordi's* technical description that explains how the MCM subsystem is specifically designed to exploit the multiprocessing capability *of the DSP processor*. EX. 1004 at 1, “*Design Flow*” section. This technical description means that the FPGA operates in *a subservient support role* under the control of the DSP processor to maximize the DSP processor’s multiprocessing functionality by, *e.g.*, preprocessing incoming data *as directed by the DSP processor* to relieve that burden from the DSP processor. No other specialized connection or functionality is shown. *See id.*

Dehkordi also describes *a special testing mode of operation* that employs the well-known industry standard JTAG and TAP testing methodologies used for testing the operation of the DSP subsystem. *See* EX. 1003 at 3, “*Cost and Testing Issues*” section. Notably, however, JTAG and TAP testing operations *necessarily* require an external JTAG computer or other controller that *controls both the DSP processor and the FPGA during testing*. Accordingly, because both the FPGA and DSP processor are under *common control* during testing, they *do not and cannot operate any independent processes* (*i.e.*, they are both under the control of another common device). Xilinx’s own JTAG/TAP documentation used for the 4010 series FPGA explains this. *See* EXs. 2004-2005. This is explained in more detail in connection with Patent Owner’s response to Ground 1 below.

Steele (EX. 1009)

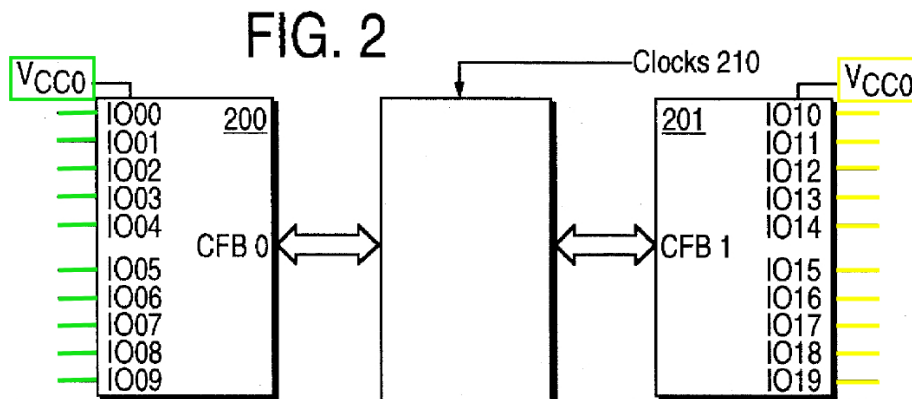
Steele describes a programmable logic device configurable to operate as a voltage aggregator that copies an applied input voltage for output at other pins. Simply stated, it operates by accepting an input voltage generated at an external source at the VCCO pin of a Configurable Logic Block (CFB) and replicates that voltage at the input/output (I/O) pins for use in external devices. EX. 1009, 4:28-58. This is explained in detail at 4:28-43 of *Steele* and shown in *Steele*'s FIG. 2 below (annotated to show the 5V level (CFB 0) (green) and the 3V level (CFB 1) (yellow)).

U.S. Patent

Oct. 7, 1997

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5,675,824



Notably, *Steele* does not generate the applied VCCO voltage levels itself, but rather merely uses them. The voltage generation is done elsewhere on another external device and those voltages are applied to the VCCO input from that external source for copying by *Steele*'s CFB.

Moreover, Steele *does not* convert power. Instead, Steele merely replicates *the same* voltage level VCCO at the output I/O pins. For example, IO00-IO09 have 5V outputs whereas IO10-IO19 have 3V outputs. See EX. 1009, 2:22-26; 4:28-43.

II. LEGAL STANDARD

A. Standard For Granting An *Inter Partes* Review

The Board may only grant a petition for *Inter Partes* Review where “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). The Petitioners bear the burden of showing that this statutory threshold is met. See Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012).

B. Standard to Deny Institution Under Section 325(d)

Pursuant to 35 U.S.C. § 325(d), “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d). In evaluating Section 325(d), the Board considers two factors: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL*

Elektromedizinische Geräte GmbH, Case No. IPR2019-01469, Paper No. 6, 2020 WL 740292, at *3 (P.T.A.B. Feb. 13, 2020). “If a condition in the first part of the framework is satisfied and the petitioner fails to make a showing of material error, the Director generally will exercise discretion not to institute *inter partes* review.” *Id.* “At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” *Id.*

In doing so, the Board considers “non-exclusive factors, such as: (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.” *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, Case No. IPR2017-01586, Paper No. 8, 2017 WL 6405100, at *6 (P.T.A.B. Dec. 15, 2017).

The Board is not “free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR.” *In re Magnum Oil Tools, Int’l, Ltd.*, 829 F.3d 1365, 1381 (Fed. Cir. 2016). “The petitioner must instead articulate specific reasoning, based on evidence of record,” as set out in its petition “to support the legal conclusion of obviousness.” *Id.* at 1380. The Board “must base its decision on arguments that were advanced by a party.” *Id.* at 1381. The PTAB cannot “decide unpatentability theories never presented by the petitioner.” *Id.*

To prevail on an obviousness ground, Petitioner may not simply identify individual claim components but instead must show why a “skilled artisan, *with no knowledge of the claimed invention*, would have selected these components for combination in the manner claimed.” *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) (*emphasis added*). A petitioner must support even simple modifications to a reference with some motivation to make the change. *See In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

In addition, a petitioner cannot rely on “mere conclusory statements.” *Magnum Oil*, 829 F.3d at 1380. Rather, the petitioner must set forth “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-19 (2007) (internal citation omitted).

Similarly, a petitioner cannot simply rely on an expert's unsubstantiated and conclusory opinions. *See* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (affirming that Petitioner failed to establish obviousness where expert testimony “add[ed] nothing beyond the conclusory statements in [the] petition.”).

An appropriate obviousness inquiry *cannot involve even a “hint of hindsight.”* *Star Sci., Inc. v. R.J. Reynolds Tobacco Co.*, 655 F.3d 1364, 1375 (Fed. Cir. 2011) (*emphasis added*). Petitioner may not “simply retrace[] the path of the inventor with hindsight, discount[] the number and complexity of the alternatives, and conclude[] that the invention . . . was obvious.” *Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008). Likewise, “[c]are must be taken to avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.” *In re NTP, Inc.*, 654 F.3d 1279, 1299 (Fed. Cir. 2011) (internal quotations omitted).

In arriving at an obviousness determination, the petitioner must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the challenged claims and a relevant skilled artisan not only could have made but would have been motivated to combine all the prior art references in

the way the patent claims. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have been motivated to combine those references. *Intelligent Bio Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Res. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual findings as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a POSITA would have had a reasonable expectation of success from such a combination). This combination determination, as supported by an articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references.” *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

The appropriate claim construction standard is provided by *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Under the *Phillips* standard, “the specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive....’ and claim terms are generally given their ordinary and customary meaning.” *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

III. THE PETITION FAILS TO MAKE OUT A *PRIMA FACIE* CASE OF OBVIOUSNESS

Petitioners present five separate Grounds of unpatentability all based on 35 U.S.C. § 103:

- **Ground 1** is directed toward claims 1 and 4 and is based on *Lyke, Dehkordi, Frantz, and Faura*.
- **Ground 2** is directed toward claim 2 and is the same as Ground 1 with the addition of *Krasner*.
- **Ground 3** is directed toward claim 3 and is the same as Ground 1 with the addition of *Christian*.
- **Ground 4** is directed toward claims 5, 10-11, 13-14, 15, 17, 19, 20 and is the same as Ground 1 with the addition of *Steele*.
- **Ground 5** is directed toward claims 12 and 18 and is the same as Ground 4 with the addition of *Christian*.

Although numerous reasons exist as to why the challenged claims are patentable over the theories advanced in the Petition, Sentient, for the convenience of the Board, focuses on certain straightforward deficiencies in Petitioner’s analysis

of independent claim 1, as found in Ground 1, and independent claims 10 and 15, as found in Ground 4, specifically with respect to the claim term “*independent processes in parallel*” (elements 1.5, 10.5, and 15.2), and of independent claims 13 and 20, as found in Ground 4, specifically with respect to the claim term “*power converter capable of... generating each operating and reference voltage*” (elements 13.6 and 20.1).

Importantly, Petitioners *did not* challenge independent claim 6, which is currently asserted in the co-pending District Court litigation (1:21-cv-00064-MN DDE) involving the same parties here. Accordingly, regardless of the outcome of this proceeding, this case will proceed to trial in Delaware.

A. Ground 1—Based on *Lyke, Dehkordi, Franz, and Faura*

Petitioners’ proposed combination in Ground 1 of *Lyke, Dehkordi, Franz, and Faura* fails to teach or suggest, among other deficiencies, a “*gate array coupled to the processor and configured to run independent processes in parallel with the processor*” as specified in claim 1 (element 1.5), which was a point of novelty described in the ’177 Patent.

Xilinx offers only two references for the proposition that element 1.5 would have been obvious to a POSA at the time of the inventions described and claimed in the ’177 Patent: *Lyke* EX. 1003 (see Petition at 27-28) and *Dehkordi* EX. 1004 (see

Petition at 28-29). But neither *Lyke* nor *Dehkordi* teaches or suggests this novel feature.

1. *Lyke (EX. 1003)*

As noted by Petitioners, Patent Owner was indeed very familiar with technology discussed in the '399 Patent. *See* Petition at 4-5. In fact, Patent Owner made no attempt to hide or conceal that fact. For example, the '177 Patent explains the function of the '399 Patent's technology in the section titled DESCRIPTION OF THE PRIOR ART. *See* '177 Patent at 1:5-2:8.

This attribution to the '399 Patent was not based on idle speculation. The U.S. Air Force specifically commissioned Patent Owner through the Space Directorate CRADA (EX. 2001) to *improve* on the systems disclosed in the '399 Patent.

During the development period that began in November 1998, numerous technical limitations of the systems of the '399 Patent were noted. For example, as specifically explained by the '177 Patent, the '399 Patent—and the AIC it describes—suffers from several deficiencies, such as its *inability to run parallel and independent processes*, and there was a need for a circuit design capable of executing multiple parallel processes in an independent fashion. *See* '177 Patent at 2:9-18:

- However, there are several limitations to the design in
- ¹⁰ U.S. Pat. No. 6,148,399. First the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel
- ¹⁵ processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

This theme is repeated throughout the '177 Patent's specification, such as at, *e.g.*, 2:48-55 and 8:18-22. It is also a specific requirement in the claims, such as, for example, independent claims 1 (element 1.5), 6 (not challenged), 10 (element 10.5, and 15 (element 15.2). *See* '177 Patent, *e.g.*, 10:61-64, 11:42-44, 12:44-46.

Given the lengthy discussion of the '399 Patent in the specification of the '177 Patent, and its use during prosecution at the USPTO, it is surprising that Petitioners nevertheless contend that the “*examiner apparently had not noticed Lyke’s teaching of... “field programmable gate arrays.”*” Petition at 5. This self-serving speculation is belied by the intrinsic evidence. That is, when the USPTO studied the '399 Patent during examination it came to the same conclusion as Mr. Blemel. Namely, that the '399 Patent does not teach or suggest *a field programmable gate array coupled to the processor and configured to run independent processes in parallel with the processor*. EX. 2006, USPTO Office Action p. 4-5. Petitioner’s suggestion to the contrary should thus be given little or no weight.

The same is true for the positions taken at pages 27 and 28 of the Petition. There Petitioners contend that, because a memory with program instructions is used

to program the reconfigurable logic in the '399 Patent (*i.e.*, EX. 1003, 8:55-59), it necessarily means the FPGA runs independently in parallel. Not so.

A POSA would understand that it is axiomatic that *every functional FPGA* must be programmed by a memory with program instructions. Otherwise, the programmable logic gates are non-functional (a “blank device”). A set of unspecified “program instructions” does not necessarily confer on any given FPGA an ability to run independent parallel operations. In fact, there is no mandatory connection between them and, notably, Petitioners have not produced any evidence other than conclusory expert testimony to substantiate its claim. By failing to do so, Petitioners have not met its burden to show that the '399 Patent's “program instructions” must operate processes in parallel and independently.

In fact, Petitioners' own technical documentation teaches differently. EX. 1036 (*Kostarnov*)—a publication referenced by Petitioners and Dr. Shanfield *but not used as a basis for any Ground of rejection*—illustrates two operating modes of the Xilinx 4013 FPGA at Figs. 2 and 3 (below) where it receives instructions from the CPU revealing that the FPGA is *not* operating, and *cannot* operate, independently in parallel. Dr. Shanfield in EX. 1002 at ¶¶ 82-83 seems to agree. There, he makes no assertions that these two configurations are operating independently in parallel. Nor can he; the references themselves clearly explain they are not. For example, in *Kostarnov* at 4, FIG. 2 the FPGA *is always in slave mode* and in FIG. 3 all data bus

operations are controlled by the CPU. Both receive instructions (in yellow) only from the CPU indicating that it is a unidirectional (one-way) path. See EX. 1036 at 3-4.

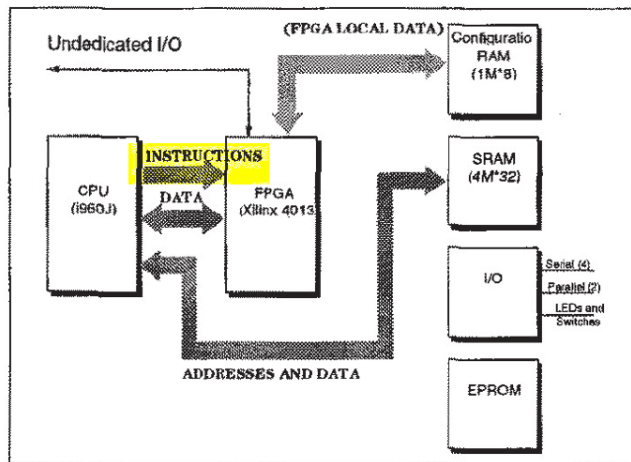


Fig. 2: Functional unit mode

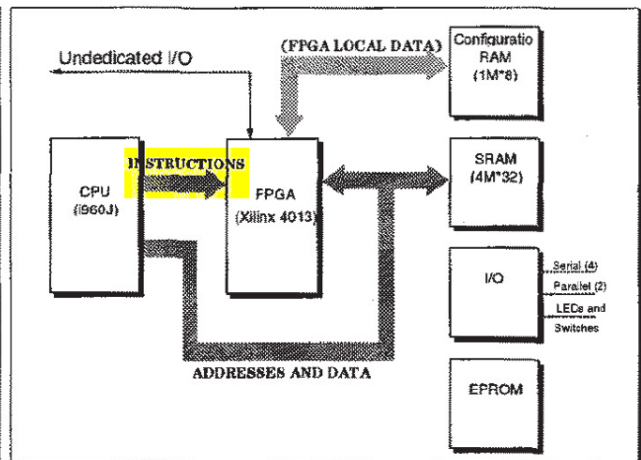


Fig. 3: Lockstep mode

Notably, Petitioners use EX. 1036 as only mere background information without explaining how or why a POSA would be motivated to combine it with *Lyke* other than an unremarkable observation that both generally discuss FPGAs. That is, Petitioners fail to provide any that evidence that the FPGA that *might generally be* included in *Lyke* needs to be configured in a certain specific way.

Indeed, the most popular configuration for the Xilinx XC4000 series of FPGAs is the serial slave mode (dependent operation). See EX. 1014 at 6-45:

In XC4000 Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most com-

No other special connection is shown or suggested in *Lyke*.

Furthermore, in forming his opinion, Dr. Shanfield relies heavily on the disclosure of another reference *also not used in any Ground of rejection—Halverson*, EX. 1025—to substantiate his analysis. This reliance is misplaced, however, because *Halverson* does not disclose *independent parallel processing* but rather discloses *just* parallel processing. Dr. Shanfield seems to agree because he does not assert that *Halverson* shows *independent* parallel processing. This observation is also corroborated by the fact that the USPTO found *Halverson* during examination but decided not to use it as a basis for a rejection. *See* EX. 2014.

Accordingly, *Lyke*, the intrinsic record, and all the supporting references relied on by Petitioners demonstrate the '399 Patent does not teach or suggest a “*gate array coupled to the processor and configured to run independent processes in parallel with the processor.*” Conclusory statements such as those offered by Petitioners are not enough to substantiate its case. *See* Petition at 28; *see also Magnum Oil*, 829 F.3d at 1380. Petitioner cannot rely on “mere conclusory statements,” but “must set forth ‘articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.’” *KSR*, 550 U.S. at 418-19 (internal citation omitted).

Similarly, a petitioner cannot simply rely on an expert’s unsubstantiated and conclusory opinions. *See* 37 C.F.R. § 42.65 (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to

little or no weight.”); *Harmonic*, 815 F.3d at 1363 (affirming that Petitioner failed to establish obviousness where expert testimony “add[ed] nothing beyond the conclusory statements in [the] petition.”). Neither Petitioners nor Dr. Shanfield substantiate the assertion that *Lyke* and *Dehkordi* would operate in the way each says.

Moreover, attempting to alter the facts of the intrinsic record with extrinsic evidence, as Petitioners attempt to do here, is improper. *See Seabed Geosolutions (US) Inc.*, 8 F.4th 1285 (Fed. Cir. 2021). As a result, Petitioners have failed to meet their burden with respect to the teachings of the ’399 Patent.

Additionally, it is noteworthy that Dr. Shanfield is not connected at all with the Air Force, James Lyke, and the AIC and was not involved at all with the work done under the Space Directorate CRADA. Indeed, the CRADA is not even mentioned in his declaration, nor are the sections of the ’177 Patent’s specification that discuss the ’399 Patent. Accordingly, Dr. Shanfield is now attempting to alter the intrinsic record with partisan conclusory opinions—extrinsic evidence—offered nearly 25 years after the development of the technology disclosed and claimed in the ’177 Patent.

2. *Dehkordi* (EX. 1004)

Dehkordi is the only other reference offered by Petitioners for allegedly teaching parallel independent operation. *Dehkordi* describes an MCM-based DSP

subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA shown below:

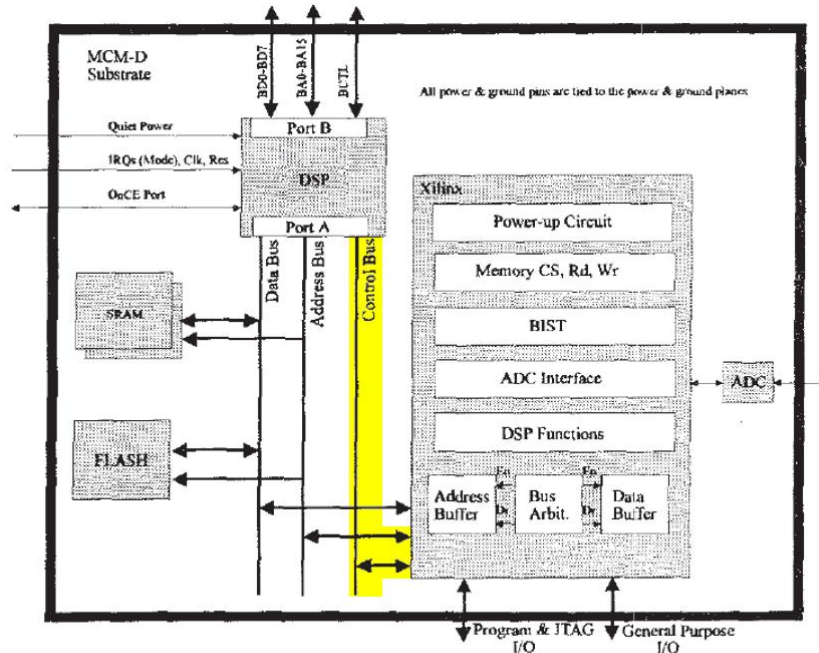


Figure 1. The Block Diagram of the DSP Sub-system.

As described above, the DSP processor and the FPGA are connected through a *control bus* (highlighted in yellow) used to control the processor, which a POSA would understand includes a common clock signal. As such, the FPGA is *dependent* on the processor, and they are necessarily in a reciprocal master/slave configuration.

Given that, no independent processes are possible during normal operation and neither the Petition nor *Dehkordi* suggest otherwise. Xilinx's own documentation confirms this. In fact, the Xilinx 4010 datasheet (EX. 1014) explains in several places that the most popular configuration of the 4010 FPGA is the Slave Serial mode as is shown here:

In XC4000 Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most com-

M0, M1, M2	I	I (M0), O (M1), I (M2)	registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down re-
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See EX. 1014 at 6-45 and 6-40, respectively. Accordingly, the DSP processor is in control of the FPGA unless specified otherwise because it is the most common mode of operation.

This is consistent with *Dehkordi*'s technical description that explains how the MCM subsystem is designed to exploit the multiprocessing capability of the DSP processor, which indicates that the FPGA operates in a subservient support role under the control of the DSP processor to maximize the processor's multiprocessing functionality by, *e.g.*, preprocessing incoming data as directed by the DSP processor. Neither Petitioners nor *Dehkordi* show any specialized connection or functionality that would suggest a different mode of operation. See EX.1004 at 1, FIG. 1 and its associated description in the "Design Flow" section.

Dehkordi, at 3, does describe a special testing mode of operation that uses the well-known industry standard JTAG and TAP testing methodologies for testing the operation of the DSP subsystem. During JTAG and TAP testing operations along with emulators, however, an external JTAG computer or other controller is always

required to control both the DSP processor and the FPGA during testing.

Independent parallel processing is not shown or suggested. See *Dehkordi* at 4:

Cost & Testing Issues

* * * * *

Due to their small feature sizes, MCMs cannot easily be probed or reworked [8]. Therefore, testing and fault isolation becomes a challenging area for MCM designs. Complete boundary scan testing was not feasible for this MCM since only the FPGA supported JTAG. The DSP supports a serial emulation port which was connected to the module pins along with the FPGA TAP port for testing purposes. The FPGA has a RAM-based configuration where the configuration may come from outside the module. A portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the module. The FPGA can easily be reconfigured to route these lines to the module pins for possible probing and debugging during testing. The DSP has a dual data and address port architecture in which the second port was also connected to the module pins for enhanced multi-processing and testing. Testing procedures are being constructed at the time of this publication.

Accordingly, because both the FPGA and DSP processor are under *common control of another device* while under test, they *do not* and *cannot* operate any *independent processes*. This is confirmed by Xilinx's own JTAG/TAP documentation used for the 4010 series FPGA. See EXs. 2002-2005.

Moreover, it is important to note that the testing procedures described in *Dehkordi* and relied on by Petitioners are *only speculative*, as *Dehkordi* explicitly explains that “[t]esting procedures [were] being constructed at the time of [*Dehkordi*’s] publication.” See *Dehkordi* at 4. Nor does *Dehkordi* establish that such procedures were ever completed or, if they were, that they operated as

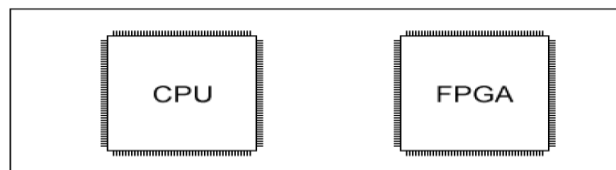
hypothesized. This is significant because, as explained below, the references themselves teach away from and directly conflict with Petitioners' unpatentability allegations.

JTAG Testing

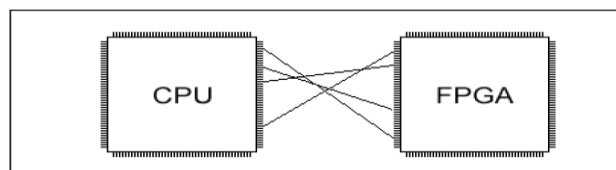
JTAG testing is very well known in the art and was developed in the early 1980s to test continuity and basic functionality of circuits as designs became increasingly more complex and difficult to probe and troubleshoot manually. JTAG testing relies on an external computer to make connections between the components under test by applying various test signals as specified by the JTAG program to confirm continuity and functionality. This is shown below with excerpts from EX. 2002 illustrating how a system, such as an MCM, with both an FPGA and processor are tested via JTAG.

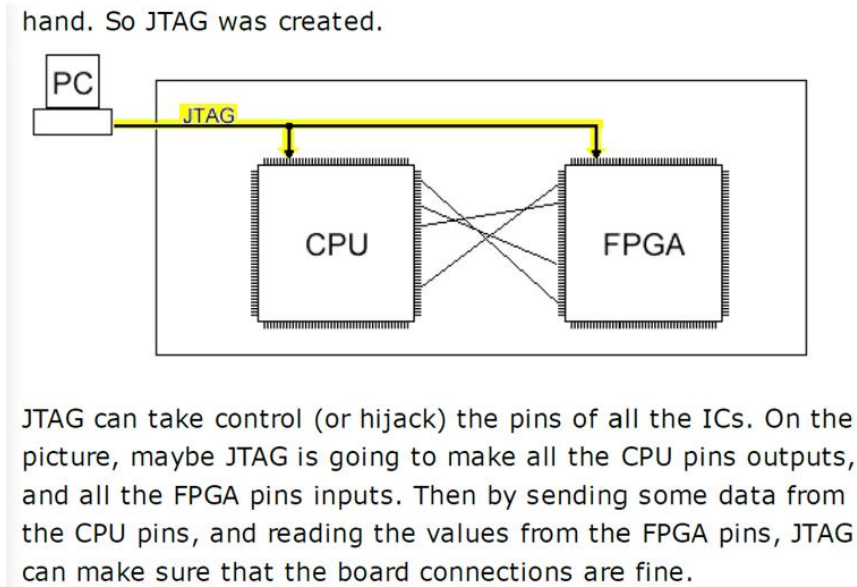
Boundary testing

Here's a simple electronic board (also called "PCB" for "printed circuit board") with two ICs ("integrated circuits"), a CPU and an FPGA. A typical board may have many more ICs.



ICs can have lots of pins. So of course, ICs are connected together with lots of connections (PCB traces). We show just four here. But you can easily have a few thousands on a PCB.





As can be seen from EX. 2002, the JTAG PC takes control of the pins *of all of the ICs* (FPGA and processor) through the JTAG connection highlighted in yellow above. This illustrates both the CPU and FPGA are under the common control of another device and therefore not independent. The JTAG PC then conducts testing by controlling the flow of data and commands to and from both the processor and FPGA. During this process, both devices are always under the common control of the JTAG PC and thus *never operate independently*.

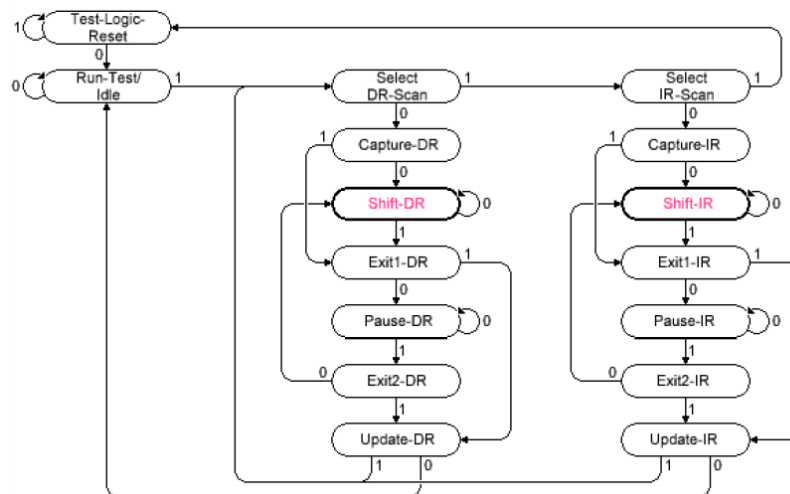
TAP Testing

TAP testing is merely a more sophisticated form of JTAG testing that relies on the same architecture and control methodology. As shown below in excerpts from EX. 2003, the same connections from the JTAG PC go to both the FPGA and processor as generally illustrated in EX. 2002 except implements a more detailed

The JTAG TAP controller

We know that a PC is connected to the JTAG bus as illustrated here:

The diagram illustrates the JTAG TAP controller connection. A PC is connected to a system containing a CPU and an FPGA. The PC has four pins: TDI, TDO, TMS, and TCK. The TCK pin is connected to the TCK pin of both the CPU and the FPGA. The TMS pin is connected to the TMS pin of both the CPU and the FPGA. The TDI pin is connected to the TDI pin of the CPU. The TDO pin of the CPU is connected to the TDI pin of the FPGA. The TDO pin of the FPGA is connected back to the TDO pin of the PC. This configuration allows the PC to communicate with the CPU and the FPGA via the JTAG bus.



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demonstrating that both the FPGA and processor are under common control and never operate independently.⁷

Moreover, it is possible that control of the bus switches back and forth from FPGA to CPU, but one component is always in control. Control is “passed” back and forth. Known as “bus arbitration,” either the FPGA or the CPU takes control of the data and address buses while the other is subservient (the “Bus Arbiter”). EX. 2018. Bus arbitration is not equivalent to independent operation, nor is independent operation required for bus arbitration. The only place that *Dehkordi* mentions bus arbitration is in the section related to JTAG/TAP testing. *Dehkordi* at 3. Notably, however, *Dehkordi* does not mention anything about independent operation anywhere, including during JTAG/TAP testing. Simply put, *Dehkordi* does not teach independent operations.

⁷ The content of EXs. 2002 and 2003 are confirmed by Xilinx’s own references which contain the same materials. EX. 2002 is confirmed by the content of EX. 2004, with EX. 2003 confirmed by EX. 2005.

Bus Arbitration refers to the process by which the current bus master accesses and then leaves the control of the bus and passes it to another bus requesting processor unit. The controller that has access to a bus at an instance is known as a **Bus master**.

A conflict may arise if the number of DMA controllers or other controllers or processors try to access the common bus at the same time, but access can be given to only one of those. Only one processor or controller can be Bus master at the same point in time. To resolve these conflicts, the Bus Arbitration procedure is implemented to coordinate the activities of all devices requesting memory transfers. The selection of the bus master must take into account the needs of various devices by establishing a priority system for gaining access to the bus. The **Bus Arbiter** decides who would become the current bus master.

Moreover, the Xilinx 4010 datasheet (EX. 1014 at 6) explains that whenever data are written into the FPGA, as is the case with JTAG/TAP testing, it acts in slave and peripheral modes—confirming yet again that the FPGA does not operate independently.

Description

XC4000 Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

3. *Franz (EX. 1005) and Faura (EX. 1006)*

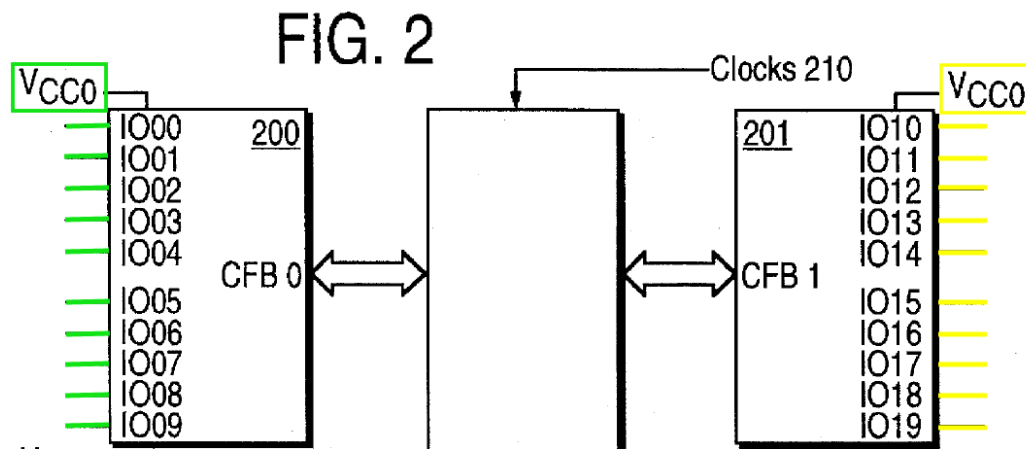
Neither *Franz* nor *Faura* cures the deficiencies of *Lyke* and *Dehkordi*.

Accordingly, Petitioners’ proposed combination of *Lyke*, *Dehkordi*, *Franz*, and *Faura* in Ground 1 fails to teach or suggest a “gate array coupled to the processor and configured to run independent processes in parallel with the processor” as specified in claims 1 (element 1.5) 10 (element 10.5) and 15 (element 15.2). Thus, claims 1-5, 10-12 and 15-19 are patentable for at least this reason alone.

B. Ground 4—Based on *Lyke*, *Dehkordi*, *Franz*, *Faura*, and *Steele*

Ground 4 is simply the references of Ground 1 further combined with *Steele*. Accordingly, Ground 4 suffers from all the same deficiencies as noted above with respect to Ground 1.

Steele describes a programmable logic device configured to operate like a voltage aggregator that copies an applied input voltage for output at other pins. Simply stated, *Steele* operates by accepting an input voltage generated at an external source at the VCCO pin of a Configurable Logic Block (CFB) and *replicates that voltage* at the input/output (I/O) pins for use in external devices. This is explained at EX. 1009 at 4:28-43, and is shown in the annotated version of FIG. 2 below where green represents a 5V level (CFB 0) and yellow represents a 3V level (CFB 1):



Steele does not *generate* the applied VCCO voltage levels as required by the challenged claims of the '177 Patent. Instead, it merely *uses* them. The generation of the voltage levels is done *elsewhere on another device* with those voltages being applied to the VCCO input for the CFB to copy. This is different from the challenged claims of the '177 Patent, which require, *e.g.*, a portion of the gates in the FPGA to operate as an internal embedded power converter capable of receiving an input voltage level and *generating each* operating and reference voltage needed within the instrument controller. *See, e.g.*, '177 Patent, claim 5.

Moreover, *Steele* does not *convert* power but rather *replicates* the *same* voltage level VCCO at the output I/O pins. For example, IO00-IO09 have 5V outputs whereas IO10-IO19 have 3V outputs. *See* EX. 1009 at 2:22-26; 4:28-43. Notably the phrase “power converter” does not appear in *Steele* nor does *Steele* describe converting power in any way.

Accordingly, *Steele* fails to teach or suggest “*a third portion of the gates in the field programmable gate array are configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed...*” for at least three reasons.

First, the claim specifies that the gates operate on “*an input voltage level and generat[e] each operating and reference voltage needed.*” Thus, the plain language of the claim term specifies that one input voltage generates multiple output voltages whereas, in *Steele*, each input voltage VCCO creates *only one corresponding output voltage* at the IO pins that is the same level as (*i.e.*, a copy of) the input voltage. Therefore, Petitioners fail to make out a *prima facie* case of obviousness, as this claim requirement is given *no treatment* in the Petition and thus must fail on this basis alone.

Second, the Petition fails to address the power conversion claim term. Power conversion is not mentioned in the *Steele* reference. Petitioners never address what power conversion is or how it is accomplished in *Steele*. Further, such treatment and explanation are also missing from the reference itself. The Petition thus offers nothing more than conclusory statements that are unsubstantiated by any analysis or explanation based on *Steele* and must therefore fail. *See Magnum Oil*, 829 F.3d at 1380, *infra*.

Third, no such combination would ever be made. Petitioners state that “[i]n the combined system with Steele, a portion of the gates in the FPGA are utilized to carry out power conversion, for the predictable benefits described above, including obviating the need for separate converter hardware apart from the existent FPGA.”

Petition at 48, emphasis added. But this statement is demonstrably wrong. As explained above, the VCCO signal that establishes the required voltage level is *not* generated by any circuitry in Steele instead is created externally. Petitioners admit this. See Petition at 48 (“a plurality of different voltages can be supplied to the V_{cco} pins of different functional blocks, resulting in a plurality of different voltages.”). Emphasis added.

Thus, Petitioners *admit* the VCCO voltages must come from *somewhere outside of Steele*. Therefore, Lyke alone provides all the necessary reference and operating voltages specified in the claim and Steele provides *no added benefit whatsoever* to the proposed combination. Accordingly, Steele is merely a superfluous, cumulative reference that belies the motivation for making the combination of Ground 4 which appears to be offered only for the sole (impermissible) reason of alleging unpatentability.

Such a combination may therefore only be formed based on impermissible hindsight reconstruction. An appropriate obviousness inquiry *cannot involve even a “hint of hindsight.”* *Star Sci., Inc.*, 655 F.3d at 1375 (*emphasis added*).

Accordingly, Petitioners' proposed combination of *Lyke*, *Dehkordi*, *Franz*, *Faura*, and *Steele* in Ground 4 fails to teach or suggest the limitations in independent claims 13 and 20 of a "*power converter capable of... generating each operating and reference voltage*" (elements 13.6 and 20.1). Thus claims 5, 14-15, and 20 are patentable for at least this reason alone.

C. Grounds 2, 3, and 5

Because Grounds 2-3 are based on Ground 1, claims 2 and 3 are patentable for at least the same reasons that claim 1 is patentable over Ground 1. Similarly, because Ground 5 is based on Ground 4, claims 12 and 18 are patentable for at least the same reasons that claims 13 and 15 are patentable over Ground 4. Claims 2, 3, 12, and 18 are independently patentable, however, and to the extent the Board determines that trial should be instituted on Petitioner's Grounds 1 and 4, Patent Owner reserves the right to separately argue the patentability of those claims over Grounds 2-3 and 5.

IV. THE PETITION IS UNSUSTAINABLE

The Petition should be denied for various other reasons.

First, the prior art references relied on by Petitioners have either already been considered by the USPTO, are cumulative, or are irrelevant. Petitioners' primary reference, *Lyke*, was extensively considered and dismissed by the USPTO, as the disclosure and prosecution history of the '177 Patent along with other evidence

demonstrates that the inventions disclosed and claimed in the '177 Patent are innovative improvements over *Lyke*. *See Infra*. Petitioners' attempts to rewrite the disclosure of *Lyke* and the story of Mr. Blemel's innovative research and development commissioned by the U.S. Air Force to improve on *Lyke's* AIC is founded in impermissible hindsight and flawed interpretations of the technology existing at the time. Simply put, Petitioner's extrinsic evidence cannot change the disclosure of *Lyke* nor the USPTO's consideration of that patent and its decision to allow the '177 patent. *See Seabed Geosolutions (US) Inc., infra*.

Petitioner's arguments based on *Dehkordi* are based on speculative testing procedures that do not operate as Petitioners contend because the reference itself teaches that such testing procedures were still in development at the time of *Dehkordi's* publication and, in any event, it is well known that JTAG testing procedures preclude independent operation. Notably, the Petition and Mr. Shanfield do not discuss the JTAG/TAP aspect of *Dehkordi* at all. Moreover, *Dehkordi* is cumulative of *Cloutier* (EX. 1040), which deals with parallel FPGA operations and was cited by USPTO during prosecution and used by the Examiner as the basis for a rejection of claim 1 that was overcome. EX. 2006 at 5.

Further, *Franz* and *Faura*—the other references that Petitioners rely on in Ground 1—are not relevant to the patentable distinctions offered by Patent Owner here for Grounds 1 and 4. Nor do Petitioners offer *Franz* and *Faura* for the

proposition that either teaches or suggests a “*gate array coupled to the processor and configured to run independent processes in parallel with the processor*” as specified in the challenged claims.

Halverson (EX. 1025) was also found by the USPTO during prosecution and dismissed as not relevant to patentability. This is confirmed by Petitioners’ failure to use *Halverson* as the basis for any Ground in the Petition.

Similarly, *Kostarnov* (EX. 1036) is not used as the basis of any Ground in the Petition, nor has Petitioners provided any argument for why a POSA would be motivated to combine *Kostarnov* with the other references in Ground 1, including *Dehkordi*, or that there would be a reasonable expectation of success in doing so. Indeed even if they were combined as proposed, they would still not produce the claimed invention.

As discussed above, *Steele* fails to make out a *prima facie* case of unpatentability because it fails to show generation of each voltage as required by the challenged claims or that it adds any useful function beyond that described in *Lyke* alone.

Thus, Petitioners have failed to provide any compelling evidence that the USPTO erred in a manner material to the patentability of challenged claims. Moreover, Petitioners are precluded from adding new arguments or evidence to

buttress their unsustainable positions because the one-year bar date elapsed in February 2023 making institution inefficient. *See* EX. 2015.

Lastly, Petitioners *did not* challenge independent claim 6, which is currently asserted in the co-pending District Court litigation involving the same parties here. Accordingly, regardless of the outcome of this proceeding, this case will proceed to trial in Delaware.

Therefore, it would be an inefficient use of Board resources and the parties time to institute an *inter partes* review.

V. RESERVATION OF RIGHTS

Should the Board decide to institute an *Inter Partes* Review, Sentient reserves all rights to make additional arguments in and present claim constructions and evidence with its Patent Owner's Response. Sentient's silence on any particular claim or limitation at this time is not a concession that the Petition's discussion of that claim or limitation is properly based. Accordingly, Sentient reserves the right to submit additional or alternative arguments of patentability, and nothing in this Preliminary Response acts or should be construed to act as an admission, acquiescence, or estoppel on the merits of the Petition.

VI. CONCLUSION

For the reasons above, the Petition should be denied.

Dated: June 23, 2023

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), Counsel for Sentient Sensors LLC hereby certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(b). According to Microsoft Office Word 2010's word count, this document contains under 14,000 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Dated: June 23, 2023

Respectfully submitted,

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Sensors LLC*

CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, a true and correct copy of **PATENT OWNER'S PRELIMINARY RESPONSE AND EXHIBITS 2001-2018** are being served electronically on June 23, 2023, to the e-mail addresses of counsel below:

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Xilinx Inc. *et. al.* v. Sentient Sensors LLC