

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRO DEVICES, INC., and
ATI TECHNOLOGIES ULC,
Petitioner,

v.

SENTIENT SENSORS LLC,
Patent Owner.

IPR2023-00195
Patent 6,938,177 B1

Before JON M. JURGOVAN, CHRISTA P. ZADO, and
KEVIN C. TROCK, *Administrative Patent Judges*.

ZADO, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background*

Xilinx, Inc., Advanced Micro Devices, Inc., and ATI Technologies ULC (“Petitioner”) filed a Petition (Paper 2, “Pet.” or “Petition”) to institute an *inter partes* review of claims 1–5, 10–15, and 17–20 (“the challenged claims”) of U.S. Patent No. 6,938,177 B1 (Ex. 1001, “the ’177 patent”). Sentient Sensors, LLC (“Patent Owner”) timely filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

An *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Upon consideration of the current record, we determine that Petitioner has shown a reasonable likelihood that it would prevail in showing the unpatentability of at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. *Real Party-in-Interest*

Petitioner identifies itself as the only real party in interest. Pet. 67. Patent Owner identifies itself and Management Sciences Inc. as the only real parties in interest. Paper 4, 1.

C. *Related Matters*

The parties identify the following as related district court matters:
Sentient Sensors, LLC v. Xilinx, Inc., No. 22-cv-00173 (D. Del.) (filed Feb. 9, 2022) (active);

Blemel Technologies LLC v. National Instruments Corp., No. 15-cv-134 (E.D. Texas) (terminated by transfer to W.D. Texas);

Blemel Technologies LLC v. National Instruments Corp., No. 16-cv-1280 (W.D. Texas) (terminated by joint motion to dismiss with prejudice);

Sentient Sensors, LLC v. Microsemi Corp., No. 18-cv-121 (E.D. Texas) (terminated by joint motion to dismiss with prejudice);

Sentient Sensors, LLC v. Cypress Semiconductor Corp., No. 19-mn-1868 (D. Del.) (terminated by joint motion to dismiss with prejudice);
Pet. 67–68; Paper 4, 1.

D. The '177 Patent (Ex. 1001)

The '177 patent is titled “Multi-Chip Module Smart Controller” and relates generally to a multi-chip module (MCM) “capable of running multiple[] processes and having non-volatile storage for numerous monitoring/controlling applications.” Ex. 1001, code (54), 1:14–18. More specifically, the '177 patent relates to an Advanced Instrument Controller (AIC) (e.g., for space-based experimental test devices) that utilizes MCM design. *See generally id.* at 1:21–2:31. In particular, the '177 patent purports to improve upon the AIC described in U.S. Patent No. 6,148,399 (“Lyke”). *Id.*

The '177 patent states that Lyke’s AIC improved upon prior art by tightly coupling MCMs (which previously were not tightly coupled, according to the '177 patent). *Id.* at 1:44–2:8. “By tightly coupling the MCM more complex interactions between the components within the design are possible, thereby providing greater functional capability than would have been possible using a single integrated circuit.” *Id.* at 1:61–64. In addition, tightly coupling MCM’s “greatly reduced size, weight, and power consumption.” *Id.* at 2:1–3.

Lyke's AIC design had drawbacks, however, according to the '177 patent. One stated drawback is the incapacity to perform "parallel independent processes":

[T]here are several limitations to the design in [Lyke]. First, the AIC is not capable of performing independent parallel processes. Although the AIC does include a specialized [application-specific intended circuit] ASIC, it is controlled and clocked by the microprocessor. Accordingly, independent parallel processes are not possible.

Id. at 2:9–15.

Another stated drawback is that Lyke does not offer variable bit-depth when performing analog to digital ("A/D") conversion of signals:

[T]he AIC in [Lyke] performs A/D conversion at a 10 bit digitizing depth and does not offer variable conversion as may be required by different processes. For example, it may be preferred that some processes execute at a higher bit depth of 14 bits while some may be able to execute at a lower bit depth of 10 bits and still ensure accuracy.

Id. at 2:18–24.

The '177 patent attributes Lyke's alleged lack of independent processing to Lyke's "need for a resistive ASIC." *Id.* at 2:47–54. The '177 patent provides independent processing capability by, instead of relying on an ASIC, adding "a separately controllable FPGA [field programmable gate array] that acts as a parallel processor with internal or separate clock" that "adds a freely re-configurable and separately programmable multi-purpose digital system which can run independent of the microprocessor." *Id.*; *see also id.* at 7:35–41 ("The design of the present invention eliminates the need for an analog application-specific intended circuit (ASIC). Instead, [the] present invention utilizes an independently operable and programmable

FPGA which is used to implement many of the key instrumentation functions of an ASIC.”).

In addition to describing the above-discussed type of independent processing—wherein an FPGA runs independently from the microprocessor (Ex. 1001, 2:51–54, 4:39–44, 7:41–45)—the ’177 patent describes another type of “independent process” run by the FPGA—namely parallel processes within the FPGA that are independent of each other. *Id.* at 8:16–32, Fig. 2. Illustrated in Figure 2, and described in the patent, three independent processes A1, A2, and A3 may run in parallel within the FPGA. *Id.*

The FPGA in the ’177 patent is not limited to independent operation, and may alternatively operate under control of the AIC’s microprocessor. *Id.* at 4:39–44. Also, the FPGA may be clocked using: (1) the same voltage controlled oscillator (*i.e.*, clock) as the microprocessor, (2) a separate, external clock, or (3) no clock (wherein the FPGA operates at gate speeds). *Id.* at 4:49–52, 7:64–8:1; *see also id.* at 6:65–7:34 (describing internal clocking).

The ’177 patent provides a non-exhaustive, exemplary list of FPGA functions, which includes performing signal processing, acting as a cross-bar switching device to select analog or digital signals, performing signal conditioning and filtering, and monitoring functionality of the microprocessor, A/D and D/A conversions. *Id.* at 7:47–50, 7:59–63.

E. Challenged Claims

Petitioner challenges claims 1–5, 10–15, and 17–20 of the ’177 patent. Pet. 1. Claim 1 is reproduced below with annotations in brackets as set forth in the Petition.

1. [1.pre] An instrument controller comprising:

[1.1] a non-volatile memory storage component for program and data storage;

[1.2] a large volatile memory storage component for additional program and data storage;

[1.3] a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory; and

[1.4] at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations;

[1.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor;

[1.6] a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby generating digital inputs, and providing, the digital inputs to the processor;

[1.7] wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing; and

[1.8] wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the instrument controller.

Ex. 1001, 9:55–10:20.

F. Asserted Prior Art References and Declarations

Reference or Declaration	Date	Exhibit No.
U.S. Patent No. 6,148,399 (“Lyke”)	Nov. 14, 2000	Ex. 1003
Dehkordi, Peyman, et al., “Development of a DSP/MCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities,” <i>Proceedings: 1996 IEEE Multi-Chip Module Conference</i> ¹ (“Dehkordi”)	No later than Aug. 30, 2001 ²	Ex. 1004
Frantz, Gene A., et al., “The Texas Instruments TMS320C25 Digital Signal Microcomputer,” <i>IEEE Micro</i> ³ (“Frantz”)	No later than Dec. 1986 ⁴	Ex. 1005
Faura, Julio, “A Novel Mixed Signal Programmable Device with On-Chip Microprocessor,” <i>Proceedings of 1997 IEEE Custom Integrated Circuits Conference</i> ⁵ (“Faura”)	No later than Feb. 10, 1998 ⁶	Ex. 1006
U.S. Patent No. 5,663,734 (“Krasner”)	Sept. 2, 1997	Ex. 1007
U.S. Patent No. 4,279,020 (“Christian”)	July 14, 1981	Ex. 1008
U.S. Patent No. 5,675,824 (“Steele”)	Oct. 7, 1997	Ex. 1009
Declaration of Dr. Stan Shanfield (“Shanfield Dec.”)	Feb. 1, 2023	Ex. 1002
Declaration of June Ann Munford (“Munford Dec.”)	Feb. 2, 2023	Ex. 1011

¹ See the Declaration of June Ann Munford (Ex. 1011) ¶¶ 6–12, App. DEHKORDI01–06.

² See Ex. 1011 ¶ 13–14, App. DEHKORDI02–06 (field 008).

³ See Ex. 1011 ¶ 24–30, App. FRANTZ01–06.

⁴ See Ex. 1011 ¶¶ 31–32, App. FRANTZ02–06 (field 008).

⁵ See Ex. 1011 ¶¶ 15–20, App. FAURA01–05.

⁶ See Ex. 1011 ¶¶ 21–23, App. FAURA01–05 (field 008).

G. Asserted Grounds of Unpatentability

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1, 4	103	Lyke, Dehkordi, Frantz, Faura
2	103	Lyke, Dehkordi, Frantz, Faura, Krasner
3	103	Lyke, Dehkordi, Frantz, Faura, Christian
5, 10, 11, 13, 14, 15, 17, 19, 20	103	Lyke, Dehkordi, Frantz, Faura, Steele
12, 18	103	Lyke, Dehkordi, Frantz, Faura, Steele, Christian

II. ANALYSIS

A. Discretionary Denial of Institution under 35 U.S.C. § 325(d)

The Preliminary Response includes a section with the following heading: “Standard to Deny Institution Under Section 325(d).” Prelim. Resp. 14. Although, under this heading, Patent Owner recites the factors set forth in *Advanced Bionics*⁷ and *Becton, Dickinson*,⁸ Patent Owner does not provide any argument that we should deny institution. Prelim. Resp. 14–15. In other words, Patent Owner merely sets forth the standard, but does not argue for discretionary denial.

⁷ *Advanced Bionics, LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential) (“*Advanced Bionics*”).

⁸ *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential) (“*Becton Dickinson*”).

Petitioner prophylactically provides argument that discretionary denial under 325(d) is not warranted. Pet. 63–65. Petitioner points out, *inter alia*, that aside from the primary reference—Lyke—none of the references relied on in the Petition were before the PTO during examination. *Id.* at 64. Also, the claims were allowed in view of two limitations (*i.e.*, limitations [1.7] and [1.8]) for which the Examiner had not found prior art—the Petition introduces prior art that it asserts teaches these limitations. *Id.* at 64–65. In view of the foregoing, Petitioner argues the art presented here is not cumulative of art reviewed during Examination, there is no overlap between arguments, and the Examiner’s reasons for allowance (in which the Examiner had not found art teaching limitations [1.7] and [1.8]) are in error. *Id.*

However, Patent Owner has not asked us to consider discretionary denial, and we do not consider such here.

B. Level of Ordinary Skill

In determining whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). “The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

In determining the level of skill in the art, we consider the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom*

Accessories, Inc. v. Jeffrey-Allan Indus. Inc., 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner contends “[t]he POSITA of the ’177 patent would have been a person with a Bachelor’s degree in Electrical Engineering or Computer Engineering, or a related field, and at least two years of experience related to the design or development of multi-chip modules operating as instrument controllers.” Pet. 7 (citing Ex. 1002 ¶¶ 24–26). Patent Owner does not provide a contention as to the level of ordinary skill in the art.

Based on the record presented, including our review of the ’177 patent and the types of problems and solutions described in the patent and the cited prior art, we adopt Petitioner’s assessment of the level of ordinary skill in the art, but without the qualifier “at least” before the words “two years,” and apply it for purposes of this Decision. To the extent the parties disagree as to the level of ordinary skill in the art, the parties may address the issue in their papers during trial and explain, for example, how a different definition would impact the obviousness analysis of the challenged claims.

C. Claim Construction

Pursuant to 37 C.F.R. § 42.100(b), we apply the claim construction standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Under *Phillips*, claim terms generally are given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and even extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic

evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17.

Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (in the context of an *inter partes* review, applying *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Neither party proposes the construction of any claim terms at this time. However, the parties’ preliminary arguments potentially raise questions as to the proper interpretation of the phrase “gate array coupled to the processor and configured to run independent processes in parallel with the processor,” as recited in limitation [1.5] of claim 1.

In particular, at least two potential questions arise: (1) the meaning of the term “independent process,”⁹ and (2) what the “process” must be independent of (*e.g.*, the processor, or each other).

1. “independent process”

Neither lexicography nor claim disavowal dictates our departure from applying the ordinary and customary meaning of “independent process” here. *GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) (explaining that departure from the ordinary and customary meaning is appropriate only in two circumstances: lexicography and disavowal). Therefore, at this preliminary stage “independent process” is

⁹ Claim 1 recites “independent processes,” which is the plural form of “independent process.” We use the phrases “independent process” and “independent processes” to refer to the same claim term, wherein one phrase is in the singular form and the other is in the plural form.

accorded its ordinary and customary meaning. *See Phillips*, 415 F.3d at 1312–17. As noted above, the parties do not provide positions concerning the ordinary and customary meaning of “independent process,” but their arguments potentially raise issues.

As to Lyke, Petitioner argues that because the FPGA retrieves the processes (*i.e.*, computer program code, also referred to as configuration information) from non-volatile memory (*i.e.*, from something that is not the processor), the processes run separately from those running on the processor. Pet. 27–28. Patent Owner responds that the FPGA retrieving program instructions from somewhere other than the processor does not, alone, mean the programs “run independent parallel operations.” Prelim. Resp. 23. Patent Owner also argues that the FPGA acts as a slave to the processor, and therefore does not run independent parallel processes. *Id.* at 23–24.

As to Dehkordi, Petitioner asserts multiple examples of independent processes running on the FPGA. *Id.* at 28–29. First, Petitioner asserts that the portion of the FPGA configured to perform multi-bus arbitration runs independently of the processor, because the arbitration (*i.e.*, management of data flow) occurs separately from computations occurring on the processor. *Id.* at 28. Petitioner identifies the following additional processes as being independent: analog to digital conversion, power management, and digital signal processing. *Id.* at 28–29. Finally, Petitioner provides an argument similar to that for Lyke—namely, the processes retrieved from RAM memory may come from outside the multichip module, and therefore would have been understood as running separately from processes run on the processor. *Id.* at 29.

Patent Owner responds that because the FPGA and processor are coupled through a common control bus, they run on a “common clock signal,” and “no independent processes are possible.” Prelim. Resp. 27. According to Patent Owner, because the FPGA and processor share a common control bus, the FPGA necessarily is a slave to (*i.e.*, dependent on) the processor. *Id.*

Although neither party offers an explicit construction, it appears that Petitioner understands the term “independent process” indicates a process that runs separately from those that run on the processor. *See, e.g.*, Pet. 28 (arguing the processes run on the FPGA run “separately” from processes running on the processor); *id.* at 29 (arguing the FPGA programming is “separate” to the program running on the processor).

Patent Owner’s arguments suggest the term “independent process” requires the components running the processes (*i.e.*, processor and FPGA) to run on separate clocks. *See, e.g.*, Prelim. Resp. 27 (arguing that running on a common clock signals indicates the FPGA is dependent on the processor). Patent Owner’s arguments also suggest that when acting as a slave to the processor, FPGA processes are not independent of the processor.¹⁰ *Id.* at 23–24, 27.

However, neither party articulates a claim construction to support their arguments.

¹⁰ Patent Owner does not provide any insight as to whether an FPGA runs independent parallel processes when acting as a master to the CPU, or when operating in peripheral modes (synchronous and/or asynchronous). For additional FPGA modes of operation other than slave, *see, e.g.*, Ex. 1014, 6–46.

For reasons discussed below, *infra* Sec. II.G.1–2, regardless of interpretation we find the evidence sufficient to support institution, and we refrain from preliminarily interpreting the term “independent process” prior to the parties providing evidence and argument. However, our determination is preliminary only. We encourage each party to provide their interpretation of the term “independent process,” and explain how their interpretation supports their respective position that the prior art teaches/does not teach this feature.

In presenting their interpretations, the parties are reminded to identify specific evidence from the intrinsic record, and may offer extrinsic evidence if appropriate. *See* 37 C.F.R. §§ 42.22–23 (providing that a petition, motion, opposition, reply, and sur-reply must include a detailed explanation of the significance of evidence); *Phillips*, 415 F.3d at 1312–17 (explaining that claims are to be construed in the context of the specification, the prosecution history, other claims, and extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises). The parties also are reminded that expert testimony as to the understanding an ordinarily skilled artisan would have had concerning the meaning of this term should be supported by corroborating evidence. *See* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

By way of example, the *Microsoft Computing Dictionary*¹¹ defines “process” as “[a] program or part of a program; a coherent sequence of steps

¹¹ MICROSOFT COMPUTING DICTIONARY (Microsoft Press, 5th ed. 2002) (“*Microsoft Computing Dictionary*,” Exhibit 3002).

undertaken by a program.” Ex. 3002, 423. *Computer Organization and Architecture Designing for Performance*¹² states that the concept of “process” first was used by designers of Multiplexed Information and Computing Services (Multics), and further states that once a program is admitted to a system for processing, it becomes a process. Ex. 3003, 234–235. *Computer Architecture: A Quantitative Approach*¹³ similarly states that multiprogramming led to the concept of a process: “[t]he invention of multiprogramming, where a computer would be shared by several programs running concurrently, led to new demands for protection and sharing among programs . . . Multiprogramming leads to the concept of a *process*.”

Ex. 3004, 469. *Computer Architecture* states further that

a process is a segment of code that may be run independently, and that the state of the process contains all the information necessary to execute that program on a processor. In a multiprogrammed environment, where the processors may be running independent tasks, each process is typically independent of the processes on other processors.

Id. at 530.

However, the parties may wish to provide additional or alternative understandings, supported by evidence.

¹² WILLIAM STALLINGS, COMPUTER ORGANIZATION AND ARCHITECTURE DESIGNING FOR PERFORMANCE, (Prentice Hall 4th ed. 1996) (“*Computer Organization*,” Ex. 3003).

¹³ JOHN L. HENNESSY & DAVID A. PATTERSON, COMPUTER ARCHITECTURE: A QUANTITATIVE APPROACH (MORGAN KAUFMANN PUBLISHERS 3rd ed. 2003) (“*Computer Architecture*,” Ex. 3004).

2. *What the processes must be “independent” of*

The parties appear to assume that the phrase “configured to run independent processes in parallel with the processor” means that processes run on the FPGA must run independently of the processor. *See, e.g.*, Prelim. Resp. 27 (arguing the prior art FPGA is dependent on the processor); *see also, e.g.*, Pet. 28 (arguing the processes run on the FPGA run separately from those run on the processor). However, grammatically speaking, the claim language imposes no such requirement. The claim language states that “independent processes” run in parallel with the processor, but is silent as to what the processes are “independent” of. The claim’s silence leaves open at least two possibilities: (1) the processes are independent of the processor, and (2) the processes are independent of each other. Both interpretations find support in the ’177 patent.

As to (1), the ’177 patent discloses, for example, “[t]he FPGA . . . adds a freely re-configurable and separately programmable multi-purpose digital system which can run independent of the microprocessor.” Ex. 1001, 2:51–54. The ’177 patent also discloses, *e.g.*, “[t]he microprocessor is further coupled to a [FPGA] . . . [i]n a preferred embodiment, the FPGA . . . may operate either under control of the microprocessor (for example as a co-processor) or, may be operated independently.” *Id.* at 4:39–44.

As to (2), in some embodiments of the ’177 patent the FPGA is not independent of the processor, but rather operates under its control. Ex. 1001, 4:40–44 (disclosing that processes run on the FPGA “may operate either under the control of the microprocessor (for example as a co-processor) or, may be operated independently).”

Moreover, the '177 patent uses the term “independent” to refer to processes within the FPGA that are independent of each other. With regard to Figure 2, the '177 patent illustrates the FPGA running three processes A1, A2, and A3 independently of each other within the FPGA:

The present invention can use the parallel processing of the FPGA to re-route a subset of interconnections . . . FIG. 2 illustrates the concept . . . As shown, gates X1, X2 and X3 [within the FPGA] are configured to route the input node at A to anyone of three independent processes A1–A3. The processes are independent configurations of a subset of gates within the FPGA.

Ex. 1001, 8:16–32. That is, the “independent processes” the FPGA is “configured to run” are processes that are independent of each other.

The parties should clarify what the processes run on the FPGA must be independent of, e.g., each other or the processor, and support their respective positions with evidence.

D. Patentability Challenges

1. Principles of Law: Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103 if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary

considerations.¹⁴ *See Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

2. *Relevant Prior Art*

a) *Lyke (Ex. 1003)*

Lyke is U.S. Patent No. 6,148,399, issued November 14, 2000, titled “Advanced Instrument Controller Statement of Government Interest.” Ex. 1004, code (11), (45), (54).

Lyke “generally relates to multi-chip module (MCM) microcircuits, and more specifically to a compact (few-chip) MCM electronics control system that exploits the tight coupling of components from non-similar processes and non-volatile storage for numerous monitoring/controlling applications under harsh conditions.” *Id.* at 1:14–19.

With regard to, e.g., space-based environments, Lyke seeks to improve upon previous MCM designs for providing controller and acquisition features, which generally were “bulky, power hungry, and expensive.” *Id.* at 1:21–30. Lyke achieves this end by “combin[ing] the controller and acquisition functions [of previous designs] into a single, tightly coupled MCM design.” *Id.* at 1:24–26. Lyke explains that tightly coupled MCMs refer to MCMs whose components possess one or more of the following features:

- (1) more input/output (I/O) terminal contacts than is normally consistent with a discrete implementation, (2) lower capacitive drive in input circuits than is normally consistent with a discrete implementation, (3) I/O terminals in locations inconsistent with

¹⁴ The current record does not present or address any objective evidence of nonobviousness.

standard integrated circuits (IC)s, (4) I/O circuitry with reduced or eliminated electrostatic discharge protection structures.

Id. at 1:29–38.

According to Lyke, “[b]y tightly coupling the MCM, more complex interactions between the components within are possible, introducing a design with similar physical appearance and size of a packaged integrated circuit, but with greater functional capability than possible with a single integrated circuit.” *Id.* at 1:38–43.

Lyke implements its tightly coupled MCM design within an Advanced Instrument Controller (AIC). *Id.* at 1:18–66. “The functional innovations within the [AIC], being a tightly coupled MCM, are based on the ensemble core and I/O functions and the way they are used.” *Id.* at 2:6–9. “The AIC combines a central processing unit, an analog application-specific integrated circuit (ASIC), a resistor ASIC, and volatile and non-volatile memory storage systems on a single tightly coupled MCM” in order to achieve “ultra-low power requirements, extremely small size and weight, versatile functionality, and the ability to operate in extreme environments.” *Id.* at 3:4–11. Figure 1, reproduced below, illustrates an AIC using tightly coupled MCM design.

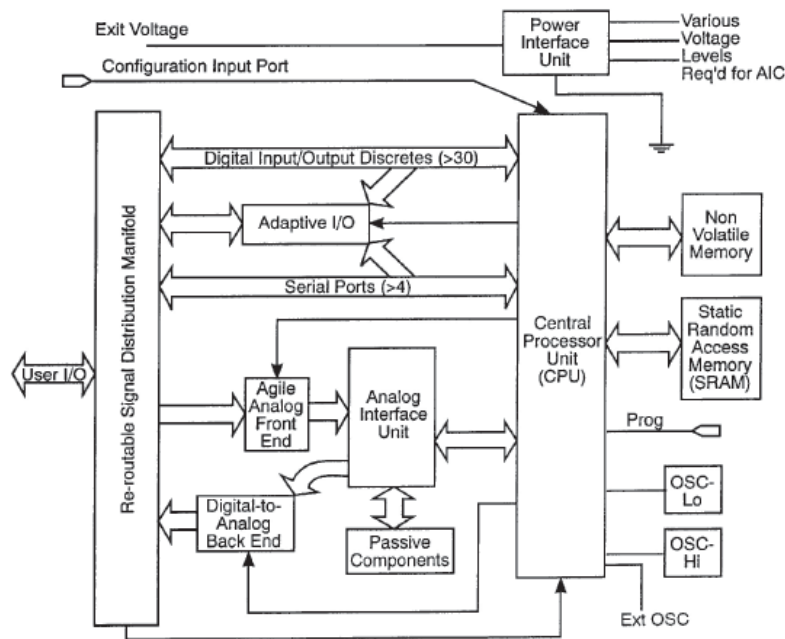


Fig. 1

*Figure 1 of Lyke is a block diagram schematic of an AIC.
 Ex. 1003, 2:36.*

Figure 1 of Lyke is a block diagram schematic of an AIC. *Id.* at 3:12–13. As shown in Figure 1 and described in Lyke, the AIC includes, *inter alia*, non-volatile memory for program and data storage (*id.* at 3:16, 4:14–15), large volatile memory (i.e., SRAM) (*id.* at 3:17, 3:66–67, 4:34–41), central processing unit (CPU) coupled to both the non-volatile and volatile memories (*id.* Fig. 1), two internal oscillators operating at two different frequencies (Hi and Lo) coupled to the CPU (*id.* at 3:19–20, 4:42–46), and multiple analog to digital converters (*see, e.g.,* 16 internal A/D channels with 12-bit resolution (*id.* at 4:64), description of analog to digital converters (*id.* at 5:18–24)).

Lyke employs a reprogrammable analog ASIC “to implement many of the key instrumentation functions,” including 32 external analog inputs, 8

interpedently programmable digital to analog converter channels with 10-bit resolution, and 16 internal analog to digital converter channels with 12-bit resolution. *Id.* at 4:58–65, 5:6–7. Lyke’s AIC also includes a resistive ASIC “to eliminate over 50 individual resistors.” *Id.* at 5:48–51.

Lyke states that the matter set forth in the description and drawings “is offered by way of illustration and not as a limitation,” and “[o]ther variations to the current design include” “RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through a downloading mechanism involving AIC’s internal CPU and access of the non-volatile memory.” *Id.* at 8:48–59.

b) Dehkordi (Ex. 1004)

Dehkordi is a paper titled, “Development of a DSP/MCM Subsystem Assessing Low-volume, Low-cost MCM Prototyping for Universities,” from *Proceedings: 1996 IEEE Multi-Chip Module Conference*.¹⁵

Dehkordi “discusses the design and development of a general-purpose DSP subsystem packaged in a multichip module.” Ex. 1004, 1.¹⁶ Dehkordi states that IBM had utilized MCM packaging for high volume, high cost products for years, but that low cost, low volume services historically had been limited. *Id.* However, according to Dehkordi, a tremendous push from Advanced Project Agency (ARPA) for widespread usage of MCM technology led to increases in services. *Id.* Dehkordi states that, as part of an ARPA project, the authors exercised the availability of MCM technology

¹⁵ See Munford Dec. (Ex. 1011) ¶¶ 6–14, App. DEHKORDI01–06.

¹⁶ For consistency with the parties, we use the pagination provided on the document by Petitioner rather than the IEEE’s original pagination.

for universities by designing and implementing an MCM subsystem. *Id.* Their implementation is a “design representing a typical application of a MCM, including a processor, memory, and gate-array.” *Id.* The design includes a “complete DSP [digital signal processing] subsystem based on the Motorola 96002 32-bit floating point DSP processor.” *Id.* The MCM also includes SRAM, EEPROM, and a Xilinx 4010 field programmable gate array (FPGA). *Id.* According to Dehkordi, the MCM is “designed to exploit the multi-processing capability of the 96002.” *Id.* The FPGA “is primarily a hardware pre-processor of incoming data but also provides other generic functions required for implementation of the entire subsystem.” *Id.* Figure 1 of Dehkordi, reproduced below, is illustrative.

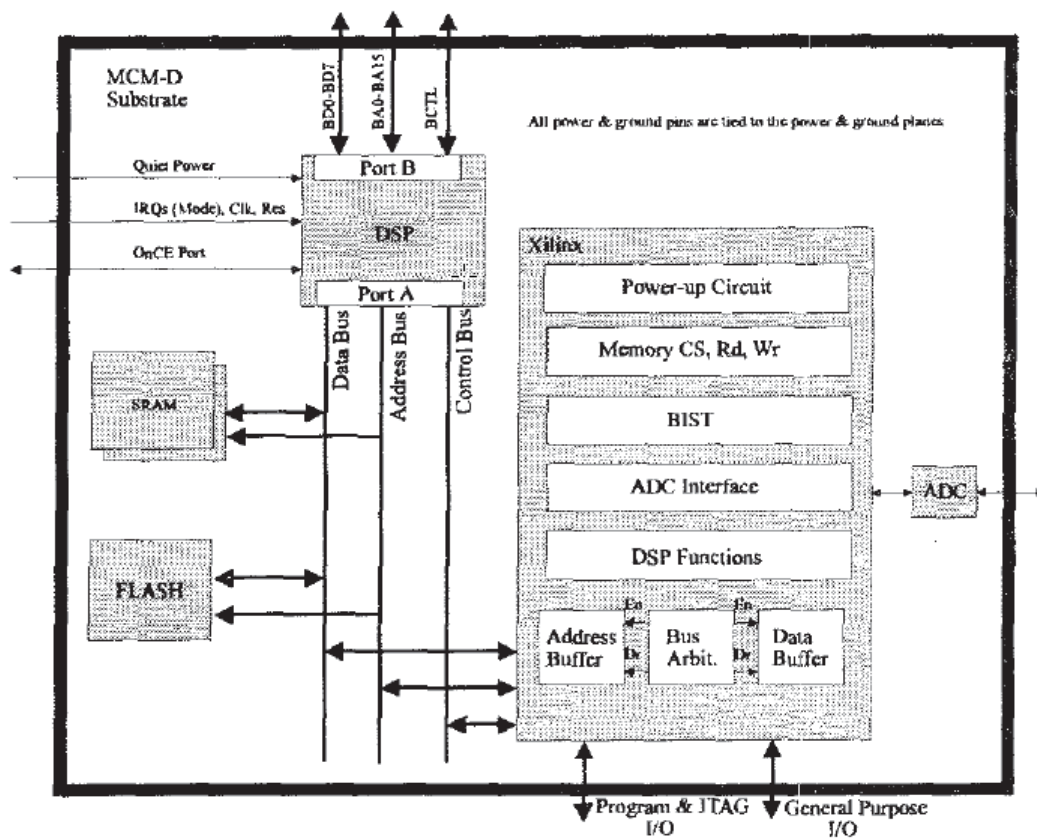


Figure 1 of Dehkordi is a block diagram of the DSP subsystem.
Ex. 1004, 1.

Figure 1 of Dehkordi illustrates a MCM substrate that includes a DSP coupled to SRAM and FLASH memories, and a Xilinx FPGA. *Id.* The DSP, SRAM, FLASH, and FPGA are shown as communicating over the same bus. *Id.* In addition, the FPGA includes means to communicate externally via JTAG I/O and general purpose I/O ports. *Id.*

Dehkordi also addresses the issue of testing their MCM design. Dehkordi states that testing and fault isolation are challenging due to the small feature sizes of MCM. *Id.* at 3. Dehkordi states another challenge is that the DSP, unlike the FPGA, does not support JTAG testing. However, according to Dehkordi, TAG testing of both the DSP and FPGA is possible because “[t]he DSP supports a serial emulation port,” which when “connected to the module pins along with the FPGA TAP port,” supports TAG. *Id.* Dehkordi states further that:

The FPGA has a RAM-based configuration where the configuration may come from outside the module. A portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the module. The FPGA can easily be reconfigured to route these lines to the module pins for possible probing and debussing during testing. The DSP has a dual data and address port architecture in which the second port was also connected to the module pins for enhanced multi-processing and testing. Testing procedures are being constructed at the time of this publication.

Id.

c) Additional References

Petitioner’s grounds of unpatentability rely on additional references. Pet. 1, 8–63. However, at this stage their descriptions are not pertinent to the issues raised by the parties, and we do not summarize them here.

E. Overview

Petitioner relies on the combination of Lyke, Dehkordi, Frantz, and Faura in challenging the patentability of claims 1–5, 10–16, and 17–20—all claims challenged in this proceeding. Pet. 1. For claims 2, 3, 5, 10–16, and 17–20, Petitioner relies on additional references. *Id.*

We first address independent claim 1. In its Preliminary Response, except as addressed below, *infra* Sec. II.I, Patent Owner does not separately address Petitioner’s evidence or arguments directed to the remaining challenged claims, apart from those issues argued with respect to claim 1. *See* Prelim. Resp. 20–35.

F. Background

Petitioner relies on Lyke as a primary reference. As discussed above (*supra* Sec. I.D), the ’177 patent states that it improves upon the AIC disclosed in Lyke. *See, e.g.*, Ex. 1001, 1:21–2:31. Patent Owner does not dispute that Lyke discloses several of the features recited in claim 1. *See* Prelim. Resp. 20–35. In addition, during the prosecution of the ’177 patent, the Examiner relied on Lyke as a primary reference in rejecting a claim containing all but the last two limitations of claim 1.¹⁷ Ex. 1010, 56–57.¹⁸ The Examiner found that Lyke teaches limitations [1.1] through [1.6], except

¹⁷ Issued claim 1 essentially is originally filed dependent claim 3, rewritten in independent form. *See* Ex. 1010, 60 (office action objecting to originally filed claim 3, indicating it would be allowable if rewritten in independent form); *see also id.* at 42 (applicant remarking, *inter alia*, that originally filed claim 3 is amended to be independent); *see also id.* at 33 (amending originally filed claim 3).

¹⁸ For the file history (Exhibit 1010), which is a multi-document exhibit, we use the pagination at the bottom center of each page.

for the embedded memory recited in limitation [1.3] and the gate array recited in limitation [1.5]. *Id.* at 56–58. For these recitations, the Examiner relied on DaCosta¹⁹ and Cloutier,²⁰ respectively. *Id.* at 57–58. As a result, the Examiner found that claim 1, without limitations [1.7] and [1.8], would have been obvious. *Id.* at 56–58.

During prosecution, the patent applicant did not challenge the Examiner’s findings. *See id.* at 42–46. As such, the applicant did not dispute that claim 1, without limitations [1.7] and [1.8], is unpatentable as obvious over Lyke combined with two additional references.

In the instant proceeding, Petitioner relies on Lyke for much of the same limitations as the Examiner, with a few exceptions. For the embedded memory recited in limitation [1.3], Petitioner relies on Frantz, whereas the Examiner relied on DaCosta. Pet. 24–26; Ex. 1010, 57–58. For the gate array recited in limitation [1.5], Petitioner relies on Lyke and Dehkordi, whereas the Examiner relied on Cloutier. Pet. 27–29; Ex. 1010, 58. Finally, as to limitation [1.6], Petitioner relies on Lyke, as did the Examiner, but Petitioner provides an alternative argument that Faura additionally teaches this limitation. Pet. 29–31; Ex. 1010, 57.

As to limitations [1.7] and [1.8], the Examiner did not find these to be taught in the prior art. Ex. 1010, 60. For these limitations, Petitioner relies on Dehkordi. Pet. 33–34. The table below summarizes the Examiner’s and Petitioner’s respective positions.

¹⁹ U.S. Patent Publication No. 2002/0129191 A1 (“DaCosta”) (Exhibit 1041).

²⁰ U.S. Patent No. 5,892,962 (“Cloutier”) (Exhibit 1040).

Claim Limitation	Reference(s) relied on by Examiner	Reference(s) relied on by Petitioner
[1.pre] An instrument controller comprising	Lyke	Lyke
[1.1] a non-volatile memory storage component for program and data storage	Lyke	Lyke
[1.2] a large volatile memory storage component for additional program and data storage	Lyke	Lyke
[1.3] a processor coupled to both the non-volatile memory storage component and the large volatile memory storage components, the processor capable of high-frequency and low-frequency operations and having an embedded memory for storing an initialization program that enables the processor to start up processing without first retrieving a program from the non-volatile memory	DaCosta (for “embedded memory” as claimed) Lyke for remainder of limitation	Franz (for “embedded memory” as claimed) Lyke for remainder of limitation
[1.4] at least two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations	Lyke	Lyke
[1.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor	Cloutier	Dehkordi Lyke (each reference separately teaches limitation)
[1.6] a plurality of analog-to-digital converters for receiving a plurality of analog inputs, digitizing the analog inputs at one of at least two possible bit depths, thereby	Lyke	Lyke Faura (separately teaches

Claim Limitation	Reference(s) relied on by Examiner	Reference(s) relied on by Petitioner
generating, and providing, the digital inputs to the processor		“plurality of [A/D] converters”)
[1.7] wherein a first portion of the gates in the field programmable gate array is configured to perform signal processing	Did not assert prior art	Dehkordi
[1.8] wherein a second portion of the gates in the field programmable gate array is configured to operate as a signal distribution matrix for rerouting signals within the instrument controller	Did not assert prior art	Dehkordi

In the Preliminary Response, with regard to claim 1, Patent Owner disputes only whether Lyke and Dehkordi teach the gate array recited in limitation [1.5].

G. Obviousness of Claim 1

Petitioner asserts unpatentability under 35 U.S.C. § 103 of claim 1 as obvious over the combination of Lyke, Dehkordi, Franz, and Faura. Pet. 12–34.

Discussed further below, Patent Owner argues that Lyke and Dehkordi do not teach the gate array recited in limitation [1.5]. Prelim. Resp. 20–35. Patent Owner does not otherwise provide arguments or evidence regarding this ground of unpatentability. *See id.*

We have considered Petitioner’s evidence and arguments, including the relevant testimony of Dr. Shanfield, as well as the evidence and arguments presented by Patent Owner. Based on this preliminary record, we

determine Petitioner has demonstrated a reasonable likelihood that claim 1 is unpatentable under 35 U.S.C. § 103 as obvious over the combination of Lyke, Dehkordi, Franz, and Faura.

We first address limitation [1.5]. In so doing, we highlight the following; however, these highlights should not be interpreted as limiting our preliminary findings and determinations.

1. Lyke

Petitioner provides evidence and arguments that Lyke teaches the following limitation of claim 1:

[1.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor.

Pet. 27–28.

Petitioner relies on Lyke’s teaching that the disclosed MCM may include, in other variations, field programmable gate array(s). *Id.*

Specifically, Lyke discloses:

The matter set forth in the foregoing description and accompanying drawings is offered by way of illustration only and not as a limitation. Other variations to the current design include . . . RAM-based field programmable gate array(s) [FPGAs] interfaced internally within the AIC and configured automatically through a downloading mechanism involving the AIC’s internal CPU and access of the non-volatile memory.

Ex. 1003, 8:48–59.

As to the recitation that the field programmable gate array is coupled to the processor, Dr. Shanfield testifies that it would have been understood that the FPGA taught in Lyke is coupled to Lyke’s processor because Lyke’s FPGA is configured by downloading configuration information from the

processor. Ex. 1002 ¶ 82; Ex. 1003, 8:55–58 (stating the FPGA is configured automatically through a downloading mechanism involving AIC’s internal CPU). Dr. Shanfield further testifies that coupling an FPGA to a processor was well known in applications such as those disclosed in Lyke. Ex. 1002 ¶ 82. In support of this testimony, Dr. Shanfield relies on Halverson.²¹ *Id.* (citing Ex. 1025, 2:50–52, 27:11–14). Patent Owner does not appear to contest that Lyke’s FPGA is coupled to the processor.

As to the recitation that the field programmable gate array is configured to run independent processes in parallel with the processor, Petitioner argues that, as taught in Lyke, configuring a FPGA from non-volatile memory—i.e., retrieving program code from something that is not the processor—would have indicated that such programs run independently of the program code running separately on the processor. Pet. 27–28. Supporting this argument, Dr. Shanfield explains that configuring a FPGA to run processes that run independently in parallel with a processor was typical in the relevant time frame. Ex. 1002 ¶ 83. To corroborate his testimony, Dr. Shanfield relies on both Kostarnov²² and Halverson. *Id.* For example, regarding independence between a CPU and FPGA, Kostarnov discloses “[t]he CPU and FPGA execute as two independent execution units.” Ex. 1036, 4, *quoted in* Ex. 1002 ¶ 83. As to parallel processes, Halverson states “the concept of parallel processing and the use of field programmable gate arrays is not new.” Ex. 1025, 2:27–32, *quoted in* Ex. 1002 ¶ 83.

²¹ U.S. Patent No. 5,574,930, Exhibit 1025 (“Halverson”).

²² Kostarnov, Igor, et al., “A Reconfigurable Approach to Low Cost Media Processing,” Appliance Computing Dept., Hewlett-Packard Laboratories, Exhibit 2036 (“Kostarnov”).

According to Dr. Shanfield, an ordinarily skilled artisan would have “readily recognized and been prompted to pursue the known benefits of using an FPGA to run independent processes in parallel with the processor . . . and would have had a reasonable expectation of success in doing so.” Ex. 1002 ¶ 83.

Kostarnov appears to support Petitioner’s position. Kostarnov relates to providing systems for processing high performance media algorithms such as video decompression. Ex. 1036, 1. Kostarnov explains that media algorithm processing by a CPU may be accelerated by using, e.g., application-specific integrated circuits (ASICs), digital signal processors (DSPs), and application-specific instruction processors (ASIPs). *Id.* However, these acceleration techniques suffered from various drawbacks including the inability to program and/or reprogram the accelerators, according to Kostarnov. *Id.* at 1–2. Kostarnov, therefore, proposes a FPGA accelerator as an improvement, explaining that unlike previous accelerators, a FPGA can be reprogrammed. *Id.* Kostarnov discloses three modes of interaction between the CPU, FPGA, and memory. Pertinent here, Kostarnov discloses a datapath mode (relied on by Petitioner and Dr. Shanfield, as discussed above) in which the CPU and FPGA operate as two independent execution units. *Id.* at 4. Kostarnov explains that datapath mode provides the best potential performance, and is “particularly effective when the FPGA can process a large independent part of the algorithm without the need for complex control and synchronization with the CPU.” *Id.* at 11. Because when in datapath mode the CPU and FPGA run as independent execution units, and because the FPGA can process portions of the algorithm without need for complex control and synchronization with the

CPU, we are persuaded sufficiently at this stage that Kostarnov teaches or suggests running independent processes in parallel with the CPU.

Patent Owner responds that Petitioner's reliance on Lyke should be accorded little to no weight on the grounds that Lyke was considered during prosecution. Prelim. Resp. 21–26. In support of this argument, Patent Owner asserts that the '177 patent discloses details of Lyke's AIC, disclosing that the AIC "suffers from several deficiencies, such as its *inability to run parallel and independent processes.*" *Id.* at 21. According to Patent Owner, "[t]his theme is repeated throughout the '177 Patent's specification." *Id.* at 22. Patent Owner further points out the Examiner's finding that "Lyke fails to disclose . . . a field programmable gate array coupled to the processor for parallel processing." *Id.* at 9, *quoting* Ex. 1010, 57; *see also id.* at 22. In light of these considerations, Patent Owner argues that the Examiner did not overlook Lyke's teachings relating to field programmable gate arrays, and urges we should not consider the teachings here. *Id.* at 22.

We disagree that Petitioner's evidence and arguments concerning Lyke should be given little to no weight. In particular, the '177 patent does not mention, or otherwise acknowledge, Lyke's disclosure that other variations of the MCM may include a FPGA. In asserting Lyke cannot run independent processes in parallel with the processor, the '177 patent considers Lyke's ASIC. In particular, Lyke discloses:

[T]here are several limitations to the design in [Lyke]. First, the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible.

Ex. 1001, 2:9–15;

[T]he circuitry of the present invention eliminates the need for a resistive ASIC. Instead, the present invention adds a separately controllable FPGA that acts as a parallel processor with internal or separate internal clock. The FPGA . . . adds a freely re-configurable and separately programmable multi-purpose digital system which can run independent of the microprocessor.

Id. at 2:47–55; and

The design of the present invention eliminates the need for an analog application-specific intended circuit (ASIC). Instead, present invention utilizes an independently operable and programmable FPGA which is used to implement many of the key instrumentation functions of an ASIC.

Id. at 7:35–41.

As these excerpts evince, the ‘177 patent’s statements regarding inability to perform parallel independent processes refer to ASICs in Lyke’s AIC. There is no discussion of the FPGA disclosed in Lyke. Indeed, there is no mention in either the ‘177 patent or the prosecution history of Lyke’s disclosure of utilizing a FPGA in “other variations” of the AIC, much less discussion of whether a FPGA implemented in Lyke’s AIC would have been capable of performing parallel independent processes. In view of the above, we find no evidence that either the patent applicant or Examiner considered Lyke’s disclosure of a FPGA in asserting or finding that Lyke’s AIC could not run independent processes in parallel with the processor.²³

²³ In view of the above, the parties may wish to further develop the record concerning the ‘177 patent’s assertion that the ASIC in Lyke cannot run independent parallel processes, including technical discussion of the rationale as to why an ASIC would not have been capable of independent parallel processing. In so doing, it would be helpful for the parties to specify (1) whether and which arguments refer to the resistive ASIC (Ex. 1003,

Having addressed Patent Owner’s argument that we should accord little to no weight to Lyke, we now turn to Patent Owner’s substantive arguments concerning Lyke.

First, Patent Owner argues it is not necessarily the case that Lyke’s FPGA runs independently in parallel with the processor simply by virtue of having logic configured from non-volatile memory. Prelim. Resp. 22–23 (arguing that the FPGA retrieving program instructions from somewhere other than the processor does not, alone, mean the programs “run independent parallel operations”). Patent Owner’s argument also applies in the other direction. That is, no evidence has been presented showing that the processes configured on the FPGA do not run separately from those run on the processor. The parties may wish to further develop the record concerning why a skilled artisan would have understood that the processes run on Lyke’s FPGA would have been/not been independent (based on proper interpretation of this term). That said, Petitioner does not rely solely on Lyke’s disclosure of configuring FPGA logic from non-volatile memory. As discussed above, Petitioner relies also on the knowledge of an ordinarily skilled artisan, as evinced by Kostarnov and Halverson. Pet. 28 (citing Ex. 1036, 4; Ex. 1025, 2:1–31).

Patent Owner dismisses Kostarnov, selectively relying only on teachings of a FPGA operating as a slave, while neglecting teachings of the FPGA and processor operating as “independent execution units.” Prelim. Resp. 23–24. Specifically, Patent Owner asserts Kostarnov does not teach

5:49–50), to the analog ASIC (*id.* at 4:58–5:16, 5:50–51), or to both ASIC’s, and (2) whether the rationale does/does not apply to a FPGA implemented in Lyke’s MCM and why/why not.

that it was well known to run parallel independent processes, arguing that the FPGA in Kostamov acts as a slave to (i.e., is controlled by) the CPU. *Id.* In so doing, Patent Owner selectively reproduces two figures in Kostamov that illustrate two modes of operation—i.e., functional unit mode and lockstep mode—in which instructions flow from the CPU to the FPGA. *Id.*; Ex. 1036, 3–4. However, Patent Owner omits a third disclosed mode of operation—i.e., datapath mode—which is the mode of operation upon which Dr. Shanfield’s testimony relies, as discussed above. Ex. 1002 ¶ 83 (citing Ex. 1036, 4). Because Patent Owner’s arguments neglect the teachings upon which Dr. Shanfield and Petitioner rely, and instead are based on disclosure of unrelated modes of operation, the arguments are not responsive and do not undermine either Petitioner or Dr. Shanfield.

Touching upon the same theme—i.e., teachings of FPGA’s acting in slave mode to a CPU—Patent Owner further argues that the “most popular configuration” of the Xilinx XC4000 series of FPGAs is serial slave mode. Prelim. Resp. 24. This argument is unavailing because, as with the Kostamov arguments, Patent Owner relies selectively on disclosure of a slave mode, while omitting disclosure of other modes. Specifically, Patent Owner relies on a statement in a Xilinx data sheet for XC4000E and XC4000X series FPGAs regarding configuration modes, namely that Slave Serial mode “is the most popular configuration mode.” *Id.*, citing Ex. 1014, 6-45. Patent Owner neglects disclosure that the XC4000E and XC4000X series FPGAs have six configuration modes, of which only one of the six modes is Slave Serial. Ex. 1014, 6-46. Three of the modes are Master modes and two are Peripheral modes (synchronous and asynchronous). *Id.* The data sheet describes all of the modes at length. *Id.* at 6-46–6-47. For

the foregoing reasons, Patent Owner's arguments regarding the Xilinx data sheet do not undermine Petitioner's arguments.

Finally, Patent Owner argues that Halverson "does not disclose *independent parallel processing* but rather discloses *just parallel processing*." Prelim. Resp. 25. This argument is inapposite because, although Dr. Shanfield relies on Halverson for teaching parallel processing, he does not appear to rely on Halverson for teaching *independent parallel processing*. Ex. 1002 ¶ 83.

Based on this preliminary record, we determine that Petitioner has demonstrated sufficiently that Lyke meets the recited limitation.

2. *Dehkordi*

Petitioner provides evidence and arguments that Dehkordi teaches the following limitation of claim 1:

[1.5] a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and configured to run independent processes in parallel with the processor.

Pet. 28–29.

Petitioner relies on Dehkordi's teaching of a Xilinx 4010 FPGA coupled with Motorola 96002 DSP processor within a MCM. Pet. 28–29; *see* Ex. 1004, 1 (describing implementing the DSP processor and FPGA on a MCM). As can be seen in Figure 1 of Dehkordi, the FPGA is coupled to the DSP processor. Ex. 1004, 1; *see also* reproduction and discussion of Dehkordi's Figure 1, *supra* Sec. II.D.2.b. Patent Owner does not appear to contest that the two are coupled.

As to the gate array being configured to run independent processes in parallel with the processor, Petitioner argues that the FPGA's multi-

processing bus arbitration functionality runs “independently and in parallel to whatever computation is happening on the processor (and other portions of the FPGA).” Pet. 28. As Dr. Shanfield explains, bus arbitration essentially is a “traffic cop” function in which data is routed for processing by either the FPGA or DSP. Ex. 1002 ¶ 84. At this stage we are sufficiently persuaded that traffic routing is an independent process because it does not appear to depend on other processes run on the DSP processor.

Dr. Shanfield also relies on Dehkordi’s disclosure of the FPGA pre-processes incoming data as teaching independent processing. *Id.* At this stage we are sufficiently persuaded that pre-processing incoming data is an independent process because it does not appear to depend on other processes run on the DSP processor.

Petitioner further submits that additional processes run on the FPGA run independently and in parallel with the processor. *Id.* at 28–29. These processes include (1) processes controlling an analog-to-digital interface, (2) power management processes, and (3) digital signal processing. *Id.*; *see also* Ex. 1004, 1 (Figure 1, “ADC Interface,” “Power-up Circuit,” and “DSP Functions” blocks within the Xilinx FPGA). In support of its position, Petitioner relies on Dehkordi’s teaching that the FPGA processes are from “RAM-based configuration where the configuration may come from outside the module,” which indicates, according to Petitioner, that these processes are separate from those running on the DSP processor. Pet. 29 (*quoting* Ex. 1004, 3). Petitioner relies on Dr. Shanfield’s testimony to support its arguments. *Id.* (*citing* Ex. 1002 ¶¶ 83–84).

Patent Owner responds that the processes run on Dehkordi’s FPGA are *dependent* on the DSP processor, because the FPGA is a slave to the

DSP processor. Prelim. Resp. 27. In support of this position, Patent Owner notes that the FPGA and DSP are connected through a common control bus (as illustrated in Figure 1 of Dehkordi). *Id.* According to Patent Owner, a skilled artisan would have understood that the DSP processor and FPGA, as a result of sharing the control bus, necessarily use a common clock signal, and as a result, the FPGA necessarily is a slave to, and dependent on, the processor.²⁴ *Id.* In addition to relying on a shared control bus to argue the FPGA is a slave to the DSP, Patent Owner also relies on a datasheet for the Xilinx 4010 FPGA, which according to Patent Owner “explains in several places that the most popular configuration of the 4010 FPGA is the Slave Serial mode.” *Id.*

It does not follow, based on this data sheet, that “the DSP processor is in control of the FPGA unless specified otherwise because it is the most common mode of operation,” as argued by Appellant. *Id.* at 28. As we discussed above, *supra* Sec. II.G.1, the Xilinx FPGA datasheet cited by Patent Owner discloses six modes of operation, of which only one mode is a slave mode. Ex. 1014, 6-46. Three modes are master modes, and two modes are peripheral modes. *Id.* We observe further that the XC4000 Series FPGAs include an internal oscillator that is used as the source clock in configuration modes in which the FPGA is master. *Id.* at 6-27. As such, the

²⁴ Patent Owner has not shown that sharing a common clock and/or common control bus means the FPGA necessarily acts as a slave to the processor. To the extent Patent Owner’s argument is that independent processes cannot run on (1) a common clock, or (2) a common bus, Patent Owner has not developed the record to show why this must necessarily be true. The parties may wish to develop the record as to whether independent processes *may* share common clocks and/or *may* share common buses.

Xilinx datasheet provides information regarding several available modes. Therefore, to ascertain the FPGA mode employed in Dehkordi we do not consider the Xilinx datasheet in a vacuum, but rather we consider it in conjunction with Dehkordi's teachings, as Petitioner has done (discussed above). Pet. 28–29.

On this score, Patent Owner argues that Dehkordi's description of the DSP Processor indicates the FPGA operates in a “*subservient support role* under the control of the DSP processor to maximize *the processor's* multiprocessing functionality by, *e.g.*, preprocessing incoming data *as directed by the DSP processor.*” Prelim. Resp. 28 (*citing* Ex. 1004, 1). However, contrary to Patent Owner's argument, the cited portion of Dehkordi does not provide any statement that maximizing the DSP processor's multi-processing functionality is achieved through the DSP processor directing the FPGA. *Id.* Rather, Dehkordi states that the “module [i.e., multichip module, or MCM] was designed to exploit the multi-processing capability of the [DSP processor].” Ex. 1004, 1. The module includes a number of components including SRAM, EEPROM, and an ADC, in addition to the FPGA. *Id.* A general statement that a multi-chip module is designed to maximize the processor's multi-processing capability is not sufficient basis to assume that the processor therefore directs the module's other components. Patent Owner's arguments, therefore, do not undermine Petitioner's showing.

Patent Owner also provides argument that “the testing procedures described in *Dehkordi* and relied on by Petitioners are *only speculative.*” Prelim. Resp. 29; *see also id.* at 29–34 (discussing JTAG and TAP testing). At this stage of the proceeding, it does not appear that Petitioner relies on

testing processes run on the FPGA as an example of “run[ning] independent processes in parallel with the processor.” *See* Pet. 28–29; Ex. 1002 ¶ 84.

Based on this preliminary record, we determine that Petitioner has demonstrated sufficiently that Dehkordi meets the recited limitation.

3. Remaining Limitations of Claim 1

As to the remaining limitations of claim 1, as well as the rationale supporting obviousness, we have reviewed the arguments and evidence in the current record, and determine that Petitioner has made a sufficient showing. Pet. 12–32. Based on this preliminary record, Petitioner has demonstrated a reasonable likelihood of showing claim 1 is unpatentable under § 103 as obvious over the combination of Lyke, Dehkordi, Franz, and Faura.

H. Obviousness of Claims 2, 3, 12, and 18

In its Preliminary Response, Patent Owner does not separately address Petitioner’s evidence or arguments directed to claims 2, 3, 12, and 18, apart from those issues discussed above with respect to independent claim 1. *See* Prelim. Resp. 19–35, 39.

Having reviewed and considered the evidence and arguments presented by the parties, based on the present record we determine Petitioner has demonstrated sufficiently, for purposes of institution, that claims 2, 3, 12, and 18 would have been unpatentable under § 103.

I. Obviousness of Claims 5, 10, 11, 13, 14, 15, 17, 19, 20

In its Preliminary Response, apart from those issues discussed above with respect to independent claim 1, Patent Owner does not separately address Petitioner’s evidence or arguments directed to claims 5, 10, 11, 13,

14, 15, 17, 19, 20, except for arguments made with regard to Steele. *See* Prelim. Resp. 19–39.

Claims 5, 10, 11, 13, 14, 15, 17, 19, and 20 recite a power converter.

By way of example, claim 5 recites:

The instrument controller of claim 1, wherein a third portion of the gates in the field programmable gate array is configured to operate as an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.

Ex. 1001, 10:38–43.

As argued by Petitioner, Lyke discloses an embedded power converter as recited in claim 5, except that it does not disclose explicitly that it is the FPGA that is configured to perform such conversion. Pet. 48 (citing Ex. 1003, 5:54–6:19). Specifically, Lyke discloses “an internal embedded power converter 10 that performs . . . generation of each operating and reference voltage needed within the AIC module.” Ex. 1003, 5:54–56. Petitioner argues that configuring an FPGA to perform power conversion in the manner claimed manner was well known, as evinced by Steele. Pet. 48–49.

Steele discloses a FPGA, comprised of eight configurable function blocks (CFBs), wherein the FPGA is powered by a 5 V supply voltage on the V_{CC} input pin, and can be configured to output a voltage on the CFBs’ eight V_{CCO} output pins. Ex. 1009, 4:7–43. Specifically, the FPGA can be configured so that different CFBs output different voltages on their respective V_{CCO} pins. *Id.* at 2:35–47, 2:54–65, 4:7–43. In an exemplary embodiment, either 3 V or 5 V is output on the various V_{CCO} pins. *Id.* at 2:66–67.

Patent Owner attempts to distinguish claim 5 from Steele, arguing that the V_{CCO} voltages output in Steel are not the claimed “operating and reference voltage[s]” of claim 5. The basis of Patent Owner’s argument is that the FPGA in Steele merely “uses” the input voltage V_{CC} and “replicates” it in generating V_{CCO} , whereas claim 5 recites “generating” operating and reference voltages. Prelim. Resp. 35–36. Patent Owner further argues, in the same vein, that the V_{CCO} output voltage of Steele is not generated by any circuitry in Steele, and is instead created externally. *Id.* at 38.

Patent Owner does not clarify the distinction it is attempting to make between “us[ing]” and “replicat[ing]” a voltage, versus “generating” a voltage, much less why such distinction is relevant to patentability. Equally unclear is what Patent Owner means by circuitry within the FPGA “generating” voltages.

First, Steele does not use either the term “use” or “replicate” in describing conversion of the input voltage V_{CC} to the output voltages V_{CCO} . To the extent Patent Owner’s critique is that Steele does not use the words “generate” or “power converter,” failure to use these terms *ipsis verbis* is not decisive. *See* Prelim. Resp. 37 (“Power conversion is not mentioned in the *Steel* reference.”). Setting aside terminology employed in Steele, we fail to see a patentably relevant distinction between conversion of voltages in the ’177 patent and Steele.

The ’177 patent describes employing “subsets of gates in the FPGA” to “provide power conversion,” and provides a functional block diagram illustrating the power conversion concept. Ex. 1001, 8:45–9:17, Fig. 3. The power converter in a first stage converts an unregulated supply voltage (from a source external to the FPGA) to a fixed, regulated supply voltage V_{REG} .

Id. at 8:64–66, Fig. 3. The power converter in the second stage converts VREG to one of the following: internal digital power, internal analog power, or one of various reference voltages. *Id.* at 9:1–4, Fig. 3. The blocks illustrated in Figure 3 do not show any internal details such as circuitry or logic, and the ’177 patent does not provide details as to how either power conversion or “generating” voltages is accomplished, other than to state, “[m]any known topologies known in the art of power convertor design may be applied, whether switching based, linear based, or a combination of the two.” *Id.* at 9:4–6. Based on the ’177 disclosure, we discern no reason why power conversion (including “generating” voltages) should preclude Steele’s teachings, in which the FPGA is configured to, e.g., receive a 5 V input at V_{CCO} and output either, e.g., 3V or 5V at various V_{CCO} pins.

Patent Owner also argues that Steele discloses “*only one corresponding output voltage*,” whereas claims 5 recites generating “*each operating and reference voltage needed*.” Prelim. Resp. 37. Contrary to Patent Owner’s argument, Steele’s exemplary FPGA outputs eight, not one, output voltage corresponding to the V_{CC} input voltage. Ex. 1009, 4:8–10 (disclosing the FPGA comprises eight CFBs coupled together by global interconnect 208), 4:23–27 (describing the FPGA as powered by a 5 V supply on the V_{CC} pin, and having eight V_{CCO} pins).

Having reviewed and considered the evidence and arguments presented by the parties, based on the present record we determine Petitioner has demonstrated sufficiently, for purposes of institution, that claims 5, 10, 11, 13, 14, 15, 17, 19, and 20 would have been unpatentable under § 103.

III. CONCLUSION

For the reasons expressed above, we determine that Petitioner has demonstrated a reasonable likelihood of showing that at least one claim of the '177 patent is unpatentable. As set forth in the Order below, we institute a trial on all challenged claims and all asserted grounds of unpatentability. *See* 37 C.F.R. § 42.108(a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

Our factual findings and determinations at this stage of the proceeding are preliminary, and based on the evidentiary record developed thus far. This is not a final decision as to the patentability of claims for which *inter partes* review is instituted. Our final decision will be based on the record as fully developed during trial.

IV. ORDER

Accordingly, it is

ORDERED that an *inter partes* review is instituted as to all challenged claims on all the grounds raised in the Petition; and

FURTHER ORDERED that *inter partes* review is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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