UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRO DEVICES, INC.,
and ATI TECHNOLOGIES ULC
Petitioner,
v.

SENTIENT SENSORS LLC
Patent Owner.

Case IPR2023-00195
U.S. Patent No. 6,938,177

PATENT OWNER'S RESPONSE

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UPDATED EXHIBIT LIST

Exhibit No.	Description
2001	**USAF Cooperative Research and Development Agreement between Air Force Research Laboratory, Space Vehicles Directorate and MSI November 24, 1998** **Confidential**
2002	**JTAG Article FPGA4fun (1)** **https://www.fpga4fun.com/JTAG1.html**
2003	**TAP Article FPGA4fun (2)** **https://www.fpga4fun.com/JTAG2.html**
2004	**Xilinx JTAG Programmer Guide 1991-1999**
2005	**XLINX XC4000 TAP Application Note November 16, 1999**
2006	**USPTO Office Action Dated December 8, 2004**
2007	**Examiner Stoynov 1st Prior Art Search 11/19/04 (5 pages)**
2008	**Examiner Stoynov 2nd Prior Art Search 11/22/04 (7 pages)**
2009	**Examiner Stoynov 3rd Prior Art Search 11/22/04 (5 pages)**

2010	**Examiner Stoynov 4th Prior Art Search 11/23/04 (8 pages)**
2011	**Examiner Stoynov 5th Prior Art Search 11/23/04 (10 pages)**
2012	**Examiner Stoynov 6th Prior Art Search 11/24/04 (5 pages)**
2013	**Examiner Stoynov 7th Prior Art Search 11/29/04 (14 pages)**
2014	**Examiner Stoynov 8th Prior Art Search 3/09/05 (3 pages)**
2015	**Proof of Service on Registered Delaware Agent**
2016	**MSI/Sentient Ownership Interest** **Confidential**
2017	**Letter from James Lyke in support of Management Sciences, Inc. dated Apr. 29, 1997** **Confidential**
2018	**Bus Arbitration In Computer Organization Article** **https://www.geeksforgeeks.org/bus-arbitration-in-computer-organization/**
2019	**Enhancement of MCM Testability Using Embedded Reconfigurable FPGA**

	J. York, T. Powell P. Dehkordi, and D. Bouldin, Proceedings 1997 IEEE Multi-Chip Module Conference (Cat. No. 0-7803-4275), 1997, pp. 165-173 ("*Dehkordi* 2")
2020	**Declaration of John Peck** (with Curriculum Vitae)
2021	**Ch. 11 in *A New Kind of Science.*** Champaign, IL: Wolfram Media, pp. 637-714, 2002.
2022	**Sentient's District Court Identification of claim constructions**
2023	**Xilinx's District Court Identification of claim constructions**
2024	**Definition of computation** https://mathworld.wolfram.com/Computation.html

STATEMENT OF MATERIAL FACTS IN DISPUTE

Petitioners XILINX, INC., ADVANCED MICRO DEVICES, INC., and ATI TECHNOLOGIES ULC (collectively, "Petitioners" or "Xilinx Inc. *et al*.") did not submit a specific articulated statement of material facts in their Petition. Accordingly, no response is required under 37 C.F.R. § 42.23(a), and no facts are admitted.

Pursuant to 35 U.S.C. § 314 and the Institution Decision dated September 20, 2023 (Paper 12), and the stipulation filed October 18, 2023 (Paper 16) Sentient Sensors, LLC ("Sentient" or "Patent Owner") hereby respectfully submits its Patent Owner Response to the Petition for *Inter Partes* Review ("IPR") of U.S. Patent No. 6,938,177 ("'177 Patent") filed by Xilinx Inc. *et. al.* ("Xilinx" or "Petitioners").

I. INTRODUCTION

Based on the fully developed record, the Board should find all challenged claims – namely claims 1-5, 10-15, and 17-20 - patentable. Petitioners' challenges merely duplicate past prior art rejections that the United States Patent & Trademark Office ("USPTO") fully considered and correctly found with good reason that Sentient overcame. Petitioners merely repackage and/or recycle similar arguments made during prosecution through using the same or cumulative prior art in an attempt to second guess the Examiner who found such positions unavailing. Petitioners' prior art references simply do not show or suggest the novel features of the claims.

Features recited in the '177 Patent claims at issue that patentably distinguish the prior art are technical improvements to functional shortcomings of the prior art and are founded on actual work with U.S. Patent No. 6,148,399 to James Lyke (the "'399 Patent" or "*Lyke*"). Lyke is Petitioners' primary reference and its described Advanced Instrument Controller ("AIC") was cited and extensively and carefully considered during prosecution. The U.S. Government also found the limitations in the '399 Patent and AIC

as compelling reasons to sponsor Mr. Kenneth Blemel's efforts to improve the AIC, which led to the inventions described and claimed in the '177 Patent. Sentient has sold products covered by the '177 Patent have been sold to many branches of the U.S. military, including the Office of the Secretary of Defense and the U.S. Missile Defense Agency, and incorporated into numerous aerospace platforms.

The lead reference Petitioner's combines with *Lyke*, EX. 1004 "*Dehkordi 1*" is a paper directed to a prototype MCM subsystem that was still in development at the time of publication (1996). Its operation and testing procedures relied on by Petitioner incomplete, hypothetical and speculative.

Patent Owner updates this unfinished story with a follow up paper (EX. 2019 "*Dehkordi 2*") by the *same authors* regarding the *same MCM subsystem* and the *same testing features* clarifying its operation and testing procedures used in a more complete subsystem, which was not included in the Petition. This reference confirms Sentient's position, that independent and/or parallel operation, among other things, is not shown in *Dehkordi 1*.

The background references Petitioners have offered into evidence - *Halverson* (EX 1025) and *Karstonov* (EX. 1036), which Petitioner does *not* use as the basis of any Ground are unhelpful in its patentability analysis and irrelevant in view of the clarification provided by *Dehkordi 2*. Any reliance on these references beyond what is

permitted for a background reference not included in a Ground, is misplaced (*i.e.*, cannot be used to fill holes in the references specifically used in the Ground).

A. Sentient Sensors

Sentient is a small family-owned business that was founded by inventor and entrepreneur Kenneth Blemel and his wife of 63 years, Marlene ("Kay") Blemel.[1] For over 50 years, Mr. Blemel, a life-long engineer, and sole inventor of the '177 Patent, has operated his small business in New Mexico providing high-tech specialty solutions for military and aerospace applications and successfully guiding multiple research and development programs for, among others, the U.S. Air Force and other branches of the U.S. military, including the R&D program culminating in the issuance of the challenged '177 Patent.

The inventions described and claimed in the '177 Patent have been used to provide instrumentation for monitoring and control of systems and components of instruments, aircraft, ships, homes, and machinery. A few examples include:

- Monitoring signals on UH-60 helicopters;
- Instrumentation for prognostic health monitoring of aircraft propulsion systems;
- Instrumentation interface to paired flight data recorders;

[1] *See, e.g.*, Sentient's website at http://www.mgtsciences.com/

- Instrumentation monitoring health signatures of aircraft propulsion systems;
- Instrumentation for monitoring and control of diesel generator sets;
- Instrumentation for monitoring health of ballistic missiles;
- Instrumentation of hybrid micro-grids; and
- Edge node flight data collection and analysis for B-52 and other military aircraft.

The teachings of the '177 Patent enable the rapid prototyping and deployment of complex hardware and software platforms thus providing enhanced flexibility for various real-world applications. As just one example, the '177 Patent describes and claims an instrument controller including a microprocessor for controlling inputs and outputs, logic gates arranged in a manner consistent with a field programmable gate array ("FPGA") that can be used as a freely reconfigurable parallel *and independent* processor, and a real-time clock for time-stamping of data before it is stored in non-volatile memory, all of which contribute to the creation of a customizable development platform that allows for a wide range of hardware controller solutions.

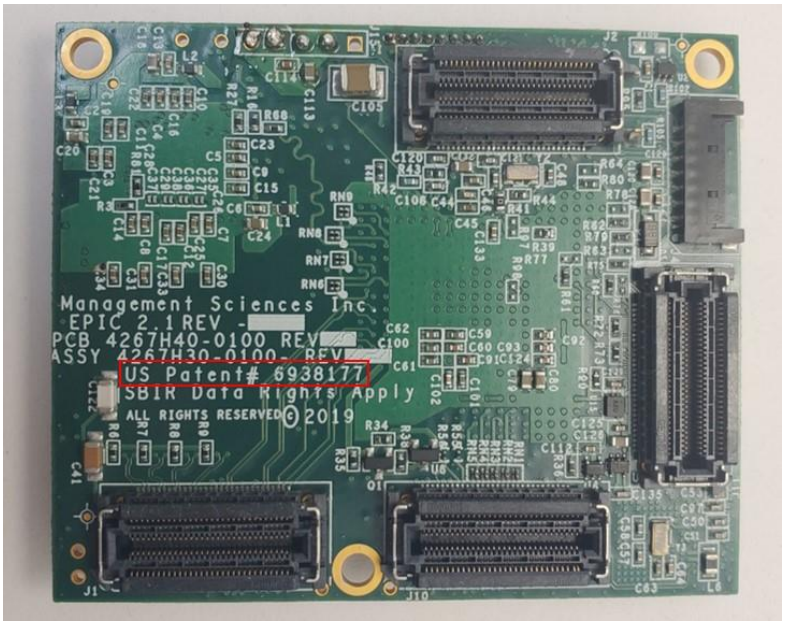
As of its filing date in December 2001, the technology described and claimed in the '177 Patent provided for novel and innovative in-field control and monitoring system with time-stamped selectable collection and digitizing of analog and digital data streams, and enabled, *inter alia*, real-time concurrent data processing to measure and control stresses on components and to generate alerts for anomalous conditions. The use of such

programmable logic-based "system on a chip" "SoC" and "network on a chip" "NoC" instrument controllers are now widespread with diverse applications, including general computer-based system control, machinery control, field programmable automation of process lines, telecommunications, and diagnostic and prognostic health monitoring of equipment.

The research and development program that led to the innovations described and claimed in the '177 Patent was funded by the U.S. Air Force and conducted at Kirtland Air Force base in Albuquerque, New Mexico. *See* EX. 1001 at 1:5-10. These advancements were initially directed toward use in the Strategic Defense Initiative program initiated in the 1980s, colloquially known at the time as "Star Wars." As a result, the U.S. government, via the Space Vehicles Directorate of the U.S. Air Force, entered into a Collaborative Research and Development Agreement (the "Space Directorate CRADA" (EX. 2001)) with Sentient and secured a license to practice the inventions of the '177 Patent. *Id*.

Products covered by the '177 Patent have been sold by Patent Owner to many branches of the U.S. military, including the Office of the Secretary of Defense and the U.S. Missile Defense Agency, among others, and incorporated into numerous aerospace platforms. Pictures of marked versions of Sentient's Embedded Programmable

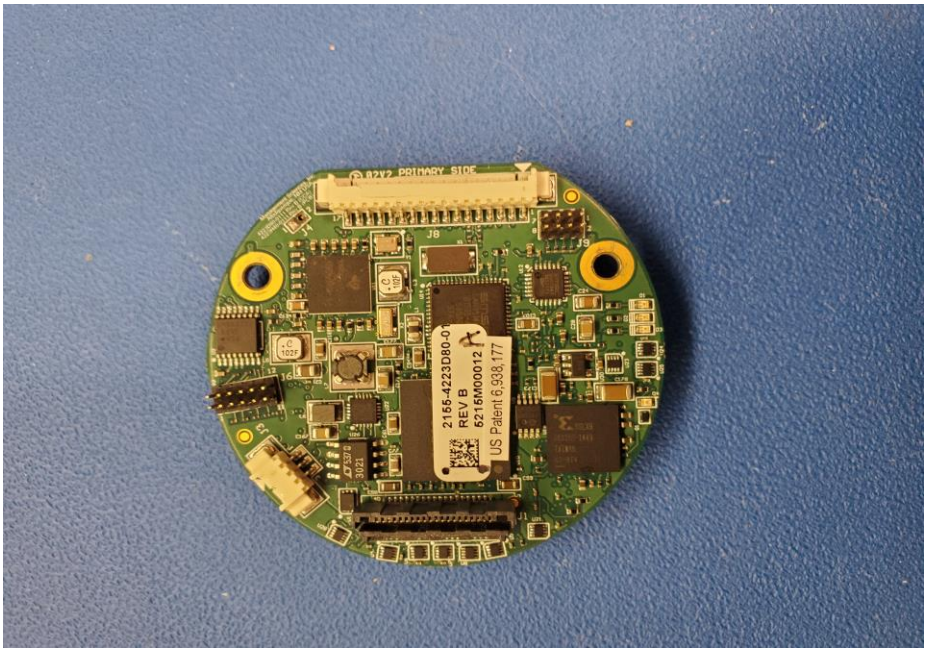
Instrumentation Controller "EPIC" products covered by the '177 Patent are shown below[2;3;4].

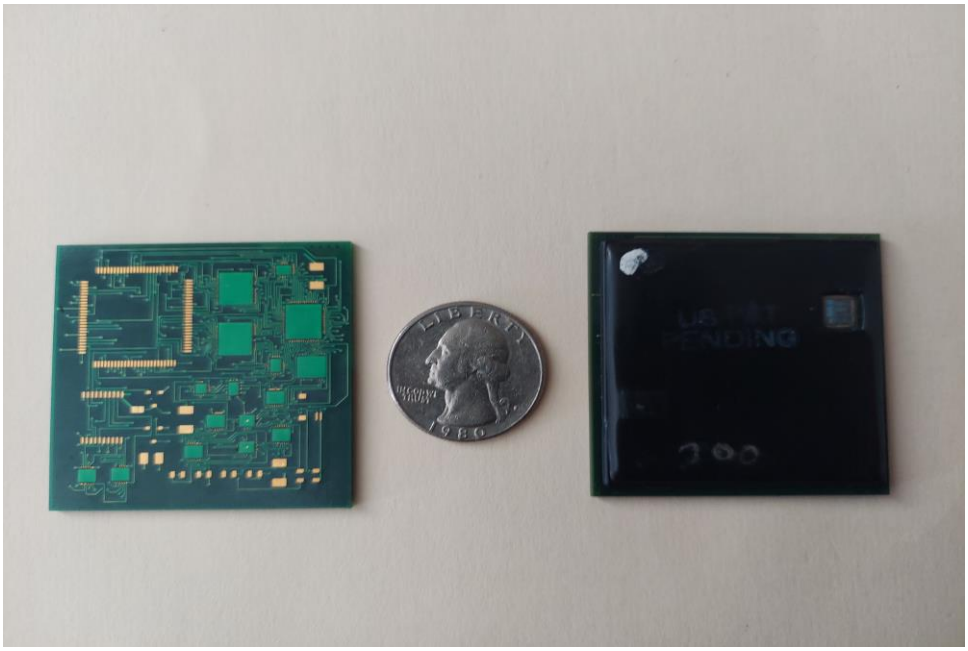


[2] https://www.mgtsciences.com/products/

[3] https://www.mgtsciences.com/wpcontent/uploads/2016/09/EPIC2_Brochure_Breif_May_31_2016.pdf

[4] https://www.mgtsciences.com/wpcontent/uploads/2016/09/Sentient_Guardian_Brochure_Aug_2016.pdf





Hardware purveyors such as Xilinx and the licensees of the '177 Patent have employed the inventions of the '177 Patent for their own commercial exploitation (*e.g.*, as automotive and industrial control devices) and used them for controllers of a wide array of electro-mechanical systems.

B. Prosecution of the '177 Patent in the USPTO In View Of *Lyke*

The '399 Patent to *Lyke*, and the AIC described therein, was considered in great detail during prosecution of the '177 Patent and its functional shortcomings were the basis for the inventions described in therein. Indeed, the purpose of the Space Directorate CRADA dated November 24, 1998, between Management Sciences, Inc. ("MSI")[5] and the Air Force Research Laboratory, Space Vehicles Directorate, was to improve the existing AIC technology to develop novel AIC-based systems. James Lyke was aware that the Air Force sought to improve upon the technology disclosed in his '399 Patent by engaging Mr. Blemel, who was highly regarded by Mr. Lyke. *See* EX. 2001 and p.14 including section 2.0; *see also* EX. 2017 (Apr. 29, 1997 Letter from J. Lyke recommending that Management Sciences, Inc.'s "Phase II SBIR proposal," which would eventually lead to the inventions in the '177 Patent, be funded).

Various technical goals were enumerated in the Space Directorate CRADA including, for example, producing "AIC technologies for the commercial market for use in sensing monitoring and controlling diverse applications across a broad spectrum of applications including, but not limited to *process control, aerospace*," *etc*. (EX. 2001 at p.14, section 2.0); creating "smarter systems" with the ability to "embed intelligence" and

[5] MSI is the managing member of Sentient. *See* paper 4; *see also* EX. 2016.

improve the capability and responsiveness of the war fighter (*id.* at p.15, section 5.2.3). *See also* Section 8 pages 16-17.

During the development period that began in 1998, numerous technical limitations were noted with regard to the systems of the '399 Patent. For example, in the DESCRIPTION OF THE PRIOR ART section, the '177 Patent explains with particularity the function of the '399 Patent technology and its limitations. *See* '177 Patent at 1:21-2:8.

The '177 Patent explains that the '399 Patent suffers from numerous deficiencies, such as its *inability to run parallel and independent processes*. *See* '177 Patent at 2:9-2:31. Thus, according to the '177 Patent, there was a need for a circuit design capable of executing multiple parallel processes in an independent fashion. EX. 1001 Patent 2:9-18.

> However, there are several limitations to the design in U.S. Pat. No. 6,148,399. First the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

This is at least because of the common clock signal used through the '399 Patent. "[W]hat is need is a separately controllable FPGA…" EX 1001 2:48-50. This theme is repeated numerous times throughout the '177 specification. *See* EX. 1001 at, *e.g.*, 2:48-55, 8:18-

22. This feature is also specified in, *e.g.*, independent claims 1, 6, 10, and 15. *See*, *e.g.*, 10:4-7 and 12:14-19.

During examination, the USPTO carefully studied the '399 Patent. By granting the '177 Patent, the USPTO came to the same conclusion as Mr. Blemel - namely that *Lyke* does not teach or suggest a field programmable gate array coupled to the processor for parallel independent processing. EX. 2006 USPTO Office Action p. 4-5:

> Lyke fails to disclose an embedded memory for storing an initialization program and a field programmable gate array coupled to the processor for parallel processing.

Accordingly, all available intrinsic evidence is consistent in that the '399 Patent *does not* teach or suggest a field programmable gate array that runs *independent parallel processes*.

C. Extensive Prior Art Searching by the USPTO

The USPTO conducted extensive prior art searching while examining the '177 Patent. As can be seen from EXs. 2007-2014, Examiner Stoynov—an experienced Examiner in the integrated circuit art unit 2116 that handles the U.S. classification 713 (Electrical computers and digital processing systems: support) under which both the '399 and '177 Patents were prosecuted (*see* EX. 1003, front page, line 52; EX. 1001, front page, line 52)—conducted no less than *eight different comprehensive prior art searches*. The first seven searches were conducted over a period of 10 days before the first Office Action (EXs. 2007-2013) and include an impressive *56 pages of search terms and*

strategy covering interwoven and overlapping search strings relating to the claimed features—all *expressly and diligently searching for* the terms "FPGA" and "independent parallel processes"—yielding dozens of U.S. Patent documents. EXs. 2007-2014. Petitioners now rely on some of those documents found by Examiner Stoynov as supposedly "new" or that Petitioners assume the USPTO found unhelpful. *See, e.g.*, EX. 2014 (showing that Examiner Stoynov found U.S. Patent 5,574,930 to *Halverson* (EX. 1025) and used it as a key term in additional searches). EX. 2014.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		* * * * *				
L12	25	("5574930").URPN.	USPAT	OR	OFF	2005/03/09 11:15

The eighth search was conducted before issuance to yet again confirm patentability and which included "FPGA" as *the first search term* – demonstrating the PTO's keen interest in the feature. EX. 2014.

After his extensive searching, Examiner Stoynov found that the *Cloutier* (EX. 1040), *Lyke* (EX. 1003) and *DaCosta* (EX. 1041) references listed on the face of the '177 Patent were the most relevant and used them to reject the pending claims. The fact that Petitioners Xilinx—the world's largest and oldest FPGA manufacturer—and AMD—one of the world's most valuable semiconductor companies—with their combined vast resources and institutional knowledge, have failed to produce non-duplicative or non-

cumulative references. Their failed efforts confirm Examiner Stoynov's diligence and the quality of his searches.

D. Bus Arbitration

Computer systems normally contain data bus-based architectures in which several different devices compete for control of the bus. Such devices include signal processors, computational circuity such as FPGAs, memories and input/output controllers and the like. An arbitration scheme is incorporated into the design of the system to determine which of these devices can access and control the bus at a given time to prevent conflicts. Such schemes are adopted based on the desired operational goals. For example, some schemes allow high priority devices to have control at the expense of other devices. Other schemes have a more egalitarian approach for bus allocation to devices more equally or on an "as needed" basis. EX. 2020 ¶34.

The most basic arbitration scheme is the so-called FIFO (First-In-First-Out). In this scheme requests to access a memory port interface through a bus are treated strictly in the order in which they arrive. This scheme may not take into account the relative importance of each of the access requests. Thus, any device urgently requiring access to the memory may have to wait while other lower-priority devices complete their operations. EX. 2020 ¶35.

Another commonly used method in processor-based with systems with FPGAs for bus arbitration involves the use of a central arbiter to communicate with all the devices

desiring to use the bus. The central arbiter determines which device has the highest bus use priority taking into account how important the device is and how long the device has been requesting the use of the data bus. It then sends out a signal permitting the device to use the bus. This processing system typically fails if the central arbiter ceases to function. EX. 2020 ¶36.

Another commonly used arbitration scheme is processor systems that include FPGAs, is "daisy-chaining." In this method a signal indicating that the bus is available for use is transmitted from device to device in priority order. Any device requiring access "captures" the signal and as a result may control the bus. Low priority devices may have to wait an undesirable length of time until they are granted access to the bus. EX. 2020 ¶37.

A two-level internal bus arbitration for the system IO bus, teaches a fourth prior art system in which a fixed priority scheme is used to determine the arbitration. All requests received while a bus is mastered by another device are latched by common logic and will be processed in priority order when the next bus becomes free. EX. 2020 ¶38.

A rotating priority scheme offers bus access to each device in strict rotation. This reduces bus access requests being delayed for too long, but it fails to take into account the need for some devices to access the bus prior to others. EX. 2020 ¶39.

Importantly, none of these arbitration schemes, which are used in processor systems that may include FPGAs, require the independent or parallel operation of any other device, whether they have logic configured from an external non-volatile memory or not. EX. 2020 ¶40.

E. ***Dehkordi 1*** **(EX. 1004)**

Dehkordi 1 ("D1") describes certain ongoing, in-process development efforts to produce an MCM-based DSP subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA. At the time of its publication in 1996, the DSP system was still *in fabrication*, with its operation and configuration still theoretical and therefore not enabled. EX. 1004 at 3-4 ("testing *and rework* issues will *continue* to be challenging" and "looking forward to *confirming functionality*"). As shown in the annotated figure from D1 below, the DSP processor and FPGA are connected through numerous buses, the most notable of which is the *control bus* (highlighted in yellow). A POSA would understand that the designers of D1 intended the control bus to allow the processor to control the FPGA with operational instructions, including providing a clock signal. Thus, for normal operation, the designers selected the FPGA to be *dependent* on and under the control of the processor. Moreover, potential additional processes such as any potential generic logic functions, power up circuitry and or ADC Interface, all need to be programmed (from RAM) into the MCM subsystem (Petition at 28) which *had not yet occurred* because the subsystem was incomplete at the time of D1 and thus such operation

was still theoretical as well and not enabled. Importantly, no code or operational flow charts pertaining to D1 MCM functions are provided in the Petition. In any event, these other functions are necessarily all controlled by the processor in configuration shown. That is why there is no discussion of any bus arbitration in connection with normal operation of the MCM subsystem. EX. 2020 ¶41.

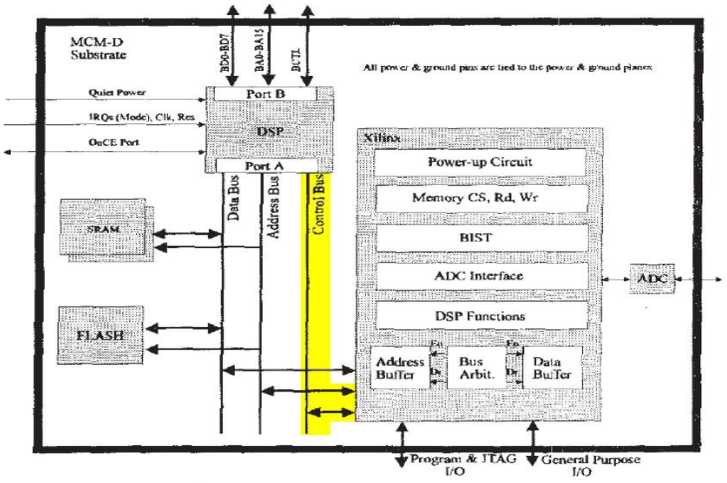


Figure 1. The Block Diagram of the DSP Sub-system.

This is consistent with D1's technical description that explains how the MCM subsystem design is intended to specifically exploit the multiprocessing capability *of the DSP processor*. EX. 1004 at 1, "*Design Flow*" section. This technical description means that the FPGA is intended to operate in *a support role* under the control of the DSP processor to maximize the DSP processor's multiprocessing functionality by, *e.g.*, preprocessing incoming data *as directed by the DSP processor* to relieve that burden from the DSP processor. No other specialized connection or functionality is shown. *See id.* EX. 2020 ¶42.

D1 further theorizes *a special testing mode of operation* might employ the well-known industry standard JTAG and TAP testing methodologies used for testing the operation of the DSP subsystem. *See* EX. 1003 at 3, "*Cost and Testing Issues*" section. Notably, however, JTAG and TAP testing operations typically require an external JTAG computer or other controller that *controls both the DSP processor and the FPGA during testing*. Accordingly, because both the FPGA and DSP processor are under *common control* during testing, they *do not operate any independent processes* (*i.e.*, they are both under the control of another common device). Xilinx's own JTAG/TAP documentation used for the 4010 series FPGA explains and confirms this. *See* EXs. 2004-2005. Institution decision at 39. This is explained in more detail in connection with Patent Owner's response to Ground 1 below. EX. 2020 ¶43.

F. ***Dehkordi 2*** **("D2") (EX. 2019)**

FIG. 1 of D2 (below) is simplified functional representation of FIG. 4, which is a more complete version of the MCM subsystem in FIG.1 of D1 (EX. 1004). EX. 2020 ¶44.

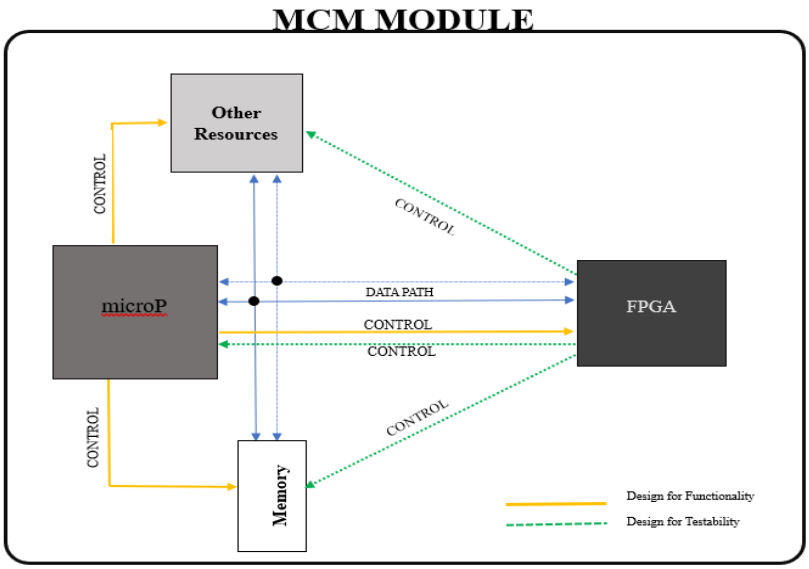


Figure 1 : Designing for Testability for a Typical MCM.

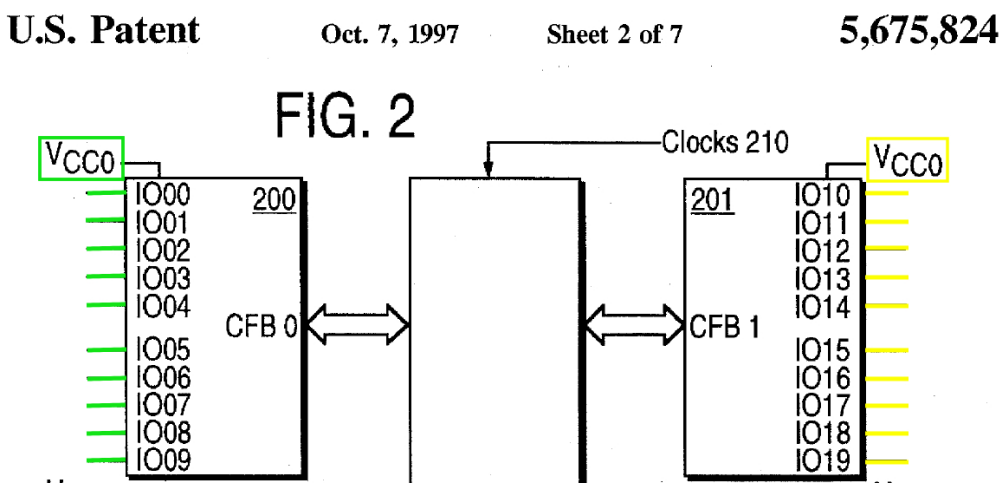
D2, a highly relevant reference that Petitioners did not identify, let alone provide to the Board to consider prior to institution, is a follow up to D1 published a year later, that describes a more complete version of the MCM subsystem by the same authors regarding the same MCM subsystem and the same testing features. D2 clarifies the operation of the MCM subsystem and its testing. D2 entitled "*Enhancement of MCM Testability Using Embedded Reconfigurable FPGA*" contradicts Petitioners unpatentability arguments. As annotated FIG. 1 of D2 shows below which in normal operation (the "design for functionality" configuration - highlighted in orange) the

processor controls the entire subsystem including the FPGA, the memory and the other resources necessary to operate the system. Alternatively, in the special testing mode (the "design for testability" configuration - highlighted in green) it is the FPGA that controls the entire subsystem including the processor, the memory and the other resources. There is no *discussion* of bus arbitration in D2, which appears to have been abandoned as the design progressed. However, D2 does employ JTAG boundary scans (IEEE 1149.1). D2 at 167. There are no other modes of operation. Thus, at no point does the D1-D2 MCM subsystem FPGA operate either parallel *or* independent processes. Either the processor or FPGA are in control. EX. 2020 ¶45.

Importantly, D1, Petitioners' *own asserted prior art* is a system that uses an external RAM-based configuration where the FPGA **does *not* run independently or in parallel with the processor**. EX. 2020 ¶46.

G. *Steele* (EX. 1009)

Steele describes a programmable logic device configurable to operate as a voltage replicator that merely distributes an applied input voltage for output at other pins. Simply stated, it operates by accepting a fixed input voltage from an external source at the VCCO pin of a Configurable Logic Block (CFB) and replicates that fixed voltage at the input/output (I/O) pins for use in external devices. EX. 1009, 4:28-58. This is explained in detail at 4:28-43 of *Steele* and shown in *Steele*'s FIG. 2 below (annotated to show the 5V level (CFB 0) (green) and the 3V level (CFB 1) (yellow). EX. 2020 ¶47.



Notably, *Steele does not* generate the applied VCCO voltage levels itself, but rather merely uses them. The voltage generation is done elsewhere on another external device and those voltages are applied to the VCCO input from that external source for reproduction by *Steele*'s CFB. Steele *does not* convert power because it does not change one voltage level to another as the claims require under Patent Owner's claim construction. Instead, *Steele* merely distributes *the same* voltage level applied VCCO at the output I/O pins. For example, IO00-IO09 have 5V outputs whereas IO10-IO19 have 3V outputs. *See* EX. 1009, 2:22-26; 4:28-43. There is no change or *conversion* (*i.e.*, changing one thing to another – plain meaning). *Cf.* Institution Decision at 42. Merely distributing *the same voltage* eight times is not converting power, but rather is merely *distributing the same voltage* multiple times. EX. 2020 ¶48.

II. THE PETITION FAILS TO ESTABLISH OBVIOUSNESS

A. Legal Standard

Burden of Proof

Petitioner has the burden of proving unpatentability in an *inter partes* review. 35 U.S.C. § 31(I). "[T]he burden of proof is on the petitioner to prove unpatentable those claims that were actually challenged in the petition for review and for which the Board instituted review." *Nike, Inc. v. Adidas AG*, 812 F.3d 1326, 1334 (Fed. Cir. 2016), overruled on other grounds by *Aqua Products, Inc., v. Matal*, 872 F.3d 1290, 1296 n. 1 (Fed. Cir. 2017).

A petition must identify, "with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3); *see also* 37 C.F.R. §42.22(a)(2) (the petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent"); 37 C.F.R. §42.104(b)(4) (the petition must identify "[h]ow the construed claim is unpatentable under the statutory grounds identified in paragraph (b)(2) of this section. The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon."); *Intelligent Bio- Sys, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016).

Congress created IPRs as a "complete substitute" to District Court litigation for assessing patent validity. *WesternGeco LLC v. ION Geophysical Corp*., 889 F.3d 1308, 1317 (Fed. Cir. 2018) "In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The Board is not "free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR*." In re Magnum Oil Tools, Int'l, Ltd*., 829 F.3d 1365, 1381 (Fed. Cir. 2016). "The petitioner must instead articulate specific reasoning, based on evidence of record," as set out in its petition "to support the legal conclusion of obviousness." *Id*. at 1380. The Board "must base its decision on arguments that were advanced by a party." *Id*. at 1381. The PTAB cannot "decide unpatentability theories never presented by the petitioner." *Id*.

To prevail on any obviousness ground, Petitioner may not simply identify individual claim components—it must show why a "skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). A petitioner must support even simple modifications to a reference with some motivation to make the change. See *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984).

In addition, a petitioner cannot rely on "mere conclusory statements." *Magnum*

Oil, 829 F.3d at 1380. Rather, the petitioner must set forth "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 418-19 (2007). Similarly, a petitioner cannot simply rely on an expert's unsubstantiated and conclusory opinions. See 37 C.F.R. § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Harmonic*, 815 F.3d at 1363 (Petitioner failed to establish obviousness where expert testimony "add[ed] nothing beyond the conclusory statements in [the] petition.").

An appropriate obviousness inquiry cannot involve even a "hint of hindsight." *Star Sci., Inc. v. R.J. Reynolds Tobacco Co*., 655 F.3d 1364, 1375 (Fed. Cir. 2011). Petitioner may not "simply retrace[] the path of the inventor with hindsight, discount[] the number and complexity of the alternatives, and conclude[] that the invention . . . was obvious." *Ortho-McNeil Pharm., Inc. v. Mylan Labs., Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008). Likewise, "[c]are must be taken to avoid hindsight reconstruction by using the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit." *In re NTP, Inc*., 654 F.3d 1279, 1299 (Fed. Cir. 2011) (internal quotations omitted).

In arriving at an obviousness determination, the Petitioner must "sufficiently explain and support the conclusions that… a relevant skilled artisan not only could

have made but would have been motivated to combine all the prior-art references in the way the patent claims." *Pers. Web Techs., LLC v. Apple, Inc*., 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have been motivated to combine those references. *Intelligent Bio Sys., Inc. v. Illumina Cambridge Ltd*., 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Res. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly Co*., 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make required factual findings.) This combination determination, as supported by an articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp*., 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a "common sense" finding is no different than the conclusory statement "would have been obvious." *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, "knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references." *Innogenetics, N.V. v. Abbott Labs*., 512 F.3d 1363, 1373 (Fed. Cir. 2008).

The appropriate claim construction standard is provided by *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Under the *Phillips* standard, "the

specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive….' and claim terms are generally given their ordinary and customary meaning." The "only two exceptions to this general rule [are] 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee clearly and unmistakably disavows the full scope of a claim term either in the specification or during prosecution." *See Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (citing *Vitronics*, 90 F.3d at 1580).

The Petitioner is required to identify "the grounds on which the challenge to each claim is based." 35 U.S.C. § 312(a)(3); see also 37 C.F.R. § 42.104(b) (requiring petitioner to identify "the patents or printed publications relied upon for each ground" and "where each element of the claim is found in the prior art patents or printed publications relied upon"). *Apple, Inc. v. MPH Techs. OY.*, No. 2021-1355, 2021-1356, 2022 WL 4103286, *7 (Fed. Cir. Sep. 8, 2022).

PERSON OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is evidenced by the references. See *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). An ordinary artisan would have been a person having, as of December 2001, a Bachelor's degree in Electrical or Computer Engineering or an equivalent degree with at least four years of experience in FPGA and processor systems design including but not limited to system on a chip "SoC" and electronic vehicle sensor systems or related technologies. Additional education may

substitute for lesser work experience and vice-versa. EX. 2020 ¶ 22.

CLAIM CONSTRUCTION

In the parallel District Court proceeding, the parties proposed constructions for disputed claim terms, which are not yet briefed, with no ruling yet on the merits. *See* Joint Claim Charts at EX. 2022-23. The relevant claim construction definitions related to the '177 patent for this IPR review are set forth below.

Notably, Xilinx has changed its definition of "embedded" as used in the Petition as simply "on-chip" (*e.g.*, Petition at 25-26) to "embedded within the component that is required in that part of the claim" for the District Court litigation. EX. 2023. Thus, Xilinx uses one broad construction in its Petition for unpatentability purposes and then uses another narrower definition for non-infringement in District Court.

No.	Claim Term	Patent Owners' Proposed Construction	Petitioner's Proposed Construction
1.	"process"	"a computational process programmed into the FPGA gates" Excludes initialization and power up sequences.	None provided
2.	"independent processes"	Plain and Ordinary Meaning. "without computational assistance from another" Independent processes are independent of each other and the processor.	None provided
3.	"power converter"	Plain and Ordinary Meaning. "a converter which changes a voltage level to another voltage level"	None provided

For the reasons set forth below, all the challenged claims of the '177 are patentable under either Patent Owner's claim constructions or Plain and Ordinary Meaning.

III. THE PETITION FAILS TO ESTABLISH OBVIOUSNESS

Petitioners present five separate Grounds of unpatentability all based on 35 U.S.C. § 103:

- **Ground 1** is directed toward claims 1 and 4 and is based on *Lyke*, *Dehkordi*, *Frantz*, and *Faura*.
- **Ground 2** is directed toward claim 2 and is the same as Ground 1 with the addition of *Krasner*.
- **Ground 3** is directed toward claim 3 and is the same as Ground 1 with the addition of *Christian*.
- **Ground 4** is directed toward claims 5, 10-11, 13-14, 15, 17, 19, 20 and is the same as Ground 1 with the addition of *Steele.*
- **Ground 5** is directed toward claims 12 and 18 and is the same as Ground 4 with the addition of *Christian*.

Although numerous reasons why the challenged claims are patentable over the theories advanced in the Petition, Sentient, focuses on the straightforward deficiencies in Petitioner's analysis of independent claim 1, as found in Ground 1, and independent claims 10 and 15, as found in Ground 4, specifically with respect to the claim term "*independent processes in parallel*" (elements 1.5, 10.5, and 15.2), and of independent claims 13 and 20, as found in Ground 4, specifically with respect

to the claim term "*power converter capable of… generating…. reference voltage*" (elements 13.6 and 20.1). or operating as a power converter *at all* as in 15.2.

A. Claim Construction

The proper construction of "process" is "a computational process programmed into the FPGA gates." Robust specification support for this definition exists in multiple areas including, *e.g.*, at EX. 1001 at 8:16-32; 9:19-35. A primary purpose of the FPGA is to act as a co-processor for various analog or digital functions that compute a result. EX. 1001 4:39-50. Power up sequences do not qualify at least because they do not produce a computational result and such features have no specification support as processes. Similarly, initialization sequences also do not qualify because they also do not produce a computational result, but rather merely prepare the FPGA to perform computations and also have no specification support. EX 2020 ¶¶ 49-51.

The proper construction of "independent processes" is "without computational assistance from another" which is consistent with Patent Owner's previous litigation definition and the specification. See, for example, EX. 1001 2:9-18; 2:48-55. The plain meaning of "independent processes" are independent of each other and the processor. This is because grammatically speaking "independent" modifies "process" which is its plain meaning, and, as the Board points out - the specification supports both. Institution Decision at 16. EX 2020 ¶52.

The proper construction of "*power converter*" is "a converter which changes a voltage level to another voltage level" which is consistent with Patent Owner's litigation definition (EX. 1012, 2023) and the specification. See, for example, EX. 1001 8:64-67. EX 2020 ¶53.

B. Ground 1—Based on *Lyke*, *Dehkordi*, *Franz*, and *Faura*

Petitioners' combination in Ground 1 of *Lyke, Dehkordi, Franz, and Faura*[6] fails to teach or suggest, among other deficiencies, a "*gate array coupled to the processor and configured to run independent processes in parallel with the processor*" as specified in claim 1 (element 1.5) which was a point of novelty described in the '177 Patent. Claims 2 -5 and 10-12 are patentable for at least the same reasons as claim 1. EX 2020 ¶54.

Xilinx offers only two references for the proposition that element 1.5 would have been obvious to a POSA at the time of the inventions described and claimed in the '177 Patent: *Lyke* EX. 1003 (*see* Petition at 27-28,) and *Dehkordi* EX. 1004 (*see* Petition at 28-29). Institution Decision a 26-27. But neither *Lyke* nor *Dehkordi* teaches or suggests this novel feature. EX. 2020 ¶55.

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[6] There are no other combinations enumerated in Ground 1 including the general knowledge of an ordinary artisan.

Lyke (EX. 1003)

As noted by Petitioners, Patent Owner was indeed very familiar with the '399 Patent. *See* Petition at 4-5. Patent Owner made no attempt to hide or conceal that fact. The '177 Patent describes the '399 Patent's technology and its limitations in the section titled DESCRIPTION OF THE PRIOR ART. *See* '177 Patent at 1:5-2:8. EX. 2020 ¶56.

This attribution to the '399 Patent was based on the U.S. Air Force's desire to advance the '399 Patent technology and specifically commissioned Patent Owner through the Space Directorate CRADA (EX. 2001) to improve on the systems disclosed in the '399 Patent. EX. 2020 ¶57.

During the development period that began in 1998, numerous technical limitations of the systems of the '399 Patent were noted. For example, as specifically explained by the '177 Patent, the '399 Patent—and the AIC it describes—suffers from several limitations, such as its *inability to run parallel and independent processes*, and there was a need for a circuit design capable of executing multiple parallel processes in an independent fashion. *See* '177 Patent at 2:9-18. EX. 2020 ¶58.

> However, there are several limitations to the design in U.S. Pat. No. 6,148,399. First the AIC is not capable of performing parallel independent processes. Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

This theme is repeated throughout the '177 Patent's specification, such as at, *e.g.*, Ex. 1001 2:48-55 and 8:18-22. It is also a specific requirement in the claims, such as, for example, independent claims 1 (element 1.5), 6 (not challenged), 10 (element 10.5, and 15. *See* '177 Patent, *e.g.*, 10:61-64, 11:42-44, 12:44-46. EX. 2020 ¶59.

Given the lengthy discussion of the '399 Patent in the specification of the '177 Patent, its use during prosecution at the USPTO, including its extensive use of "FPGA" as a core search term in multiple searches, (EXs. 2007-2014) it is surprising that Petitioners nevertheless contend that the "*examiner apparently had not noticed Lyke's teaching of…* "*field programmable gate arrays*." Petition at 5. This unsupported speculation is belied by the intrinsic evidence (discussed in more detail below).

That is, when the USPTO studied the '399 Patent during examination it came to the same conclusion as Mr. Blemel. Namely, that the '399 Patent does not teach or suggest *a field programmable gate array coupled to the processor and configured*

to run independent processes in parallel with the processor. EX. 2006, USPTO Office Action p. 4-5, and Reply to Office Action dated 2-25-2005. Thus, Petitioner's suggestions to the contrary are entitled to little or no weight.

The same is true for the positions at pages 27 and 28 of the Petition. There Petitioners contend that, because a memory with program instructions might be used to program logic in the '399 Patent (*i.e.*, EX. 1003, 8:55-59), it necessarily means the FPGA runs independently in parallel. Not so. This has been shown to be an illusory requirement in connection with D1-D2 above. *Supra* at 17-18. *Halverson, which is not included in any Ground* also does not operate independently and thus suffers from the same deficiency, even if it could be used supply the missing feature. EX. 2020 ¶60.

A POSA would understand it is axiomatic that *every functional FPGA* must be programmed by a memory with program instructions and that such memory was likely external. Otherwise, the programmable logic gates are non-functional (a "blank device"). A set of unspecified "program instructions" does not confer on any given FPGA an unstated ability to run "independent parallel operations." In fact, as common sense would dictate, there is no mandatory connection between them and, notably, Petitioners have not produced any evidence other than conclusory expert testimony to substantiate its claim. For example, Petitioner's own reference, *Marchal* (EX 1035) explains that it "operates *whatever program is contained* in that

memory," with no other implications. *Infra* at 33. EX. 2020 ¶61. To contend otherwise is nothing more than a form of impermissible hindsight reconstruction.

Moreover, in failing to do so, Petitioners have not met their burden to show that the '399 Patent's "program instructions" must operate processes in parallel and independently. The Board seems to agree no such evidence has been provided (especially in view of D2 above). Institution Decision at 36.

The Board is correct that there is no discussion *at all* of how the FPGA is used in the '399 Patent. Institution Decision at 32. Therefore, it teaches little if anything other than its mere potential presence (no functions) - making it unsuitable for Petitioners' purpose. In fact, there is no discernable pragmatic use for the FPGA in the system of the '399 Patent at all, as explained below. EX. 2020 ¶62.

First, to the extent that there is any question whether the '399 Patent shows any independent parallel processes, the clear answer is no. As the '177 specification correctly notes, the '399 Patent runs from a clock controlled by the processor, making computing circuitry dependent on that processor-controlled clock. EX 1001 2:48-50[7]. Furthermore, neither the resistive or analog ASIC are capable of any

[7] The record demonstrates it is unlikely that the diligent PTO, that performed *eight different prior art searches*, that included the core search terms for *both*

"autonomous," "independent" or "parallel" operation[8]. For example, the '399 explains that the "resistive" ASIC is merely a set of "dumb resistors" such as a custom resistor IC that are passive circuit elements and whose only purpose is to conserve space. EX.1001; 8:49-53. EX. 2020 ¶63.

> A resistor ASIC is used in the AIC design to eliminate over 50 individual resistors. Its primary function is to provide support for the analog ASIC. Embedded passive elements within the interconnection system can also be used to further reduce floor plan congestion within the MCM.

FPGA devices of the '399 era do not supply features that relate to the implementation of resistors and are therefore unsuitable for the application requirements described in *Lyke*. Even if they did, the great cost, size, and power consumption disparity would strongly discourage such use (the FPGA being much larger, expensive and power intensive). EX. 2020 ¶64.

The analog ASIC in the '399 (EX. 1003 4:59-5:16) is described as implementing analog-to-digital converters (ADCs), digital-to-analog converters (DACs), a band-gap reference, and a proportional to absolute temperature

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"independent" and "FPGA," in multiple instances somehow missed both the object of the invention, as clearly stated in the SUMMARY OF THE INVENTION section, *and* the recitation of the FPGA in the '399 specification.

[8] Terms also all specifically searched for by the PTO. EXs. 2007-2014.

sensor. The DACs and ADCs require processor control. The reference and sensor are simple circuit elements, that are not capable of independent parallel processes. Moreover, FPGAs devices of the '399 era do not supply any of these sensors or measurement devices and are thus unsuitable for the requirements described in the '399 Patent. EX. 2020 ¶65.

Additionally, the '399 explains that "the use of *a separate integrated circuit* for analog functions *is important* as it permits better electrical isolation from ICs within the IC containing digital switching circuitry (*e.g.* the processor and memory components). Such an approach permits better control of the analog system electrical environment." EX. 1003, 4:67-5:59 (emphasis added). A POSA would understand that analog ASIC components are susceptible to electrical noise created by digital switching circuitry, including voltage spikes on power rails caused by inductive effects. Therefore, a POSA would not implement such analog functions on an FPGA of that era even if it were possible. Indeed, the '399 specification teaches away from such an implementation. EX. 2020 ¶66.

Accordingly, the '399 Patent's silence on the FPGA coupled with its unsuitability for use as an ASIC provides no support for Petitioner's position, and in fact, militates against it. However, one technical constraint is clear, even if an FPGA was added to the '399 system in an unspecified capacity, it would necessarily be

governed by the same processor controlled and suffer from the deficiencies that inspired the '177. EX. 2020 ¶67.

Therefore, *Lyke,* the intrinsic record, and all the supporting references relied on by Petitioners demonstrate the '399 Patent does not teach or suggest a "*gate array coupled to the processor and configured to run independent processes in parallel with the processor"* whether using Patent Owner's definition or any other reasonably appropriate definition. EX. 2020 ¶68. Conclusory statements such as those offered by Petitioners are not enough to substantiate its case. *See* Petition at 28; *see also Magnum Oil*, 829 F.3d at 1380. Petitioner cannot rely on "mere conclusory statements," but "must set forth 'articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR*, 550 U.S. at 418-19 (internal citation omitted).

Similarly, a petitioner cannot simply rely on an expert's unsubstantiated and conclusory opinions. *See* 37 C.F.R. § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Harmonic*, 815 F.3d at 1363 (affirming that Petitioner failed to establish obviousness where expert testimony "add[ed] nothing beyond the conclusory statements in [the] petition."). Neither Petitioners nor Dr. Shanfield substantiate the assertion that *Lyke* would operate in the way they suggest or how to overcome the technical incompatibilities that would result.

Additionally, it is noteworthy that Dr. Shanfield is not connected at all with the Air Force, James Lyke, and the AIC and was not involved at all with the work done under the Space Directorate CRADA. Indeed, the CRADA is not even mentioned in his declaration, was not part of his analysis, which Petitioners ignore, nor are the sections of the '177 Patent's specification that discuss the '399 Patent. Accordingly, Dr. Shenfield conclusory opinions conflict with the intrinsic record offered nearly 25 years after the development of the technology disclosed and claimed in the '177 Patent.

D1 (EX. 1004)

D1 is the only other reference offered by Petitioners for allegedly teaching parallel independent operation. D1 describes an MCM-based DSP subsystem that includes a Motorola 96002 DSP processor and Xilinx 4010 series FPGA shown below. EX. 2020 ¶69.

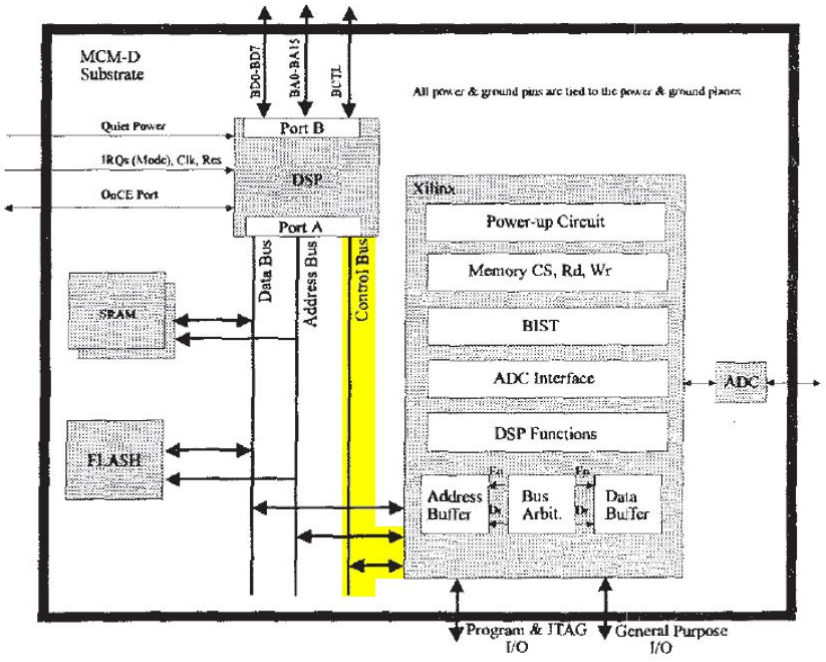


Figure 1. The Block Diagram of the DSP Sub-system.

As shown above, the DSP processor and the FPGA are connected through a *control bus* (highlighted in yellow) used to control the FPGA, with both components relying on the same clock, and which a POSA would understand were synchronized[9]. As such, the FPGA is *dependent* on the processor, and they are necessarily in a

[9] May also include synchronization signals, including for example the Transfer Strobe that is an output when the DSP is the bus master. See DSP96002_processor reference manual at PDF 12 (within the Port A,B bus pin definitions). Ex 1013 at 12.

dependent configuration. Consequently, no independent processes are possible during normal operation and neither the Petition nor D1 suggest otherwise. EX. 2020 ¶68.

This is consistent with D1's technical description that explains how the MCM subsystem is designed to exploit the multiprocessing capability *of the DSP processor*, which indicates that the FPGA operates in *a subservient support role* under the control of the DSP processor to maximize *the processor's* multiprocessing functionality by, *e.g.*, preprocessing incoming data *as directed by the DSP processor*. Neither Petitioners nor *Dehkordi* show any specialized connection or functionality that would suggest a different mode of operation. *See* EX.1004 at 1, FIG. 1 and its associated description in the "Design Flow" section. . EX. 2020 ¶71.

C. D2 (EX. 2019) in view of *Kostarnov* (EX 1036)

D2, a highly relevant reference not provided by Petitioners, is a follow up to D1 published a year later, that describes a closer to complete version of the MCM subsystem by the *same authors* regarding the *same MCM subsystem* and the *same testing features* that clarifies certain operations of the MCM subsystem and its testing. D2 *directly* contradicts Petitioners' case. FIG. 1 of D2 (EX. 2019) is simplified functional representation of FIG. 4, which is a more complete version of the MCM subsystem in FIG.1 of D1(EX. 1004). As annotated FIG. 1 of D2 shows, in normal operation (the "design for functionality" configuration -

highlighted in orange) the processor controls the entire subsystem including the FPGA, the memory and the other resources necessary to operate the system. Alternatively, in the special testing mode (the "design for testability" configuration - highlighted in green) it is the FPGA that controls the entire subsystem including the processor, the memory and the other resources. There is *no discussion* of bus arbitration in D2, which appears to have been abandoned as the MCM design changed as compared to D1. However, D2 does employ JTAG boundary scans (IEEE 1149.2). D2 at 167. There are no other modes of operation. EX. 2020 ¶72.

Thus, at no point does the D1-D2 MCM subsystem FPGA operate either parallel *or* independent processes. Either the processor or FPGA are in control. This confirms Sentient's position, that independent and/or parallel operation, among other things, is not shown in D1-D2. EX. 2020 ¶73.

Importantly, D1, Petitioners' *own asserted prior art* is a system that uses an external RAM-based configuration where the FPGA **does *not* run independently or in parallel with the processor**. EX. 2020 ¶74.

Petitioners' own technical documentation illustrates this. When D2 is considered in view of *Kostarnov* (EX. 1036) - a publication referenced by Petitioners and Dr. Shanfield (but not used as a basis for any Ground) - illustrates the relevant mode of operation in D2 is the "Functional Unit Mode" of the Xilinx 4013 FPGA from *Kostarnov*. As shown, the FPGA receives instructions from the CPU

confirming that it is *not* operating independently in parallel. . There, he makes no assertions that the FIG. 2 Functional Unit Mode configuration is operating independently in parallel with the processor. Nor can he; the references themselves clearly explain they are not. For example, in *Kostarnov* at 4, FIG. 2 the FPGA is controlled by the CPU and all data bus operations are controlled by the CPU. The FIG. 2 architecture receives instructions (in orange) only from the CPU indicating that it is a unidirectional (one-way) path. *See* EX. 1036 at 3-4. Thus the "Datapath Mode" mentioned in *Kostarnov* is not relevant to the operation of the D1-D2 MCM subsystem and POSA would clearly understand it as such and that no such operation is shown or suggested. EX 2020 ¶75. *Cf.* Institution Decision at 30.

This is illustrated below by comparing the first operating mode of D1-D2 the "design for functionality" mode with Functional Unit Mode of *Kostarnov* which is the most relevant. EX 2020 ¶76.

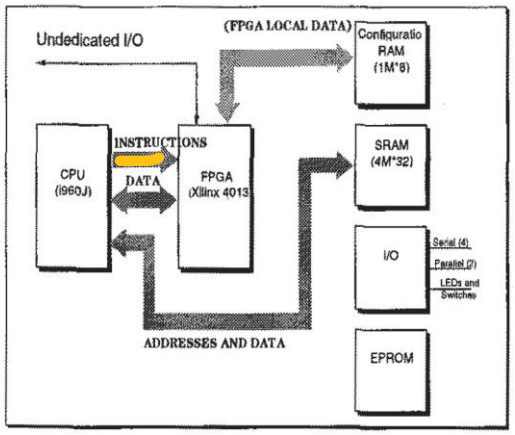


Fig. 2: Functional unit mode

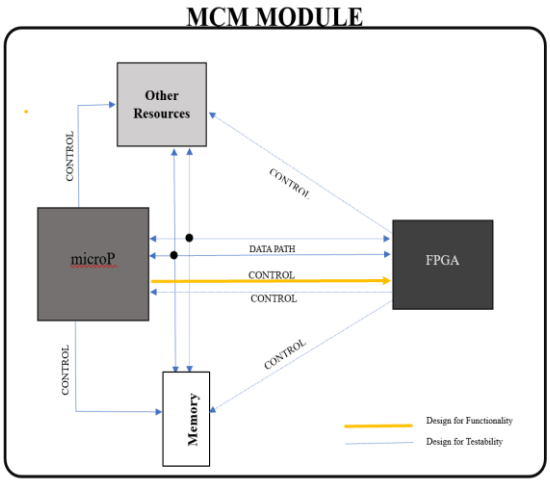


Figure 1 : Designing for Testability for a Typical MCM.

As is clearly apparent from the above, D1-D2 operates under the control of the processor, meaning that its FPGA neither operates independently or in parallel during normal operation. Thus, in light of D2, D1 is not operating independently or in parallel. In the other mode (design for testability), the FPGA in control and the opposite is true – that is the CPU is under FPGA control. EX 2020 ¶ 77.

Accordingly, for the reasons above, D1 does not show or suggest "*gate array coupled to the processor and configured to run independent processes in parallel with the processor"* whether using Patent Owner's definition or any other reasonably appropriate definition. EX 2020 ¶ 78.

D. D1 Theoretical Testing

D1 at 3, does theorize about *a special testing mode of operation* that uses the well-known industry standard JTAG and TAP testing methodologies for testing the operation of the DSP subsystem. During JTAG and TAP testing operations,

however, an external JTAG computer or other similar common controller is required to control both the DSP processor and the FPGA during testing. Independent parallel processing (such as that alleged is Datapath Mode on *Kostarnov)* is not shown or suggested. *See Dehkordi* at 4. EX 2020 ¶ 79.

Cost & Testing Issues

* * * * *

Due to their small feature sizes, MCMs cannot easily be probed or reworked [8]. Therefore, testing and fault isolation becomes a challenging area for MCM designs. Complete boundary scan testing was not feasible for this MCM since only the FPGA supported JTAG. The DSP supports a serial emulation port which was connected to the module pins along with the FPGA TAP port for testing purposes. The FPGA has a RAM-based configuration where the configuration may come from outside the module. A portion of the FPGA is configured for multi-processing bus arbitration and is connected to the internal data and address bus on the module. The FPGA can easily be reconfigured to route these lines to the module pins for possible probing and debugging during testing. The DSP has a dual data and address port architecture in which the second port was also connected to the module pins for enhanced multi-processing and testing. Testing procedures are being constructed at the time of this publication.

Accordingly, because JTAG is control of FPGA which controls DSP they are both under *common control of another device* while under test, they do not operate any *independent processes*. This is confirmed by Xilinx's own JTAG/TAP documentation used for the 4010 series FPGA. *See* EXs. 2002-2005. EX 2020 ¶ 80.

Moreover, it is important to note that the testing procedures described in D1 and relied on by Petitioners are *only speculative*, as D1 explicitly explains that "[t]esting procedures [were] being constructed at the time of [*Dehkordi's*]

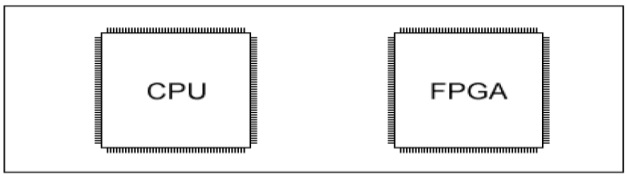
publication." *See* D1 at 4. Nor does D1 establish that such procedures were ever completed or, if they were, that they operated as hypothesized. In fact, the reference itself confirms as of the publication date of D1, the MCM system itself was still in fabrication and its overall operation and including yet to be formulated testing procedures, theoretical and therefore not enabled. This is significant because, as explained below, the references themselves teach away from and directly conflict with Petitioners' unpatentability allegations. EX 2020 ¶ 81.

E. JTAG Testing

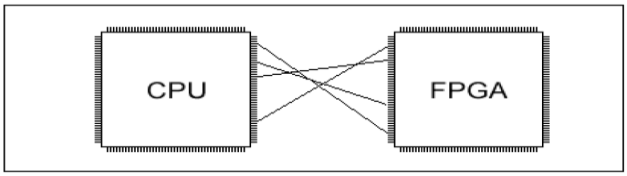
JTAG testing is very well known in the art and was developed in the early 1980s to test continuity and basic functionality of circuits as designs became increasingly more complex and difficult to probe and troubleshoot manually. JTAG testing relies on an external computer to make connections between the components under test by applying various test signals as specified by the JTAG program to confirm continuity and functionality. This is shown below with excerpts from EX. 2002 illustrating how a system, such as an MCM, with both an FPGA and processor are tested via JTAG. EX 2020 ¶ 82.

Boundary testing

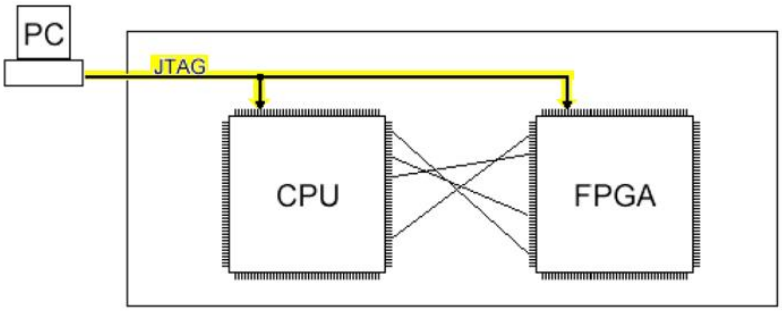
Here's a simple electronic board (also called "PCB" for "printed circuit board") with two ICs ("integrated circuits"), a CPU and an FPGA. A typical board may have many more ICs.



ICs can have lots of pins. So of course, ICs are connected together with lots of connections (PCB traces).
We show just four here. But you can easily have a few thousands on a PCB.



hand. So JTAG was created.



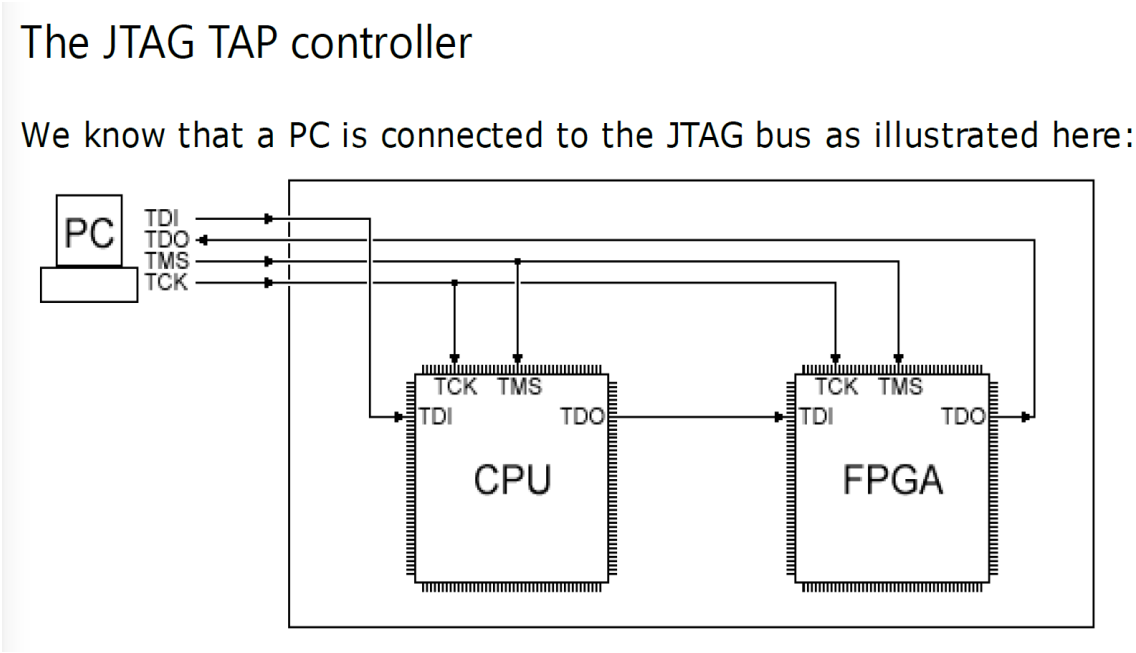
JTAG can take control (or hijack) the pins of all the ICs. On the picture, maybe JTAG is going to make all the CPU pins outputs, and all the FPGA pins inputs. Then by sending some data from the CPU pins, and reading the values from the FPGA pins, JTAG can make sure that the board connections are fine.

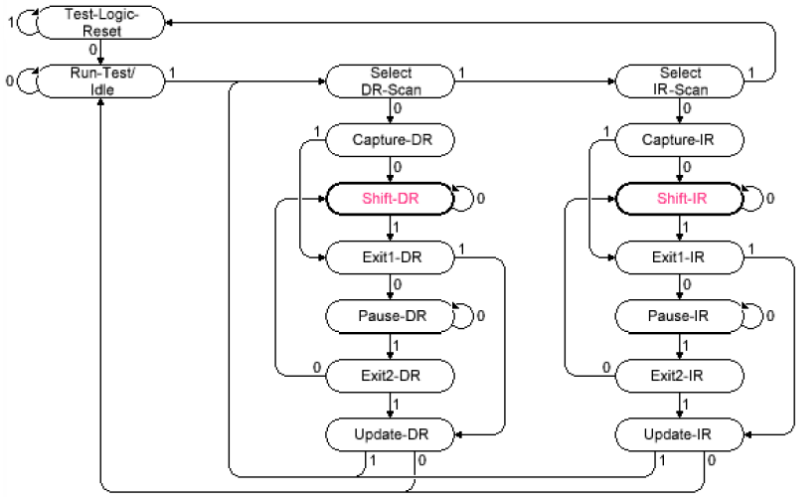
As can be seen from EX. 2002, the JTAG PC takes control of the pins *of all of the ICs* (FPGA and processor) through the JTAG connection highlighted in yellow above. This illustrates both the CPU and FPGA are under the common control of another device and therefore not independent. The JTAG PC then conducts testing

by controlling the flow of data and commands to and from both the processor and FPGA. During this process, both devices are always under the common control of the JTAG PC and thus *never* operate *independently.* EX 2020 ¶83.

F. TAP Testing

TAP testing is merely a more sophisticated form of JTAG testing that relies on the same architecture and control methodology. As shown below in excerpts from EX. 2003, the same connections from the JTAG PC go to both the FPGA and processor as generally illustrated in EX. 2002 except implements a more detailed testing procedure involving a TAP state machine having 16 states as shown in the flowchart below. EX 2020 ¶84.





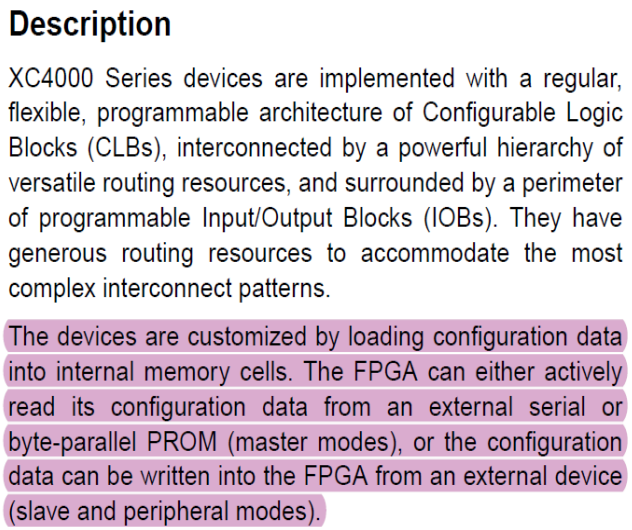
The consequence is that the FPGA and processor are again both controlled by the JTAG PC, which merely implements a more thorough TAP methodology. As explained, "all TAP controllers move together (to the same state)" thus demonstrating that both the FPGA and processor are under common control and never operate independently.[10] EX 2020 ¶85.

Moreover, Bus arbitration is not equivalent to independent operation, nor is independent operation required for bus arbitration. The only place that D1 mentions bus arbitration is in the section related to JTAG/TAP testing. D1 at 3. Notably, however, D1 does not mention anything about independent or parallel operation

[10] The content of EXs. 2002 and 2003 are confirmed by Xilinx's own references which contain the same materials. EX. 2002 is confirmed by the content of EX. 2004, with EX. 2003 confirmed by EX. 2005. EX 2020 ¶ 86.

anywhere, including during JTAG/TAP testing. Simply put, D1 does not teach independent operations. EX 2020 ¶ 87.

Moreover, the Xilinx 4010 datasheet (EX. 1014 at 6) explains that whenever data are written into the FPGA, as is the case with JTAG/TAP testing, it acts in slave and peripheral modes—confirming yet again that the FPGA does not operate independently. EX 2020 ¶ 88.



Description

XC4000 Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

Franz (EX. 1005) and Faura (EX. 1006)

Neither *Franz* nor *Faura* cures the deficiencies of *Lyke* and D1. Accordingly, Petitioners' proposed combination of D1, *Lyke, Franz, and Faura* in Ground 1 fails to teach or suggest a "*gate array coupled to the processor and configured to run independent processes in parallel with the processor*" as specified in claims 1 (element 1.5) 10 (element 10.5). Thus, claims 1-5, 10-12 are patentable for at least this reason alone. EX 2020 ¶ 89.

Halverson (Ex.1025), Marchal (EX.1035), Lyke and D1 All Do Not Show Independent Operation Which is Not Common Knowledge

In forming his opinions, Dr. Shanfield relies broadly on his assertion that that FPGA independent operation based on external configuration was common knowledge. However, there is no substantial evidence on the record that supports that assertion. In fact, the opposite is true. As discussed above, D1 in view of D2 *does not run independently or in parallel with the processor* despite being externally configured. This is also true for *Halverson* and *Marchal*. The same is true for *Lyke* because despite external configuration – it still operates on a processor-controlled clock. EX 2020 ¶ 90.

Halverson does not disclose *independent parallel processing* but rather discloses *just* parallel processing. Dr. Shanfield does not assert that *Halverson* shows *independent* parallel processing. This observation is also corroborated by the fact that the USPTO found *Halverson* during examination but decided not to use it as a basis for a rejection. *See* EX. 2014; EX 2020 ¶ 91.

Furthermore, *Halverson* itself also explains that its system processor and FPGA devices *do not operate independently*. *Halverson* at 9:62-10:3 describes the port 1 register that appears in Fig. 14. All bits of the register are set to values of "1" when the machine is reset. Fig. 14 describes the register bit P1.1 as "START mP Run = 0, mP Rset = 1". The minimal processor (implemented by a Xilinx 3090

FPGA as shown in Fig. 10) is dependent on the system processor to set P1.1 to value 0 in order for the minimal processor run, 10:2-3. In view of this dependency, the other FPGA(s) in *Halverson* (e.g. Fig. 2 FPGA labeled 304) which have their operations directed by the minimal processor, are also *necessarily dependent* on the minimal processor and the system processor by implication. EX 2020 ¶ 92.

Importantly, *Halverson*, like D1, is another system that uses an external-based configuration where the FPGA configuration *does not run independently or in parallel with the processor – again disproving Petitioner's theory* at externally configured FPGAs must operate independently. EX 2020 ¶ 93.

Marcha1 (EX. 1035) – also does not relate to independent processes. Indeed, the term independent does not appear in *Marchal*, nor does process. Petitioner and its expert acknowledge the distinction between these two devices in EX. 1035, 1; see also EX. 1035, 2-3 (describing loading the FPGA configuration string from "memory"). The FPGA merely loads this configuration (the program) and then operates *whatever program is contained* in that memory - which has nothing to do with independent or parallel operation. EX. 2020 ¶ 94.

Kostarnov (EX. 1036) Is Not Used as the Basis of Any Ground

There is no evidence on the record that FPGAs operated independently in parallel let alone this was "common knowledge" or "a standard way that FPGAs were deployed with processors" as Petitioner contends. In fact, as established above,

all Ground 1 references teach otherwise, with the alleged exception of background reference *Korstanov*. Thus, Petitioners have failed to establish this feature was common knowledge of one of ordinary skill rather than isolated specialized reference. EX 2020 ¶ 95.

Petitioners were aware of this at the time of their petition but chose not to use *Korstanov* as a basis for any Ground[11]. Petitioner cannot combine the features or teachings of *Korstanov* to *Lyke* or *any other reference* in the Petition to arrive at a conclusion that any challenged claim is unpatentable. Petitioner is required to identify "the *grounds* on which the challenge to each claim is based." 35 U.S.C. §312(a)(3); see also 37 C.F.R. § 42.104(b) (requiring petitioner to identify "the

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[11]Further, Petitioner does include the general knowledge of a person of ordinary skill as a basis for combination in Ground 1. See, *e.g*., Petition at 1. Even at page 28 it relies on *Kostarnov* merely as a support reference. The word "combine" or "combination" is not used anywhere (including EX. 1002 ¶83) as opposed to the express use of combinations involving four references relied on in Ground 1. Indeed, the Board only cites the references included in the Ground as basis. Institution Decision at 7-8 and 26-27. Thus, no such *combination* or Ground involving *Kostarnov* is presented.

patents or printed publications relied upon for each *ground*" and "where each element of the claim is found in the prior art patents or printed publications relied upon"). *Apple, Inc. v. MPH Techs. OY.*, No. 2021-1355, 2021-1356, 2022 WL 4103286, *7 (Fed. Cir. Sep. 8, 2022) "we held the Board erred in instituting *a ground* … 'because [Petitioner] did not advance *such a combination* of references in its petition.'" *Id* (emphasis added). Thus, the Board's statement that "Kostarnov *teaches or suggests* running independent process in parallel…" (emphasis added) appears to be legal error and any reliance on features provided by *Korstanov in combination* with other references or to "teach or suggest" such features must be rejected as procedurally improper. Institution decision at 31[12].

G. Ground 4—Based on Lyke, Dehkordi, Franz, Faura, and Steele

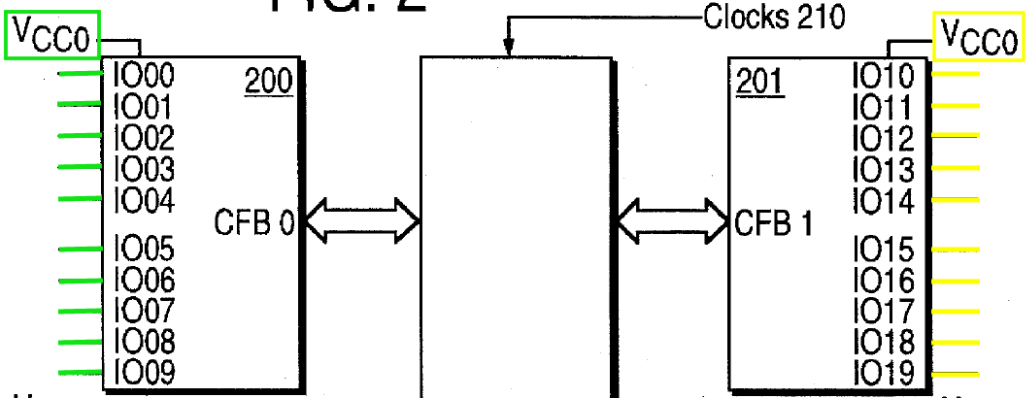
Ground 4 is simply the references of Ground 1 further combined with *Steele*. Accordingly, Ground 4 suffers from all the same deficiencies as noted above with

[12] *Cf.* Institution Decision at 33, regarding alleged "knowledge of an ordinary artisan" which attempts to *add features* from *Korstanov* and *Halverson* that are clearly absent from *Lyke* (and Lyke and *Halverson* being shown not operate independently, *Lyke* requires a processor controlled clock (ALOGCLK FIG. 12 EX 1003) despite petition not specifying such a combination.

respect to Ground 1. Claims 5, 10-11, 13-14, 15, 17, 19-20 are patentable additionally because Steele fails to show or suggest a "*power converter*" as specified in these claims. EX. 2020 ¶ 96.

Steele describes a programmable logic device configured to operate like a voltage replicator that distributes an applied input voltage for output at other pins. Simply stated, *Steele* operates by accepting an input voltage generated at an external source at the VCCO pin of a Configurable Logic Block (CFB) and merely *distributes that voltage* at the input/output (I/O) pins for to external devices. This is explained at EX. 1009 at 4:28-43, and is shown in the annotated version of FIG. 2 below where green represents a 5V level (CFB 0) and yellow represents a 3V level (CFB 1). EX 2020 ¶ 97.

FIG. 2



Notably, *Steele does not* generate the applied VCCO voltage levels itself, but rather merely uses them. The voltage generation is done elsewhere on another

external device and those voltages are applied to the VCCO input from that external source for reproduction by *Steele*'s CFB. Steele *does not* convert power because it does not change one voltage level to another as the claims require under Patent Owner's claim construction. Instead, *Steele* merely *distributes the same* voltage level applied VCCO at the output I/O pins. For example, IO00-IO09 have 5V outputs whereas IO10-IO19 have 3V outputs. *See* EX. 1009, 2:22-26; 4:28-43. There is no change or *conversion* (*i.e.*, changing one thing to another – plain meaning). *Cf.* Institution Decision at 42. Merely distributing *the same voltage* eight times is not converting power, but rather is merely *distributing the same voltage* multiple times. EX 2020 ¶ 98.

This is different from the challenged claims of the '177 Patent, which require, *e.g.*, a portion of the gates in the FPGA to operate as an power converter capable of receiving an input voltage level and changing it to another voltage level as the claims require. *See, e.g.*, '177 Patent, claim 5. EX 2020 ¶ 99.

Steele does not *convert* power but rather merely *distributes* the *same* voltage level VCCO at the output I/O pins. For example, IO00-IO09 have 5V outputs whereas IO10-IO19 have 3V outputs. *See* EX. 1009 at 2:22-26; 4:28-43. Notably the phrase "power converter" does not appear in *Steele* nor does *Steele* describe converting power in any way. EX 2020 ¶ 100.

Accordingly, *Steele* fails to teach or suggest "[*a*] *... embedded power converter* **…**" for at least three reasons. The Petition fails to address the power conversion claim term which requires changing one voltage level to another different voltage level. Power conversion is not mentioned in the *Steele* reference. Petitioners never address what power conversion is or how it is accomplished in *Steele*. Further, such treatment and explanation are also missing from the reference itself. The Petition thus offers nothing more than conclusory statements that are unsubstantiated by any analysis or explanation based on *Steele* and must therefore fail. EX 2020 ¶ 101. *See Magnum Oil*, 829 F.3d at 1380, *infra*.

Third, no such combination would ever be made. Petitioners state that "*[i]n the combined system with Steele, a portion of the gates in the FPGA are utilized to carry out power conversion, for the predictable benefits described above, including obviating the need for separate converter hardware apart from the existent FPGA*." Petition at 48, emphasis added. But this statement is demonstrably wrong. As explained above, the VCCO signal that establishes the required voltage level is *not* generated by any circuitry in *Steele* instead is created externally. Petitioners admit this. *See* Petition at 48 ("*a plurality of different voltages can be supplied to the* V_{cco} *pins of different functional blocks, resulting in a plurality of different voltages*."). Emphasis added. EX 2020 ¶ 102.

Thus, Petitioners *admit* the VCCO voltages must come from *somewhere outside of Steele*. Therefore, *Lyke* alone provides all the necessary reference and operating voltages specified in the claim and *Steele* provides *no added benefit whatsoever* to the proposed combination. Accordingly, *Steele* is merely a superfluous, cumulative reference that belies the motivation for making the combination of Ground 4 which appears to be offered only for the sole (impermissible) reason of alleging unpatentability. EX 2020 ¶ 103.

Such a combination may therefore only be formed based on impermissible hindsight reconstruction. An appropriate obviousness inquiry *cannot involve even a "hint of hindsight." Star Sci., Inc.*, 655 F.3d at 1375 (*emphasis added*).

Accordingly, Petitioners' proposed combination of *Lyke, Dehkordi, Franz, Faura, and Steele* in Ground 4 fails to teach or suggest the limitations in independent claims 13, and 20 of a "*power converter capable of… generating… reference voltage*" (elements 13.6 and 20.1) or *an internal embedded power converter* (claim 15). Thus claims 5, 14-15, and 20 are patentable for at least this reason alone. EX 2020 ¶ 104.

H. Grounds 2, 3, and 5

Because Grounds 2-3 are based on Ground 1, claims 2 and 3 are patentable for at least the same reasons that claim 1 is patentable over Ground 1. Similarly, because Ground 5 is based on Ground 4, claims 12 and 18 are patentable for at least

the same reasons that claims 13 and 15 are patentable over Ground 4. Claims 2, 3, 12, and 18 are independently patentable. Patent Owner reserves the right to separately argue the patentability of those claims over Grounds 2-3 and 5. EX 2020 ¶105.

IV. THE PETITION IS UNSUSTAINABLE

All of the challenged claims are patentable over the prior art relied on by Petitioner. EX 2020 ¶ 106.

First, the prior art references relied on by Petitioners have either already been considered by the USPTO, are cumulative, or are irrelevant. Petitioners' primary reference, *Lyke*, was extensively considered and dismissed by the USPTO, as the disclosure and prosecution history of the '177 Patent along with other evidence such as extensive search history for FPGA during prosecution, demonstrates that the inventions disclosed and claimed in the '177 Patent are innovative improvements over *Lyke*. *See Infra*. Petitioners' attempts to rewrite the disclosure of *Lyke* and the story of Mr. Blemel's innovative research and development commissioned by the U.S. Air Force to improve on *Lyke's* AIC is founded in impermissible hindsight and flawed interpretations of the technology existing at the time. Simply put, Petitioner's extrinsic evidence cannot change the disclosure of *Lyke* nor the USPTO's consideration of that patent and its decision to allow the '177 patent.

Petitioner's arguments based on D1 are based on an incomplete MCM subsystem and speculative testing procedures that do not operate as Petitioners contend because the reference itself teaches that such testing procedures were still in development at the time of D1's publication and, in any event, it is well known that JTAG testing procedures preclude independent operation. Notably, the Petition and Dr. Shanfield do not discuss the JTAG/TAP aspect of D1 at all.

D2 was not included in the Petition which confirms the accuracy and compelling nature if Patent Owner's arguments which respect to D1 and *Lyke*.

Moreover, *Halverson* is cumulative of *Cloutier* (EX. 1040), which is a far superior reference to *Halverson* that deals with parallel FPGA operations and was cited by USPTO during prosecution and used by the Examiner as the basis for a rejection of claim 1 that was overcome. EX. 2006 at 5.

Further, *Franz* and *Faura*—the other references that Petitioners rely on in Ground 1—are not relevant to the patentable distinctions offered by Patent Owner here for Grounds 1 and 4. Nor do Petitioners offer *Franz* and *Faura* for the proposition that either teaches or suggests a "*gate array coupled to the processor and configured to run independent processes in parallel with the processor*" as specified in the challenged claims.

Marcha1 (EX. 1035) – Does not relate to independent processes. Indeed, the term independent does not appear in *Marchal*, nor does process. Petitioners and its

expert acknowledges the distinction between these two devices in EX1035, 1; see also EX1035, 2-3 (describing loading the FPGA configuration string from "memory"). The FPGA merely loads this configuration (the program) and then operates *whatever program is contained* in that memory.

Similarly, *Kostarnov* (EX. 1036) is not used as the basis of any Ground in the Petition, nor has Petitioners attempted to combine features from *Kostarnov* with *Lyke* or D1 provided any argument for why a POSA would be motivated to combine conbine Lyke and D1 in view of *Kostarnov* with the other references in Ground 1, including *Dehkordi*, or that there would be a reasonable expectation of success in doing so. Indeed, even if they were combined as proposed, they would still not produce the claimed invention.

V. RESERVATION OF RIGHTS

Sentient reserves all rights to make additional arguments in and present claim constructions and evidence with its Patent Owner's Response. Sentient's silence on any particular claim or limitation at this time is not a concession that the Petition's discussion of that claim or limitation is properly based. Accordingly, Sentient reserves the right to submit additional or alternative arguments of patentability, and nothing in this Response acts or should be construed to act as an admission, acquiescence, or estoppel on the merits of the Petition.

VI. CONCLUSION

For the reasons above, the Grounds in the Petition should be denied, and claims 5, 10-15, and 17-20 conformed as patentable.

Dated: December 21, 2023

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), Counsel for Sentient Sensors LLC hereby certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(b). According to Microsoft Office Word 2010's word count, this document contains under 14,000 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Dated: December 21, 2023

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CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, a true and correct copy of **PATENT OWNER'S RESPONSE AND EXHIBITS 2019 - 2024** are being served electronically on December 21, 2023, to the e-mail addresses of counsel below:

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