Enhancement of MCM Testability Using an Embedded Reconfigurable FPGA

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Abstract

The testability of an MCM can be enhanced significantly for very little cost whenever a reprogrammable FPGA component that is already embedded in the MCM for functionality is utilized for diagnostics. This approach can have some of the characteristics of a smart substrate which uses the scan cell beside–the–signal–path (BSP) methodology. The design and implementation of an MCM with this capability is presented along with descriptions of the self–test algorithms, fault isolation and real–time testing and monitoring that this method provides.

1. Introduction

One of the major obstacles inhibiting MCMs to be a widely accepted and mass–produced technology is testability. In most cases, MCM testing involves the verification of substrate interconnects, logical connections and IC interaction functionality. Testing methods for ICs are difficult to apply to MCMs since they often contain a heterogeneous mix of components. The testing of MCMs can involve the use of capacitive or resistive probing with flying probes, high-density probe cards or electron-beam probe testing, all of which can be expensive and time consuming. It is possible for the cost of testing to exceed the design and fabrication cost of the MCMs themselves [1, 2, 3, 4, 5, 6, 7, 8, 9, 10].

One method of reducing test cost and time, thereby reducing overall MCM cost, is the utilization of boundary scan features found on some ICs devices. If all devices on the MCM have boundary scan features, a complete substrate test is possible. Unfortunately, most IC devices, including custom designed chips, do not incorportate boundary scan circuits, so other methods of testing are needed [4].

Known good die (KGD) is an issue for MCM testability, since previously untested dies may be assembled in a MCM system. With the advent of different levels of KGD, the functionality of ICs in a MCM can be assured *at some level* depending on cost. However, the IC interconnects and system functionality must still be tested as a complete module. There are two drawbacks with depending on KGD for a MCM design. First, fully tested KGD of the highest level can be

*The authors gratefully acknowledge the support of DARPA grant DAAH04-94-G0004.

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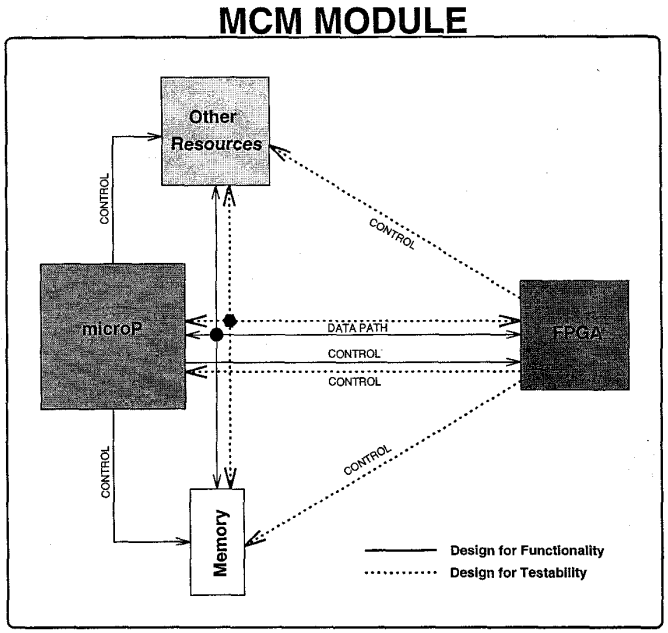

Figure 1: Designing for Testability for a Typical MCM.

relatively expensive compared to their IC packaged equivalents. This can substantially raise the cost of a MCM, thereby overwhelming the benefits of using thoroughly tested MCMs over an equivalent printed circuit board (PCB). Second, not all ICs on the market today are available as KGD at any level.

Section 2 of this report will discuss some of the testability features an embedded reconfigurable FPGA can provide and will very briefly describe the concept of BSP Smart Substrates. In Section 3, the design and implementation of a prototype MCM will be given to illustrate the versatility of a reconfigurable FPGA in enhancing testing. Conclusions are presented in Section 4.

2. Testing with an Embedded FPGA

MCMs with an embedded reconfigurable FPGA in the design can enhance its testability. As with some IC designs, the MCM system must be designed and planned for testability to maximize the effectiveness of the testing. As shown in Figure 1, the MCM design should not only consider functionality but also testability.

Critical signal paths can be connected to the FPGA I/O, and some of the FPGA logic can be configured as scan cells for boundary scan. This setup is similar to that of the BSP method for

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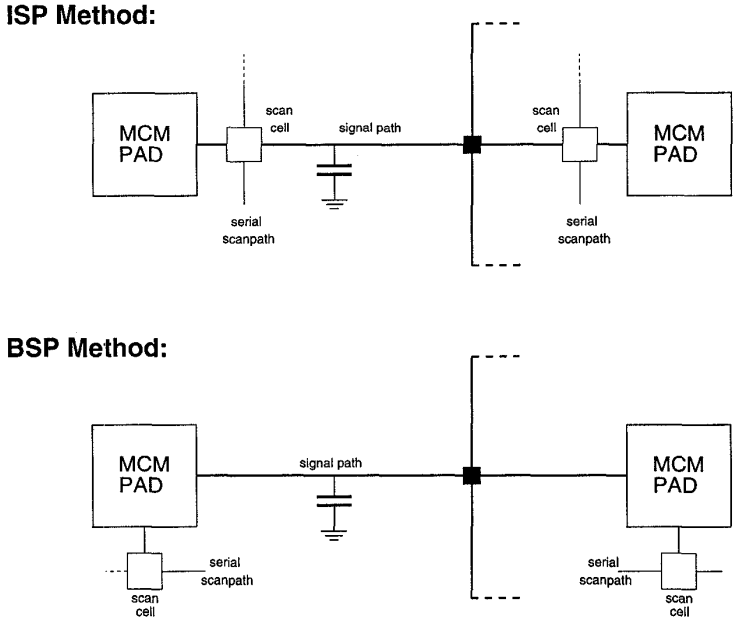

Figure 2: Placement of the Scan Cells In and Beside the Signal Path [4].

Smart Substrates. Smart Substrates have the potential to tolerate incompletely tested dies and can provide the means to control and monitor individual MCM dies from the module's pins. In the BSP Smart Substrate method, scan cells within the substrate are placed beside the signal path to be tested as shown in Figure 2. The figure also shows the ISP (In Signal Path) method scan cells, which has similiar benefits as the BSP method except the scan cells are placed in series along signal paths. Since the BSP method places scan cells in 'parallel' to the MCM pads, only a small capacitive load is seen during regular operation when the scan cells are disabled. The BSP method can provide the features of standard IEEE 1149.1 boundary scan, and can allow for bare substrate tests [3, 4]. However, BSP testing using an embedded FPGA would be possible only after final assembly of the dies onto the substrate so bare substrate tests would be impractical. Fortunately, the I/Os on some FPGAs can be tri-stated to reduce capacitive effects on signal lines.

Careful planning for testability, proper connectivity and configuration of the FPGA not only can allow for an emulated BSP methodology, but can also allow thorough testing of the MCM in its environment. The FPGA can be configured as a pseudo built-in logic analyzer that can monitor core dies within the MCM in real time. This allows testing of not only the hardware aspect, but also allows monitoring of software execution in a limited manner. Moreover, a FPGA can be configured as a self-tester for the module by creating stimuli and monitoring results. If the FPGA has access to the external I/O of the module itself, testing results can be sent as output and observed as they become available. With the proper reconfigurable resources and

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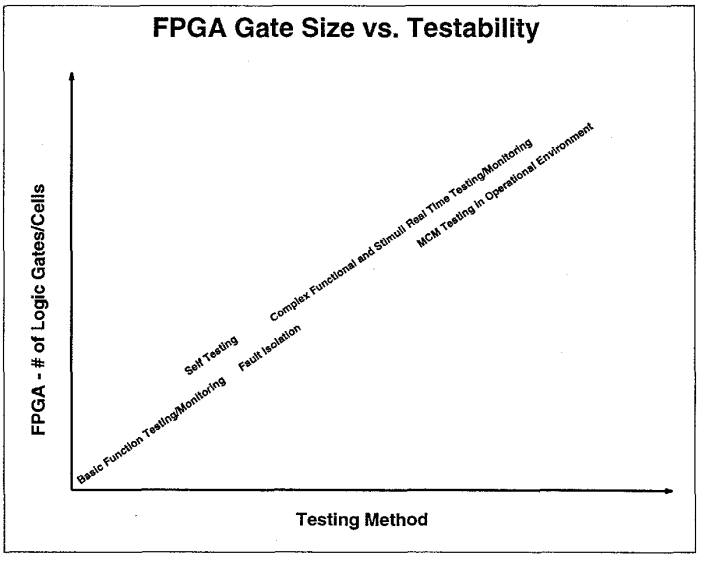

Figure 3: FPGA Gate Size vs Complexity of Testing.

connectivity, the FPGA can provide all of the above forms of testing in a virtually self-contained unit.

It has been stated above that the testability of a MCM can be enhanced with an embedded FPGA with the proper connectivity and configuration. The question arises as to what size (number of logic gates/cell blocks) FPGA to use and what connections must be made between the FPGA and other ICs on the MCM and between the FPGA and MCM I/O. The optimum size is dependent on the particular design and is currently under investigation for our specific example MCM described in the next section. The questions are important since a FPGA can occupy a significant amount a routing and substrate area. The size of the FPGA can depend on the complexity of the MCM and the desired complexity of testing required. Figure 3 gives a qualitative illustration of the spectrum of possibilities.

It can be assumed that there is no one setup that will work for all MCMs, as applications of MCMs vary. However, for processor-based MCMs, some common bases can be set. In a processor-based MCM, the critical signal paths will likely be the address and data buses. Therefore, the FPGA I/O should tap into those signal lines. In order for the FPGA to isolate chips for testing or fault identification, the FPGA needs access to the control lines of the other ICs. This allows the FPGA to turn off chips for isolated testing and enables an algorithm to identify a functionally faulty chip in the system. As with the BSP Smart Substrate method, the necessity of using KGD can be avoided. With proper rework facilities, faulty chips could be replaced on the MCM to increase yield. While other testing methods such as the BSP Smart Substrate method may tolerate the use of all untested dies, a FPGA used for testing would

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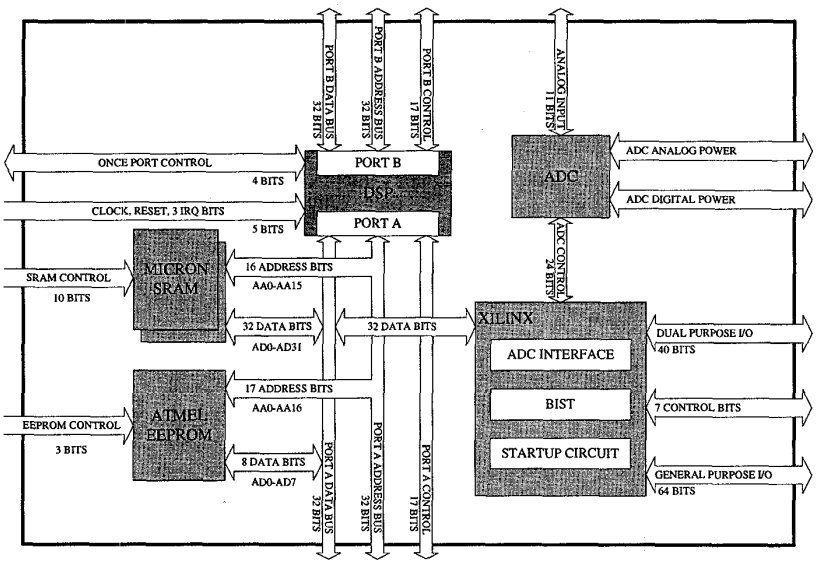

Figure 4: Block (Flow) Diagram of DSP MCM.

obviously have to be a KGD, perferably of the highest level.

In general, it would not be a wise decision to include a FPGA in a MCM design just for testing purposes since FPGAs can take up a significant amount of area on the MCM substrate. It is recommended that an embedded FPGA be used for testing purposes if a MCM core design already incorporates a reconfigurable FPGA in the unit. Unfortunately, design constraints may not allow an embedded FPGA to be used for testing. For instance, to perform testing of a MCM may require the FPGA to be larger in gate size, have more I/O or require additional routing within the substrate. The gate size of the FPGA can be increased without significantly increasing the overall size of the IC. However, even with the additional gates, using the FPGA for testing may still be impractical if additional routing is required and routing within the substrate is saturated. If a FPGA is included in a MCM design for resource or glue logic, and the design is adequately flexible to allow for additional routing and/or increases in FPGA gate and/or I/O size, design considerations in I/O routing must be made so that the FPGA can be established as a KGD. It is essential that the FPGA be tested to be a KGD before it is used to test the remainder of the MCM system. If the FPGA is not established as a high level KGD, it could be difficult to determine sources of random occuring faults. The ideal case would be to manufacture MCMs with high level, KGD FPGAs.

3. Prototype MCM

Figure 4 shows a block diagram of an MCM designed at the University of Tennessee [11].

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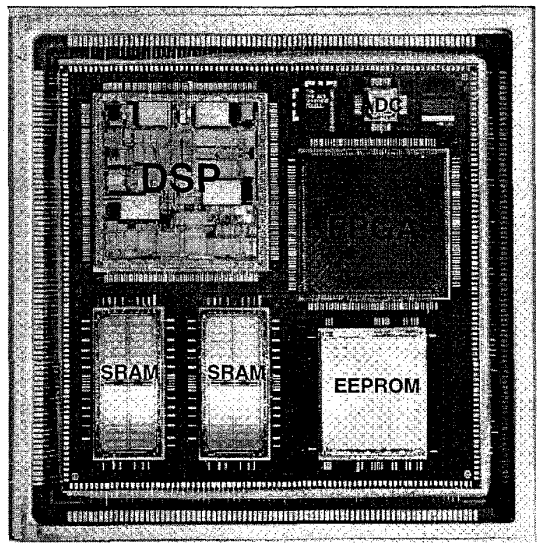

Figure 5: Photograph of the DSP MCM.

There are a total of six ICs on the MCM including a Motorola 32-bit digital signal processor (DSP). Figure 5 shows a photograph of the MCM which was fabricated by Micro Module Systems via the MIDAS Service. The other ICs include two Micron 64K x 16 SRAM, an Atmel 128K x 8 EEPROM, a Xilinx XC4010 series FPGA and a 12-bit Analog-to-Digital Converter (ADC) from the nearby Oak Ridge National Laboratory. Note that a full data bus (Port A) is interconnected to the Xilinx 4010 FPGA die within the module. Since this was an experimental prototype and none of the dies were KGD, most of the I/O of the FPGA (and other ICs) were brought out as external I/O for the module. This helps isolate ICs for testing and fault isolation. The MCM I/O of the FPGA are 'wrapped' back into the MCM for connection to the address bus (Port A) and control bus of the DSP processor and other ICs in the module. Some of the FPGA-MCM I/O can be used to communicate with the MCM's environment. A PCB is currently being developed to allow for these 'wrapped' back connections, to provide resources for FPGA configuration and to allow communication between the MCM and its environment. Figure 6 shows a block diagram of the PCB that will be used to provide this environment.

It is important to note that the FPGA in the MCM was not originally designed into the system for testability. The FPGA was deemed as necessary glue logic to provide operational resources for the system. For example, the FPGA provides logic for an address decoder, an interactive user I/O interface and the means for reconfigurable computing with the DSP processor. During the development process, concern for testing of the MCM became an issue. It was decided that with the flexibility of the MCM I/O and the proper environment, the FPGA could be used to test the MCM system.

Note from the PCB block diagram that auxiliary resources, such has an address decoder, are provided for the MCM. This is to help establish the FPGA as a KGD before it is used for testing,

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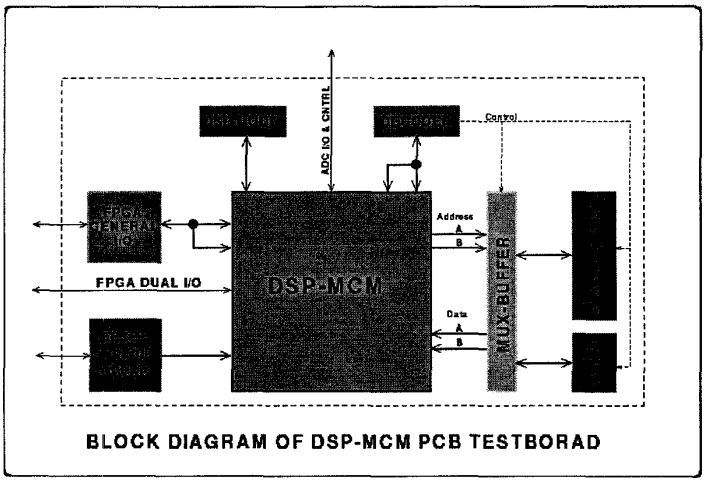

Figure 6: Block (Flow) Diagram of the Test Environment PCB for the DSP MCM.

and allow testing of the MCM to be continued regardless of certain faults that may occur within the module. Also notice from the diagram that there are 'wrapped around' connections on the PCB for the MCM. The 'wrapped around' routing, as described before, allows connections between the FPGA and the main address bus and the control lines of the other ICs, including the main processor unit. The PCB is designed to allow the FPGA to be the main interface between the MCM and its environment and will be used to establish the FPGA as a KGD at the functional, at-speed level.

Figure 7 shows the actual layout of the MCM testboard PCB. Note the many intervias between the MCM and PCB resources. The board is comprised of four signal layers and two (VCC and GND) power layers. This level of complexity is needed to provide the MCM a testing and functional environment. If the MCM were to be manufactured as a stand alone application unit, many of the 'wrapped around' connections (MCM to glue logic resources to MCM) would be fabricated with the substrate of the MCM. For example, on the PCB, address lines from the prototype MCM are traced to a PAL device, and then traced back to the MCM. This was necessary since an address decoder was not incorporated onto the MCM. The PAL would be configured as a custom address decoder. For an application, the address lines would be routed internally to the embedded FPGA, which would be configured as an address decoder, among other things. However, since this MCM was a prototype, most I/O lines within the MCM were routed to external pins to aid in testing of the MCM, and help establish ICs within the MCM as functional, partially functional or nonfunctional.

Once the FPGA is establised as a functional unit (KGD), testing of the MCM and its components can begin. One of the simplest testing that can be done is data monitoring (pseudo logic analyzer) with fault isolation. For example, the FPGA can be configured to 'turn off' all of the ICs except for the internal EEPROM and DSP processor. The Motorola DSP processor has a built-in boot algorithm that allows the loading of the 4K instruction set from a byte-wide memory source. Simple instruction codes can be loaded into the EEPROM. With the DSP initiated in

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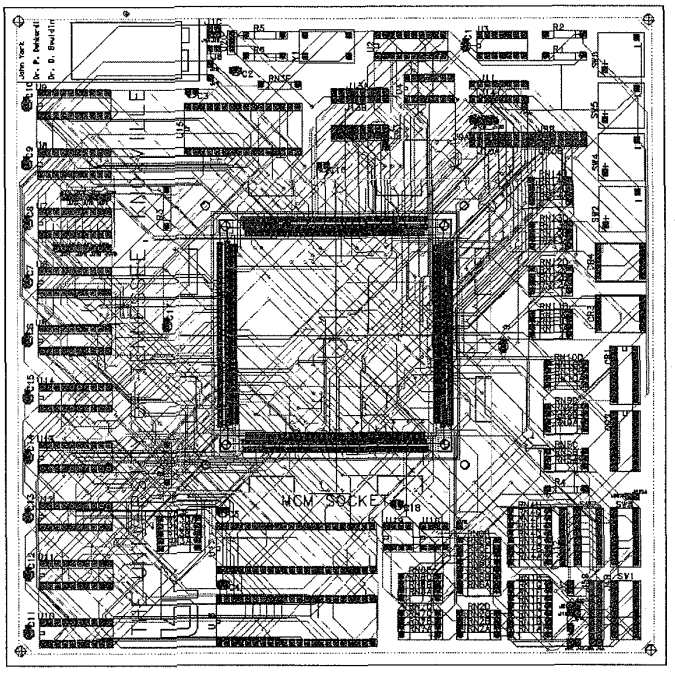

Figure 7: Actual Layout (Place and Route) of the PCB in Layout Tool (Mentor Gaphics)

the proper mode, transfer of address code and data (instruction code) can be monitored by the FPGA. Since the address bus has to go through the FPGA first for decoding, it can determine if the DSP processor is sending the proper addresses. This should be simple since the addressing will be sequential and an initial address value will be known.

Monitoring of the address bus will validate or invalidate not only the DSP's address capability, but also the routing lines from the DSP's address bus. If the instruction set within the EEPROM is kept to an alternating, repeating code, the FPGA can monitor the data bus for errors from the EEPROM. Since this particular FPGA has an internal system clock, it can stop operations once an error or fault is detected and notify its environment (PCB - LEDs) the probable cause of the error/fault. If the FPGA receives an incorrect address midway through the boot cycle, it can flag the DSP as the fault cause. Then, if an incorrect instruction code is seen, it can flag the EEPROM as the cause of the error. However, if incorrect address values and/or incorrect instruction codes are seen by the FPGA continuously from the start, it will be difficult to determine whether the device or the routing are at fault. In this case, a more complex algorithm will be needed for the FPGA to determine the difference between routing faults and device faults.

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4. Conclusions

MCM designs that include a reprogrammable FPGA for glue logic can have the benefits of enhanced testability. Even though additional design costs may be needed to consider using the FPGA for testing purposes, the benefits of testability can far outweigh those costs, depending on the interconnections and size of the FPGA in the design. Again, it is not recommended that an FPGA be incorportated into an MCM solely for testing. Design for testability utilizing an embedded FPGA is recommended only when an FPGA is already needed as a resource for the MCM system.

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