

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRO DEVICES, INC.,
and ATI TECHNOLOGIES ULC,
Petitioner,

v.

SENTIENT SENSORS, LLC,
Patent Owner.

Case IPR2023-00195
Patent 6,938,177

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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UPDATED EXHIBIT LIST

- 1001 U.S. Patent No. 6,938,177 to Blemel (“the ’177 patent”)
- 1002 Declaration of Dr. Stan Shanfield, Ph.D. (with Curriculum Vitae)
- 1003 U.S. Patent No. 6,148,399 to James C. Lyke (“**Lyke**”)
- 1004 P. Dehkordi, T. Powell and D. Bouldin, *Development of a DSP/MCM subsystem assessing low-volume, low-cost MCM prototyping for universities*, Proceedings 1996 IEEE Multi-Chip Module Conference (Cat. No. 96CH35893), 1996, pp. 89-94 (“**Dehkordi**”)
- 1005 G. A. Frantz, K. Lin, J. B. Reimer and J. Bradley, “The Texas Instruments TMS320C25 Digital Signal Microcomputer,” in IEEE Micro, vol. 6, no. 6, pp. 10-28, Dec. 1986 (“**Frantz**”)
- 1006 J. Faura, C. Horton, P. van Duong, J. Madrenas, M. A. Aguirre and J. M. Inerser, *A novel mixed signal programmable device with on-chip microprocessor*, Proceedings of 1997 IEEE Custom Integrated Circuits Conference, 1997, pp. 103-106 (“**Faura**”)
- 1007 U.S. Patent No. 5,663,734 to Norman F. Krasner (“**Krasner**”)
- 1008 U.S. Patent No. 4,279,020 to Ronald W. Christian et al (“**Christian**”)
- 1009 U.S. Patent No. 5,675,824 to Randy C. Steele (“**Steele**”)
- 1010 File Wrapper of the ’177 Patent
- 1011 Declaration of June Munford
- 1012 Claim Construction Order in *Sentient Sensors v. Cypress Semiconductor Corp.*, 19-1868 (MN), (Jan. 28, 2021, D. Delaware) (D.I. 89)
- 1013 Data Sheet for Motorola 96002 Digital Signal Processor
- 1014 Data Sheet for Xilinx XC4000E and XC4000X Series (including Xilinx XC4010)
- 1015 K. Avery and D. Alexander, *Recent progress in space-based micro-controller design*, 16th DASC. AIAA/IEEE Digital Avionics Systems

- Conference. Reflections to the Future. Proceedings, 1997, pp. 2.1-7 (“Avery”)
- 1016 T. Goforth, S. Cannon, J. Lyke, *Space Testing of the Advanced Instrument Controller*, Proceedings of the 13th AIAA/USU Conference on Small Satellites, Aug. 23–26, 1999, Logan UT, SSC99-XI-3 pp. 1-11 (“Goforth”)
- 1017 L. Muller, M. H. Hecht, L. M. Miller, H. K. Rockstad and J. C. Lyke, *Packaging and qualification of MEMS-based space systems*, Proceedings of Ninth International Workshop on Micro Electromechanical Systems, 1996, pp. 503-508 (“Muller”).
- 1018 K. G. Blemel, *Reactive Prognostic Management of Corrosion With Autonomous Sensors*. Paper presented at the CORROSION 2000, Orlando, Florida, March 2000.
- 1019 S. Hauck, *The Roles of FPGAs in Reprogrammable Systems*, Proceedings of the IEEE, Vol. 86, No. 4, pp. 615-638, April 1998
- 1020 Complaint in *Sentient Sensors v. Xilinx*, 22-cv-173 (D. Delaware) D.I. 1.
- 1021 Docket in *Sentient Sensors v. Xilinx*, 22-cv-173 (D. Delaware)
- 1022 Xilinx Notice of Stipulation Letter
- 1023 U.S. Patent No. 5,867,535 to William C. Phillips (“Phillips”)
- 1024 U.S. Patent No. 6,178,494 to Steve M. Casselman (“Casselman”)
- 1025 U.S. Patent No. 5,574,930 to Richard P. Halverson, Jr. (“Halverson”)
- 1026 U.S. Patent No. 5,872,960 to Oved Oz (“Oz”)
- 1027 T. Nishitani, I. Kuroda, Y. Kawakami, H. Tanaka and T. Nukiyama, *Advanced single-chip signal processor*, ICASSP ‘86. IEEE International Conference on Acoustics, Speech, and Signal Processing, 1986, pp. 409-412 (“Nishitani”)
- 1028 P. R. Christensen, et al. (2001), *Mars Global Surveyor Thermal Emission Spectrometer experiment: Investigation description and surface science results*, J. Geophys. Res., 106 (E10), 23823–23871 (“Christensen”)
- 1029 U.S. Patent No. 5,936,562 to Todd L. Brooks (“Brooks”)

- 1030 U.S. Patent No. 5,861,831 to Franklin M. Murden (“Murden”)
- 1031 U.S. Patent No. 5,638,092 to Tommy K. Eng (“Eng”)
- 1032 J. Faura, J.M. Moreno, M.A. Aguirre, P. van Duong, J.M. Insenser, *Multicontext dynamic reconfiguration and real-time probing on a novel mixed signal programmable device with on-chip microprocessor*. In: Luk, W., Cheung, P.Y.K., Glesner, M. (eds) Field-Programmable Logic and Applications. FPL 1997. Lecture Notes in Computer Science, vol 1304. Springer (1997) (“FauraMoreno”)
- 1033 Y. Tian, J. Ying, X. Ye, W. Gu, *DDGIPS: a general image processing system in robot vision*; Proc. SPIE 4212, Reconfigurable Technology: FPGAs for Computing and Applications II, Oct. 6, 2000 (“Tian”)
- 1034 U.S. Patent No. 5,874,834 to Bernard J. New (“New”)
- 1035 P. Marchal, *Field-programmable gate arrays*, Communications of the ACM, Vol. 42, No. 4 (1999), p. 57-59 (“Marchal”)
- 1036 I. Kostarnov, S. Morley, J. Osmany, C. Solomon, *A reconfigurable approach to low cost media processing*. In: Luk, W., Cheung, P.Y.K., Glesner, M. (eds.) Field-Programmable Logic and Applications. FPL 1997. Lecture Notes in Computer Science, vol 1304. Springer, Berlin, Heidelberg (“Kostarnov”)
- 1037 U.S. Patent No. 5,757,690 to Scott H. R. McMahon (“McMahon”)
- 1038 Analog Devices, ADuC824, MicroConverter, Dual-Channel 16-/24-Bit ADCs with Embedded FLASH MCU, 2001
- 1039 Analog Devices, ADuC824 FAQ, January 2001
- 1040 U.S. Patent No 5,892,962 to Jocelyn Cloutier (“Cloutier”)
- 1041 U.S. Patent Publication No. to 2002/0129191 to Behram DaCosta (“DaCosta”)
- 1042 de Lima, F.G., *Designing A Radiation Hardened 8051-like Micro-Controller*, Proceedings 13th Symposium on Integrated Circuits and Systems Design (Cat. No. PR00843), 18-24 September 2000 (“de Lima”)

- 1043 J. J. Wang et al., *SRAM based re-programmable FPGA for space applications*, in IEEE Transactions on Nuclear Science, vol. 46, no. 6, pp. 1728-1735, Dec. 1999
- 1044 U.S. Patent No. 5,936,971 to Ellyahou Harari (“Harari”)
- 1045 U.S. Patent No. 5,261,109 to Sudarshan B. Cadambi (“Cadambi”)
- 1046 T. Griffin, *Multichip Modules Including Processing: A Literature Survey*, Army Research Laboratory publication ARL-MR-257, August 1995
- 1047 J. Nedeau, D. King, D. Lanza, K. Hunt and L. Byington, *32-bit radiation-hardened computers for space*, 1998 IEEE Aerospace Conference Proceedings (Cat. No. 98TH8339), 1998, pp. 241-253 vol. 2
- 1048 Transcript of Board Call held August 1, 2023
- 1049 Declaration of Jeffrey Shneidman in support of Motion for *Pro Hac Vice* Admission
- 1050 Supplemental Declaration of Dr. Stan Shanfield, Ph.D.
- 1051 Joint Claim Construction Brief in *Sentient Sensors, LLC v. Cypress Semiconductor Corp.*, ECF No. 63 in 19-cv-01868-MN (D. Del.)
- 1052 NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS, IEEE Press, 1993 (highlighted definition: “parallel”)
- 1053 Wikipedia entry: microprocessor (December 18, 2023 version)
- 1054 U.S. Patent No. 5,317,696 to Rolf B. Hilgendorf (“Hilgendorf”)
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- 1056 D.A. Doane, P. D. Franzon, eds. *Multichip Module Technologies and Alternatives: The Basics*, Van Nostrand Reinhold, 1993 (“Doane”) (highlighted)
- 1057 M. Alderighi, F. Casini, S. D’Angelo, D. Salvi and G. R. Sechi, *A fault-tolerance strategy for an FPGA-based multi-stage interconnection network in a multi-sensor system for space application*," Proc. 2001 IEEE Int’l Symposium on Defect and Fault Tolerance in VLSI Systems, San Francisco, CA, USA, 2001, pp. 191-199. (“Alderighi”)

- 1058 Diessel, O., H ElGindy, M. Middendorf, H. Schmeck, B. Schmidt, *Dynamic Scheduling of Tasks on Partially Reconfigurable FPGAs*, IEEE Proceedings-Computers and Digital Techniques, vol. 147, no. 3, pp. 181-188, ISSN 1350-2387 (2000) (“Diessel”).
- 1059 J. Emmert, C. Stroud, B. Skaggs and M. Abramovici, *Dynamic fault tolerance in FPGAs via partial reconfiguration*, Proc. 2000 IEEE Symposium on Field-Programmable Custom Computing Machines, Napa Valley, CA, USA, pp. 165-174 (2000) (“Emmert”)
- 1060 W. Fornaciari, V. Piuri, *Virtual FPGAs: Some steps behind the physical barriers*, In: Rolim, J. (eds) Parallel and Distributed Processing. IPPS 1998. Lecture Notes in Computer Science, vol 1388. Springer, Berlin, Heidelberg (1998) (“Fornaciari”)
- 1061 L. Levinson, R. Manner, M. Sessler and H. Simmler, *Preemptive multitasking on FPGAs*, Proc. 2000 IEEE Symposium on Field-Programmable Custom Computing Machines, Napa Valley, CA, USA, pp. 301-302 (2000) (“Levinson”)
- 1062 M. Ade, R. Lauwereins and J. A. Peperstrate, *Implementing DSP applications on heterogeneous targets using minimal size data buffers*, Proc. 7th IEEE International Workshop on Rapid System Prototyping. Shortening the Path from Specification to Prototype, Thessaloniki, Greece, pp. 166-172 (1996) (“Ade”)
- 1063 Microsoft Computer Dictionary, 5th Edition (2002) (highlighted definitions: “MIMD”, “multiprocessing”)
- 1064 W. Stallings, COMPUTER ORGANIZATION AND ARCHITECTURE: DESIGNING FOR PERFORMANCE (Prentice Hall 4th ed. 1996) (highlighted)
- 1065 Deposition Transcript of John C. Peck
- 1066 U.S. Patent No. 5,978,260 to Stephen M. Trimberger *et al.* (“Trimberger”)
- 1067 Oxford English Dictionary (<http://www.oed.com>: “computational”)
- 1068 Comparison “redline” between POPR and POR as to Ground 4

I. Introduction

The Patent Owner (“Sentient”) does not contest that the prior art teaches every element of the challenged claims, except for two limitations in dispute. *First*, as to Ground 1, Sentient advances an outcome-driven claim construction for “independent processes.” In doing so, Sentient largely ignores both the Petition and the Institution Decision’s reasoning on this term. But the prior art teaches the claimed invention even under Sentient’s new construction, which renders the dispute mostly academic for deciding unpatentability.

Second, as to Ground 4, Sentient challenges the “power converter” element. But Sentient’s POR advances the same argument (nearly word-for-word) from its POPR. The Board has already explained why Sentient’s argument is incorrect. Petitioner asks that the Board find that these challenged claims are unpatentable for the same reasons it did on institution.

Sentient’s remaining attorney arguments do not move the needle. Petitioner respectfully requests the Board confirm its initial findings that all challenged claims are unpatentable.

II. Person of Ordinary Skill in the Art

Petitioner proposed that “[t]he POSITA of the ’177 patent would have been a person with a Bachelor’s degree in Electrical Engineering or Computer Engineering, or a related field, and at least two years of experience related to the design or

development of multi-chip modules operating as instrument controllers.” Pet., 7 (citing Ex. 1002 ¶¶ 24–26); ID, 10. The Board adopted Petitioner’s assessment of the level of ordinary skill in the art, “but without the qualifier ‘at least’ before the words ‘two years,’ and apply it for purposes of this Decision.” ID, 10.

For unexplained reasons, Sentient has now proposed the POSITA as a person having “a Bachelor’s degree in Electrical or Computer Engineering or an equivalent degree with at least four years of experience in FPGA and processor systems design including but not limited to system on a chip ‘SoC’ and electronic vehicle sensor systems or related technologies.” POR, 24-25.¹ While Petitioner does not believe Sentient’s formulation changes the obviousness analysis, EX1050 ¶¶14-16, the Board’s POSITA ruling may influence future proceedings, and so Petitioner explains further why the ID’s POSITA statement is correct.

The ’177 patent is not about “FPGA and processor systems design.” It is instead about multi-chip module design. *See* EX1050 ¶17 (citing EX1001, 3:26-30, 3:40-46). Nor is the ’177 patent about “system on a chip ‘SoC’ and electronic vehicle sensor systems.” In fact, the ’177 patent *distinguishes and contrasts* its “multi-chip module” invention *against* “system on a chip” or monolithic IC devices.

¹ Both experts agree that education may substitute for work experience. EX1002 ¶26; EX2020 ¶22.

EX1050 ¶18 (quoting EX1001, 3:55-60). As Sentient’s own expert explained, MCMs and SoCs are different, including that an MCM opens up “possibilities in the design and implementation space” not available in an SoC. EX1065, 15:12-18:6.

Similarly, the focus on “electronic vehicle sensor systems” is unwarranted in view of the ’177 patent’s examples. The ’177 patent discusses instrument controllers for “test devices and modules” used in space, EX1001, 1:24-30 & 1:44-51 as well as more than a dozen examples of instrument controllers that have nothing to do with electronic vehicle sensors. EX1050 ¶19 (quoting 1001, 9:8-18).

Nor does Sentient explain why it posits “*four years of experience*” instead of Petitioner’s “*two years of experience*,” or why it thinks the outcome would be any different based on two or four years of experience. *See also* EX1050 ¶13 (citing EX1056 and discussing experience of workers in the field).

In contrast, the ID’s POSITA statement is well matched to the ’177 patent’s description of background prior art. *See, e.g.,* EX1001, 2:34-44 (“[A]n *electronics instrument controller* designed in accordance with the invention includes a significant improvement in functionality and circuitry design *over prior art MCM controllers*”), 1:20-2:1 (discussing prior art “advanced instrument controller” MCM); *see also* EX1050 ¶10-12 (describing the types of problems in the prior art and known solutions as “fairly straightforward implementations of MCMs”, as supported by EX1003, EX1004, EX1015-EX1017). Even Sentient’s expert agreed

that “the POSITA would be familiar with the design of prior art multi-chip modules operating as instrument controllers.” EX1065, 14:7-11. The ID’s POSITA is correct. EX1050 ¶¶9-19.

III. Claim Construction

The claim construction issues for each ground are addressed below with that Ground. *See* §§IV.A, V.A.²

IV. Ground 1: The Prior Art Provides a “gate array...configured to run independent processes in parallel with the processor”

A. Claim Construction: “independent processes”

The plain meaning of an “independent process” is “a process that runs separately from another process.” (Independent processes is the plural form.) Sentient’s new proposed construction of “independent processes” is a flawed, result-oriented construction. Sentient argues that a “process” is “a computational process programmed into the FPGA gates [that] excludes initialization and power up

² Separately, Sentient makes an incorrect statement that Xilinx “changes its definition of ‘embedded.’” POR, 25. Sentient’s argument is peculiar because Sentient does not dispute the Petition’s showing as to “embedded.” Regardless, Xilinx used the same construction of “embedded” as construed by a prior court throughout the disputes. *See* Pet., 8, 24, 48-49.

sequences.” POR, 26. Sentient then argues that the term “independent processes” should be construed to mean both “without computational assistance from another” and “independent of each other and the processor.” *Id.* POR, 28. To these constructions, Sentient then bolts on an additional requirement that their proposed construction prohibits the gate array and the processor from being “connected through a *control bus*” (emphasis in original) or “relying on the same clock.” POR, 14, 38; EX1050 ¶¶34-35. Sentient’s complicated proposal is inconsistent with the intrinsic record and should be rejected.

1. “processes”

A POSITA would have understood the plain and ordinary meaning of “process” to include the meanings noted by the Board, including that a process includes “a segment of code that may be run independently” (EX3004, 469), or “[a] program or part of a program; a coherent sequence of steps undertaken by a program” (EX3002, 423). *See* EX1050 ¶¶47-59 (citing EX1001, EX3002-EX3004).

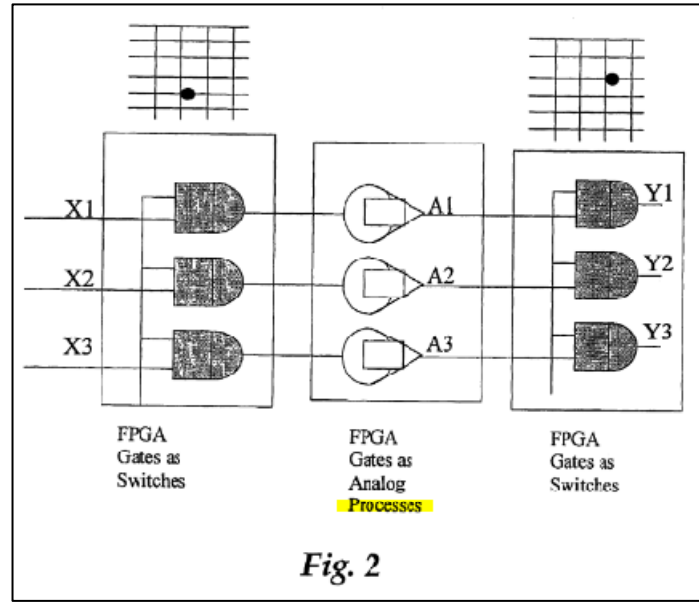
The ’177 patent does not provide a lexicographic definition of a “process” and instead discusses “processing” on an FPGA in terms of how the FPGA is configured to perform various tasks. EX1001, 4:45-49; EX1050 ¶¶47-55 (citing EX1066, 34:25-26 (referring to “a plurality of [FPGA gate] partitions, i.e., processes”); 34:55-65 (describing tasks running on the FPGA as “processes”); *id.* at 37:60-63 (same)).

In contrast, Sentient’s proposal (POR, 26) of “process” as “a computational process programmed into the FPGA gates” is circular and unsupported: *First*, it is a self-referential, defining a “process” as a “process.” *Second*, Sentient’s two citations to the specification do not provide insight, POR, 28 (citing EX1001, 8:16-32 & 9:19-35), and Sentient fails to engage with the extrinsic evidence. *See also* EX1050 ¶¶56-58 (citing EX1067; noting the definition of “computational is ‘relating to, or used for computation; relating to or making use of computers,’ which adds nothing in the context of the patent.”). *Third*, restricting a process to something “programmed into the FPGA gates” makes redundant the claim limitation that the process runs on “a plurality of gates arranged in a field programmable gate array.” EX1001, 10:4-7.

2. “independent processes”

(a) Plain meaning

The plain and ordinary meaning of “*independent* process” is “a process that runs separately from another process.” As the Board observed, the ’177 specification mentions “independent processes” when describing Figure 2. ID, 5 (“[T]he ’177 patent describes another type of “independent process” run by the FPGA—namely parallel processes within the FPGA that are independent of each other.”). *See also* EX1001, 8:16-32, Fig. 2:



The patent describes such processes as “independent configurations of a subset of gates within the FPGA,” i.e., they are processes that run separately. EX1001, 8:18-26; EX1050 ¶¶60-71. This plain meaning is supported by the file history and extrinsic evidence, as discussed next.

(b) “Independent Processing” in the File History refers to Multiprocessing

First, it is important to note the “independent processes” element was not a point of novelty during prosecution: The examiner found this element taught by Cloutier, EX1040. EX1010, 58. The applicant did not traverse this rejection or dispute Cloutier’s teachings and instead cancelled the affected claims. EX1010, 44.

Looking in more detail, the examiner’s rejection was not based on “control” or “clocking.” Instead, the examiner found that “Cloutier teaches a multiprocessor” and cited a paragraph where Cloutier explained the FPGA “can be programmed in a

wide variety of ways to perform a wide variety of applications [and] function as a parallel processor.” EX1010, 58 (citing EX1040, 2:65-67). That paragraph goes on to explain that the FPGA can function as a matrix of processing elements, each running a set of instructions. *See also* EX1050 ¶¶37-43 (citing EX1063, 354 (dictionary defining “multiprocessing” as: “A mode of operation in which two or more ... processing units carry out one or more processes (programs or sets of instructions) in tandem”)). Thus, during prosecution, the examiner and applicant were focused on multiprocessing, and not on processor clocking or control. *Id.*

**(c) Sentient Offers Two Conflicting Proposals,
Neither of Which Is Correct**

In contrast, Sentient proposes two incorrect constructions. Sentient’s first proposal, “without computational assistance from another” finds no support in the specification. EX1050 ¶¶72-73. Indeed, the words “computational assistance” (or even “assistance”) do not appear anywhere in the ’177 patent—or even again in the POR. Sentient’s two citations to the ’177 patent say nothing about “computational assistance from another.” POR, 28 (citing EX1001, 2:9-18 & 2:48-55).

Sentient’s second proposal, that “‘independent processes’ are independent of each other and the processor” also goes astray. EX1050 ¶¶74-78. Sentient’s only “support” for this construction is its identical expert declaration. POR, 28; EX2020 ¶52. As discussed below, Sentient adds in hidden unjustified limitations into its proposed construction.

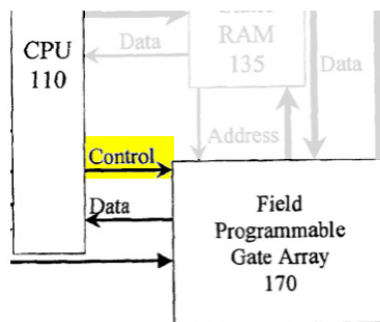
(d) “Independent Processes” Are Not Restricted by Control and Clocking

While largely ignoring the sections of the '177 patent addressing “independent processes” in the gate array, Sentient focuses its attention on the '177 patent’s description of Lyke’s “specialized ASIC” not being able to “run independently of the microprocessor.” This argument is misdirection.

First, the “independent processes” in the '177 patent claims are directed to what is running on the FPGA, not on a “specialized ASIC.” The fact that the '177 patent describes a “specialized ASIC” not being able to run independently does *not* describe whether “independent processes” run on the claimed FPGA.

As the ID noted, “[t]he '177 patent attributes Lyke’s alleged lack of independent processing to Lyke’s ‘need for a resistive ASIC.’ [EX1001] at 2:47–54.” ID, 4. *See also* EX1010,43 (applicant repeating the same statement in prosecution). Sentient describes Lyke’s “‘resistive’ ASIC is merely a set of ‘dumb resistors,’” apparently conceding that such an ASIC would not run processes at all. POR, 34; EX1050 ¶¶84. Moreover, Lyke’s disclosure of an FPGA went unnoticed by the applicant and examiner; in fact, Lyke’s FPGA would have operated in the same manner described by the '177 patent’s Figure 2, meaning that the applicant did not appreciate and/or accurately describe Lyke’s teachings. EX1050 ¶¶79-84 (citing EX1001, 8:16-32, Fig. 2).

Second, Sentient incorrectly embeds a notion of processor “control” in its claim construction. Sentient focuses on the presence of “control” signals found in the prior art as being relevant to the “independent processes” claim term, by presenting them as a purported counterexample. POR, 14-15, 38. But for claim construction purposes, the presence of “control” signals from the processor to the FPGA isn’t informative to whether the FPGA is configured to run “independent processes.” This is apparent from the ’177 patent itself: Figure 1 is described as “a preferred embodiment of the MCM Controller of the present invention.” EX1001, 3:34-37; EX1065, 18:16-19:1 (Sentient’s expert agreeing that “Figure 1 is an example of the multi-chip module that’s claimed in the ’177 patent”); EX1050 ¶¶85-87. Figure 1 shows a control line from the processor to the FPGA, and yet this is the same FPGA claimed to be running “independent processes”:

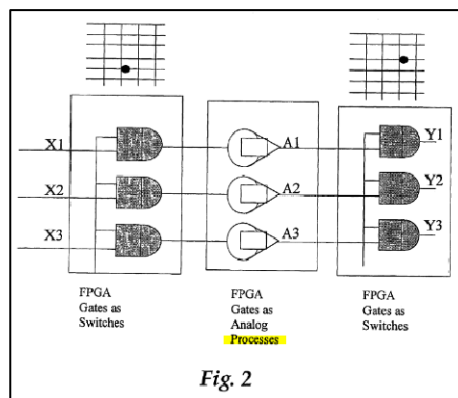


EX1001, Fig. 1 (extract, emphasis added). Thus, the presence of processor “control” doesn’t determine the meaning of “independent processes.”

Third, similarly, Sentient incorrectly embeds a notion of processor “clocking” in its claim construction. But the ’177 patent gives four examples of ways that its

FPGA could be clocked, with no comment that any of these four ways affects “independent processes.” EX1001, 4:49-51 & 7:64-8:1. For example, the ’177 patent describes its FPGA as potentially being “clocked using the same on-board VCO as the microprocessor” without identifying any effect on “independent processes.” *Id.* EX1050 ¶¶88-89.

Further, the patent’s affirmative example of “independent processes” undermines a definition based on clocking. EX1050 ¶¶90-92 (explaining that the ’177 patent statement that “when...A1-A3 are identical, then a form of functional redundancy is achieved, giving an increased fault tolerance” means the same clock is used to compare the simultaneously computed results; i.e., that “independent processes” may run on the same clock):



EX1001, Fig. 2 (highlighting added).

Lastly, the patent claim requires “independent processes” and not “independent hardware.” The statement that “Although [Lyke’s] AIC does include a specialized ASIC, *it* is controlled and clocked by the microprocessor and *cannot*

run independently of the microprocessor” (emphasis added) is a statement about Lyke’s particular ASIC hardware (as described above). It is not a statement about what it means for a *process* to be independent. Lower-level details like clocking and hardware control signals are typically not visible to a process or define independence of a process to another. EX1050 ¶¶93 (noting that “[a]t the level of a ‘process’ (i.e., ‘segments of code,’ or ‘programs or parts of programs’), a process typically will not have visibility into how it is clocked or initiated, but the processes can still be ‘independent’”; citing EX1061).³

B. Challenged Claims 1 and 4 Are Obvious Under Any Claim Construction at Issue

The prior art provides element [1.5] under any reasonable interpretation.

1. The Ground 1 Art Satisfies the Plain Meaning

(a) Dehkordi Provides the Challenged Element

Dehkordi provides multiple independent processes that run independently and in parallel from each other and the processor. Dehkordi depicts these independent

³ Although seemingly undisputed, Petitioner comments on “in parallel.” In a prior proceeding not involving the Petitioner, Sentient claimed that “the plain and ordinary meaning of the phrase “in parallel” is “at the same time.” EX1051, 71. Petitioner agrees that “in parallel” is such a temporal statement, consistent with the ’177 patent specification. EX1001, 7:45-50; EX1052, 914; EX1050 ¶¶44-46.

processes as separate blocks within the “Xilinx” FPGA in Dehkordi’s block diagram. *See* EX1004, Fig 1; *See also* EX1002 ¶84; EX1050 ¶¶96-104 (quoting EX1058, EX1061, EX1060); EX1058, 2 (describing “partitioning the FPGA logic resource so that each function or task obtains as much resource as it needs and executes *independently of all others* as if it were the sole application executing on a chip”); EX1060, 9; EX1061, 301.

In Dekhordi, the Xilinx FPGA runs multiple independent processes that do not overlap with each other, all at the same time as other operations happening on the Motorola DSP processor: Dehkordi teaches that “a portion of the FPGA is configured for multi-processing bus arbitration.” EX1004, 3. This “portion of the FPGA” runs an arbitration process to manage the flow of data throughout the remainder of the MCM, independently (e.g., separately) and in parallel (e.g., at the same time) to whatever computation is happening at other “portion[s] of the FPGA” or on the processor. EX1002 ¶84 (citing EX1045, 1:49-68; EX1004, Fig. 1 (showing “bus arbit[ration]” process in the Xilinx FPGA block)). Dehkordi also depicts additional independent processes, including the process controlling the analog-to-digital converter and power management processes.

Dehkordi also teaches that these FPGA processes are separate and simultaneous from what is running on the DSP processor chip shown in Figure 1. EX1004, 89 (“The [MCM] module was designed to exploit the multi-processing

capability of the 96002 [processor]. The FPGA is primarily a hardware pre-processor of incoming data, but also provides other generic logic functions required for implementation of the entire subsystem.”). Thus, Dehkordi discloses “in parallel” with regard to both the independent processes running during normal operation on its FPGA and between the FPGA and the DSP processor.

Moreover, Sentient’s own D2 reference (EX2019) confirms the POSITA would have known that Dehkordi would be used to implement separate processes during normal operation for “an address decoder, an interactive user I/O interface and the means for reconfigurable computing with the DSP processor,” EX2019, 170, as well as a “data monitoring” process described in detail. *Id.* at 171-72.

(b) Lyke Also Discloses the Plain Meaning

The prior art combination also provides the plain meaning of this limitation through Lyke. As pointed out in the Petition, neither the applicant nor the examiner noted Lyke’s FPGA teachings. EX1003, 8:55-59. *See* Pet., 27-28. *See also* ID, 32.

Lyke’s disclosure of using “RAM-based field programmable gate array(s) interfaced internally within the AIC and configured automatically through...access of the non-volatile memory” was sufficient to teach the challenged element to the POSITA, who would have come to Lyke with the common knowledge of a POSITA as reflected in exemplary prior art. EX1050 ¶¶105-109 (quoting EX1058, EX1061,

EX1060); EX1061, 301 (“to execute several algorithms...in parallel in one FPGA, i.e., true multitasking”); EX1062, 167.

The POSITA would have read Lyke with the knowledge of FPGAs, and would have seen Lyke’s explicit teaching of a “processor” coupled to a “RAM-based field-programmable gate array(s) interfaced internally within the AIC and configured automatically through...access of the non-volatile memory.” EX1003, 8:55-59. From this, the POSITA would have recognized that Lyke provided the “independent processes” limitation through the use of the disclosed FPGA. EX1050 ¶¶105-109 (quoting EX1058, EX1061, EX1060).

In sum, the ’171 patent inventor did not create anything new with this element: he simply took the inventions described and suggested by others (including Lyke, from which the ’171 inventor copied much of his patent, *see* EX1002 ¶29) and claimed it as his own.

2. The Ground 1 Art Discloses Sentient’s Construction that “‘independent processes’ [means] ‘without computational assistance from another.’”

For the same reasons laid out immediately above, the prior art provides this element under Sentient’s first proposed construction that “independent processes” means “without computational assistance from another.” POR, 28. *First*, the processes disclosed in Dehkordi are not operating with the “computational assistance” of another process. In Dehkordi, the resources of the FPGA are shown

partitioned across several different unrelated tasks. *See* discussion above, §IV.B.1(a). *Second*, as to Lyke, the presence of the FPGA configured from a separate non-volatile memory would have suggested to the POSITA that the programs running on the FPGA would run on their own, as described above in §IV.B.1(b). The POSITA would have read Lyke’s teaching with the background of how such a configured FPGA supports independent processes. EX1050 ¶¶110-114 (quoting EX1058, EX1061, EX1060).

3. The Ground 1 Art Satisfies Sentient’s Construction that “‘independent processes’ are independent of each other and the processor.”

The prior art also teaches this element under Sentient’s second proposed construction that ‘independent processes’ are independent of each other and the processor” for each of the reasons set forth above regarding Sentient’s “without computation assistance” proposal, as processes operating on the FPGA without computational assistance are independent of other processes, e.g., as depicted in Dehkordi or as suggested to the POSITA on reading Lyke with the background knowledge cited above. EX1050 ¶¶115-116.

4. The Ground 1 Art Satisfies Even if “independent processes” excludes processor “control” or clocking”

Nor does it make a difference to unpatentability if “independent processes” were (wrongly) construed to exclude processor clocking or control lines.

(a) The combination has independent clocking

To the extent a separate clock is required, the POSITA would have known that Dehkordi's "Xilinx 4010 FPGA" (taught in EX1004) had its own internal clock signal for use by programs running in the FPGA. EX1050 ¶¶117-124. Indeed, Sentient argues that EX2019 (which it calls the "D2" reference) is "a highly relevant reference" to understanding Dehkordi's teachings. POR, 17. *See also* EX1065, 24:15-26:19 (Sentient's expert explaining why it is "fair game to use D2 to evaluate what was known to the POSITA about Dehkordi," and that "D2 provides more detail in order for one to understand D[ehkordi]"). EX2019 explicitly says what was suggested in Dehkordi (and what was confirmed by the Xilinx 4010 manual), i.e., that the Xilinx 4010 "*has an internal system clock*," EX2019, 172.

In particular, EX2019 goes into detail explaining what the POSITA would already know, i.e., that the Xilinx 4010 allows processes to run on their own using its internal system clock:

Since this particular FPGA has an internal system clock, it can stop operations once an error or fault is detected and notify its environment (PCB - LEDs) the probable cause of the error/fault. [The] FPGA can flag the DSP as the fault cause.

EX2019, 172. *See also* EX1004, 3 (suggesting "fault isolation" and "possible probing and debugging" performed by the FPGA); EX1050 ¶120 (explaining that such tasks on the FPGA would require independence from the components being

monitored). In other words, EX2019, which Sentient argues as relevant and known to the POSITA, confirms that Dehkordi's FPGA had the ability to run processes using its own clock and without using the processor's clock. *Id.*, 171-72. *See also* EX1050 ¶¶120-124 (citing EX1014).

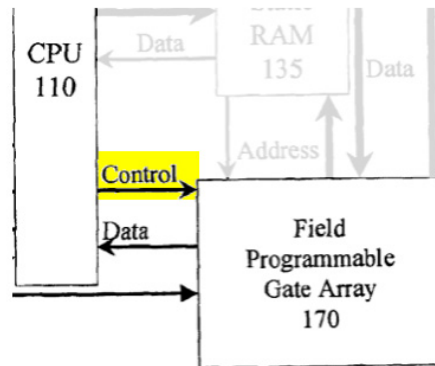
The independent clocking and operation described in EX2019 further supports Petitioner's record evidence. *See, e.g.*, EX1014, 6-46 (describing multiple modes of operation and internal clocking); *see also* ID, 37 (citing EX1014; noting that "XC4000 Series FPGAs include an internal oscillator that is used as the source clock in configuration modes in which the FPGA is master"). The POR didn't engage with any of this evidence, and simply ignored the ID's findings on this point.

(b) The combination also has independent control

To the extent independent control of the FPGA is required, Ground 1 has it. Each of the independent FPGA processes shown in Dehkordi's Figure 1 has its own separate code that "could come from outside the module," i.e., not be provided by the processor. EX1050 ¶¶125-136 (quoting EX1004, 3). And again the "highly relevant reference" EX2019 ("D2") reference supports Petitioner's case. (As a preliminary point, D2 doesn't "undo" any of what Dehkordi would have taught or suggested to the POSITA.)

First, while Sentient tries to rely on the fact that a purported "typical MCM" shown in D2's Figure 1 does not show a double-sided arrow on the "control" line,

the presence of a hardware control bus does not speak to whether the *processes* running on the FPGA are independent from the processor (*i.e.*, what is required by the '177 patent claims). Low level control lines, like the control signals disclosed on the Xilinx 4000 series FPGA present in Dehkordi are not about *process* control. EX1050 ¶132 (citing EX1014). Again, we know this where the '177 patent itself depicts only a control line from the processor to the FPGA, and yet the '177 patent claims the FPGA as running independent processes:



EX1001, Fig. 1 (extract, emphasis added)

If, as Sentient now argues, the presence or absence of a double-sided arrow were the litmus test for independence, the '177 patent would also fail to disclose independent processes—something that Sentient failed to mention. *See also* EX1001, 3:34-37; EX1065, 15:24-16:10. EX1050 ¶¶133-134.

Second, D2 describes how “[t]he FPGA can be configured as a pseudo built-in logic analyzer that can monitor core dies within the MCM in real time.” EX1050 ¶135 (citing EX2019, 167). D2 describes this testing process in some detail, where the testing process (1) is independent from whatever process is running on the

processor (e.g., the FPGA can run as a passive monitor of MCM behavior, including all chips/dies in the system, even if those other chips stop functioning), (2) runs in parallel with the processor (e.g., the FPGA testing process runs in simultaneously with whatever is running on the processor.⁴) *Id.*

In sum, even if “independent processes” was read to require no clocking and control from the processor, the prior art provides this limitation.

C. The Board Should Adopt Petitioner’s Showing as to Motivation to Combine and Expectation of Success

For completeness, the Board should adopt Petitioner’s unchallenged rationale regarding combination of the prior art references and the expectation of success in making that combination. Pet., 12-18 (citing EX1002 ¶¶50-66).

⁴ As to the independent process running on the DSP processor, the Petition (at 57) pointed out that “the processor has its own built-in embedded ‘bootstrap ROM’ and ‘program memory,’ as shown in the 96002 data sheet, which control the operation of the DSP. EX1002 ¶149 (citing EX1013, 1).” D2 further shows the processor is running its own process separate from what is running on the FPGA. EX2019, 171 (discussing running programs from “the 4K instruction set” on the Motorola DSP processor and being monitored by the FPGA).

V. Ground 4: The Board Should Adopt the Same Reasoning as in the ID and Find the Challenged Claims Unpatentable

A. Claim Construction: The Court Should Reject Plaintiff's Proposed Construction of "Power Converter" (Which Was Rejected by a Prior Court)

The Board should adopt the same plain and ordinary construction issued by a prior district court judge, i.e., a "power converter" has "its plain and ordinary meaning, specifically, a power converter converts power." EX1012, 6-7; EX1050 ¶¶137-142. The Petition noted this prior construction. Pet., 8 (quoting EX1012).

Sentient's POR proposes a construction that was previously rejected by that same district court: "a converter which changes a voltage level to another voltage level." *Compare* POR, 26 with EX1012, 7 (district court rejecting same)). Sentient provides no reason to depart from the prior district court's "plain and ordinary meaning" construction. Sentient's entire argument is one cursory sentence saying its proposal is "consistent with" its earlier rejected position. POR, 29. Moreover, the dispute is academic as *Steele* (EX1009) provides the element under either construction, as described below.

B. Challenged Claims 5, 10-11, 13-14, 15, 17, and 19-20 Are Obvious for the Reasons Set Forth in the Petition and As Already Found in the Institution Decision

Sentient repeats largely word-for-word the same argument in POR that it presented in POPR. *Compare* POPR, 35-39 with POR, 52-56. Petitioner submits as EX1068 a "redline" comparison of those arguments, showing that Sentient is

presenting essentially the same arguments in POR that it did in POPR. Sentient's arguments fail for the same reasons put forward in the Petition and as found in the ID. Pet., 45-61; ID, 39-42.

The slight differences in Sentient's presentation from its POPR to its POR do not change the result. Sentient now argues that Steele "merely distribut[es] the same voltage multiple times." POR, 54; EX1058. As with the POPR, the POR ignores Steele, which provides that: "Yet another object of the present invention is to provide an output signal voltage level *which is derived from* that signal's input power supply." EX1009 at 2:40-43. *See also* EX1009 at 4:41-42 ("Meanwhile, output signals *generated* by CFB1 are at a 3 volt level."); 4:50-52 ("Note that even though the PLD, itself, is powered by 5 volts, a user has the ability *to choose the voltage level for signals output from the CFBs.*"). *See also* EX1002 ¶¶47-48, 114-120 (citing EX1009, 4:50-58); EX1050 ¶¶144-145.

C. The Board Should Adopt Petitioner's Showing as to Motivation to Combine and Expectation of Success

For completeness, the Board should adopt Petitioner's unchallenged three reasons to combine Steele with other prior art references and the expectation of success in making that combination. Pet., 46-47 (citing EX1002 ¶¶115-118).

Sentient (at 55-56) briefly argues that "no such combination would ever be made" and that "Lyke alone provides all the necessary reference and operating voltages specified in the claim" so that "Steele" is "superfluous" and the

combination “hindsight.” Not so. Petitioner explained and supported with contemporaneous extrinsic evidence the “(i) space savings, (ii) reliability advantages, and (iii) cost savings [and the need] to avoid spending extra MCM real estate that would have been taken up by a separate power converter” such as in Lyke, Pet., 46; EX1002 ¶¶115-118, and noted Steele itself directed “a user to incrementally stuff in logic if there is availability.” *Id.*; *see also* EX1009, 8:3-24. Sentient does not engage with—or dispute—any of this evidence.

VI. None of Sentient’s Remaining Arguments Have Merit

A. Sentient Does Not Dispute Grounds 2, 3, or 5

Sentient has no separate arguments for Grounds 2, 3, or 5. *See* POR at 56-57. Claims 2, 3, 12, and 18 are unpatentable for the reasons given in Xilinx’s Petition. Pet., 37-44 & 62-63.

B. Sentient’s Miscellaneous Arguments Are Wrong And/Or Irrelevant

1. Dehkordi Was Not “Speculative”

Sentient is wrong when it claims that Dehkordi’s teachings are “not enabled.” POR, 14, 44 & 58. This is factually and legally incorrect.

First, the POR is wrong on the facts. The Dehkordi authors had built “5 MCM” modules and provided details of same. EX1050 ¶146 (quoting EX1004, 1, 3). Nor would Dehkordi have presented an enablement challenge to the POSITA. *Id.* (quoting EX1004: “Our experience shows that low-volume MCM prototyping is

achievable...for universities.”; “This technology is no longer considered to be an exotic technology.”). Sentient’s own expert testified: “I think a POSITA would have understood D[ehkordi] and D2 and -- and how those systems operate.” EX1065, 26:10-19.

Second, POR is wrong on the law. “Prior art is presumed to be enabling, and Sentient bears the burden of presenting persuasive evidence to overcome the presumption.” *Centers v. Reddy*, IPR2015-00306, Paper 37 at 11-12 (PTAB Mar. 30, 2016) (citing *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003)). Moreover, “[f]or an obviousness analysis ... a prior art reference need not be enabled, and the reference qualifies as prior art for all that it teaches one of ordinary skill in the art.” *Id.*; *see also Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1382 (Fed. Cir. 2021). To the extent even required, Sentient has not met its burden to show non-enablement.

2. Petitioner Correctly Shows What Was Known to the POSITA

Petitioner’s expert correctly supports his opinions about what was known to the POSITA by citing and explaining many references, including Halverson (EX1025) and Karstonov (EX1036).

The POSITA is a hypothetical person presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *Koninklijke Philips v. Google, LLC*, 948 F.3d 1130, 1337-39 (Fed. Cir. 2020)

(“Regardless of the tribunal, the inquiry into whether any ‘differences’ between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan’s knowledge.”).

Here, the Petitioner’s expert supported his opinions with references showing why a POSITA would have known basic characteristics of what is described in the prior art. EX1050 ¶¶147-151. For example, it is incontestable that when Dehkordi describes using an off-the-shelf commercial part like a “Xilinx 4010 FPGA” that the POSITA would have had background knowledge as to what that was. *Id.* The Petitioner’s expert described this background knowledge and supported his opinions with extensive primary source material to demonstrate the “artisan’s knowledge” that the POSITA would have had when reading the disclosures in asserted prior art combinations. *Id.*

Petitioner’s expert relied on Kostarnov, which used the same Xilinx 4000 series FPGA as in Dehkordi. *See* EX1036, 2; EX1002, 1; EX1014, 45 (data sheet for both “XC4000 family” parts). Crucially, Sentient concedes that Kostarnov illustrates exactly the independence described by Dr. Shanfield, and so instead the POR tries to downplay Kostarnov as an “isolated specialized reference.” POR, 51. But Sentient does not contend that Kostarnov wasn’t relevant or accessible, and of course it was. EX1050 ¶152. Even Sentient’s expert conceded Kostarnov would have been “background knowledge for the POSITA.” EX1065, 26:17-27:13.

Contrary to the POR (at 52), there was no “legal error” in the Board’s statement summarizing Kostarnov’s teachings, which was a reference that Dr. Shanfield had used to support his opinions about background knowledge that the POSITA would have had and used when reviewing the primary references. All of this relevant art is in the record, was clearly presented by the Petitioner’s expert to support his opinions (and cited in the Petition) and is properly before the Board.

Similarly, the POR’s attempt to downplay Halverson (at 11, 49) by claiming that “the USPTO found Halverson during examination but decided not to use it as a basis for rejection” is not correct. The record demonstrates the examiner searched for Halverson’s patent number only *after* the IPR-disputed issues were mooted to the examiner because the applicant had cancelled the affected claims. *Compare* EX1010, 58 (December, 2001 rejection) *with* EX1010, 44 (February, 2005 amendment cancelling claims) *and* EX1010, 26 (March, 2005 search record, showing search for U.S. Patent No. 5,574,930). Halverson remains solid art to show what was known to the POSITA at the time of the ’177 patent invention.

3. The POR’s Focus on “JTAG”/“TAP” Is Irrelevant.

The Petition does not mention JTAG or TAP. The POR’s extensive discussion of JTAG and TAP testing (e.g., at 42-48) is non-responsive.

4. Sentient's Expert Is Entitled to No Weight

Finally, Sentient's "expert" declaration is entitled to no weight. It is a copy of the POR with "in my opinion" sprinkled throughout, *without relevant extrinsic evidence*. Compare EX2020 ¶¶34-48 with POR, 12-19 and EX2020 ¶¶54-105 with POR, 29-57. Sentient's expert was also apparently unaware that portions of his report had been copied from Wikipedia (*see* EX1065, 35:4-36:20; *compare* EX2020 ¶¶31-32 with EX1053). Sentient's unsupported expert declaration is not a source of credible evidence regarding the contested issues in this case.

VII. CONCLUSION

The asserted prior art provides the two allegedly missing elements. The POR's miscellaneous arguments are wrong. Xilinx respectfully request that the Board confirm its initial findings that the challenged claims are unpatentable.

Respectfully submitted,

Dated: March 21, 2024

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petitioner's Reply to Patent Owner's Response totals 5,588 words, which is less than the 5,600 allowed under 37 CFR § 42.24(c)(1).

Dated: March 21, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(1) and 42.6(e)(4)(iii), the undersigned certifies that on March 21, 2024, a complete and entire copy of this Petitioner's Reply to Patent Owner's Response and accompanying exhibits were provided by email to the Patent Owner by serving the email correspondence addresses of record as follows:

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