

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

SENTIENT SENSORS, LLC,

Plaintiff,

v.

CYPRESS SEMICONDUCTOR
CORPORATION,

Defendant.

Civil Action No. 1:19-cv-01868-MN

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TABLE OF CONTENTS

I. Agreed Upon Constructions	2
II. Disputed Constructions.....	2
<i>Term 1: “an instrument controller”</i>	2
1. Plaintiff’s Opening Position.....	2
i. Overview of Patented Technology.....	2
ii. Claim Construction	4
2. Defendant’s Answering Position.....	5
i. Specification <i>Defines</i> the Alleged Invention as a Multi-Chip Module	6
ii. Specification Provides Support for <i>Only</i> a Multi-Chip Module	9
iii. Prosecution History Evidences the Alleged Invention is a Multi-Chip Module.....	11
iv. Sentient’s Proposed Construction Must be Rejected.....	13
3. Plaintiff’s Reply Position	16
4. Defendant’s Sur-Reply Position.....	22
<i>Term 2: “embedded”</i>	27
1. Plaintiff’s Opening Position.....	27
2. Defendant’s Answering Position.....	29
i. Plain Meaning of “Embedded” Is Unequivocally Established by the Intrinsic Evidence	29
ii. Sentient’s Proposed Construction Lacks Intrinsic Evidentiary Support.....	30
iii. Sentient’s Proposed Construction Would Render “Embedded” Meaningless	30
3. Plaintiff’s Reply Position	33
4. Defendant’s Sur-Reply Position.....	36
<i>Term 3: “oscillator”</i>	38
1. Plaintiff’s Opening Position.....	38
2. Defendant’s Answering Position.....	39
3. Plaintiff’s Reply Position	40

4. Defendant’s Sur-Reply Position.....	41
<i>Term 4: “two internal oscillators”</i>	<i>42</i>
1. Plaintiff’s Opening Position.....	42
2. Defendant’s Answering Position.....	43
3. Plaintiff’s Reply Position	45
4. Defendant’s Sur-Reply Position.....	46
<i>Term 5: “power converter”</i>	<i>47</i>
1. Plaintiff’s Opening Position.....	47
2. Defendant’s Answering Position.....	48
3. Plaintiff’s Reply Position	51
4. Defendant’s Sur-Reply Position.....	53
<i>Term 6: “processor configured to automatically activate...”</i>	<i>55</i>
1. Plaintiff’s Opening Position.....	55
2. Defendant’s Answering Position.....	56
3. Plaintiff’s Reply Position	59
4. Defendant’s Sur-Reply Position.....	61
<i>Term 7: “a plurality of gates arranged in a field programmable gate array”</i>	<i>62</i>
1. Plaintiff’s Opening Position.....	62
2. Defendant’s Answering Position.....	64
3. Plaintiff’s Reply Position	68
4. Defendant’s Sur-Reply Position	70
<i>Term 8: “configured to run independent processes”</i>	<i>71</i>
1. Plaintiff’s Opening Position.....	71
2. Defendant’s Answering Position.....	73
3. Plaintiff’s Reply Position	74
4. Defendant’s Sur-Reply Position.....	75

TABLE OF AUTHORITIES

Cases

<i>Abbott Labs. v. Sandoz, Inc.</i> , 566 F.3d 1282 (Fed. Cir. 2009).....	31, 32, 33
<i>Ariad Pharm., Inc. v. Eli Lilly & Co.</i> , 598 F.3d 1336 (Fed. Cir. 2010).....	10, 19
<i>Biogen, Inc. v. Berlex Labs., Inc.</i> , 318 F.3d 1132 (Fed. Cir. 2003).....	13
<i>C.R. Bard, Inc. v. U.S. Surgical Corp.</i> , 388 F.3d 858 (Fed. Cir. 2004).....	8
<i>Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.</i> , 289 F.3d 801 (Fed. Cir. 2002).....	passim
<i>Chicago & N.W. Ry. Co. v. Sayles</i> , 97 U.S. 554 (1878)	12
<i>ContentGuard Holdings, Inc. v. Apple Inc.</i> , 701 Fed. App’x. 957 (Fed. Cir. 2017)	65
<i>Continental Circuits LLC v. Intel Corp.</i> , 915 F.3d 788 (Fed. Cir. 2019)	passim
<i>Dealertrack, Inc. v. Huber</i> , 674 F.3d 1315 (Fed. Cir. 2012).....	18, 26
<i>Eastman Kodak Co. v. Goodyear Tire & Rubber Co.</i> , 114 F.3d 1547 (Fed. Cir. 1997)	41
<i>Edwards Lifesciences LLC v. Cook Inc.</i> , 582 F.3d 1322 (Fed. Cir. 2009)	11
<i>Enova Tech. Corp. v. Initio Corp.</i> , 2012 WL 6738398 at *2 (D. Del. Dec. 28, 2012).....	52
<i>Enzo Biochem, Inc. v. Applera Corp.</i> , 599 F.3d 1325 (Fed. Cir. 2010).....	18
<i>Exxon Chem. Patents, Inc. v. Lubrizol Corp.</i> , 64 F.3d 1553 (Fed. Cir. 1995).....	7
<i>Hill-Rom Co. v. Kinetic Concepts, Inc.</i> , 209 F.3d 1337 (Fed. Cir. 2000).....	7, 69
<i>Honeywell Int’l, Inc. v. ITT Indus.</i> , 452 F.3d 1312 (Fed. Cir. 2006).....	8, 9, 13
<i>IMS Tech., Inc. v. Haas Automation, Inc.</i> , 206 F.3d 1422 (Fed. Cir. 2000).....	18, 26
<i>In re Am. Acad. of Sci. Tech. Ctr.</i> , 367 F.3d 1359 (Fed. Cir. 2004).....	18, 26
<i>In re Fought</i> , 941 F.3d 1175 (Fed. Cir. 2019)	25, 26
<i>In re Global IP Holdings LLC</i> , 927 F.3d 1373 (Fed. Cir. 2019)	19, 27, 41
<i>In re Lew</i> , 257 F. App’x 281 (Fed. Cir. 2007).....	13
<i>In American Medical Systems, Inc. v. Biolitec, Inc.</i> , 618 F.3d 1354 (Fed. Cir. 2010)	passim
<i>Layne Christensen Co. v. Bro-Tech Corp.</i> , 836 F.Supp.2d 1203 (D. Kan. 2011)	17, 18, 25
<i>Liebel-Flarsheim Co. v. Medrad, Inc.</i> , 481 F.3d 1371 (Fed. Cir. 2007).....	10, 11, 41
<i>LizardTech, Inc. v. Earth Resource Mapping, Inc.</i> , 424 F.3d 1336 (Fed. Cir. 2005).....	passim

<i>Nautilus, Inc. v. Biosig Instruments, Inc.</i> , 572 U.S. 898 (2014)	13
<i>NeoMagic Corp. v. Trident Microsys., Inc.</i> , 287 F.3d 1062 (Fed. Cir. 2002)	22, 36
<i>NTP, Inc. v. Research In Motion, Ltd.</i> , 418 F.3d 1282 (Fed. Cir. 2005)	6
<i>Pall Corp. v. Hemasure Inc.</i> , 181 F.3d 1305 (Fed. Cir. 1999)	31
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	17, 52
<i>Pitney Bowes, Inc. v. Hewlett-Packard Co.</i> , 182 F.3d 1298 (Fed. Cir. 1999)	passim
<i>Poly-Am., L.P. v. GSE Lining Tech., Inc.</i> , 383 F.3d 1303 (Fed. Cir. 2004)	26
<i>Rembrandt Patent Innovations, LLC v. Apple, Inc.</i> , 716 F. App'x 965 (Fed. Cir. 2017)	7
<i>ResQNet.com, Inc. v. Lansa, Inc.</i> , 346 F.3d 1374 (Fed. Cir. 2003)	46, 47
<i>RSA Protective Tech, LLC v. Secure USA, Inc.</i> , 2019 WL 9048994 (S.D. Fla. May 15, 2019)	21
<i>SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.</i> , 242 F.3d 1337 (Fed. Cir. 2001)	8, 9
<i>Scripps Clinic & Research Found. v. Genentech, Inc.</i> , 927 F.2d 1565 (Fed. Cir. 1991)	31, 36
<i>SRI Int'l v. Matsushita Elec. Corp. of Am.</i> , 775 F.2d 1107 (Fed. Cir. 1985)	22
<i>Thorner v. Sony Computer Entm't Am. LLC</i> , 669 F.3d 1362 (Fed. Cir. 2012)	36
<i>Typhoon Touch Techs., Inc. v. Dell, Inc.</i> , 659 F.3d 1376 (Fed. Cir. 2011)	24
<i>UltimatePointer, L.L.C. v. Nintendo Co.</i> , 816 F.3d 816 (Fed. Cir. 2016)	6, 7
<i>Verizon Servs. Corp. v. Vonage Holdings Corp.</i> , 503 F.3d 1295 (Fed. Cir. 2007)	9
<i>Wang Labs., Inc. v. Am. Online, Inc.</i> , 197 F.3d 1377 (Fed. Cir. 1999)	40, 41
<i>Wilson Sporting Goods Co. v. Hillerich & Bradsby Co.</i> , 442 F.3d 1322 (Fed. Cir. 2006)	24
Statutory Authorities	
35 U.S.C. § 112	19, 20, 41
Rules and Regulations	
MPEP § 2111.02 II	21, 26

JOINT CLAIM CONSTRUCTION BRIEF

Plaintiff, Sentient Sensors, LLC (“Sentient” or “Plaintiff”) and Defendant, Cypress Semiconductor Corporation (“Cypress” or “Defendant”), by and through their undersigned counsel, hereby submit this Joint Claim Construction Brief. At issue are eight disputed terms of U.S. Patent No. 6,938,177 (the “‘177 Patent”), the single patent that Sentient has asserted against Cypress.

Plaintiff:

Sentient maintains that most of the disputed terms have simple, straightforward plain and ordinary meanings which are supported by the specification and the originally filed claims in this case, but are briefed here because Cypress insists on incorporating numerous limitations not present in the claims or otherwise introduced through amendment or other estoppel. Sentient asserts that its proposed constructions should be adopted because they are supported by both the intrinsic and extrinsic evidence and will be helpful to the jury and the Court in understanding the invention. Cypress’s proposals, in contrast, ignore the plain language of the claims and improperly import limitations at odds with the invention and explicit intent of the Patentee, and serve to erroneously complicate the claims—mostly likely in an attempt to manufacture non-infringement positions.

Defendant:

Cypress asserts that, as explained below, the eight terms at issue can largely be defined by plain meaning, but with at least a couple of important exceptions. First, Sentient cannot hide behind plain meaning with regard to the critical term “instrument controller,” given that the entire intrinsic evidence—specification and prosecution history—unequivocally, clearly and repeatedly *define* the alleged invention to be a *multi-chip module* instrument controller.

Second, the Patent likewise requires an unusual type of FPGA with “a subset of gates” that is capable of performing analog functions that the patent defines as being among the “core elements” of the alleged invention. Therefore, the definition of the FPGA must incorporate this core feature.

I. Agreed Upon Constructions

None.

II. Disputed Constructions

Term 1: “an instrument controller”

Term	Sentient’s Proposal	Cypress’s Proposal
“An instrument controller”	“An electronic circuit that provides "System on a Chip" control functions consistent with the performance and operation of an Integrated Circuit device”	“multichip module instrument controller”

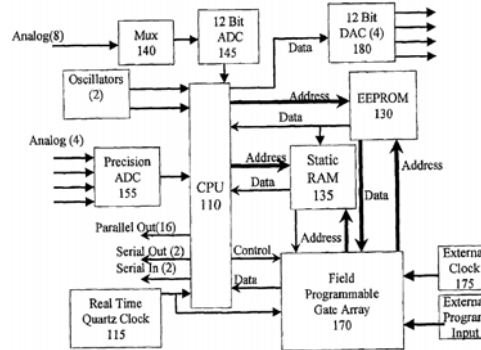
1. Plaintiff’s Opening Position

i. Overview of Patented Technology

The invention claimed and described in the ‘177 Patent was conceived by Kenneth G. Blemel, a small technology business owner in Albuquerque, New Mexico with a long history of providing custom high tech solutions to the United States government through his family owned business Management Sciences Inc. (“MSI”), the managing member of Sentient.¹ Sentient is a practicing entity that produces products covered by the patent. Mr. Blemel diligently worked on his invention up through at least December 19, 2001 at which time the invention was constructively reduced to practice with the filing of U.S. Patent Application No. 10/028,556. The ‘556 application was prosecuted and ultimately issued as the ‘177 Patent on August 30, 2005 with 20 claims.

¹ See for example <http://www.mgtsciences.com/>.

As expressly described in the specification, the ‘177 Patent relates to “System on a Chip” (“SOC”) architecture which is commonly used as an instrument controller. One of ordinary skill in the art would immediately understand from the schematic diagram of Figure 1 of the ‘177 below that it represents an electronic system architecture – *i.e.*, a collection of certain interconnected circuit elements that operate together to form an electronic system.



This understanding is further supported by the express teachings in the specification which explain that: “As such, *the invention* is similar to a “*system-on-a-chip*” and appears similar to a chip in size, weight and physical configuration...” ‘177 Patent at 3:55-58. And the specific constituent components of the SOC control systems of the present invention are set forth in the 20 claims of the ‘177 Patent. *Id.* at 2:66-3:5 (“The core elements of the present invention include a microprocessor, static random access memory (single or multi-ported), non-volatile memory (*e.g.*, flash or EEPROM), a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion” which form a control system); Figure 1, *etc.*

The specification explains that the invention may be used for a variety of control applications. “Such applications include motor controllers, cryocooler refrigerator controllers, distributed health and status monitoring systems, configuration management processors, safety interlock protocol management security systems, miniature weapons computers, space probe

central control processor, beacon processor, and jet engine control. The invention may also be used on the manufacturing floor for smart, discontinuous low-level sensing test equipment probes, embedded credit card processors, wearable computers, or remote data logging.” *Id.* at 9:7-17.

ii. Claim Construction

“Instrument controller” appears in the preamble of the ‘177 Patent claims in the context of a system of electronic components that are specifically enumerated by the claimed elements that follow. Namely, it serves to define the penumbra under which constituent electronic components, their interconnection, and their interaction are defined. This is the plain and ordinary meaning of the term. A person of ordinary skill in the art would have an innate natural understanding that comports with this arrangement based on everyday usage of language and the application of common sense.

However, Patentee went further and took the time in the specification to explain the invention in more detail, specifically: “As such, *the invention* is similar to a “*system-on-a-chip*” and appears similar to a chip in size, weight and physical configuration...” ‘177 Patent at 3:55-58. And further still, the specification provides an explanation of what an ordinarily skilled artisan at the time of the invention would understand that the invention “is built like a hybrid microcircuit, but possesses a highly integrated behavior more consistent with “*system-on-a-chip*” or monolithic IC designs.” *Id.* at 1:65-2:1.

Accordingly, Patentee’s proposed construction of: “An electronic circuit that provides “System on a Chip” control functions consistent with the performance and operation of an Integrated Circuit device” is based directly on the teachings of the specification and the understanding of one of ordinary skill in the art without distortion or extrapolation. As such, it should be adopted.

Tellingly, the phrase “multichip module” was specifically removed from all the pending original claims – including both the preamble of original independent claims 3, 5, and 6, and dependent claims 2, 12, and 13. All newly added claims did not include this limitation. *See* Feb. 25, 2005 Reply to Office action claim amendments pages 2-10 (SENTIENT 000347-351).

Claim 3 (amended): ~~[[The]]An multi-chip module instrument controller of claim 1,~~
~~wherein comprising:~~

Claim 12 (amended): The method for conducting multiple parallel ~~monitoring and control~~
~~functions processing~~ using a single ~~multi-chip module instrument controller~~ as in claim ~~[[11]]13~~,
 further comprising the additional step of providing at least two internal oscillator signals to the
 processor for low-speed and high-speed digital signal processing operations.

Claim 13 (amended): ~~[[The]]A method for conducting multiple parallel monitoring and control~~
~~functions processing~~ using a single ~~multi-chip module instrument controller~~ as in claim ~~11~~;
~~further comprising the step of having a processor and a field programmable array, the method~~
~~comprising:~~

As a result, the term “multichip module” does not appear in *any* of the claims in the issued ‘177 Patent. This was the clear intent of the Patentee through these specific and intentional amendments. Defendant’s proposal seeks to impermissibly re-introduce this limitation back into the claim despite being specifically removed during prosecution.

Additionally, Sentient’s construction actually defines the term, which may be helpful to jurors, whereas Defendant’s construction merely adds more highly technical words (“multichip module”) to the phrase to be construed and therefore is no help in clarifying the term at issue. If anything, Defendant’s construction adds a further complication that is likely to confuse a jury. In sum, Defendant’s proposal should be rejected as inconsistent with the intrinsic evidence.

2. Defendant’s Answering Position

The ‘177 patent and the intrinsic evidence unequivocally **define** the alleged invention as being a “multi-chip module” (*i.e.*, “MCM”). Rarely has a patent and prosecution been more

clear: from the title of the alleged invention, the description of how the alleged invention was specifically intended to improve upon the prior art, the abstract of the alleged invention, the summary of the alleged invention, the description throughout the specification and the prosecution history—the entire body of intrinsic evidence—consistently, repeatedly, and without contradiction evidence that the patentee’s alleged invention is *defined* as a “**multi-chip module**.”² See, e.g., ’177 Patent at Title (“**Multi-chip module** smart controller”) (one of 26 mentions in the patent). See also, e.g., *UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 823 (Fed. Cir. 2016) (affirming the district court’s construction that relied on the patent’s title, repeated emphasis in the specification, and disparagement of other contrary options to define a term). Moreover, Sentient does not appear to dispute that the preamble is limiting here and, in any event, case law confirms—especially given that the “instrument controller” term must be limited to a multi-chip controller—that the preamble contains structure to be construed. See *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1305 (Fed. Cir. 2005) (abrogated on other grounds) (“a preamble generally limits the claimed invention if it recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim”) (internal quotations omitted). Because the public must be entitled to rely upon Sentient’s clear and unequivocal statements of what the alleged invention is, the claims must be interpreted as limited to a “multi-chip module.”

i. Specification **Defines** the Alleged Invention as a Multi-Chip Module

The specification does not merely describe one possible “embodiment” as including a multi-chip module, it repeatedly *defines* the alleged invention as being a multi-chip module,

² Note that unless otherwise indicated, all emphasis in Cypress’s briefing have been added. In addition, the corrections to the errors in the patent as stated in the Certificate of Correction are incorporated into all patent quotations herein.

beginning with the title of the '177 patent: "MULTI-CHIP MODULE SMART CONTROLLER." See, e.g., *Exxon Chem. Patents, Inc. v. Lubrizol Corp.*, 64 F.3d 1553, 1557 (Fed. Cir. 1995) (using patent title to inform claim construction); see also (Hassoun Decl.) ¶¶ 9-10. The patent similarly defines the alleged invention in the Abstract and the Field of the Invention:

A multi-chip module instrument controller having various interface and operational capabilities.

'177 Patent at Abstract. See also *Hill-Rom Co. v. Kinetic Concepts, Inc.*, 209 F.3d 1337, 1341 n.1 (Fed. Cir. 2000) (holding that an abstract can be a "helpful source of intrinsic evidence as to the meaning of claims").

The present invention generally relates to multi-chip modules (MCM). More specifically, ***the present invention relates to an MCM capable of...***

'177 Patent at 1:11-18 (Field of the Invention). See also *Rembrandt Patent Innovations, LLC v. Apple, Inc.*, 716 F. App'x 965, 971 (Fed. Cir. 2017) (citing language in the "Field of the Invention" section in affirming the district court's decision to include the word "automatic" in a construction even though "[t]he asserted claims do not recite the word automatic or any variation thereof").

The patent next discusses the prior art and further confirms that the alleged invention is a "multi-chip module." See Hassoun Decl. ¶¶ 10-11. The prior art discussion focuses on one patent, U.S. Patent 6,148,399, that Sentient describes as being "...a single, tightly coupled **MCM design**." After a detailed discussion of this prior MCM invention, the '177 Patent clearly and repeatedly states—as the goal of the '177 Patent—that what is needed is an improved "MCM design":

Accordingly, ***what is needed is an MCM design*** capable of executing multiple parallel processes in an independent fashion. . . .

Accordingly, ***what is needed is an MCM design*** capable of performing A/D conversion at different bit depths such that multiple parallel processes which require different bit depths can be executed in an independent fashion.

Id. at 2:15-17, 2:26-31. *See also UltimatePointer*, 816 F.3d at 823 (giving claim-construction weight to how a patent distinguishes other options); *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343 (Fed. Cir. 2001) (considering how prior art is distinguished).

Next, the “Summary” expressly confirms the alleged invention is an MCM design:

SUMMARY OF THE INVENTION

The present invention is embodied in a stand-alone, compact low-power electronics instrument controller ***which utilizes an MCM design.***”

’177 Patent at 2:33-36. *See also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004) (recognizing that because statements in the “summary of the invention” section of a specification tend to describe the invention overall, they may be more likely to have a limiting impact than statements in the section describing preferred embodiments).

The specification goes on to repeatedly define the alleged invention as a multi-chip module or MCM design, starting in the first sentence:

The present invention is embodiment in a tightly coupled smart control system which uses ***a multi-chip module (MCM) instrument controller*** which uniquely combines conventional high-density interconnects patterned in an overlay of ***MCM*** substrates.

’177 Patent at 3:41-45.

The invention combines all of these elements ***on a single tightly coupled MCM*** to achieve its stand-alone capabilities.

Id. at 4:1-2. All in all, the specification points to the alleged invention as an MCM or MCM design at least 14 times. *Id.* at Title; Abstract; 1:14-15; 1:15-16; 2:15:17; 2:27-31; 2:34-36; 3:27-29; 3:41-45 (two references); 3:46-49; 3:55-60; 4:1-2; 6:9-11.

The Federal Circuit has routinely limited claims to what a patentee publicly and repeatedly announces as being “the invention.” *See, e.g., Honeywell Int’l, Inc. v. ITT Indus.*, 452 F.3d 1312,

1318 (Fed. Cir. 2006) (“On at least four occasions, the written description refers to the fuel filter as ‘this invention’ or ‘the present invention’ ... The public is entitled to take the patentee at his word and the word was that the invention is a fuel filter.”); *SciMed Life Sys.*, 242 F.3d at 1343 (“the characterization of the coaxial configuration as part of the ‘present invention’ is strong evidence that the claims should not be read to encompass the opposite structure”); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) (“When a patent thus describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.”). Thus, the claims—all of which include the term “instrument controller”—must be interpreted to require a “multi-chip module” instrument controller, because the specification uniformly, clearly, and repeatedly defines the alleged invention as being an “MCM” that the patent explains was the result of an effort to invent a better “MCM design.” See Hassoun Decl. ¶¶9-13.

ii. Specification Provides Support for Only a Multi-Chip Module

As detailed above, the one and only embodiment consistently, repeatedly, and solely describes a multi-chip module. See, e.g., *id.* at 3:28-30 (“FIG. 1 is a functional schematic block diagram of a ***preferred embodiment of the MCM Controller*** of the present invention.”); *id.* at 3:41-45 (“***The present invention is embodied in a tightly coupled smart control system which uses a multi-chip module (MCM) instrument controller*** which uniquely combines conventional high-density interconnects patterned in an overlay of MCM substrates.”); *id.* at 6:7-11 (“The present invention further includes a combination of large volatile and non-volatile memory storage components. These memory storage components are ***preferably customized and tightly coupled within the MCM*** for maximum performance.”); see also Hassoun Decl. ¶¶ 8-13. Indeed, no approach other than to utilize a MCM is taught to one of skill in the art—much less even mentioned—in any manner by the specification. Hassoun Decl. ¶¶ 8-13. See, e.g., *Honeywell*, 452

F.3d at 1318-20 (construing generic terms narrowly based on the specification’s narrow definition of “the present invention” and disavowals of other methods, despite statements during the prosecution history that the invention was directed more broadly); *Rembrandt*, 716 Fed. App’x at 972 (finding that “[t]he clear, repetitive, and uniform nature of the ’678 patent’s description of the automated recovery process, in combination with its rejection of prior art methods that require some human involvement, limit the scope of the invention” such that the word “automatic” had to be read into the claims even though “[t]he asserted claims do not recite the word “automatic” or any variation thereof”). Sentient’s attempt to broadly claim a generic electronic instrument controller must be rejected because the title, specification, and embodiments clearly evidence that the patentee defined the controller as being a multi-chip module.

Indeed, unless instrument controller is interpreted to be an MCM instrument controller, the patent would be invalid for failing to enable or provide a written description to support the scope of the claims sought by Sentient. The patent teaches only one approach—an MCM design—and clearly shows that the patentee did not possess anything beyond an MCM instrument controller design, nor does the specification teach how to implement the alleged invention via anything other than an MCM design. Hassoun Decl. ¶¶ 8-13. *See LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1343-44 (Fed. Cir. 2005) (description of one method of meeting an objective “d[id] not entitle the inventor of the ’835 patent to claim any and all means for achieving that objective”); *see also Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1349 (Fed. Cir. 2010) (reiterating that the written description requirement “requires that the specification objectively demonstrate that the applicant actually invented—was in possession of—the claimed subject matter”); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 481 F.3d 1371, 1380 (Fed. Cir. 2007) (“The irony of this situation is that Liebel successfully pressed to have its claims include a jacketless system,

but, having won that battle, it then had to show that such a claim was fully enabled, a challenge it could not meet. The motto, ‘beware of what one asks for,’ might be applicable here.”). Thus, the case law as well as the unequivocal intrinsic evidence compels a finding that the instrument controller is an MCM.

iii. Prosecution History Evidences the Alleged Invention is a Multi-Chip Module

The prosecution history further evidences that both the Patent Office and Sentient agreed the instrument controller of the allowed claims was a multi-chip module. First, each and every original claim included the term “multi-chip module instrument controller,” and in the first Office Action, the examiner expressly determined that the relevant original claims were “**drawn to multi-chip module** instrument controller.” SENTIENT 367. After rejecting various claims, the examiner then approved certain dependent claims, but stated they would be allowable only “if rewritten in independent form ***including all of the limitations of the base claim and any intervening claims.***” *Id.* at 372. In response, Sentient submitted amended claims expressly representing that: “Applicant has amended dependent claims 3, 5, 6, and 13 so as to be written in independent form.” *Id.* at 359. Sentient also added new claims similarly based on the approved dependent claims—and ***twice*** assured the Patent Office, and the public, that “[n]o new matter ha[d] been added” to the claims. *Id.* at 347, 360. The Federal Circuit has found that the patentee’s statements made when deleting matter are relevant in interpreting the scope claim terms that facially may seem broad, post-deletion. *See, e.g., Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330-31 (Fed. Cir. 2009) (finding that even though the modifier “intraluminal” had been deleted, the accompanying remarks stated that the claim defined an intraluminal graft, and thus the deletion from the prosecution history did not override the fact that the specification showed the patent’s graft must be intraluminal). Similarly, here, Sentient ***twice*** assuring the

examiner and the public that “no new matter” was added can only be understood to mean that the claims were not broadened from the original “multi-chip module instrument controller.” Therefore, even though the rewritten claims removed the modifier “multi chip module” from “instrument controller,” the patentee assured the Patent Office—and the public—that nothing materially had changed from the original claims.

Sentient’s representations to the Patent Office, and the public, that no new subject matter had been added to the claims could only be true if Sentient agreed with the Patent Office’s prior determination that the original claims were “drawn to multi-chip module instrument controller” and agreed that determination continued to apply to the claims Sentient submitted via its response to the Office Action. Indeed, given that the original specification clearly, unequivocally, and repeatedly *defined* the alleged invention as a “multi-chip module,” it is understandable that Sentient during prosecution would have understood that the claimed invention would be limited to a “multi-chip module”—whether or not the claims expressly included that phrase. Sentient’s representation that “[n]o new matter has been added” and that Sentient had followed the Patent Office’s direction to include “all of the limitations” in the allowed dependent original claims, therefore, makes sense. Of course, we assume that Sentient, while representing to the Patent Office that it was not adding new subject matter, did not *intentionally* attempt to change the scope of the claims to no longer require multi-chip modules. Had Sentient done so, it would face serious questions regarding its conduct.

At a minimum, however, Sentient now apparently seeks to retroactively do what it promised the Patent Office it would **not** do: add new matter to the originally allowed dependent claims. Case law, as well basic notions of public notice, of course preclude any such effort. *See Chicago & N.W. Ry. Co. v. Sayles*, 97 U.S. 554, 563 (1878) (“The law does not permit such

enlargements of an original specification[.] . . . Courts should regard with jealousy and disfavor any attempts to enlarge the scope of an application once filed”); *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 899 (2014) (“[A] patent must be precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them.”) (internal quotations and alterations incorporated); *Honeywell*, 452 F.3d at 1318-20 (“Where, as here, the written description clearly identifies what his invention is, an expression by a patentee during prosecution that he intends his claims to cover more than what his specification discloses is entitled to little weight”); *Biogen, Inc. v. Berlex Labs., Inc.*, 318 F.3d 1132, 1140 (Fed. Cir. 2003) (“Representations during prosecution cannot enlarge the content of the specification, and the district court was correct in relying on the specification in analyzing the claims.”); *In re Lew*, 257 F. App’x 281, 286 (Fed. Cir. 2007) (upholding PTAB’s determination that “Lew’s amendments to replace the term ‘ball bearing’ with the broader term ‘curved member’ were not supported by the initial disclosure, and, therefore, the examiner did not err in rejecting claim 19 under § 112,” noting *inter alia* that “each time ‘the invention’ is described, including in the summary of the invention and the abstract, it is stated to include ‘ball bearings’”). Moreover, as noted above, if Sentient is now asserting that during prosecution it purposely attempted to change the scope of the claims by removing the phrase “multi-chip module”—despite representing the contrary to the Patent Office—that would raise serious questions concerning the ethics of such conduct. Thus, the prosecution history, including both the Patent Office’s express determination that the claims were drawn to a multi-chip module and the statements of Sentient that it was not broadening the claims to include new matter, clearly supports Cypress’s proposed construction.

iv. Sentient’s Proposed Construction Must be Rejected

In addition to impermissibly broadening the scope of the “instrument controller” beyond

the alleged invention that was defined throughout the file history and the specification, Sentient’s proposal seeks to recapture what it clearly disclaimed in the Patent’s own specification.

As support for its proposal, Sentient’s brief relies upon truncated quotes from two portions of the specification that mention the phrase “system-on-a-chip.” But, in both instances, the entire relevant quote plainly shows that the specification *distinguishes* the multi-chip module alleged invention *from* a “system-on-a-chip”, rather than equating the two. First, Sentient, regrettably, provides the Court with just a portion of the first relevant citation—omitting the key phrase beginning with “but” that is underlined and emphasized below:

As such the invention is similar to a ‘system-on-a-chip’ and appears similar to a chip in size, weight and physical configuration, *but through a tightly coupled MCM implementation, transcends the functional capability of a single integrated circuit.*

’177 Patent at 3:55-60. The full sentence powerfully *distinguishes* the patented MCM design *from* a system-on-a-chip—and thus disclaims the single chip design—by representing that the MCM approach “transcends the functional capability of a single integrated circuit.” *See also* Hassoun Decl. ¶¶ 10-12. Moreover, the omitted portion of the sentence, yet again, confirms that the alleged invention is, in fact, an “MCM implementation.” As discussed above, the Patent’s defining of the alleged invention to be a multi-chip module provides a compelling basis under the law for holding Sentient to these statements made to the public.

Sentient then cites just one other mention of the phrase “system-on-a-chip,” which is located in the patent’s preamble. Again, Sentient regrettably fails to provide the full quote for the Court. As shown below, the full quote shows that the reference to a “system-on-a-chip” was specifically used as a point of reference for a prior art MCM design found in U.S. Patent No. 6,148,399, **not** the allegedly patented invention:

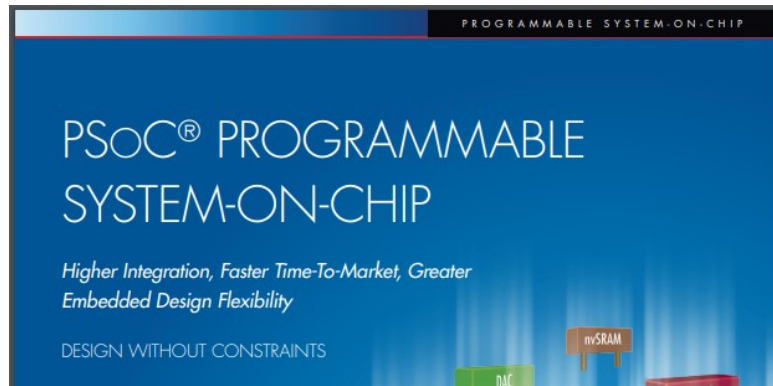
In other words, a tightly coupled MCM is built like a hybrid microcircuit but possesses a highly integrated behavior ***more consistent with “system-on-a-chip” or monolithic IC designs***. The result is that ***Lyke’s invention*** greatly reduced size, weight, and power consumption over discrete implementations (“discrete” referring to an arrangement of several individually packaged ICs built onto a circuit board or other presumably multilayer wiring medium). Accordingly, the invention in U.S. Pat. No. 6,148,399 ***combines in a small MCM a number of functions which could not have previously been executed using a single integrated circuit.***

’177 Patent at 1:64-2:8. More critically, even this generic point of reference between a prior art MCM and a “system-on-a-chip” emphasizes, again, how the MCM design is dramatically different from system-on-a-chip by going so far as to state that the MCM combines “a number of functions which ***could not have previously been executed using a single integrated circuit.***”

Lastly, Cypress notes that Sentient’s effort to shoehorn “system-on-a-chip” into the definition of “instrument controller” is plainly an effort to incorporate the name of the Cypress accused products into the Court’s construction of a claim term. See Dkt. 6 (Am. Compl.) ¶ 18 (accusing the “Programmable System on a Chip (‘PSoC®’) lines”). Cypress’s accused products heavily emphasize that the devices are a programmable system-on-chip (a.k.a., “PSoC”). For example, product datasheets include the name on the cover page:



Ex. 1 (PSoC 5LP: CY8C52LP Family Datasheet) at 2, www.cypress.com/file/45916/download (last accessed Sept. 2, 2020). And general marketing materials for the accused product lines feature the language prominently on the title page and throughout:



Ex. 2 (PSoC® *Programmable System-on-Chip Manual*) at 1, <https://www.cypress.com/file/121931/download> (last accessed Sept. 2, 2020) (“system-on-chip” or “system on chip” appears on almost every page to describe the Cypress’s products). Moreover, it bears noting that when Sentient previously asserted the ’177 Patent against a different accused product—a product that was not a “system-on-a-chip”—Sentient’s construction for “instrument controller” nowhere even mentioned the phrase “system-on-a-chip”. *Blemel Technologies, LLC v. Nat’l Instruments Corp.*, No. 2:15-cv-0134-RWS-RSP, Dkt. 75-2 (Joint Claim Construction Chart, App. B), at 1 (stating “No construction necessary. Plain and ordinary meaning”). Thus, Sentient’s proposal, in addition to being entirely unmoored from the specification (and indeed attempting to recapture claim scope it disclaimed in the specification), should be rejected as an effort to unfairly incorporate the name of Cypress’s accused product directly into the Court’s claim construction.

For the above reasons, Cypress respectfully requests that its construction be adopted, and that the Court entirely reject Sentient’s proposal.

3. Plaintiff’s Reply Position

This dispute revolves around one basic question. Is it proper for Cypress to rewrite the

non-limiting preamble term³ “Instrument Controller” to re-introduce the previously deleted multichip module language (“MCM”) and then make that rewritten preamble limiting on the Patentee? The answer is no. The prosecution of the ‘177 Patent is clear from the public record. The phrase “MCM” was specifically, intentionally, and with the knowledge and consent of the PTO, removed from all the pending original claims (independent claims 3, 5 and 6 and dependent claims 2, 12 and 13) during prosecution. Further, all newly added claims were specifically written *to not include* this limitation.⁴ (See SENTIENT 000347-356). Moreover, the prosecution history points to the originally filed claims as written description support for the new claims that do not include the MCM language in the preamble, with no objection from the PTO. *See id.* This clearly establishes what Patentee intended the claims to mean and informs the public on the scope of the invention.

It is undisputed that the term MCM does not appear in any of the claims of the ‘177 Patent as issued. The plain and ordinary meaning of the claim language in the preamble cannot under any reasonable interpretation be limited to *only* the explicitly excluded language. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (claim terms “are generally given their ordinary and customary meaning.”). Cypress offers no response to this point, and focuses solely on certain embodiments of the specification and the extrinsic opinions of its expert, not on the words of the preamble itself (“an instrument controller”).

It is black letter law that the preamble of a claim is not considered limiting absent circumstances not present in this case. *See Am. Med. Sys. v. Biolitec, Inc.*, 618 F.3d 1354, 1358

³ Cypress erroneously contends that Sentient has admitted the preamble is limited to MCM devices (p. 6, *supra*). Sentient has made no such admission and Cypress points to nothing in support of its assertion. *See Layne Christensen Co. v. Bro-Tech Corp.*, 836 F.Supp.2d 1203, 1254 (D. Kan. 2011) (request for construction of the preamble not an admission it was limiting).

⁴ The public would understand from this explicit interaction between inventor and PTO, and the express removal of the MCM term from the claims, that the claims were not limited to MCM designs.

(Fed. Cir. 2010) (finding that lower court erred in construing preamble as limitation, and noting that “generally...the preamble does not limit the claims”);⁵ *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298 (Fed. Cir. 1999) (finding that the term in the preamble merely gave a descriptive name to the set of limitations in the body of the claim that completely set forth the invention).

Clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention....*Without such reliance, however a preamble generally is not limiting* when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention.

Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808-09 (Fed. Cir. 2002) (emphasis added). *See also IMS Tech. v. Haas Automation*, 206 F.3d 1422, 1434 (Fed. Cir. 2000) (“If the preamble adds no limitations to those in the body of the claim, the preamble is not itself a claim limitation and is irrelevant to proper construction of the claim.”). Moreover, limitations must generally not be read into the claims from the specification. The Federal Circuit has repeatedly “cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described.” *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004); *see also Dealertrack, Inc. v. Huber*, 674 F.3d 1315, 1327 (Fed. Cir. 2012) (citing *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1342 (Fed. Cir. 2010)) (improper to read limitations from a preferred embodiment absent a clear indication in the intrinsic record that patentee intended claims to be so limited).

Bearing in mind these basic guiding principles, and that *none* of the cases cited by

⁵ The Court explained that, “most importantly, the descriptor “photosensitive” does not embody an essential component of the invention. Instead, the term “photosensitive vaporization” is simply a descriptive name for the invention that is fully set forth in the bodies of the claims. *Id.* at 1359.

Cypress relate to the type of preamble amendment present in this case (or its effect on claim scope), no such reliance on the preamble exists in this case. Here, the only interaction Patentee had with the preamble during prosecution was to specifically remove the MCM term to make clear it always intended the preamble *not to* include such a limitation. The PTO clearly agreed the preamble was non-limiting because no 35 U.S.C. § 112 rejection to the new or amended claims was issued, which was based on a representation that there was “no new matter” added in the Reply to Office Action. (SENTIENT 00360). The PTO and allowed the claims on that basis. (SENTIENT 00330).

With respect to the points raised by Cypress, it would appear the parties agree that the claims at issue should be interpreted at least to include MCM designs. However, Cypress contends that the claims must be limited *only* to MCM embodiments, whereas Sentient submits that its “System on Chip” type invention is not properly limited only to MCM embodiments.

Cypress’s brief pursues several variations on this theme – namely that the deleted MCM term *must* be re-introduced and the claims limited thereto based on the content of certain sections of the specification and the extrinsic opinions of its expert. Cypress contends that because supposedly only one embodiment is disclosed, the claims can be no broader than that preferred embodiment. Notwithstanding that this premise is legally incorrect,⁶ close examination of the specification, including certain portions relied on by Cypress, fails to support this contention. For example, in its brief, Cypress states: “The present invention *generally* relates to multi-chip modules (MCM). More specifically, the present invention relates to an MCM capable of...” (§

⁶ In *In re Global IP Holdings*, 927 F.3d 1373 (Fed. Cir. 2019), the Examiner rejected the patentee’s attempt to seek a reissue to broaden the claims from “thermoplastics” to “plastics” because the amendment was not supported by the written description, which only disclosed thermoplastics. The PTAB affirmed, but the Court vacated, holding that the PTAB “legally erred,” and stating that a specification disclosing a species can support claiming a genus. 927 F.3d at 1375-77 (citing *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010)).

2(i), *supra*) (citing '177 Patent at 1:11-18) (emphasis added). This explains what the invention *generally* relates to. It *does not say* that the invention is limited to MCM constructions either specifically or exclusively as Cypress suggests.

Similarly, Cypress relies on a portion of the specification describing the MCM design as an embodiment of the System on a Chip type invention: “The present invention *is embodiment* in a tightly coupled smart control system *which uses* a multi-chip module (MCM) instrument controller which uniquely combines conventional high-density interconnects patterned in an overlay of MCM substrates.” (§ 2(i), *supra*) (citing '177 Patent a 3:41-45) (emphasis added). Cypress, however, omits that the MCM based construction *is not* identified by the specification as a core element of the “System on a Chip” type invention described:

The *core elements* of the present invention include a microprocessor, static random access memory (single or multi-ported), non-volatile memory (e.g., flash or EEPROM), a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion.

'177 Patent at 3:41-45 (emphasis added). (*See also* SENTIENT 000357-358) (prosecution history wherein Patentee re-affirms these elements as core elements of the invention).

Cypress also cannot point to any clear and unmistakable disclaimer in the intrinsic evidence to show that its MCM construction is required and that the claims of the '177 Patent are so limited. In fact, the specification excerpts and the file history exchange noted above inform the public exactly otherwise. Further, the public would understand: “[T]he invention is similar to a “system-on-a-chip” and appears similar to a chip in size, weight and physical configuration...” *See, e.g.*, '177 Patent at 3:55-58. And the public would understand that the claimed invention is “is built like a hybrid microcircuit but possesses a highly integrated behavior more consistent with “system-on-a-chip” or monolithic IC designs.” *Id.* at 1:65-2:1. Accordingly, Patentee’s

proposed construction of instrument controller as “*an electronic circuit that provides "System on a Chip" control functions consistent with the performance and operation of an Integrated Circuit device*” is based directly on the teachings of the specification and the understanding of one of ordinary skill in the art. It should be adopted.

Additionally, Cypress seems to contend that Sentient believed its invention and claims were of a narrower scope and somehow misled the PTO into allowing the issued claims in error. This is nothing more than mere speculation and should be rejected.

The preamble is typically non-limiting. In its Office Action dated December 8, 2004, the PTO merely restated the preamble in its communication, consistent with its regular practice regarding restriction requirements, but never identifies the preamble as limiting in any way. (SENTIENT 000367). This included several rejections and indicated what the allowable subject matter was, none of which was related at all to the preamble language. (SENTIENT 000368-372). Consistent with the PTO’s guidance on analyzing preambles during examination in accordance with the *Catalina* standard (*supra*) as set forth in MPEP § 2111.02 II, the preamble was determined not limiting. Patentee in its response, amended the pending claims *removing the MCM language* and added new claims 14-27, none of which included the MCM language in the preamble, and indicated there was there was “no new matter.” (SENTIENT 000347-356). A Notice of Allowance issued on March 14, 2005. (SENTIENT 000330-000333). No Section 112 concern was ever raised by the PTO and, most importantly, the ‘177 Patent issued without any MCM limitation. Cypress’s contention that something other than this publicly reported series of events occurred has no support in the record and is nothing more than speculation. *See RSA Protective Tech, LLC v. Secure USA, Inc.*, 2019 WL 9048994, at *4 (S.D. Fla. May 15, 2019) (declining to find any disclaimer and noting that amendment was not made to overcome prior

art). Accordingly, it should be rejected.

Cypress also complains that Sentient’s use of the “System on Chip” terminology from its specification describing the invention is somehow improper, unfair or misleading. But a patentee is entitled to use its disclosure as a basis for defining the scope the invention. Cypress itself relies on this practice extensively in its briefing. That Cypress later decided to use the same “System on Chip” terminology for its own accused product does not undermine this otherwise proper claim construction based on the intrinsic evidence. Moreover, any suggestion by Cypress that claim construction should somehow be influenced based on references to the accused products is legally flawed. *See NeoMagic Corp. v. Trident Microsys., Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) (citing *SRI Int’l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 118 (Fed. Cir. 1985)) (“It is well settled that claims may not be construed by reference to the accused device.”).

There are at least two additional flaws in Cypress’s argument that the preamble is limited to MCM constructions. The body of the claims here “describe[s] a structurally complete System on a Chip type invention” and the preamble is therefore not so limited. *Catalina*, 289 F.3d at 808-09; *Am. Med. Sys.*, 618 F.3d at 1359; *Pitney*, 182 F.3d at 1305. The original preamble of “an MCM instrument controller” could easily be replaced with the words “an apparatus” or “a device” serving as a mere container of claim elements without changing the scope of the claims at all because: 1) the MCM term does not appear anywhere in the issued claims, and, because 2) it “describes a structurally complete invention.” *Catalina*, 289 F.3d at 808-09.

4. Defendant’s Sur-Reply Position

Sentient cannot change the intrinsic record on the term “instrument controller,” so its Reply all but ignores the record. Sentient throws out a new argument that the preamble should not be given patentable weight, but Sentient’s new argument is both wrong and lacks credibility as

Sentient itself proposed a limiting construction for the preamble.

Turning first to the evidence that Sentient ignores. The specification explains that “**The invention** combines all of these elements on a **single tightly coupled MCM** to achieve its stand-alone capabilities.” ’177 Patent at 4:1-2. The title of the patent is “Multi-Chip Module Smart Controller.” Sentient nowhere addresses either of these unequivocal descriptions of the invention. Not an embodiment—the invention. The specification also states “the present invention relates to an MCM capable of...” *Id.* at 1:11-18. Sentient does at least quote this language in its brief, but then dismisses it by pointing to the word “generally” in the *previous* sentence. But this statement is clear; it does not say generally, it says “the present invention relates.” *Id.* Sentient also never addresses the patent’s discussion of the prior art and the patent’s multiple statements that “what is needed is an MCM design...” *See id.* at 2:15-16; 2:27. Sentient similarly never addresses the Summary of the Invention section of the patent that unequivocally states: “The **present invention is** embodied in a stand-alone, compact low-power electronics instrument controller which utilizes an MCM design.” *Id.* at 2:33-36. Sentient likewise does not address the multitude of other statements in the specification defining the invention as being an MCM. *Id.* at Abstract; 3:27-29; 3:46-49; 6:9-11. Lacking any rebuttal to the repeated and clear statements defining the invention as being an MCM, Sentient attempts to distract by pointing to other portions of the specification and emphasizing that they merely describe an embodiment having an MCM. Since the patent states numerous times that the invention **is** an MCM, of course the one and only embodiment is an MCM. Finally, Sentient resorts, again, to quoting a truncated version of the two lone places that the phrase “system-on-a-chip” appears, ignoring that the full language provides forceful support for limiting the claims to an MCM and distinguishes the MCM invention **from** a “system-on-a-chip.” *See Answering*

Brief (“AB”), Term 1.⁷ Moreover, while claims should not be construed ***based upon*** the accused product, the Federal Circuit has made equally clear that this rule “does not forbid awareness of the accused product or process to supply the parameters and scope of the infringement analysis, including its claim construction component.” *Wilson Sporting Goods Co. v. Hillerich & Bradsby Co.*, 442 F.3d 1322, 1331 (Fed. Cir. 2006); *see also Typhoon Touch Techs., Inc. v. Dell, Inc.*, 659 F.3d 1376, 1383 (Fed. Cir. 2011) (“It is not inappropriate for a court to consider the accused devices when construing claim terms, for the purpose of “claim construction” is to resolve issues of infringement.”).

Beyond this, the prosecution history supports an identical conclusion. While Sentient may wish to rewrite its statements to the Patent Office, it cannot deny it stated that removing the term MCM from the claims did not alter their scope. No amount of *post hoc* rationalization can change the fact that these statements can only be honest ones if the instrument controller was drawn to an MCM as the title, field of the invention, summary of the invention, and specification demand.⁸

Lastly, Sentient presents a brand new argument that the preamble is not limiting—despite having proposed the term and provided a construction. To be clear, proposing a construction for a preamble term (not in the alternative) is an argument that it is entitled to patentable weight. Preambles that are not entitled to patentable weight are not construed, because they have no weight. Moreover, at no point until its Reply brief (both in prosecution and litigation) did Sentient ever

⁷ Sentient also nowhere disputes that against prior defendants it saw no need to define the instrument controller as a “system on a chip,” or that its purpose to do so now is to ensnare products solely because of their names. Indeed, Sentient’s complaints about referring to the accused products are ironic, because Cypress is not the one actually doing this—Sentient is. Here, Cypress merely notes the names of the products to give context on how Sentient’s construction is an effort to unfairly incorporate the accused product’s name directly into the Court’s claim construction.

⁸ Also, contrary to Sentient’s unsupported assertion, the examiner nowhere determined the preamble to not be limiting.

assert that the preamble here is not limiting. It should not even be permitted to now offer this inconsistent position—especially since it continues to propose a construction for the term.

Regardless, the term instrument controller is entitled to patentable weight for multiple reasons. First, the term “instrument controller” provides antecedent basis for every claim set. The Federal Circuit has “repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.” *In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019); *see also Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). And here, the term “instrument controller” must be given patentable weight in every independent claim because it serves as antecedent basis for either that independent claim, one or more of its dependent claims, or both. In particular, “**the** instrument controller” is recited in the body of claims 1-5 and 10-20. This term is also recited in dependent claim 9, which depends on independent claim 6. Due to this dependency, “instrument controller” in independent claim 6 must also be given patentable weight and thus, it limits claims 6 and claims 7, 8, and 9 that depend from 6.

This use as antecedent basis is by itself dispositive of Sentient’s argument, but beyond this, the case Sentient primarily cites dealt with no antecedent basis and had a preamble describing the invention’s intended use, not its structure (unlike the ’177 patent). *See Layne Christensen Co. v. Bro-Tech Corp.*, 836 F. Supp. 2d 1203, 1254 (D. Kan. 2011). In fact, *Layne* states:

In general a preamble limits the invention if it **recites essential structure** or steps, or if it is necessary to **give life, meaning, and vitality to the claim**. Conversely, a preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. . . . Additionally, **dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope** because it indicates a reliance on both the preamble and claim body to define the claimed invention.

Id. (quoting *Catalina*, 289 F.3d at 808–09 (emphasis added)). Here, “instrument

controller”— especially as the specification repeatedly defines it—provides essential overall structure of the invention (not merely “a purpose or intended use”) **and** is an antecedent basis for multiple claims. *See e.g.*, ’177 Patent Claims 1 and 2; *see also In re Fought*, 941 F.3d at 1178 (Federal Circuit has “repeatedly held a preamble limiting when it serves as antecedent basis for a term appearing in the body of a claim.”). Thus, *Layne* and Circuit precedent teach the preamble here is indeed limiting.

Sentient also mistakenly cites MPEP § 2111.02 II which is entitled, “Preamble Statements Reciting Purpose or Intended Use.” An MCM instrument controller is neither; rather, it is “a fundamental characteristic of the claimed invention that is properly construed as a limitation of the claim.” *See Poly-Am., L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004) (reaching the same conclusion on a term when the specification was “replete with references” to the term, “including the title of the patent itself and the ‘Summary of the Invention,’” “repeatedly” used to describe the preferred embodiments and restated in all of the patent’s claims). Sentient also quotes *Catalina* in support, but *Catalina*’s very next sentence illustrates how the preamble is more likely limiting because the ’177 Patent’s specification shows “clear reliance on the benefits or features” of an MCM “as patentability significant.” *See* 289 F.3d at 809. In *American Medical Systems, Inc. v. Biolitec, Inc.*, another of Sentient’s cases, the Circuit expressly clarified how antecedent basis was not in play. 618 F.3d 1354, 1359 (Fed. Cir. 2010). And neither *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298 (Fed. Cir. 1999), nor *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422 (Fed. Cir. 2000) discuss the relevance of antecedent basis at all. Sentient’s remaining cases (*In re Am. Acad. of Sci. Tech.*, 367 F.3d 1359 (Fed. Cir. 2004); *Dealertrack, Inc. v. Huber*, 674 F.3d 1315 (Fed. Cir. 2012)) do not opine on whether the preambles limited the claims at issue, nor did they

deal with specifications and embodiments that clearly limited the inventions. As to the patent’s lack of written description, Sentient’s footnote that “disclosing a species can support claiming a genus” does not consider the “number of factors that bear on whether a written description disclosing a species supports generic claims,” as its case law instructs it to do. *See In re Global IP Holdings LLC*, 927 F.3d 1373, at 1377-78 (Fed. Cir. 2019). Thus, Cypress respectfully requests adoption of its proposed construction.

Term 2: “embedded”

Term	Sentient’s Proposal	Cypress’s Proposal
“embedded”	“on-chip”	Plain Meaning. Specifically, embedded means what it says, embedded within the component that is required in that part of the claim (<i>e.g.</i> , embedded in processor, means embedded (<i>i.e.</i> , implanted) in the processor; embedded within FPGA means embedded (<i>i.e.</i> , implanted) within the FPGA).

1. Plaintiff’s Opening Position

“Embedded” appears in the claims of the ‘177 Patent in the context of certain electronic components, namely an “embedded memory” (*e.g.*, Claims 1-12) and an “embedded power converter” (*e.g.*, Claims 5, 9-20). Although not explicitly defined in the ‘177 Patent, “embedded” in this context is a term of art well understood by those of ordinary skill to mean “on-chip.”

An artisan of ordinary skill would understand that an “embedded” component is not a stand-alone component but is rather integrated “on-chip” with at least one other component. For example, the Integrated Circuit Engineering “Memory 97” Report, an industry standard overview of memory products available at the time of filing, explains that an “[e]mbedded memory is any non-stand-alone memory. It is an integrated on-chip memory that supports the logic core to accomplish intended functions.” (SENTIENT 000260-274).

This meaning is consistent with the use of the term “embedded” in the claims, and the rest of the specification. To illustrate, the context in which “embedded” appears in the claims is instructive—*e.g.*, Claims 1-12 require “the processor...having an *embedded* memory for storing an initialization program.” Using the Memory 97 teaching, this phrase translates into “the processor having an *on-chip* memory that supports the logic core for storing an initialization program.” This is perfectly consistent with the ‘177 Patent specification where the processor is disclosed to include an embedded memory that enables the startup of processing. *See, e.g.*, ‘177 Patent at 4:57-59 (“In a preferred embodiment, the microprocessor of the present invention preferably includes an embedded memory that enables the startup of processing.”). Nothing in the specification shows, requires, or otherwise suggests that the embedded memory can be, let alone *must* be, *physically inside* the processor as Cypress proposes. Further, no such suggestion, disclosure or requirement exists in the intrinsic record or the claims themselves.

Cypress’s proposal of “implanted within” seeks to narrow the meaning of “embedded” in exactly this way, that is – beyond how the skilled artisan would understand the term in the context of electronic components. In the context of electronic components, while an “embedded memory,” for example, could be included “implanted within” another component, it need not be. The plain claim language is simply “embedded”—not “embedded *into*” or “embedded *in*”—which more arguably could support a narrower construction including “implanted within.” Construing “embedded” as “on-chip” is consistent with this plain claim language and the understanding of those of ordinary skill in the art.

Furthermore, the intrinsic record contains persuasive evidence of why the Cypress proposal is incorrect. For example, claims 5 and 9-20 recite an “internal embedded power converter.” When Patentee intended for a certain structure to be “within” another structure it chose to use the

term “internal embedded” in accordance with a preferred embodiment of the invention. For example, see ‘177 Patent at 8:59-9:5 and Fig. 3, which explains that the gates used to form the power converter are physically inside the FPGA structure. Thus, it is clear from the intrinsic record that Patentee specifically chose to use the word “internal” to modify embedded in the case where “physically within” was intended, and in doing so acted as its own lexicographer. *See Thorner*, 669 F.3d at 1365. By choosing not to use the term “internal” in conjunction with the “embedded memory” in either the specification, the claims, or elsewhere in the intrinsic record, it is clear Patentee did not intend the “implanted within” limitation that Cypress urges.

Moreover, it is also notable that “within” is a term that appears numerous times in the claims. *See, e.g.*, ‘177 Patent Claims 1, 3, 5, 9, 13, and 17. If Patentee intended “embedded memory” to be limited to “within,” he could have just as easily used the word “within,” as it did in other places, but did not. *See CAE Screenplates, Inc.*, 224 F.3d 1308, 1317 (Fed. Cir. 2000). Accordingly, Defendant’s proposal should be rejected.

2. Defendant’s Answering Position

i. Plain Meaning of “Embedded” Is Unequivocally Established by the Intrinsic Evidence

The plain meaning of “embedded” is readily apparent from its repeated use in the claims as referring to something that is implanted (or integrated into) a specific portion of the controller device—nothing more, nothing less. *See, e.g.*, ‘177 Patent at Claims 1-12 (all requiring a “processor” ... “having an embedded memory”). Cypress’s proposed construction conveys this plain meaning of the term. Moreover, in addition to the plain meaning in the claims, the specification confirms that “*the microprocessor* of the present invention preferably *includes an embedded memory* that enables the startup of processing without first loading a program from the non-volatile memory.” Given the language of the claims and the

specification, a person of ordinary skill in the art—indeed, anyone familiar with the English language⁹—would readily understand that the memory must be embedded (*i.e.*, “implanted”) in the microprocessor, and not simply located anywhere “on-chip,” much less anywhere on a controller device. See Hassoun Decl. ¶¶ 14, 16-17. Thus, the term “embedded” should simply be given its plain and ordinary meaning as proposed by Cypress.

ii. Sentient’s Proposed Construction Lacks Intrinsic Evidentiary Support

Nowhere does the specification use Sentient’s proposed phrase “on-chip” to explain the location of the embedded memory or the embedded power converter. Sentient’s proposal, therefore, is entirely unmoored from the intrinsic evidence. Lacking any intrinsic support for its use of the term “on-chip,” Sentient resorts to extrinsic evidence in the form of a book that it asserts provides support for equating embedded with “on-chip.” But, even with regard to its own extrinsic evidence, Sentient is mistaken. Rather than evidence a uniform understanding that embedded equates to being “on-chip”, the book demonstrates that “embedded” memory can mean being integrated on a single chip, or it could refer to the memory being embedded within an overall device, for example on a larger board along with other chip components. Hassoun Decl. ¶¶ 14-17. Therefore, even Sentient’s extrinsic evidence merely shows that embedded means being integrated on (*i.e.*, implanted within) something else—which is precisely the plain meaning that Cypress proposes for the term.

iii. Sentient’s Proposed Construction Would Render “Embedded” Meaningless

In addition to being at odds with the plain meaning that is repeatedly confirmed by the

⁹ An adjective like “embedded” is used to describe the relationship between two objects. It would only be proper to incorporate one of those objects into the definition of the adjective if that object was used every time the adjective was used. But here, embedded is used to describe the specific relationship between a variety of different objects, including between the microprocessor and memory—not generically in reference to being on a “chip.”

Patent’s claims and specification, Sentient’s approach would render the term “embedded” meaningless in the context of this dispute. As the Federal Circuit has emphasized, while claims are not to be construed in light of the accused products, the accused products provide meaningful context for the court to assess the parties’ disputes. *See, e.g., Pall Corp. v. Hemasure Inc.*, 181 F.3d 1305, 1308 (Fed. Cir. 1999) (“Although the construction of the claim is independent of the device charged with infringement, it is convenient for the court to concentrate on those aspects of the claim whose relation to the accused device is in dispute.”); *Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1580 (Fed. Cir. 1991) overruled in part on other grounds, *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1293 (Fed. Cir. 2009) (en banc) (“Of course the particular accused product (or process) is kept in mind, for it is efficient to focus on the construction of only the disputed elements or limitations of the claims.”).

Here, the accused product is constructed entirely on a single chip—which according to the specification itself is dramatically different from the type of MCM design of the ’177 patent. *See* ’177 Patent at 3:55-60 (alleged invention’s “MCM implementation, ***transcends*** the functional capability of a single integrated circuit”); *id.* at 1:64-2:8 (distinguishing even prior art MCMs from single-chip designs). Not surprisingly, therefore, Sentient’s effort to simply equate “embedded” as being “on-chip” would have a dramatically different meaning in the context of the ***multi***-chip module design of the ’177 patent, as opposed to the ***single*** chip design of the accused products. Specifically, if Sentient’s proposed construction is adopted, it would produce the absurd result that any component the Patent specifically requires to be “embedded” in a particular portion of the device—such as embedded in the processor or embedded in the FPGA—could instead be satisfied by simply being located *anywhere* “on-chip” in the Cypress accused single chip devices. In other words, for the Cypress accused products, literally every relevant component is somewhere “on-

chip.” Thus, in the context of this dispute, Sentient’s proposal would render the term “embedded” as being meaningless.¹⁰

Lastly, lacking intrinsic evidence regarding the straight-forward “embedded” term, Sentient sows confusion by introducing the term “internal.” Specifically, referencing the term “internal embedded power converter” and arguing that “embedded” means anywhere on-chip and “internal” means within the FPGA. See Sentient’s Opening Discussion of Term 2. Given that the term “embedded” is unequivocally established by the claims and the specification as meaning implanted within or on a specific component, Sentient’s reference to “internal” and its attempt to construe that term is irrelevant. Moreover, Sentient’s assertion that internal means inside a component, as opposed to being outside (*see id.*), is both unremarkable and inapposite to the dispute. The specification is replete with references showing that the term “internal” means located somewhere inside, as opposed to being external (*i.e.*, inside the device rather than outside the device). For example, nearly all of the claims require “at least two internal oscillators,” which are recited in the claims as being one of the various elements within the claimed MCM device. And the specification confirms the use of internal beginning with the heading: “Internal Clocking,” ’177 Patent at 6:65; and expressly states that the invention “can operate without need for control of an **internal or external clock**,” *id.* at 5:1-4. The section goes on to identify other components as likewise being internal to the controller. *See, e.g., id.* at 5:4-7 (“internal capacitive oscillating circuit”); *id.* at 5:19-21 (“internal 10 bit analog-to-digital (A/D) converter”). Similarly, the patent juxtaposes “internal” with “external” when describing the clocking of the FPGA. *Id.* at 2:48-50 (“Instead, the present invention adds a separately controllable FPGA that

¹⁰ In the context of the Patent, embedded could only possibly mean “on-chip” if the term was explicitly used in relationship **to a chip**, for example “the **chip** preferably includes an **embedded microprocessor**.” No such phrasing exists in the ’177 Patent.

acts as a parallel processor with **internal or separate external clock.**"); *see also id.* at 7:64-65 ("The invention provides for either **external or internal** input of a clock signal ..."); *id.* at 4:49-51 ("As shown, the FPGA may be clocked using the same **on-board** VCO as the microprocessor; or it may be clocked separately via an **external** clock 175."). The plain meaning of the term "internal" is, therefore, both unremarkable and in no sense contradicted by the plain meaning of "embedded" (*i.e.*, intimately connected or integrated or implanted within or on a referenced component).¹¹

For all the above reasons, Cypress respectfully requests that Sentient's proposed construction be rejected, and the term "embedded" be given its plain meaning as simply requiring the claimed embedded object to be implanted within and/or integrated onto, etc. the component that is identified in the relevant portion of the claim—*e.g.*, a processor having an embedded memory means the processor actually includes the embedded memory.

3. Plaintiff's Reply Position

As established in Sentient's Opening Brief, the term "embedded" has a common meaning to those in the art as being "on-chip" and not implanted as Cypress contends. In support of its position, Sentient cites to well-known industry standard reference "Memory '97." (SENTIENT 000260-274). Although extrinsic evidence, this reference is a contemporaneous and unbiased overview of all major memory manufactures and their products (including defendant Cypress's products) and explains the state of the art regarding "embedded" as it would be understood by

¹¹ Sentient argues that "internal" is needed to modify "embedded" when the two terms are used in the phrase "internal embedded power converter." *See* Sentient's Opening Discussion of Term 2. But Sentient's argument lacks merit, given that the terms "internal" and "embedded" are perfectly consistent. Moreover, Sentient's assertion that "internal" is necessary to modify "embedded" begs the question as to how one could possibly have an **external** embedded component.

one of ordinary skill in the art at the time of the invention to mean “on-chip.” (SENTIENT 000001-011). As Memory '97 explains:

Embedded memory is any non-stand-alone memory. *It is an integrated **on-chip memory*** that supports the logic core to accomplish intended functions. High-performance embedded memory is a key component in VLSI because of its high-speed and wide bus-width capability, which eliminates inter-chip communication.

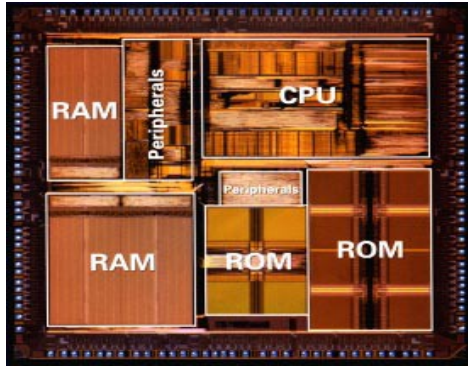
Figure 11-1 shows the increasing performance gap between microprocessors and DRAMs. As this gap has widened, chip designers placed greater emphasis on the development of embedded memory devices. Their task was made easier by at least two factors. *First, the complexity of process technology made it possible to incorporate logic and **memory on the same chip**.* Secondly, larger die size *allows the incorporation of both logic and **memory on the same chip**.*

Several advantages of using embedded memories are provided below. They include reduced number of chips, reduced pin count, multi-port memories, less board space requirements, faster response ***with memory embedded on-chip***, dedicated architecture, memory capacity specific for an application, reduced power consumption, and greater cost effectiveness at the system level.

The main disadvantages of embedded memories are that they are generally larger in size and are more complex to design and manufacture. Additionally, a trade-off must often be found between design and technology since the optimized technology for a memory cell is not the same as that for embedded logic devices. Furthermore, processing becomes even more complex when the designer *integrates different types **of memory on the same chip**.* Figure 11-2 presents a DSP from Texas Instruments that includes embedded memories. Note that the memory portion consumes about half the total area of the chip. RAM, ROM, and logic on one chip makes for a challenging design and for challenging manufacturing.

(SENTIENT 000260) (emphasis added).

Memory '97 provides an explicit illustration (Figure 11-2) of an embedded memory with respect to its physical location in relationship to a processor (CPU). (SENTIENT 262).



This industry standard reference not only explains that embedded simply means “on-chip” as Sentient proposes, but this understanding is further confirmed by Figure 11-2 that shows embedded memory “on the same chip” as the CPU but not “implanted within” (*i.e.*, all the memory blocks on the chip (labelled RAM and ROM) are all outside of the CPU block region).

Putting this straightforward explanation aside, the parties appear to agree that embedded, at a minimum, means “on-chip.” However, Cypress adds the constraint that embedded is both “on-chip” *and* further “implanted within” another circuit component. This is incorrect in view of the intrinsic record. Nothing in the specification or the claims show, require, or otherwise suggest that the embedded memory can be, let alone must be, physically inside the processor.

Moreover, Cypress’s contention that Sentient’s proposal would render the term “embedded” meaningless is without merit. Rather, Sentient’s proposal is based on a simple, logical and hierarchically sensible approach to the evidence – namely, that embedded means “on-chip” rather than “off-chip” (as discussed above in the Memory ’97 excerpt above) and that “internally embedded” further means “physically within” as explained at page 8-9 of its Opening Brief. When Patentee intended for a certain structure to be “within” another structure, it used the term “internal embedded” in accordance with a preferred embodiment of the invention. *See* ‘177 Patent at 8:59-9:5, Fig. 3 (explaining that the gates used to form the power converter are *physically inside* the FPGA structure). The intrinsic record establishes that Patentee specifically

chose to use the word “internal” to modify “embedded” in the case where “physically within” was intended, and in doing so acted as its own lexicographer. *See Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). By choosing *not* to use the term “internal” in conjunction with the “embedded memory” in either the specification, the claims, or elsewhere in the intrinsic record, it is clear to the public and PTO that Patentee did not intend the “implanted within” limitation that Cypress urges.

Cypress’s attempt to further complicate this analysis by reference to the accused products is misguided as the case law it relies on demonstrates. *See Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1580 (Fed. Cir. 1991) (“the construction of the claim is independent of the device charged with infringement.”); *NeoMagic*, 287 F.3d at 1074 (“claims may not be construed by reference to the accused device.”).

Lastly, it is telling that Cypress, a major purveyor of integrated circuit devices including memory devices for over 30 years, provides no contemporaneous or unbiased third-party evidence to rebut the industry standard meaning of “embedded” explained in Memory ’97. Rather, it is forced to rely on speculation and the partisan opinions of its expert generated solely in connection with this litigation.

4. Defendant’s Sur-Reply Position

As an initial matter, Cypress does not agree and has never advocated that “embedded” means “on-chip.” As exhaustively discussed previously, the intrinsic record is dispositive—“embedded” means implanted in a reference object—which, in the ’177 Patent, is never just “a chip.” For example, Claim 1’s language clearly and simply requires a “processor ... having an embedded memory.” The patent also gives the rationale, and indeed, specifically distinguishes the prior art based on its feature of having memory implanted directly in the processor: explaining

that locating memory in the processor is essential to allowing “abbreviated time to activation” of the processor without waiting for the “loading of the initiating program” from outside the processor. *See* ’177 Patent at 4:57-67. The Reply does not address this critical part of the specification. Remarkably, the Reply barely cites the patent at all—and when it does so, it does not even address the disputed term: “embedded.” Rather, the Reply’s sole discussion of the intrinsic evidence concerns the term “internal” (which no one seeks to construe). Ignoring the intrinsic record, Sentient relies almost exclusively on the book “Memory 1997” in an effort to alter the plain meaning of the claims and the intrinsic evidence. This is particularly inappropriate here where the intrinsic record provides a clear meaning for “embedded.” *See Pitney Bowes*, 182 F.3d at 1308.

And even the Memory ’97 extrinsic evidence merely confirms that “embedded” means implanted within an area—as Dr. Hassoun explained, Sentient selectively presents only a definition of “embedded memory” that is on-chip, despite the fact that the book gives many examples of types of “embedded” memory that are embedded elsewhere, such as within a multi-chip system mounted on the same board. *See* Hassoun Decl. ¶ 15. Sentient does not rebut this fact. Instead, Sentient cites Fig. 11-2 and asserts that it shows memory “on-chip” but not “embedded” within the CPU. This is both true and irrelevant. As Cypress has explained, many examples exist of memory “embedded” on a chip; there are also many examples where memory is embedded generally within a multi-chip system; and, of course, memory can be embedded specifically in a component such as a processor. The plain meaning of “embedded,” thus, simply depends upon the context of its use. *See also, e.g.,* Halkowski Decl. Ex. 4 at 17:27-41 (asserted prior art patent disclosing “embedded CPU 212” within multi-chip “interface card”). Here, as detailed above, the language of the claims (“processor ... having an embedded memory”)—

confirmed by the clear explanation in the specification—compels the plain meaning proposed by Cypress.

Term 3: “oscillator”

Term	Sentient’s Proposal	Cypress’s Proposal
“oscillator”	“a circuit which is used to generate or produce a clock signal”	“voltage controlled oscillator”

1. Plaintiff’s Opening Position

The term “oscillator” is a term of art that is commonly used by those of ordinary skill. To the extent that Cypress contends that “oscillator” must be limited to a “voltage controlled oscillator,” such a construction should be rejected.

Cypress’s proposal seeks to impermissibly limit the meaning of oscillator to a “voltage controlled oscillator.” This proposal, on its face, provides no clarity for the jury on what the term “oscillator” means, and even more problematically, it improperly reads two additional technical words or limitations—“voltage and controlled”—into the claim term. This adds no clarity but instead creates confusion as to what an oscillator does within the context of the claim. Although the ‘177 Patent does discuss the use of a voltage controlled oscillator (“VCO”) in some instances of the specification, nothing in the intrinsic record limits the claimed “oscillator” to be a “VCO.” Instead, the claims simply use the word “oscillator.” In addition, the specification describes numerous different varieties of oscillators, not just VCOs *See, e.g.*, ‘177 Patent at 7:15-19 (disclosing the possible use of “crystal oscillators,” “non-crystal based oscillators,” and “external oscillators”); 6:66-67 (disclosing the possible use of an “internal oscillator”); 4:10-13 (disclosing the possible use of a “voltage controlled oscillator (VCO) or external clock”).

The ‘177 Patent explains in detail that an oscillator is used to generate or produce a clock signal for electronic components such as a microprocessor and a field programmable gate array

(“FPGA”). *See, e.g., id.* at 7:1-12 (“the oscillators are *used to produce internal clock signals* which clock the microprocessor. In a preferred embodiment, one oscillator *generates a high-frequency clock signal....*The other oscillator *generates a low-frequency clock signal* for low-frequency operations, respectively....The third oscillator *generates a clock signal* which is used for the individually programmable FPGA.”).

Thus, the Court should adopt Sentient’s proposal that “oscillator” simply be construed as: “a circuit which is used to generate or produce a clock signal.” This construction is consistent with the intrinsic record. This construction is also consistent with the extrinsic evidence. For example, The Computer Glossary defines oscillator as “[a]n electronic *circuit used to generate high-frequency pulses.*” (SENTIENT 000314-316); (*see also* SENTIENT 000308-310) (McGraw Hill Illustrated Dictionary of Personal Computers defining “oscillator” as “[a] low-current source of an alternating voltage at any frequency. Oscillators may be electrical, electronic, or mechanical. Most microcomputer systems use an oscillator with a piezoelectric crystal to provide a stable reference frequency for clocking.”); (SENTIENT 000304-307) (The Modern Dictionary Electronics Technology defining “oscillator” as a “[c]ircuit design consisting of resistors, inductors, and capacitors capable of sustained generation of an ac voltage. Self-sustained frequencies are emitted at the resonant frequency of the tuned circuit network.”).

2. Defendant’s Answering Position

As Sentient’s citations to dictionary definitions show, there are many types of oscillators that were already known in the art. However, the only oscillators expressly claimed in the patent are the “at least two internal oscillators” coupled to the processor. *See* Claims 1, 6, 10, 14, 19. And the specification identifies only one type of internal oscillator that is coupled to the processor: a “voltage controlled oscillator” or “VCO.” For example:

FIG. 1 is a schematic block diagram which illustrates a preferred embodiment of the present invention. As shown, the invention is comprised of a microprocessor 110 having a plurality of I/O ports, including analog inputs/outputs and digital serial inputs/outputs. The **microprocessor** 110 is preferably clocked by a system clock signal SYS CLK which is generated by either **an on-module voltage controlled oscillator (VCO)** 115 or an external clock 120. In a preferred embodiment the present invention actually **includes two different on-module VCOs for generating a high frequency clock signal and a low frequency clock signal.**

'177 Patent at 4:6-13. In fact, this is the only description anywhere in the specification that describes the “at least two oscillators connected to the processor.” In short, voltage controlled oscillators are the only type of oscillator that is enabled. While enablement issues are not always addressed at claim construction, the lack of enablement supporting any other type of oscillator will persist if a broad construction, such as Sentient’s, is adopted. *See Wang Labs., Inc. v. Am. Online, Inc.*, 197 F.3d 1377, 1383 (Fed. Cir. 1999) (“claims should be construed, when feasible, to sustain their validity”). Thus, Cypress respectfully requests that its proposed construction be adopted.

3. Plaintiff’s Reply Position

The specification describes many types of oscillators, with the common characteristic being the production of clock signals. Cypress’s suggestion to further limit “oscillator” to just a “voltage controlled oscillator” (“VCO”) attempts to impermissibly limit the claim to a preferred embodiment even though its own cite demonstrates this: “FIG. 1 is a...block diagram which illustrates a *preferred embodiment*.” (§ 2, *supra*) (emphasis added). Notably, Cypress does not dispute that neither the originally filed claims or the issued claims include this limitation. This is strong intrinsic record support that the claims do not require a VCO. The “only oscillators expressly claimed are ‘at least two internal oscillators’....” (§ 2, *supra*) (citing ‘177 Patent, Claims 1,6, 10, 14, 19). Simply put, none of the claims include a VCO term.

Moreover, Cypress's attempt to introduce enablement and/or written description concepts in the claim construction is improper.¹² Furthermore, Cypress's heavy reliance on *Wang* is misplaced. That case was concerned with a means plus function claim element which was subject to a different more restrictive standard than here under 35 U.S.C. § 112, paragraph 6. Further, the patentee in *Wang* specifically disclaimed the scope of the claim during prosecution that it was seeking to "recapture" in litigation. Neither of these factors are present in this case. *See also Liebel-Flarsheim Co. v. Medrad, Inc.* 358 F.3d 898, 906 (Fed. Cir. 2004) (warning against limiting the claims to single disclosed embodiment to satisfy (or in view of) other legal requirements such as § 112 or other validity concerns). Thus, Cypress's proposal should be rejected.

4. Defendant's Sur-Reply Position

Sentient agrees that the only two oscillators in the claims are "two internal oscillators" coupled to the processor, and does not dispute that the intrinsic record describes these oscillators specifically as voltage controlled oscillators. *See* '177 Patent at 4:9-19. With regard to § 112 issues, Sentient fails to conduct the analysis *In re Global IP* outlines regarding when a species disclosure supports a genus claim. *See* 927 F.3d at 1377-78. And Sentient's dismissal of *Wang Laboratories, Inc. v. America Online, Inc.*, 197 F.3d 1377 (Fed. Cir. 1999) on means-plus-function grounds is unfounded. There are many other cases that warn of § 112 problems, if a term is construed too broadly. *See* AB, Term 1 n.5. *Wang* itself reiterates that a court should "seek[] to interpret claims to preserve, rather than defeat, their validity" *Id.* at 1383 (quoting *Eastman Kodak Co. v. Goodyear Tire & Rubber Co.*, 114 F.3d 1547, 1556 (Fed. Cir. 1997) (abrogated on other grounds)).

¹² In any event, Cypress's position is legally unavailing as a species disclosure of a voltage controlled oscillator (VCO) provides written support for the genus claim element (oscillator). *See In re Global IP Holdings*, 927 F.3d at 1375-77.

Term 4: “two internal oscillators”

Term	Sentient’s Proposal	Cypress’s Proposal
“two internal oscillators coupled to the processor, for providing clock signals for the low-frequency and high-frequency operations”	Plain and ordinary meaning (after “oscillator” construed) Namely “two internal circuits which are used to generate or produce a clock signal coupled to the processor for providing clock signals for the low-frequency and high-frequency operations”	“two independent internal oscillators coupled to the processor, for providing clock signals one for the low-frequency and another for the high-frequency operations”

1. Plaintiff’s Opening Position

Plaintiff Sentient believes that after “oscillator” is construed above, this term requires no further construction and may be afforded its plain and ordinary meaning. On the other hand, Cypress’s proposal should be rejected because it again seeks add a limitation that is simply not in the claims. The new limitation of “independent” with respect to oscillator is not in any new, amended, or original claim nor can Cypress point to any “clear and unmistakable” disavowal of claim scope made during prosecution requiring this new limitation to now be written into the claim. *See Continental Circuits LLC*, 915 F.3d at 797.

To the extent Cypress contends that such a limitation is necessary, *e.g.*, for embodiments concerned with power conservation, Patentee points out that no such power conservation concept or requirement is recited in *any* of the claims. Any attempt to “back-door” such a new concept now through claim construction would only serve to further limit the claim beyond what was intended by the Patentee during prosecution. *See In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d at 1369 (cautioning “against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described”).

Further, the term “independent” or “independently” appears 12 times in 7 claims in the

‘177 Patent (claims 1, 4-5, 8, 10-11 and 15), but never once in connection with an oscillator(s). Although Patentee describes in a preferred embodiment that a low frequency clock signal may be “independently generated” – it did not use the term “independent” or “independently” in the claim language – either in the originally filed claims or through argument or amendment. Such a concept is completely absent from the claims. Moreover, this limitation is *not identified as being a core feature of the invention* in the specification, and therefore is *not* required. *See, e.g.*, ‘177 Patent at 2:66-3:5. Accordingly, the intrinsic evidence demonstrates that Patentee manifested a clear intent not to include such a limitation (*i.e.*, knew how to introduce this limitation, but instead specifically chose not to do so with regard to the claimed oscillators). *See CAE Screenplates*, 224 F.3d at 1317.

Accordingly, Defendant’s claim construction should be rejected.

2. Defendant’s Answering Position

Cypress agrees that the plain meaning of this term suffices and that is what Cypress’s proposal is intended to capture. However, Sentient’s purported “plain meaning” would genericize this element as being two “internal circuits” and open the door to Sentient effectively eliminating the requirement that there actually be **two** internal oscillators. Specifically, under Sentient’s proposal it could attempt to double-count one oscillator as satisfying the Patent’s clear requirement for two oscillators. Sentient could do so by labeling one oscillator as being the first “internal circuit” and a then defining a second “internal circuit” as being that **same** oscillator plus other internal circuitry. Under Sentient’s definition, therefore, it could argue that it had identified two “internal circuits” and—under this “Alice In Wonderland” logic—could conclude there were “two oscillators.” Cypress’s simple proposal would foreclose such mischief and, indeed, is merely an effort to clearly set forth the plain meaning of this term—*i.e.*, that the claims

actually require two oscillators.

Also, the only embodiment in the specification clearly and repeatedly states that the “at least two internal oscillators” required by the claims must be independent, with one of the oscillators providing a low frequency clock signal and the other providing a high frequency clock signal. *See, e.g.,* ’177 Patent at 4:10-16 (“In a preferred embodiment the present invention actually includes ***two different on-module VCOs for generating a high frequency clock signal and a low frequency clock signal.***”). This begs a critical question: Why does the patent specification and claims over and over again state that the “at least two internal oscillators” must provide “clock signals for the low-frequency and high-frequency operations”? The answer is clearly, and repeatedly, provided by the specification which teaches that it is “***necessary***” for the two claimed internal oscillators to be “independent” for power preservation:

“The distinction between the high-frequency and low-frequency oscillators is important as ***it is necessary for power preservation to maintain an independent oscillator that operates at a lower frequency.***”

Id. at 6:66-7:30. Power preservation is a core aspect of the alleged invention as repeatedly stated in the “Summary of the Invention”:

However, ***an electronics instrument controller designed in accordance with the present invention has less complexity, includes enhanced power management,*** and offers more functional flexibility than prior art controllers. . . .

Along with its increased functionality and unique circuit design, the ***primary characteristics of the present invention*** are its compact size, light weight, ***low power consumption***, and compatibility with robust application regimes.

Id. at 2:36-40; 2:62-66. Similarly, in a section of the specification entitled, “Overall Functional Elements and Configuration”, the Patent again clearly teaches:

The invention combines all of these elements on a single tightly coupled MCM to achieve its stand-alone capabilities. ***These capabilities include ultra-low power requirements***, extremely small size and weight, versatile functionality, and the ability to operate in extreme environments.

Id. at 4:1-5.

Later, the specification discusses multiple different possible combinations of oscillators in addition to the “at least two internal oscillators”, and then provides this plain and unequivocal statement defining the alleged invention “[i]n all cases” as requiring an “independently” generated low frequency signal in order to ensure that a core aspect of the alleged invention—the ability to minimize power consumption—can be achieved:

In all cases, the low frequency clock signal is independently generated to minimize power consumption in divider networks and fast-switching drivers

Id. at 7:19-22.

Given the clear and unequivocal statements made by the patentee to the public that to achieve the alleged invention’s core functions, in “**all cases**” it is “**necessary**” to independently generate a low frequency clock signal, the plain meaning of the claims when read in light of the specification compels the adoption of Cypress’s proposed construction for this term. Cypress therefore respectfully requests that the Court adopts its proposed construction for this term.

3. Plaintiff’s Reply Position

As pointed out in its Opening Brief, although the term “independent” or “independently” appears 12 times in 7 claims in the ‘177 Patent (claims 1, 4-5, 8, 10-11 and 15), Patentee with clear intent chose not to use it even once in connection with an oscillator(s). Nor did the PTO identify the oscillators as, or require them to be, “independent” from one another. Moreover, this proposed “independent” oscillator limitation is not identified as being a core feature of the invention in the specification, and therefore is *not* required. *See, e.g.* ‘177 Patent at 2:66-3:5.¹³

Further, Sentient points out that for virtually all operations, only one clock signal is used

¹³ Cypress therefore cannot meet the clear and unmistakable threshold required for disavowal of claim scope. *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019).

depending on the frequency of operation (high or low). Cypress's newly proposed requirement that these be mutually exclusive without one modifying the other is simply not in the claims – and further, the question of what constitutes two oscillators is the subject of expert testimony and is not at issue here.

Moreover, any backhanded attempt by Cypress to justify rewriting the claims now based on a power preservation concern, is merely an improper attempt to impose a new power conservation requirement – which is completely absent from the claims as written – through claim construction now, would only serve to further limit the claims far beyond what was intended by the Patentee during prosecution. Cypress is impermissibly attempting to read limitations into the claim from a preferred embodiment in contradiction of governing law.

4. Defendant's Sur-Reply Position

Again Sentient leaves Cypress's intrinsic evidence substantively unaddressed. *See* AB, Term 4. As the patent states, “[t]he **distinction** between the high-frequency and low-frequency oscillators **is important as it is necessary** for power preservation **to maintain an independent oscillator** that operates at a lower frequency.” ’177 Patent at 7:7-10. And, “[i]n **all cases, the low frequency clock signal is independently generated** to minimize power consumption in divider networks and fast-switching drivers.” *Id.* at 7:19-22. The Federal Circuit has also recognized in similar circumstances that the descriptor “at least two” is synonymous with the requirement for “a plurality of specific, individual” items. *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1383 (Fed. Cir. 2003). Nor does Sentient dispute that its intent is to double-count a single oscillator as explained in Cypress's AB, which would alter the express claim language that there be “at least **two**” oscillators into an invention with only **one**. To borrow from Sentient's argument, the patentee with clear intent chose not to claim “one” oscillator, but two. The plain

and ordinary meaning of two is two; not one. Cypress’s proposal clarifies this.

Term 5: “power converter”

Term	Sentient’s Proposal	Cypress’s Proposal
“power converter”	“a converter which changes a voltage level to another voltage level”	Plain Meaning. Specifically, the required power converter is ~~actually~~ converting power (i.e., “a first stage in the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG).”). Col. 8:64-66.

1. Plaintiff’s Opening Position

“Power converter” is also a term well understood by artisans of ordinary skill. Thus, the plain and ordinary meaning should suffice here, which is proposed by Sentient above, with some particularity to avoid any confusion. Thus, Sentient proposes that one of ordinary skill would understand “power converter” to mean “converter which changes a voltage level to another voltage level.” The ‘177 Patent claims generally recite the feature of receiving an input voltage and from that input voltage generating “another voltage” which is fully consistent with the specification and the functional block diagram of FIG. 3. *See, e.g.*, ‘177 Patent Claims 5, 9-10; *id.* at 10:40-43; 11:20-23; 11:52-55) (specifically claiming a “*power converter* capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller.”). For example, the specification describes that a “power converter” converts or changes a voltage level to another voltage level.

In a preferred, embodiment subsets of gates in the FPGA can be used to provide power conversion, thereby forming an internal embedded power conversion module without requiring any additional circuitry. FIG. 3 is a functional block diagram which illustrates the internal power conversion concept. As shown in FIG. 3... the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG). A number of second stages convert from the fixed VREG to several power voltages consumed internal to the module. These second stage voltages provide for the supply of internal digital power, internal analog power, and a series of reference voltages.

Id. at 8:59-9:4; Figure 3; (*see also* SENTIENT 000311-313) (Microsoft Press Computer User's Dictionary defining “converter” as “[a]ny device that changes electrical signals or computer data from one form to another.”). Thus, Sentient’s proposal is consistent with both the intrinsic and extrinsic evidence.

On the other hand, Cypress’s proposal should be rejected because it again seeks to add numerous limitations from the specification and certain preferred embodiments that are simply not in the claims. *See, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d at 1369 (warning such a practice is inappropriate). For example, adding the new limitation of “*i.e.*, “a first stage in the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG).”), ‘177 Patent at 8:64-66, means including, at a minimum, the new unrecited concepts of: 1) a first stage, 2) internal (another claim term of significance);¹⁴ and 3) fixed regulated voltage; along with the other potential unclaimed and unexplained interactions between these new features. None of these limitations are in the claims, nor can Cypress point to any “clear and unmistakable” disavowal of claim scope requiring these new and very specific limitations to be written into the claims. *See Continental Circuits LLC*, 915 F.3d at 797.

Moreover, adding the term “actually,” a superfluous adverb, serves not only to add yet another unsupported limitation, but further confuses the otherwise plain meaning of the term. In sum, Cypress’ proposal should be rejected.

2. Defendant’s Answering Position¹⁵

Cypress seeks a plain-meaning construction that simply makes it clear that the claimed “power converter” in fact converts **power**, unlike Sentient’s which mistakenly limits this term to

¹⁴ *See* Section 2, *infra*.

¹⁵ Cypress’s originally proposed construction included the word “actually.” As the modifier is not essential to the definition and Sentient objects to the term, Cypress hereby removes this term from its proposal, in an effort to reach a compromise with Sentient

only changing voltage level. The Patent's own explanation of the claimed power converter confirms power is not interchangeable with voltage; rather, the Patent's discussion is entirely consistent with the fundamental and undisputed law of electrical energy that power equals voltage multiplied by current.¹⁶ Sentient's construction requiring a mere change in voltage is, therefore, at odds with both the express description of power converter in the Patent, as well as the undisputed and fundamental definition of electrical power. Sentient, therefore, entirely fails to capture what is happening in the power convertor as taught by the Patent—and in fact in any power converter.

The Patent, in a portion of the specification that is unfortunately omitted from Sentient's lengthy quote in its section above, explains exactly what the claimed power converter is doing:

a first stage in the internal **power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREG).**

'177 Patent at 8:64-66. As a person of ordinary skill in the art would readily understand, "convert[ing] an unregulated supply voltage to a fixed, regulated voltage" is in fact changing the power level. Hassoun Decl. ¶¶ 18-21. This basic concept is explained by Mr. Hassoun, an expert with over 25 years of experience working on FPGA circuits:

18 A power converter would be well-known to one of ordinary skill as a component that transfers energy (power is the rate at which energy is transferred) from an unregulated supply voltage to a regulated (fixed) output voltage.

19 A power converter is designed to supply power to an operating component (*e.g.*, a microprocessor that is demanding varying amount of power depending on how busy, how hard it is working, and/or how much computing it is being asked to do) and deliver that power via voltage and current (generally $\text{Power} = \text{Voltage} \times \text{Current}$). An unregulated supply could result in the voltage changing when a current demand rises or falls. Such changes can result in, for example, incorrect operation of the microprocessor or some of its circuitry due to

¹⁶ Given the clear and undisputed definition of electrical power, Sentient would need to show that the Patent somehow intended a different special meaning for the "power converter" term. Yet, the Patent shows that the patentee intended to use the term "power" in its ordinary and plain meaning.

that change. As a result, microprocessors typically require a stable/fixed/regulated voltage supply.

20 A power converter is able to take an unregulated supply whose voltage can vary greatly as the current demand changes and, after applying its power converter circuitry, produce a fixed voltage supply that does not change as the current demand changes as well as supply the necessary current to produce the power demanded by the microprocessor.

21 The Patent confirms that it is using the term “power converter” according to its well-understood meaning by teaching that the internal **power** converter regulates and filters **power supply** irregularities over a very wide voltage range and converts an unregulated supply voltage to a fixed, regulated voltage; thereby converting power and producing a stable voltage (*see* Col 8:54-58). *Also see generally* Col 8:45-9:5. In fact, the Patent states “[a]s shown in FIG. 3, a first stage in the internal power converter converts an unregulated supply voltage to a fixed, regulated voltage (VREF),” (*see* Col 8:64-66), and one of skill in the art would have known that a power converter can, for example, take a +5 Volt unregulated voltage (that keeps varying as loads change), *see e.g.* Fig. 3 “+3v to +15V”, to a +5V regulated voltage (that is stable/fixed as loads change), *see e.g.* Fig. 3 “Primary Analog Supply +5Volts.”

Hassoun Decl. ¶¶ 18-21 (emphasis in original). Mr. Hassoun goes on to explain that extrinsic references support precisely the description of power converter that is provided by the Patent itself. *See id.* ¶ 23 (power converter performs “controlled transfer of energy from a unregulated DC source to a regulated output voltage”) (*quoting* Ex. C (Cheong paper)); *see also id.* ¶¶ 22-24. Thus, Cypress’s proposed construction—unlike the proposal from Sentient—follows directly from the Patent’s own description of what the claimed power converter does, comports with the fundamental definition of electrical power, and is precisely consistent with the relevant external evidence.

Sentient cites incomplete snippets from the specification and a generic dictionary definition of “converter”, all the while studiously avoiding the claim’s express and fundamental requirement that the converter change “power.” Sentient’s proposal that a “power converter” is limited to changing one level of voltage to another, as explained above, ignores the express teaching in the

Patent that the power converter in fact changes power, by converting the type of voltage from unregulated to regulated voltage. *See* '177 Patent at 8:64-66; *see also* Hassoun Decl. ¶¶ 25-26.

Moreover, as Mr. Hassoun explains:

One of ordinary skill would have understood that a converter which can only change a voltage level to another voltage level is not a “power converter”; it is merely a simple level-shifter, a common circuit that changes voltage levels without supplying any current (*i.e.*, without converting power).

Hassoun Decl. ¶ 26. Sentient’s construction would, therefore, ensnare components much simpler than the power converter required by the claims of the Patent. The broad sweep of Sentient’s proposed construction is not surprising given that, as noted above, it relies upon extrinsic evidence that defines a generic “converter”—not a **power** converter. *See* Sentient’s Opening Discussion of Term 5 (citing SENTIENT 311-313).

Lastly, Sentient complains that the plain meaning of the term “power converter” should not include the Patent’s own explanation of what the claimed power converter does. Cypress included this language in its proposed plain meaning, because that is how the patentee chose to describe the power converter. Of course, any plain meaning of the claimed power converter would suffice as long as it makes clear that the power converter is actually converting power, not merely changing the level of voltage.

Thus, for the above reasons, Cypress respectfully submits that Sentient’s proposal must be rejected as mistakenly being limited to only voltage, and that Cypress’s plain meaning be adopted as requiring that the claimed “power converter” actually convert electrical power.

3. Plaintiff’s Reply Position

Although the plain and ordinary meaning should suffice here – which is proposed by Sentient above with some particularity to avoid any confusion – Cypress insists on re-writing this claim by introducing additional concepts absent in the claim such as “first stage” and

“unregulated supply voltage.” Inspection of the immediately following language in the claim provides helpful context in interpreting its meaning, namely “power converter capable of receiving *an input voltage level* and generating each operating and reference *voltage*.” ‘177 Patent, Claim 5, 10:40-43. This is consistent with the specification, which explains the two key functions of the power converter are “generation of each operating and reference voltage” and filtering out irregularities (*i.e.*, modifying input voltages to be one or more output voltages). *See id.* at 8:54-58, 8:64-66. Accordingly, it is clear the power converter is merely changing one voltage level (an input voltage level) to another (operating and reference voltage) as specifically set forth in the claim language and consistent with Sentient’s proposal. In sum, Patentee’s specification explains how power conversion is relevant to the claimed invention. Sentient’s proposed construction is consistent with that intrinsic evidence.

Rather than accepting this straightforward meaning, Cypress asks the Court to walk through an extensive expert declaration¹⁷ that provides largely extraneous, overly complicated, and irrelevant extrinsic opinions and information. While Mr. Hassoun’s declaration provides discussion of how power converters *can* work, it has no bearing on how the claimed power converter of the ‘177 Patent *must* work. For example, Sentient points out that there is at least one commonly experienced mode of operation for the power converter, *e.g.*, when it is driving a small number of very high impedance loads (such as the gate of a transistor) which results in a negligible current draw. In this instance, Sentient agrees the power converter does substantially act as a voltage shifter as Cypress’s expert points out. *See Hassoun Decl.* at ¶ 26. This is consistent with Sentient’s proposed construction.

¹⁷ Reliance on expert declarations in claim construction is disfavored due to, among other things, the danger of litigation-based bias. *See Phillips*, 415 F.3d at 1318-19. This District in particular also disfavors this practice. *See Enova Tech. Corp. v. Initio Corp.*, 2012 WL 6738398 at *2 (D. Del. Dec. 28, 2012) (citing *Phillips*, 415 F.3d at 1318).

Sentient also agrees that there can be some instances when certain voltage conversion operations affect current draw causing power fluctuation. Those instances are certainly not excluded from the penumbra of the claim, but rather simply are not required by the claim as written which by its plain terms merely requires only the transformation of one voltage to another. The power and current constraints relied on by Cypress and extensively discussed by its expert are simply not in the claim, and neither the Patentee nor the PTO require them. Therefore, Cypress's proposal should be rejected.

4. Defendant's Sur-Reply Position

Sentient *concedes* that its definition is really just that of a level or "voltage shifter," as opposed to requiring converting of power. *See* Reply, Term 5. Its effort to thereby remove the word "power" from the claims must be rejected. Sentient's complaints regarding the parenthetical Cypress proposes also lack merit. First, the inclusion of the parenthetical—as Cypress has already explained—is not critical, as long as whatever plain meaning chosen by the Court conveys the simple reality that the required "power converter" actually must convert power. Second, the description is straight from a part of the patent directly relied on by Sentient (*see id.* (citing '177 Patent at 8:66-68)), and if the Court chooses to include it, would aid a POSITA in explaining to a jury what the required power converter does. Moreover, Sentient's Reply, again, regrettably provides the Court with an incomplete paraphrase instead of an accurate quote. The full quote of the very excerpts upon which Sentient relies compels the plain meaning identified by Cypress:

'177 Patent at 8:54-58	<i>Sentient's</i> Reply Brief
“This internal embedded power convertor performs two key functions: generation of each operating and reference voltage needed within the module and regulation and filtering of power supply irregularities over a very wide voltage range.”	This is consistent with the specification, which explains the two key functions of the power converter are “generation of each operating and reference voltage” and filtering out irregularities (<i>i.e.</i> , modifying input voltages to be one or more output voltages). <i>See id.</i> at 8:54-58, 8:64-66.

Thus, while it may be “clear” to Sentient based on its incomplete paraphrase that power somehow is not involved with the required “power converter”, the patent itself is clear and, indeed, compels that power converter means what it says, that a power converter converts power.

Lastly, contrary to Sentient’s complaints, Cypress’s definition is not dependent on Dr. Hassoun’s declaration. The intrinsic evidence compels the plain meaning for this term as a component that converts power. Period. As discussed in the AB, Dr. Hassoun’s declaration provides context for the Court by describing fundamental concepts of engineering (such as the difference between electrical power and voltage) and how a POSITA would understand relevant phrases within the specification. Both areas are well within the bounds of expert testimony, and here un rebutted. *See Pitney Bowes*, 182 F.3d at 1309 (“[I]t is entirely appropriate, perhaps even preferable, for a court to consult trustworthy extrinsic evidence to ensure that the claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field.”). Dr. Hassoun’s declaration simply shows why Sentient’s proposal is unmoored from fundamental engineering and a POSITA’s understanding. Sentient provides no rebuttal opinion or convincing intrinsic evidence to support its conclusion that the patentee—one assumed to be a POSTIA—would have used the term “power converter” if voltage or level shifter was the concept actually intended.

Term 6: “processor configured to automatically activate...”

Term	Sentient’s Proposal	Cypress’s Proposal
“processor configured to automatically activate from a totally deactivated (unpowered) state”	“Processor configured to automatically turn ON from a turned OFF or disabled state”	Plain Meaning. Specifically, claim literally requires that the processor be ‘automatically activate[d]’ after being “totally deactivated” to an “unpowered” state. Not after merely being “turned off” or “disabled.” Alternate (simplified) Plain Meaning: “processor configured to automatically activate after being totally deactivated to an unpowered state”

1. Plaintiff’s Opening Position

A person of ordinary skill in the art would have an innate understanding that the claim term “processor configured to automatically activate from totally deactivated (unpowered) state” is concerned with the situation when the processor is switched to an ON *state* from an OFF *state*. That is the plain and ordinary meaning of these words, and the specification confirms it. Although not specifically in the context of the processor, but rather with respect to the FPGA, the specification states that: “The FPGA can be switched off to consume no power during sleep and restarted by the external signal or by the processor program when the processor is reactivated.” ‘177 Patent at 7:50-55 (emphasis added).

Thus, one of ordinary skill would understand from the teaching of the ‘177 specification that when a circuit component is switched to an active state from deactive state in which it consumed no power - that it is being switched from OFF to ON (based on an external signal). This is exactly the definition Sentient proposes.

Furthermore, the excerpt above also teaches that, in the context of the ‘177 Patent, when a circuit component (the processor) is in an unpowered state, it has no operational capability, and

therefore it is OFF (*i.e.*, it needs to be “reactivated”).¹⁸ This is consistent with the definition Sentient proposes. Importantly, what the claim does not say is that there is no power *applied* to the processor whatsoever, but merely that the processor is unpowered, because as part of a system on chip, when the chip is powered, the “whole system” is powered and some minute incidental amount of current may flow by virtue of being on this same substrate – but the component remains OFF and consumes no power.

In contrast, Cypress’s proposal should be rejected for several reasons. First, it does not appear to provide a claim construction at all. Rather, it appears to be just a confusing jumble of two sentence fragments, which merely repeats a few of the exact same words already in the claim and then proposes what the claim does not mean, rather than providing a positive recitation of what Cypress believes the term actually means. As such, it provides no assistance to a lay juror in understanding the scope of the claim regarding the activation criteria, the processor state, or what deactivated state means and in fact, may create confusion on the key point as to what unpowered means, how it is different from OFF or disabled, *etc.* Second, Cypress’s proposal is at odds with the specification, which teaches that a component that consumes no power is properly characterized as OFF. Accordingly, the Cypress proposal should be rejected.

2. Defendant’s Answering Position

Here again Cypress simply seeks a plain meaning definition for this term. The mention of plain meaning, along with the first several lines of Cypress’s proposal, was inexplicably omitted in the discussion of this term in Sentient’s opening brief. *See* Ex. 3 (Sentient’s Opening Brief) at

¹⁸ More specifically, this claim is concerned with a processor that “is *configured* to automatically activate....” The specification explains that the processor accomplishes this (*i.e.*, is configured) by coupling to an embedded memory that provides for an improved start up time as compared to the prior art systems. *See* ‘177 Patent at 4:57-62.

14. After mistakenly truncating Cypress's proposal,¹⁹ Sentient then compounded its own error by attacking Cypress's position as being "confusing." See Sentient's Opening Discussion of Term 6.

Cypress's proposal is drawn straight from the claim language, which the specification clearly and repeatedly supports. First, in the claims, the term "deactivated" is modified by the word "totally." Therefore, generically being deactivated, idle, disabled, or any other state that encompasses partial measures is not what the claim encompasses. Second, the specification shows that a "totally unpowered" state is expressly emphasized as an improvement over the prior art:

In a preferred embodiment, the microprocessor of the present invention preferably includes an embedded memory that enables the startup of processing without first loading a program from the non-volatile memory. This improves on the prior art systems which can only operate after a program is first loaded from non-volatile memory. Moreover, ***the improvement provides a totally unpowered ready state***, reduces power consumption when idle, and provides an abbreviated time to activation by retaining the active program in non volatile memory thereby eliminating need for loading of the initiating program.

'177 Patent at 4:57-67. The Patent goes on to further distinguish the alleged invention from prior art that still require power, as follows:

This means the present invention can function with discontinuous applied power whereas ***prior art controllers can only go into a sleep mode that requires power*** to the internal capacitive oscillating circuit. ***This means the present invention is able to display history-dependent behavior and be put to zero-power sleep for extended periods of time to be awakened by application of power from another device. This also means the invention can turn itself off completely allowing for wakeup on activation by the next input of power (e.g. from solar energy).***

Id. at 5:4-13. And:

[u]nlike prior art controllers, such as that in U.S. Pat. No. 6,148,399, where some components such as the SRAM are always powered, ***the present invention is able to totally shut down all electronics to achieve a zero power state.***

¹⁹ The discussion of this term in Sentient's opening brief omitted the below underlined portion of Cypress's proposed construction: "Plain Meaning. Specifically, claim literally requires that the processor be 'automatically activate[d]' after being 'totally deactivated' to an 'unpowered' state. Not after merely being 'turned off' or 'disabled.'"

Id. at 6:35-39.

Meanwhile Sentient’s proposal suffers from multiple fatal flaws. First, Sentient’s brief provides no support for its proposal that the term includes “Processor configured to automatically turn ON from a . . . disabled state.” The failure to support that portion of its proposal is reason alone to reject that phrase. Moreover, neither the phrase nor the concept is found in the Patent, and to include it would be genericide. *See LizardTech*, 424 F.3d at 1345 (rejecting the plaintiff’s generic definition for a claim term in part because the specification provided no support for a broad definition, and could not support the conclusion that the patentee possessed all variants that the broad term would encompass).

Second, Sentient’s proposal that the term’s meaning is “Processor configured to automatically turn ON from a turned OFF . . . state” does not accurately capture that the claims expressly require automatic activation from a “totally deactivated (unpowered) state.” The phrase “turned OFF” does not aid a jury in navigating the claims. Indeed, it is well-known that even devices that are “off” may still draw some, albeit minimal, power.²⁰ Yet the Patent and claims require that the processor be “totally deactivated” and “unpowered”, as discussed above.

Third, Sentient’s first citation to the Patent is in the context of the FPGA, **not** the processor. *See* Sentient’s Opening Discussion of Term 6. But, even in the context of the FPGA, the patentee recognized that describing a component as “switched off” does not sufficiently convey the fact that the component is unpowered. *See* ’177 Patent at 7:50-55 (specifying that the FPGA can be “switched off **to consume no power**”). Therefore, even Sentient’s off-topic citation

²⁰ For example, common consumer electronics like cell phones draw power to keep their internal clocks running. Indeed, use of an unplugged, “turned off” cell phone as an alarm is now commonplace

confirms that the simple phrase “turned off” is insufficient, and instead must include the concept of being “unpowered” as the claim expressly requires for the processor.

In sum, Cypress’ construction is simply a reflection of plain meaning required by the Patent and drawn straight from the actual language in the claims. Sentient seeks a construction that it has already half-disavowed, and that the Patent expressly teaches against. Thus, for the above reasons, Cypress respectfully requests that the Court adopt Cypress’s proposed construction.

3. Plaintiff’s Reply Position

Sentient agrees that the underlined portion of Cypress’s final proposal was inadvertently omitted from its Opening Brief as it was evolving up to the date of filing with the Court. Nevertheless, these additional words do not improve Cypress’s flawed proposal. Sentient’s common sense approach of equating “totally deactivated” (no power) with “OFF” and “activate” with “ON” (powered) provides an accurate definition of the claim term which will allow the jury to fairly assess its real world meaning.²¹ As an initial matter, the Court should note that nowhere in the claim at issue (*e.g.*, Claim 3, 10:26-31) does it require the *entire system on chip device* be totally unpowered, rather *just the processor* – although an unpowered device is mentioned in the specification. Therefore, as far as the claims are concerned, the remainder of the device may be ON with *only the processor* unpowered. Cypress’s remarks justifying its position seem to require that the *entire device* be completely devoid of power when this is simply not the case – especially with respect to what the *claim* or any other intrinsic evidence requires.

With this in mind, evaluating what “totally deactivated” means needs to be considered in the context of the operating environment of the claimed invention. That the claim does not require that the remainder of the device have no power (*i.e.*, components other than the

²¹ Cypress apparently does not object to its definition of “automatically activated” as “ON” but rather focuses its dispute on the meaning of “totally deactivated (unpowered) state – as OFF.”

processor) and only processor itself “totally unpowered,” does not mean the processor *must always* have absolutely zero power applied to it. Rather, simply that it does not need to constantly power a clock or “oscillating circuit.” ‘177 Patent at 5:1-7. The processor may be connected to the same power bus that the other “ON” (powered components) are coupled to – even if that applied power is “discontinuous.” *Id.* at 5:5. Therefore, as part of a system on chip, when the system is powered, the “whole system” has “applied power” and some minute incidental amount of current may flow through the processor by virtue of being on this same substrate – but the processor itself remains “OFF” and consumes substantially no power. That is all that the claims require.

The intrinsic evidence supports Sentient’s proposed construction. It is accurately reflected in the specification with respect to the FPGA operation – which teaches that a component that consumes no power is properly characterized as OFF and which, as the specification clearly explains the FPGA can be restarted from its OFF state by the same external signal that restarts the microprocessor. “The FPGA can be switched off to consume no power during sleep and restarted by the external signal or by the processor program when the processor is reactivated.” *Id.* at 7:52-55. And, notably, the processor is not described as operating any differently in this context. Cypress appears to have no material response to this position or this intrinsic evidence.

Moreover, Cypress’s proposal relies on specification excerpts referring to operating constraints not in the claim term itself, and provides no assistance to a lay juror in understanding the scope of the claim regarding the activation criteria, the processor state, or what deactivated state means. It would only serve to create confusion on the key point as to what unpowered

means, and how it is different from OFF or disabled. Accordingly, Cypress's proposal should be rejected, and Sentient's adopted.

4. Defendant's Sur-Reply Position

Here again, Cypress only seeks plain meaning. Sentient's attorney argument that the patentee did not mean what it said does not even arise to the level of extrinsic evidence. Moreover, Sentient's discussion as to whether or not the entire device must be totally deactivated or unpowered is a red herring—the required “unpowered” state, of course, relates to the processor, and Cypress's support for its definition comes directly from the section describing the “Microprocessor.” '177 Patent at 4:57-5:13. Consistent with this discussion, the patentee chose to claim a processor that is configured to automatically activate “from a totally deactivated (unpowered) state.” *Id.* Claim 3. Indeed, the patentee distinguishes the prior art based on this precise feature:

This means the present invention can function with ***discontinuous applied power*** whereas ***prior art controllers can only go into a sleep mode*** that requires power to the internal capacitive oscillating circuit. ***This means the present invention*** is able to display history-dependent behavior and be put to ***zero-power sleep*** for extended periods of time to be awakened by application of power from another device.

Id. at 5:7-11. Because the plain meaning is compelled by the intrinsic evidence, Cypress respectfully requests that its proposal be adopted.²²

²² Note that Cypress has streamlined its plain meaning definition to: “processor configured to automatically activate after being totally deactivated to an unpowered state.” Cypress *does* object to construing “automatically activate” as vaguely being “on,” as Sentient proposes.

Term 7: “a plurality of gates arranged in a field programmable gate array”

Term	Sentient’s Proposal	Cypress’s Proposal
“a plurality of gates arranged in a field programmable gate array”	“Logic circuits or elements arranged such that they are programmable to perform a programmed function”	“a large number (<i>e.g.</i> , roughly 30,000 or more) of basic logic gates arranged in a grid pattern, a subset of which can be freely re-configurable into at least switches and analog functions” Alternate compromise: “logic circuits or elements arranged such that they are programmable to perform a programmed function, including at least analog functions.”

1. Plaintiff’s Opening Position

At the time the ‘177 Patent was filed, Field Programmable Gate Arrays were known in the art and had a commonly understood meaning. (SENTIENT 000304-306) (Modern Dictionary of Electronics Technology defining “field programmable gate array (FPGA)” as a “[s]emiconductor logic array that is able to be programmed by the user to satisfy individual design requirements.”). Thus, it was well known that the logic gates of the FPGA could be programmed to provide a wide variety of functions and that such versatility was a common reason for choosing to use such FPGA circuits.

This commonly understood meaning comports closely with the teachings of the ‘177 Patent. For example, the ‘177 Patent teaches that the gates in a field programmable gate array of the present invention can be arranged to perform a panoply of different processing functions including digital signal processing to satisfy certain design requirements. As described, these functions include:

[The] present invention utilizes an independently operable and programmable FPGA which is used to implement many of the key instrumentation functions of an ASIC... For example, the FPGA could be *performing signal processing...* and

performing signal conditioning and filtering at the same time. This can be extended *to re-route* almost all external conductors and selected internal conductors, whether power or signal bearing... More specifically, the FPGA can be *programmed to monitor the functionality of the microprocessor*, the analog-to-digital conversion operations, and the digital-to-analog conversion operations... Preferably, the FPGA can be configured in numerous gate array patterns... Because of the fast and high precision ADC included in *preferred embodiment* the FPGA can perform *vibration signature analysis and harmonic analysis using DSP algorithms*.

‘177 Patent at 7:39-41, 45-49, 59-62; *id.* at 8:35-36; *id.* at 9: 25-28.

Accordingly, Sentient’s proposed claim construction should be adopted because it comports with both the intrinsic and extrinsic evidence (specification and dictionary definition) and further represents the plain and ordinary meaning of the words in the claim as understood by one of ordinary skill.

On the other hand, Cypress’s proposal contains a variety of unrecited limitations not in the claim and should be rejected as erroneous. For example, Cypress suggests adding no less than 7 new limitations in this claim term, which now would include the unrecited concepts of: 1) large; 2) roughly 30,000 or more; 3) basic logic gates; 4) in a grid pattern; 5) reconfigurable in subsets; 6) analog switches; and 7) analog functions – along with a host of other potential unclaimed but implied interactions between these new claim limitations. Such a construction would add in these new limitations from a preferred embodiment of the invention despite such a practice being disfavored by law. *See, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d at 1369 (warning that importing preferred embodiment limitations as inappropriate).

Furthermore, none of these 7 new limitations (or implied interactions) are in the claims as originally filed or otherwise, nor can Cypress point to any “clear and unmistakable” disavowal of claim scope requiring these new, very specific and numerous limitations to now be written into the claim. *See Continental Circuits LLC*, 915 F.3d at 797.

Equally disconcerting is Cypress’s attempt to distort the plain meaning of this term by

“cherry picking” certain narrow limitations to be included in its construction such as “switches” and “analog functions,” while excluding the digital processing functions required by preferred embodiments of the invention. For example, the specification clearly teaches that the “the FPGA can be *programmed to monitor the functionality of the microprocessor...*” ‘177 Patent at 7:59-62; and “in a preferred embodiment, the can *FPGA can perform vibration signature analysis and harmonic analysis using DSP algorithms.*” *Id.* at 9:25-28. A person of ordinary skill would recognize these as necessarily being digital processing functions.

Moreover, nothing in the intrinsic record requires that the plurality of gates are necessarily configured as both “switches” and “analog functions.” In fact, the invention includes certain preferred embodiments that require a wide variety of completely different types of processing functions such as DSP (digital signal processing) algorithms and processor monitoring among others, but do not require others. Any claim construction that requires that a narrow subset of features necessarily requiring certain specific configurations be present over a host of other preferred embodiment features (such as digital processing features) is legally flawed. Accordingly, the Cypress proposal should be rejected.

2. Defendant’s Answering Position²³

Cypress’s proposal simply seeks to define this term as one of ordinary skill would understand it in light of the specification. Sentient, conversely, attempts to read the term “field programmable gate array” out of the claim, including the unusual purported capabilities of the array that are claimed as part of the alleged invention. Field programmable gate arrays (FPGAs) are a particular type of programmable circuitry with particular capabilities. The ‘177 Patent claims a specific type of FPGA that, according to the Patent, includes “a subset of gates”

²³ Cypress offers the following alternate compromise to its proposed construction: “logic circuits or elements arranged such that they are programmable to perform a programmed function, including at least analog functions.”

with the special ability to perform “analog functions” which the Patent describes as being a “core feature.” Cypress’s proposal captures this critical feature and is entirely grounded in the specification.

First, regarding the type and number of gates, the Abstract describes the claimed FPGA:

the controller includes a ***separately controllable*** field programmable gate array that acts as a parallel processor with internal or separate external clock. The FPGA ***preferably includes more than thirty thousand gates (30,000)*** and adds a ***freely re- configurable*** and separately programmable multi-purpose digital system that can run independent of the microprocessor.

’177 Patent at Abstract; *id.* at 2:47-54 (similar); *id.* at 7:41-45 (“large (greater than 30,000 gate)”); *see also id.* at 6:61-64 (describing “reconfigurable logic (*e.g.* the FPGA)”); *id.* 3:12-17 (describing a preferred embodiment including “in-situ reprogramming of the FPGA’s operational software programs with adaptive parallel program codes”); *id.* at 8:5-15 (describing how the activities of the FPGA are constructed “on the fly” and how “the FPGA of the present invention has the ability to be dynamically configured”). These passages are clear support for the conclusion that the patentee envisioned a FPGA with a large number (*e.g.*, roughly 30,000 or more) logic gates that can be freely re-configurable.

But even setting aside the parties’ dispute over the Patent’s general guidance regarding the number or types of gates—the construction of FPGA must at a minimum account for the fact that the Patent’s FPGA is specialized beyond any generic FPGA. Indeed, Sentient’s own logic compels a definition that includes the unusual analog functionality identified in the Patent. As Sentient concedes in its defense of Term 4, when the Patent identifies something as a core element, it is required. *See* Sentient’s Opening Discussion of Term 4 (citing ’177 Patent at 2:66-3:5) (“Moreover, this limitation is *not identified as being a core feature of the invention in the specification*, and therefore is *not* required.”) (emphasis in original); *see also ContentGuard*

Holdings, Inc. v. Apple Inc., 701 Fed. App'x. 957, 961-62 (Fed. Cir. 2017) (approving of the district court's construction of a term because it included a "key feature" as defined in the specification and in the specification's glossary). Here, the patent expressly states that "**core elements** of the invention" include "analog function blocks, and embedded power conversion":

The **core elements** of the present invention include a microprocessor, static random access memory (single or multi-ported), non-volatile memory (e.g., flash or EEPROM), a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion.

'177 Patent at 2:66-3:4. From the grouping of the last four items together at the end of this list and from the discussion through-out the Patent specification, one of ordinary skill would understand that the FPGA of the alleged invention must be capable of performing these "core elements." See Hassoun Decl. ¶¶ 27-30.

For example, the discussion of Figure 2 in the Patent expressly states that "analog functions" can allegedly be performed within the FPGA as part of a "parallel processing" feature. *Id.* at 8:18-32. Also, all power conversion is another example of an analog function. Hassoun Decl. ¶ 30. The claims require the power converter be embedded in the FPGA, (*see id.* at Claims 5, 9, 10-12, 13-14, 15-17, 20), and the specification, including Figure 3, teaches that this function is specifically performed within "subsets of gates in the FPGA." *See, e.g., id.* at 10:38-43 (Claim 5); *id.* at 8:59-9:5 (describing how "subsets of gates in the FPGA can be used to provide power conversion," pointing to Figure 3 as showing how the FPGA subset of gates "converts an unregulated supply voltage to a fixed, regulated voltage," and identifying topologies to be applied to achieve this result, including "switching based, linear based, or a combination of the two.")). Moreover, at the beginning of the specification section entitled "Field Programmable Gate Array" the patent states unequivocally that "[t]he design of the present invention eliminates

the need for an analog application-specific intended circuit (ASIC). Instead, present invention utilizes an independently operable and programmable FPGA which is used to implement many of the key instrumentation functions of an ASIC.” 177 Patent at 7:36-41. The FPGA subset of gates must, therefore, at least have the capability to perform the core element of analog functions as well as the analog function of power conversion as required in the claims.

However, one of ordinary skill would readily understand that analog functions for a “subset of gates” would be an unusual feature for an FPGA. Hassoun Decl. ¶¶ 31-33. Indeed, Marwan Hassoun, an expert with over 25 years of experience in the field of FPGAs, has never seen any FPGA perform such analog functions within its subset of gates, nor is he aware of any paper or article describing how such analog functions within a subset of gates could even be performed by an FPGA. Hassoun Decl. ¶ 32. Yet, the alleged inventors of the ’177 patent purportedly discovered that a subset of gates within the claimed FPGA could somehow be utilized to perform such functions. Given the unusual nature of the FPGA required by the alleged invention of the ’177 patent, therefore, the term FPGA in the claims cannot accurately be construed as simply a generic FPGA. Without construing the unusual nature of the specific type of FPGA required by the claims when read in light of the specification, the term would mistakenly encompass any generic FPGA. Moreover, failing to properly construe the FPGA would also run afoul of the enablement and written description requirements of section 112. *See, supra*, Cypress’s Discussion of Term 1 at footnote (“The patent teaches only one approach . . .”). Thus, for all of the above reasons, Cypress respectfully requests that its proposed construction be adopted. Alternatively, in an effort to reach a compromise, Cypress proposes that the term could be interpreted as being: “logic circuits or elements arranged such that they are programmable to

perform a programmed function, including at least analog functions.”²⁴

3. Plaintiff’s Reply Position

Cypress appears to abandon its original proposal with respect to this term that attempted to include numerous unrecited new limitations in the claim in favor of a more streamlined and supportable alternate proposal. Sentient agrees with the new Cypress proposal except for the phrase “including at least analog functions,” which should be rejected based on Cypress’s misreading of the specification.

The basis for Cypress’s new proposal is rooted in its belief that the following excerpt requires “analog function blocks” to be within the FPGA structure:

The core elements of the present invention include a microprocessor, static random access memory (single or multi-ported), non-volatile memory (e.g., flash or EEPROM), a dynamically reconfigurable field programmable gate array (FPGA), reconfigurable interconnect devices, analog function blocks, and embedded power conversion.

(§ 2, *supra*) (citing ’177 Patent at 2:66-3:4). Cypress is mistaken. Its position is based solely on its expert’s partisan view concerning the grouping of the names of various components in this general sentence about the invention. But the sentence does not say that the FPGA itself must include analog function blocks.

First, the general term “analog function block” does not appear anywhere else in the specification, and Cypress’s attempts to definitively equate this with the FPGA or other parts of the specification that use different terminology is misguided. As the plain writing of these words demonstrates, this list means the components are discrete from one another and not necessarily “within” or part of one another at all as Cypress suggests. For example, “embedded power conversion” means “on-chip” power conversion, (not something within the FPGA) whereas if

²⁴ Neither Cypress’s proposed definition nor its compromise proposal eliminates preferred embodiments like digital signal processing, as Sentient professes to fear.

written as “internally embedded power conversion” it could reasonably be interpreted as “inside” the FPGA. “Analog function blocks” on the other hand relates to a component separate from the FPGA – A/D converter 150 – which is consistent with original claim features (a plurality of analog to digital converters). See ‘177 Patent, Claim 1, 10:8; 5:20-21. (See also SENTIENT 00465). This is further supported by inspection of the Abstract, which describes the A/D converter with no mention of any internal FPGA “analog function blocks.” See *Hill-Rom Co. v. Kinetic Concepts, Inc.*, 209 F.3d 1337, 1341 n.1 (Fed. Cir. 2000) (holding that an abstract can be a “helpful source of intrinsic evidence as to the meaning of claims”).

Accordingly, Cypress cannot support its position regarding the “core elements” of the invention. Nothing in the intrinsic record requires that the plurality of gates are necessarily configured as “analog function blocks.” The invention, however, does include certain preferred embodiments that require a wide variety of completely different types of processing functions such as DSP (digital signal processing) algorithms and processor monitoring among others, but don’t require analog function blocks. Any claim construction that requires such a narrow subset of features necessarily including certain specific configurations be present over a host of other preferred embodiment features (such as digital processing features) would be erroneous.

Consequently, once the incorrect notion that “analog function blocks” are a required or core element of the FPGA is dispelled, Cypress’s new proposal may be properly amended to exclude the reference to the “including at least analog functions” portion, resulting in “logic circuits or elements arranged such that they are programmable to perform a programmed function.” Or stated another way, Sentient’s original proposal should be adopted.

4. Defendant's Sur-Reply Position

The parties' primary dispute is whether this term must clarify that the patentee's FPGA is not a typical FPGA, but one that includes analog functions. Cypress says yes—the specification demands it. Sentient tortures the specification and ignores the clear teachings that analog functions are performed in the FPGA. Sentient also fails to dispute either (1) the fact that FPGAs do not typically perform analog functions or (2) that power conversion—which the claims require, and the specification teaches, to be within the FPGA—is an analog function.

First and foremost, the specification describes analog functions as taking place in the FPGA, just as Cypress explains. '177 Patent at 8:18-32 (describing the “analog functions represented by A1-A3” in “Fig. 2[, which] illustrates the concept of using the FPGA to reroute a subset of the external inputs in order to perform parallel processes.”). And as explained in Cypress's AB, supported by Dr. Hassoun's declaration, and all but conceded by Sentient, power conversion is also a uniquely analog function that the patent teaches to only occur within the FPGA, and which the claims require to be embedded within the FPGA. See Reply at Term 2 (pointing at Figure 3 and “explaining that the gates used to form the power converter are *physically inside* the FPGA structure”) (emphasis in original).

Second, Sentient's contorted view of the patent's “core elements” is unsupported. Sentient relies upon a definition of a term no one seeks to construe (“internal”) and that makes no sense; Sentient doesn't even attempt to provide its logic.²⁵ And Sentient's bald assertion that when the patentee said “analog function blocks,” it somehow meant the A/D converters 150 (a number that appears nowhere in the Figures) is not supported by the patent. It is pure attorney argument.

In sum, the patent requires that the FPGA include analog functions. Because it is

²⁵ Sentient's assertion that the patentee would have listed “internal embedded power conversion” as a key element if it was intended to be a part of the FPGA ignores the fact that the patent only teaches power conversion to take place within the FPGA.

undisputed that analog functions are not usual properties of an FPGA, the term properly defined should include that requirement. Thus, Cypress respectfully requests adoption of its proposal.

Term 8: “configured to run independent processes”

Term	Sentient’s Proposal	Cypress’s Proposal
“configured to run independent processes”	“configured to run without computational assistance from the processor (in parallel)”	“configured to run processes not under control of the processor”

1. Plaintiff’s Opening Position

The claim term “configured to run independent processes” is concerned with the imposition of an additional condition when the processor and the plurality of gates are operating in parallel with one another. More specifically, this claim term is concerned with a plurality of gates that are *configured to run* independent processes (in parallel with the processor). At the outset, for context, it is helpful to bear in mind while construing this claim term that the plain and ordinary meaning of the phrase *in parallel*, is “at the same time.” This is not in dispute. Because the two processes in question necessarily execute at the same time, they are independent when there is the absence of computational assistance from the other.

This can be seen, for example, by considering a preferred embodiment of the invention set forth below, where the processor dynamically programs the plurality of gates from a memory at a specified time (*e.g.*, at power up) and *then* the programmed process *runs* independently. For example:

The FPGA utilized in a preferred embodiment of the present invention has the ability to be *reprogrammed from non-volatile memory, by the microcontroller*, or through a serial port. This enables the parallel activities of the FPGA to be constructed *“on the fly”* and personalized with a variety of unique programs and data, such as serial codes, calibration coefficients, or a reduced “traveler” containing process history. Accordingly, the FPGA of the present invention has the ability to be *dynamically configured as a processor* with extended mathematical or logical precision (*e.g.* 32 bit or 64 bit).

‘177 Patent at 8:5-15.

So, as seen from the above, *after* the plurality of gates are configured or programmed, (*e.g.*, as a logic primitive such as a filter or comparator, *etc.*), they are capable of performing their programmed function *without computational assistance*. Nothing in the intrinsic record requires the FPGA gates to receive any computational assistance from the processor after being programmed. This is the purpose of such programming. Accordingly, Sentient’s proposal represents the natural and proper meaning of the claim term in the parallel processing context²⁶ and should be adopted.

The Cypress proposal, on the other hand, is too broad and vague to be of any help to a lay juror and confusingly substitutes one term requiring a contextual definition for another (*i.e.*, “control” for the actual claim term “independent”). For example, it is unclear what “not under control” or just “control” means in this context. Again, Cypress attempts to define the term by what it is not rather than what it is. Would any interaction *at any time* where the processor acts to direct the plurality of gates, such as when programmed, constitute control? If so, the proposed construction would clearly be untenable because the claim requires the processes to be independent when the parallel processes are *running*, and not at some other time – such as when being programmed. The Cypress proposal provides no clarity on this common operational circumstance envisioned by the ‘177 Patent, but rather simply mis-describes the relationship described in the specification and clearly intended by Patentee.

Moreover, Defendant’s proposed construction would read out the preferred embodiment of the present invention cited above, specifically where the processor dynamically programs the plurality of gates from a memory at a specified time (for example at power up) *and then* the process *runs* independently. Accordingly, such actions cannot constitute control as contemplated by the

²⁶ Moreover, it will be appreciated as axiomatic that the whole purpose of the FPGA gates component on the SOC is to offload certain basic computations from the processor core. *See, e.g.*, ‘177 Patent at 8:8-13.

'177 Patent specification. In sum, processes that are configured to run independently are those which (are programmed) to run without computational assistance from the processor. Thus, Cypress's mere substitution of "control" for "independent" is incorrect and unsuitable in the clear context of the invention claimed and described in the '177 Patent. Sentient's construction should be adopted.

2. Defendant's Answering Position

Again, Cypress's proposed construction strives to simply capture the plain meaning of the term. The Patent expressly *defines* the alleged invention in the terms proposed by Cypress:

[T]he present invention incorporates a stand alone FPGA based parallel processor which can be ***configured to run under control of a microprocessor or independently.***

'177 Patent at 3:50-53. In *defining* the alleged invention, the patentee clearly states that the claimed "independent" processes of the FPGA are processes *not* "under the control of" the processor, just as Cypress proposes. Cypress's proposal is supported throughout the specification. For example, the Abstract also contrasts "control" by the processor with "independence":

A multi-chip module instrument controller having various interface and operational capabilities. The controller incorporates a microprocessor and both volatile and non-volatile memories. The controller includes variable analog-to-digital conversion bit depths, with higher bit depths for some applications. Additionally, ***the controller includes a separately controllable field programmable gate array*** that acts as a parallel processor with internal or separate external clock. The ***FPGA preferably includes more than thirty thousand gates (30,000) and adds a freely re-configurable and separately programmable multi-purpose digital system that can run independent of the microprocessor.***

Id. at Abstract. In distinguishing prior art, the Patent makes a similar distinction between control and independence:

However, there are *several limitations to the design in U.S. Pat. No. 6,148,399*. First the AIC is *not capable of performing parallel independent processes*.

Although the AIC does include a specialized ASIC, it is controlled and clocked by the microprocessor and cannot run independently of the microprocessor. Accordingly, independent parallel processes are not possible. Accordingly, what is needed is an MCM design capable of executing multiple parallel processes in an independent fashion.

Id. at 2:9-18. Conversely, Sentient’s vague reference to “computational assistance” is found nowhere in the patent.

Lastly, Cypress notes that its definition does not imply that there is **never** communication with the processor. The configuring of the FPGA may, of course, initially involve the processor, but once that takes place, the FPGA’s independent processes are not under control of the processor. In fact, the claim term makes clear—by use of the past tense of “configured”—that configuration has already taken place and thereafter the FPGA is “configured to run independent processes in parallel with the processor:”

a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and **configured** to run independent processes in parallel with the processor;

E.g. id. at Claim 1. Thus, for the reasons above, Cypress respectfully requests that the Court adopt its proposed plain meaning for this term.

3. Plaintiff’s Reply Position

In its Answering Brief, Cypress tellingly declines Sentient’s invitation to define what it means by “control” or “not under control” and explain what that should mean to lay juror and why. It again merely substitutes the words “not under control” for “independent” in rote fashion. It also merely unhelpfully suggests what it believes the claim term “is not,” instead of what “it is.” Cypress’s proposal should be rejected.

The Sentient proposal, on the other hand, points out that, *after* the plurality of gates are configured or programmed, (*e.g.*, as a logic primitive such as a filter or comparator, *etc.*), they are capable of performing *their programmed function without computational assistance*. See

‘177 Patent at 8:5-15. After all, a purpose of the invention is to strategically offload processing responsibility from the processor to the FPGA *during the parallel processing window* (i.e., to provide computational independence for the FPGA when the processor is doing other things). See ‘177 Patent, Abstract, 2:16-18, 49-50; 3:51 (describing FPGA as a parallel processor).

For example, in the case where the microprocessor directs data to and from the FPGA for processing and result reporting, the parallel processing by the FPGA is then performed without any computational assistance and is “not under control” because the claim requires that *independent part is the part that is done in parallel* (at the same time), and not the operations that occur before or after this specific window. *Id.* at Claim 1, 10:5-7. Cypress seems to admit this in its briefing when it explains that interactions between the processor and FPGA that occur before the processing starts do not constitute control. Axiomatically, this also extends to interaction that occurs after the independent parallel processing is complete. To the extent Cypress believes “not under control” extends beyond this discrete parallel processing window, it is at odds with the intrinsic evidence cited above and adds significant limitations to the claims far beyond what the plain meaning of the term requires.

4. Defendant’s Sur-Reply Position

Cypress’s construction relies upon the claims and the specification. See, e.g., ‘177 Patent at 3:50-53 (contrasting being run “under control of a microprocessor” with being run “independently”). Sentient’s “computational assistance” construction does not. Indeed, since this term does not even exist in the patent, Sentient resorts to pure attorney argument. In addition to this fatal defect, there is no basis in the patent to limit the definition of “independent” processes to just those that are run “without *computational* assistance.” Cypress, therefore, requests its proposal be adopted.

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