

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC., ADVANCED MICRO DEVICES, INC.,
and ATI TECHNOLOGIES ULC

Petitioner,

v.

SENTIENT SENSORS LLC

Patent Owner.

Case IPR2023-00195
U.S. Patent No. 6,938,177

**PATENT OWNER'S SUR-REPLY
TO PETITIONER'S REPLY**

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EXHIBIT LIST

Exhibit No.	Description
2001	USAF Cooperative Research and Development Agreement between Air Force Research Laboratory, Space Vehicles Directorate and MSI November 24, 1998
2002	JTAG Article FPGA4fun (1) https://www.fpga4fun.com/JTAG1.html
2003	TAP Article FPGA4fun (2) https://www.fpga4fun.com/JTAG2.html
2004	Xilinx JTAG Programmer Guide 1991-1999
2005	XLINX XC4000 TAP Application Note November 16, 1999
2006	USPTO Office Action Dated December 8, 2004
2007	Examiner Stoynov 1st Prior Art Search 11/19/04 (5 pages)
2008	Examiner Stoynov 2nd Prior Art Search 11/22/04 (7 pages)
2009	Examiner Stoynov 3rd Prior Art Search 11/22/04 (5 pages)
2010	Examiner Stoynov 4th Prior Art Search 11/23/04 (8 pages)
2011	Examiner Stoynov 5th Prior Art Search 11/23/04 (10 pages)
2012	Examiner Stoynov 6th Prior Art Search 11/24/04 (5 pages)

2013	Examiner Stoynov 7th Prior Art Search 11/29/04 (14 pages)
2014	Examiner Stoynov 8th Prior Art Search 3/09/05 (3 pages)
2015	Proof of Service on Registered Delaware Agent
2016	MSI/Sentient Ownership Interest
2017	Letter from James Lyke in support of Management Sciences, Inc. dated Apr. 29, 1997
2018	Bus Arbitration In Computer Organization Article https://www.geeksforgeeks.org/bus-arbitration-in-computer-organization/
2019	Enhancement of MCM Testability Using Embedded Reconfigurable FPGA J. York, T. Powell P. Dehkordi, and D. Bouldin, Proceedings 1997 IEEE Multi-Chip Module Conference (Cat. No. 0-7803-4275), 1997, pp. 165-173 (“ <i>Dehkordi 2</i> ”)
2020	Declaration of John Peck (with Curriculum Vitae)
2021	Ch. 11 in <i>A New Kind of Science</i>. Champaign, IL: Wolfram Media, pp. 637-714, 2002.
2022	Sentient's District Court Identification of claim constructions
2023	Xilinx's District Court Identification of claim constructions
2024	Definition of computation https://mathworld.wolfram.com/Computation.html
2025	October 19, 2020 Joint Claim Construction Brief (D.I. 63) from the Cypress Litigation

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2026	November 12, 2020 Second Amended Joint Claim Construction Chart (D.I. 77-1) from the <i>Cypress</i> Litigation
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Patent Owner’s Sur-Reply

Pursuant to the Scheduling Order (Paper No. 13) and its subsequent stipulated modifications (Paper Nos. 16, 23), Patent Owner Sentient Sensors, LLC (“Sentient” or “Patent Owner”) hereby respectfully submits this Patent Owner Sur-Reply to Petitioner’s Reply (Paper No. 21) that Petitioner Xilinx Inc. *et al.* (“Xilinx” or “Petitioner”) filed on March 21, 2024 in the above-identified *Inter Partes* Review.

I. INTRODUCTION

Xilinx still fails to prove the unpatentability of claims 1-5, 10-15, and 17-20 of the ’177 patent. Xilinx’s prior art references simply do not show or suggest the novel features of the claims or render the claims obvious.

Xilinx’s primary prior art reference is U.S. Patent No. 6,148,399 to James Lyke (the “’399 Patent” or “*Lyke*”). *Lyke* was cited extensively, and the Examiner carefully considered it, during prosecution of the ’177 patent. The Examiner ultimately found that *Lyke*, either alone or in combination with other references, did not teach or suggest all of the elements of the claims to Mr. Blemel’s novel and nonobvious instrument controller. Indeed, the U.S. Federal Government has twice confirmed that the “Advanced Instrument Controller” (“AIC”) described in *Lyke* needed improvement and that Mr. Blemel succeeded in improving it: once when the U.S. Government sponsored Mr. Blemel’s efforts to improve the AIC; and once again when the Examiner allowed the claims of the ’177 patent after carefully considering *Lyke* in combination with other prior art.

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Additionally, Xilinx also acknowledges that *Lyke* does not teach or suggest all the elements of the challenged claims of the '177 patent because Xilinx does not contend that *Lyke* anticipates those claims. Instead, Xilinx was forced to combine *Lyke* with four to five other references to cobble together a theory that the technical and functional improvements disclosed and claimed in the '177 patent were already known in the art before its filing date on December 19, 2001. But Xilinx's theory is only part of the story, and it crumbles when the full story is told.

Xilinx's main secondary reference, "*Dehkordi 1*" (EX. 1004) is a paper directed to a prototype MCM subsystem that was still in development at the time of its publication in 1996. And the aspects of *Dehkordi 1* that Xilinx relies on were still incomplete and speculative.

Patent Owner has now updated and completed that story with "*Dehkordi 2*" (EX. 2019), a follow-on paper published the next year in 1997 by the **same** authors of *Dehkordi 1* from the **same** university under the **same** DAPRA grant, DAAH04-94-G0004, regarding the **same** MCM subsystem and the **same** testing features clarifying its operation and testing procedures used in a more complete subsystem. As set forth in Patent Owner's Response (Paper No. 18), *Dehkordi 2* confirms what Patent Owner has argued all along: that *Dehkordi 1* simply does not teach or suggest what Xilinx contends it does. POR at 39-42; EX 2020 at ¶¶ 44-46, 72-78.

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Specifically, among other things, *Dehkordi 1* does not teach or suggest independent and/or parallel operation. Without that, all of Xilinx's Grounds fail.

II. CLAIM CONSTRUCTION**A. The Construction of "Process" and "Independent Processes"****1. *Patent Owner's Proposed Construction is Consistent with the Intrinsic Evidence***

The claim limitation at issue for this claim construction dispute is: "a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor and *configured to run independent processes in parallel with the processor.*" EX 1001 at 10:4-7 (emphasis added).

As set forth in Patent Owner's Response, the proper construction of "process" is "a computational process programmed into the FPGA gates." POR at 28 (citing EX 1001 at 8:16-32; 9:19-35; 4:39-50; EX. 2020 ¶¶ 49-52 (citing EXS. 1012, 1023)). The proper construction of "independent processes" is "without computational assistance from another." *Id.* Thus, the plain meaning of "independent processes" is that each computational process programmed into the FPGA gates must be independent—*i.e.*, occur without computational assistance—from another computational process programmed into the FPGA gates, and from the processor. *Id.*

With this construction, the claim language would read as: "a plurality of gates arranged in a field programmable gate array, the gate array coupled to the processor

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and configured to run *[computation processes programmed into the FPGA, which must each be independent—i.e., occur without computational assistance—from another computational process programmed into the FPGA, and from the processor,]* in parallel with the processor.”

Xilinx provides three arguments in response: (1) that the definition is “self-referential;” (2) the ’177 patent specification does not provide support and Patent Owner “failed to engage with the extrinsic evidence;” and (3) the definition is “redundant” with other claim language. Pet. Reply at 6. Based on the claim language as proposed by Patent Owner above, however, Xilinx’s first and third arguments are simply incorrect. The definition is not “self-referential” or “redundant.” Even if it were “self-referential,” it is because it is clarifying a particular type, category, or subset of processes, *i.e.*, “*computational*” processes, which provides additional insight and meaning to the general term “processes.” See EX 2024. This clarification is not adding a limitation to the claim, as alleged by Dr. Shanfield (EX 1050 at ¶ 57 (“it’s not clear to me what the Patent Owner is trying to do in adding the word computational.”)), but simply clarifying what Patent Owner contends that claim already says, consistent with the specification.

Further, though Xilinx alleges that the ’177 patent’s specification does not provide support for Patent Owner’s proposed construction, Xilinx never explains how the portions of the specification that Patent Owner pointed to for support fail to

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provide that support. Nor is Patent Owner required to engage with extrinsic evidence when the intrinsic evidence is clear. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005).

Instead, Patent Owner has provided ample support in the intrinsic evidence for its proposed claim construction. See POR at 28 (citing EX 1001 at 2:9-18; 2:48-55; 4:39-50; 8:16-32; 9:19-35); EX 2020 at ¶¶ 50-52.

Xilinx's argument that "the 'independent processes' element was not a point of novelty during prosecution" is also misleading. Pet. Reply at 7. Though Xilinx is correct that the Examiner pointed to Cloutier for the "independent processes in parallel" limitation, the Examiner did not say that Cloutier taught that limitation, just that the limitation would have allegedly been obvious in view of the combination of Lyke and Cloutier. EX 1010 at 58 of 167. The Examiner also indicated that there was allowable subject matter in a few dependent claims. *Id.* at 60 of 167. The applicant simply chose to accept that allowable subject matter. *Id.* at 44 of 167. This acceptance of allowable subject matter cannot be inferred as an acceptance of what Cloutier does or does not teach. It follows that Xilinx's inference that "the 'independent processes' element was not a point of novelty during prosecution" is not accurate. In fact, the applicant pointed to that functionality when stating that "the present invention offers enhanced power management and functional flexibility:"

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The instrument controller of the present invention offers enhanced power management and functional flexibility, more specifically, the instrument controller offers variable analog-to-digital conversion bit depths, along with higher bit depths for some applications. Also, the present invention eliminates the need for a resistive ASIC. Instead, the present invention adds a separately controllable FPGA that acts as a parallel processor with an internal clock or separate external clock. The FPGA preferably includes more than thirty thousand gates and adds a freely reconfigurable, and separately programmable, multi-purpose digital system that can run independent of the microprocessor. Also, the present invention incorporates a microprocessor with a processing speed of up to 33 MHz.

Id. at 43 of 167.

Further, Xilinx's argument that Patent Owner is allegedly embedding notions of "control" and "clocking" into the claim construction is not an effective rebuttal. Pet. Reply at 9-12. For one, those words do not appear in Patent Owner's proposed construction. And, second, Xilinx did not explain how Patent Owner's proposed construction can be read to implicitly include those concepts.

Xilinx's proposed construction for, quote, "independent process"—which ignores that the claim language is to plural processes—as "a process that runs separately from another process," Pet. Reply at 6, does not provide any clarity to the claim language, the meaning of which is obviously in dispute among the parties. It also appears inconsistent with the plain meaning of "independent" because merely saying that a process runs separately from another process does not account for whether one of those process controls the other. Thus, adopting Xilinx's proposal would not resolve the parties' dispute. *See O2 Micro Intern. v. Beyond Innovation Technology*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("When the parties present a

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fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.”).

2. Xilinx Waived Its Claim Construction Position

Additionally, Xilinx waived its opportunity to present its own claim construction position with respect to the “independent processes” limitation and the new evidence that allegedly supports that construction.

As Xilinx noted in its Petition (Paper No. 1), “a district court judge in the District of Delaware,” “[i]n an unrelated proceeding,” “ruled that [configured to run independent processes]” has its “‘plain and ordinary meaning’ with no additional construction.” Pet. at 7 (citing EX 1012, and referring to the *Sentient Sensors, LLC v. Cypress Semiconductor Corp.*, No. 19-01868-MN (D. Del.) (the “Cypress Litigation”)¹). During claim construction proceedings in that litigation, and similar to what it has done here, Sentient proposed that the claim term “configured to run independent processes” be construed as “configured to run without computational assistance from the processor (in parallel).” See EX 2025 at 71. Before the oral

¹ Counsel for Xilinx is the same counsel that represented Cypress Semiconductors in the *Cypress* Litigation.

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hearing, however, and prompted by the district court, the parties agreed that the term should have its plain and ordinary meaning. *See* EX 2026 at 1.

Xilinx was aware of the *Cypress* Litigation and had an opportunity to present a position on the construction of the “independent processes” term when it filed its Petition. It chose not to.

Sentient has not changed course since the *Cypress* Litigation. Instead, it has merely further clarified the plain and ordinary meaning of that term, consistent with the position it took in that earlier litigation. Xilinx, on the other hand, has improperly used the opportunity to submit another expert declaration and additional evidence on a claim construction it should have proposed and presented earlier.

Sentient recognizes that “the Board is capable of identifying new issues or belatedly presented evidence when weighing the evidence at the close of trial, and disregarding any new issues or belatedly presented evidence that exceeds the proper scope of reply.” Patent Trial and Appeal Board Consolidated Trial Practice Guide November 2019, at 80. Sentient thus respectfully requests that the Board view Xilinx’s new claim construction position and corresponding evidence as belatedly produced and weigh it accordingly.

III. SUR-REPLY REGARDING XILINX’S GROUNDS

Much of Xilinx’s Reply retreads old ground that was already addressed in the Patent Owner Response. Patent Owner provides the additional responses below as a sur-reply to Xilinx’s reply.

A. Neither *Lyke* Nor *Dehkordi 1* Teach or Suggest the “Independent Processes” Limitation

As noted in the Patent Owner response, Xilinx offers only two references for the proposition that claim element [1.5]—a “gate array coupled to the processor and configured to run independent processes in parallel with the processor”—would have been obvious to a POSA at the time of the inventions described and claimed in the ’177 patent: *Lyke* (EX. 1003) and *Dehkordi 1* (EX. 1004). POR at 29.

Patent Owner already addressed why *Lyke* does not teach that limitation in its Patent Owner Response. POR at 29-37. Xilinx did not substantively respond to Patent Owner’s arguments. Pet. Reply at 14-15. Instead, it appears that Xilinx’s allegations rest on an observation that *Lyke* mentions a “RAM-based [FPGA].” *Lyke* at 8:55-59; Pet. Reply at 14. But this mere mention of an FPGA is not enough to meet Xilinx’s burden to show that *Lyke* teaches an FPGA that is “configured to run independent processes in parallel with the processor.” See POR at 31-36.

Additionally, and contrary to Xilinx’s allegations, *Dehkordi 1* similarly fails to teach or suggest claim element [1.5].

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Claim terms should be interpreted in the context of the claim as a whole. *See Abbott Lab'ys v. Syntron Bioresearch, Inc.*, 334 F.3d 1343, 1351 (Fed. Cir. 2003) (“The usage of the disputed claim terms in the context of the claims as a whole also informs the proper construction of the terms.”) citing *RF Delaware, Inc. v. Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1263 (Fed. Cir. 2003). Thus, here, the claim term involving “independent processes” must be interpreted within the context of the claimed “instrument controller” as whole,² which requires viewing the “independent processes” on a system level instead of the sub-application level.

When there are, for example, two processes, and interactions between them that are essential for both of them to operate at the system level as intended, the two processes are not independent under Patent Owner's proposed construction because at least one process requires computational assistance from another. That same principle of independence, and the provided example, also applies to an FPGA process and the processor. That is, if a process on the FPGA and a task on the processor interact at the system level in an essential way, the process and

² As noted by Xilinx, the district court in the *Cypress* Litigation ordered that “the preamble, which recites ‘an instrument controller,’ is not limiting and need not be construed. Pet. at 8. That is the correct construction of the preamble.

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corresponding task are not independent. This is why the processes that *Dehkordi 1* and *Dehkordi 2* are capable of are not “independent” under a proper construction and interpretation of that claim term. Xilinx points to examples of sub-components in various newly- and late-produced references (EX 1058, EX 1060, EX 1061) and argues these are independent processes. Pet. Reply at 12-15. But these do not clarify the relationship of independent processes to the processor. Nor do the new references form part of Xilinx’s Grounds 1-5.

Further, if a process on the FPGA is involved with the processor (*e.g.*, the FPGA is monitoring the processor bus), then the FPGA-associated process is not independent of the processor. At the system level, the interaction between tasks on the processor and processes on the FPGA in *Dehkordi 1* and *Dehkordi 2* are clearly not independent because the application described—*e.g.*, the application during testing in *Dehkordi 2* when the FPGA is monitoring the bus between the processor and the memory for errors—involves the processor bus. The operation of the monitor on the FPGA depends on the activity on the processor bus and whether errors occur.

Additionally, in *Lyke*, the processor supplies the clock to the AIC. EX 2020 at ¶¶ 60, 63, 67 (citing EX 1003, Fig. 12). Without a clock, the AIC does not function, so no processes can exist in the AIC. This observation extends more

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generally where, for example, an FPGA is in place of the AIC, in which case no processes can exist in the FPGA.

If the processor and FPGA share a clock (*e.g.*, a clock is supplied by a circuit outside of both the processor and the FPGA), one must examine other criteria at the system level, including interaction between the processes within the FPGA and the interaction between process(es) in the FPGA and the processor to determine the independence of processes within the FPGA and independence from the processor. Also, if the processor and FPGA each have their own clock—irrespective of the origin of each clock—again, one must examine other criteria at the system level, including interaction between the processes within the FPGA and the interaction between process(es) in the FPGA and the processor (*i.e.*, in the context of bus monitoring) to determine the independence of processes within the FPGA and independence from the processor.

Patent Owner's proposed construction is agnostic to the type of clock. The specification supports this. For example, at 4:48-55, the specification discusses how “the FPGA may be clocked using the same on-board VCO as the microprocessor; or it may be clocked separately via an external clock 175,” and “[a]lternatively, where no clock is used, the FPGA will operate at gate speeds.” EX 1001 at 4:48-55.

Dehkordi 2 teaches that the FPGA makes use of an internal clock. EX 2019 at 172. But the FPGA process is performing a processor bus monitoring function

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that is clearly **not** independent from operation of the processor. As a follow-on publication involving a more complete version of the MCM subsystem in *Dehkordi 1*, it follows that *Dehkordi 1* also does not teach or suggest “independent processes” as required by the claim and under Patent Owner’s proposed construction. The discussion in *Dehkordi 2* regarding the “Design for testability” mode supports Patent Owner’s position that the FPGA process that monitors the bus between the processor and memory is not independent from the processor. See Ex 2020 at ¶¶ 43-46.

Further, in hardware design, circuits perform computations based on inputs and produce outputs. When “circuit A” performs a computation and produces an output that is received as an input by “circuit B” and used to perform a computation, this is an example of two processes that are not independent. In relation to *Dehkordi 2* at 172, the FPGA circuit that decodes the address bus between the processor and memory is not independent from the circuit that monitors and stops operations once an error is detected to notify its environment. Without an input from the former circuit, the latter circuit would not monitor and report an error upon detection.

The bus monitoring process in *Dehkordi 2* is not independent of the processor. *Dehkordi 2* at 171 makes this clear, “when the DSP initiated in the proper mode, transfer of address code and data (instruction code) can be monitored by the FPGA.” EX 2019 at 171. Additionally, “[s]ince the address bus has to go through the FPGA first for decoding, it can determine if the DSP processor is sending the proper

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addresses.” *Id.* at 172. The bus monitoring process in the FPGA would not perform its function in the absence of bus activity created by the processor.

1. *The Teachings of Dehkordi 1 are Speculative*

Xilinx alleges that Patent Owner's arguments concerning *Dehkordi 1* as not being enabled are “wrong on the facts.” *Pet. Reply* at 23. Patent Owner disagrees. According to Dr. Shanfield, “Dehkordi states that those university authors had built ‘a total of 5 MCMs’ and reported on the same,” and cites a quote in *Dehkordi 1* that says “[w]e have prototyped a total of 5 MCMs which each MCM costing about \$ 2,780.” *EX 1050* at ¶ 146.

Dr. Shanfield is embellishing what *Dehkordi 1*, in fact, teaches, and misunderstands the context of its disclosure. In the section in *Dehkordi 1* under the heading “Cost & Testing Issues,” the authors state their intention “to provide the reader with a *rather realistic* cost for this MCM.” *Dehkordi 1* at 3 (emphasis in original). The authors next state that they “have prototyped a total of 5 MCMs which each MCM costing about \$ 2,780.” *Id.* Each of the “5 MCMs” the authors of *Dehkordi 1* refer to is a manufactured copy of the single design disclosed in *Dehkordi 1*. They are not distinct designs that the authors have undertaken previously. The single cost figure of “\$2,780” refers to the cost of a single copy of the design in *Dehkordi 1*. It seems unlikely that the cost of distinct designs, each

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comprising unique types and numbers of components, would cost the exact same amount, \$2,780. Xilinx has not identified any evidence to dispute that.

Moreover, in the Institution Decision, the Board criticized Patent Owner for “omit[ting] a third disclosed mode of operation—i.e., datapath mode—which is the mode of operation upon which Dr. Shanfield’s testimony relies.” Institution Decision at 34. *Dehkordi 2*, however, makes it clear that the relevant mode of operation in *Dehkordi 2* is the “Functional Unit Mode” of the Xilinx 4013 FPGA from *Kostarnov*.” EX 2020 at ¶¶ 75-78. Thus, Dr. Shanfield’s testimony that relies on *Kostarnov*’s datapath mode is no longer relevant.

B. Steele Fails to Teach the “Power Converter” Element

Patent Owner provided extensive arguments in its Response as to why *Steele* does not teach or suggest the “power converter” element of the challenged claims. *E.g.*, POR at 53-56. Thus, Xilinx’s allegation that its arguments regarding *Steele* were “unchallenged,” Pet. Reply at 22, is inaccurate.

On the contrary, Patent Owner’s arguments regarding *Steele* appear to be largely unchallenged. Xilinx’s only arguments in response are: (1) Patent Owner proposes a claim construction that was rejected in the *Cypress* Litigation; (2) the arguments regarding *Steele* in Patent Owner’s POR are largely the same as in Patent Owner’s POPR; and (3) the Board should credit the argument regarding *Steele* in Xilinx’s Petition. Pet. Reply at 21-23.

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As to the first argument, the district court's construction of "power converter" in the *Cypress* Litigation is not binding on the Board. Further, Xilinx does not offer any substantive reason why Patent Owner's construction proposed in its POR should not be adopted here. Nor does Xilinx offer any legitimate reason why the Board should adopt its construction for "power converter"—which could have been, but was not, presented in its Petition.

Xilinx's second and third arguments are non-starters. Simply put, and as set forth in Patent Owner's POR and Mr. Peck's Declaration, *Steele* does not teach or suggest the "power converter" element.

The full context of the "power converter" element within the relevant claim limitations is: "an internal embedded power converter capable of receiving an input voltage level and generating each operating and reference voltage needed within the instrument controller." *See, e.g.*, EX 1001 at Claim 5. Thus, the context of the claim itself contemplates multiple voltages, consistent with Patent Owner's proposed construction.

Moreover, it is undisputed that the equation for electrical power is:

$$\text{POWER (P)} = \text{CURRENT (I)} \times \text{VOLTAGE (V)}$$

By definition, then, a power converter capable of generating multiple voltages requires changing one voltage level to another voltage level.

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Steele does not change one voltage level to another voltage level and thus does not teach a power converter. Instead, and as already set forth in the POR at 52-55, *Steele* describes a programmable logic device configured to operate like a voltage replicator that distributes an applied input voltage for output at other pins. Simply stated, *Steele* operates by accepting an input voltage generated at an external source at the VCCO pin of a Configurable Logic Block (CLB) and merely distributes that voltage at the input/output (I/O) pins for to external devices. Xilinx provides no response to this.

C. All of Xilinx's Grounds 1-5 Fail

Xilinx relies on the teachings of *Lyke* and *Dehkordi 1* for all five of its Grounds. Because neither *Lyke* nor *Dehkordi* teach or suggest the claim element regarding “independent processes” as Xilinx contends, all five of Xilinx's Grounds fail to prove the unpatentability of any challenged claim.

Moreover, Xilinx's Ground 4 additionally relies on *Steele*. As set forth above, and in Patent Owner's POR, *Steele* fails to teach or suggest the “power converter” limitation of the applicable challenged claims. This is an independent reason why Xilinx's Ground 4 fails to prove the unpatentability of any applicable challenged claim.

IV. THE CREDENTIALS OF MR. PECK ARE UNCHALLENGED

Xilinx's attacks on Mr. Peck are unnecessary, speculative, and unsupported. Pet. Reply at 27. Xilinx incorrectly criticizes Mr. Peck's opinions as made "without relevant extrinsic evidence" (citing EX. 2020 ¶¶ 34-48 (the Technology Background and Overview Certain Prior Art and Patentability Analysis Sections of his Declaration, which have nothing to do with claim construction or are given based on the claim construction that he has opined is correct that Patent Owner has proposed), but ignores that Mr. Peck's opinions on claim construction rely extensively on *intrinsic evidence* and are consistent with extrinsic evidence. EX. 2020 ¶¶ 49-52 (citing EX 1001 at 2:9-18; 2:48-55; 8:16-32; 9:19-35; 4:39-50; FIG.2; EXS. 1012; 2021; 2024).

Further, as set forth in Mr. Peck's Declaration, he has extensive experience in the relevant field of the invention. Nor does Xilinx challenge Mr. Peck as a person of ordinary skill in the art. In fact, Xilinx itself has used Mr. Peck's services in work on identifying low-power optimizations for FPGA devices using a hand placement methodology applied to cells from standard libraries. EX 2020 at ¶ 8. He has also been accepted as an expert in fields similar to the relevant one here by numerous federal district courts and the Patent Trial and Appeal Board. EX 2020, Appx A.

It should come as no surprise that Patent Owner's positions are consistent with the opinions of the expert it relies on to support them. Indeed, Xilinx's positions are

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consistent with those of its expert Dr. Shanfield. That consistency is not a valid basis to attack either expert's opinion. Xilinx's baseless allegations against Mr. Peck should therefore be dismissed.

V. CONCLUSION

Patent Owner respectfully submits that the Board should confirm the patentability of claims 1-5, 10-15, and 17-20 of the '177 patent.

Dated: May 2, 2024

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), Counsel for Sentient Sensors LLC hereby certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(c). According to Microsoft Office Word 2010's word count, this document contains under 5,600 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Dated: May 2, 2024

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Patent Owner's Sur-Reply

CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, a true and correct copy of **PATENT OWNER'S SUR-REPLY TO PETITIONER'S REPLY AND EXHIBITS 2025-2026** are being served electronically on May 2, 2023, to the e-mail addresses shown below:

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